HEWLETT PACKARD

Communications Components



GaAs & Silicon Products

Designer's Catalog

HEWLETT PACKARD

Sergio Lujan

Inside Sales Engineer
Electronic Components

Hewlett-Packard Company
930 East Campbell Road
Richardson, Texas 75081

214/699-4117
Fax 214/699-4384/4337

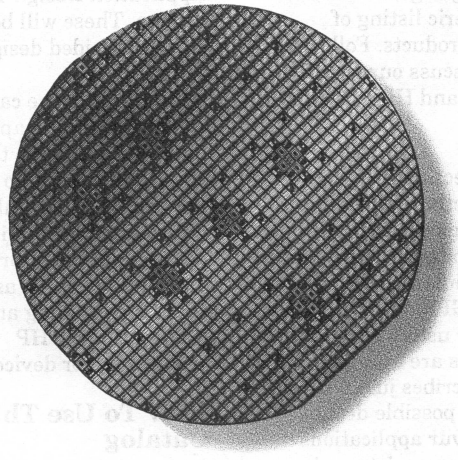
HEWLETT PACKARD

Communications Components Designer's Catalog, GaAs and Silicon Products

A Brief Sketch

Hewlett-Packard is one of the world's leading designers and manufacturers of RF and microwave semiconductors, optoelectronic, and fiber optic components, as well as electronic products and systems used for measurement and computation. Since its founding in Palo Alto, California, in 1939, Hewlett-Packard has done its best to offer only products that represent significant technological advances, and that can be reliably produced, delivered, and supported on a continuing basis.

In November 1991, Hewlett-Packard acquired Avantek, Inc. Together, the complementary products, people, and technologies of HP and Avantek create a broad-based RF and microwave semiconductor business to serve the worldwide market. As a result, Hewlett-Packard can now offer its customers complete solutions of RF and microwave silicon and GaAs semiconductor devices and subsystems, for use in communications, consumer, industrial, transportation, computer, and defense markets.



The body of this book is printed on recycled paper.

About This Catalog

This Communications Components Designer's Catalog contains detailed specifications for our complete line of silicon and GaAs semiconductor products. Included are discrete devices, integrated circuits, and integrated products such as LNAs, power amplifiers, switches, comb generators and communication link products.

The catalog begins with an alphanumeric listing of available products. Following sections discuss our Quality Assurance and High Reliability programs.

The next section illustrates semiconductor product design solutions, including block diagrams for typical applications such as cellular radio, Satcom, DBS, and GPS. Products suitable for use in each of these applications are also listed. This section describes just a sample of the total possible design solutions. Our applications engineers can assist you in choosing the right HP component for your particular need.

Complete data sheets for available products are divided into sections based on product type. Each section also includes application information about the family of products, as well as selection guides. The reliability pages at the end of each product section include information concerning the MTTF design goals for most of the devices. Where possible, the equivalent circuits of many devices can be found in the product sections and in the Application Design Tools section. These will be of use in computer-aided design circuits.

At the back of the catalog is a complete index of application notes pertaining to the use of these products. Also included at the back of this catalog is information on application design, general information on ordering products, as well as specific packaging and ordering information for HP semiconductor devices.

How To Use This Catalog

Several indexes are included to help locate components in this catalog:

- a Table of Contents lists devices by their general description
- an Alphanumeric Index lists all devices by part number
- a Design Solution section describes block diagrams and HP semiconductor solutions for typical communications applications
- Selection Guides at the beginning of each product section group products by major specifications, frequency, etc., and
- Page Tabs identify product groups as well as other important sections of the catalog

Although product information and illustrations in this catalog were current at the time it was approved for printing, Hewlett-Packard, in a continuing effort to offer excellent products at a fair value, reserves the right to change specifications, designs, and models without notice.

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* Standard Hi-Rel version available, consult your local HP sales representative. ** Hi-Rel version available in package 35 only.

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* Standard Hi-Rel version available, consult your local HP sales representative. ** Hi-Rel version available in package.
†Consult your local HP sales representative.

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†Consult your local HP sales representative.

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HSMP-3833	Surface Mount PIN Diode	5082-0012	4-25
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* Standard Hi-Rel version available, consult your local HP sales representative. ** Hi-Rel version available in package.

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HSMS-0012*	Batch Matched HSMS-0002		3-12
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HSMS-2801	Surface Mount Schottky Barrier Diode	HSMS-0001	3-55
HSMS-2802	Surface Mount Schottky Barrier Diode	HSMS-0001	3-55
HSMS-2803	Surface Mount Schottky Barrier Diode	HSMS-0001	3-55
HSMS-2804	Surface Mount Schottky Barrier Diode	HSMS-0001	3-55
HSMS-2805	Surface Mount Schottky Barrier Diode	HSMS-0001	3-55
HSMS-2807	Surface Mount Schottky Barrier Diode	HSMS-0001	3-55
HSMS-2808	Surface Mount Schottky Barrier Diode	HSMS-0001	3-55
HSMS-2810	Surface Mount Schottky Barrier Diode	HSMS-0002	3-55
HSMS-2811	Surface Mount Schottky Barrier Diode	HSMS-0002	3-55
HSMS-2812	Surface Mount Schottky Barrier Diode	HSMS-0002	3-55
HSMS-2813	Surface Mount Schottky Barrier Diode	HSMS-0002	3-55
HSMS-2814	Surface Mount Schottky Barrier Diode	HSMS-0002	3-55
HSMS-2815	Surface Mount Schottky Barrier Diode	HSMS-0002	3-55
HSMS-2817	Surface Mount Schottky Barrier Diode	HSMS-0002	3-55
HSMS-2818	Surface Mount Schottky Barrier Diode	HSMS-0002	3-55
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HSMS-8001	Schottky Diode Chips for X/Ku Band Hybrid Integrated Circuit		3-15
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HSMX-3655	Refer to AT-41511 or AT-00511		
HXTR-2001	Refer to AT-41500 or AT-42000		
HXTR-2101	Refer to AT-41410 or AT-42010		
HXTR-2102	Refer to AT-41470 or AT-42070		
HXTR-3001	Refer to AT-41400 or AT-42000		
HXTR-3002	Refer to AT-42000		
HXTR-3101	Refer to AT-41435 or AT-42035		
HXTR-3102	Refer to AT-42035		
HXTR-3103	Refer to AT-41435 or AT-42035		
HXTR-3104	Refer to AT-42035		
HXTR-3185	Refer to AT-41485 or AT-42085		
HXTR-3186	Refer to AT-41486 or AT-42086		
HXTR-3615	Refer to AT-41435		
HXTR-3645	Refer to AT-41435		
HXTR-3675	Refer to AT-41435		

* Standard Hi-Rel version available, consult your local HP sales representative. ** Hi-Rel version available in package.

MODEL NO.	DESCRIPTION	GENERIC CHIP	PAGE NO.
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HXTR-3686	Refer to AT-41486		
HXTR-4101	General Purpose Oscillator Transistor (obsolete)		
HXTR-4103	High Output Power Oscillator Transistor (obsolete)		
HXTR-5001	Refer to AT-42000		
HXTR-5002	Linear Power Transistor Chip (obsolete)		
HXTR-5101	Refer to AT-42010		
HXTR-5102	Refer to AT-64023		
HXTR-5103	Linear Power Transistor (obsolete)		
HXTR-5104	Refer to AT-64020		
HXTR-6001	Refer to AT-60500		
HXTR-6101	Refer to AT-60570		
HXTR-6102	Refer to AT-60570		
HXTR-6103	Refer to AT-60510		
HXTR-6104	Refer to AT-60510		
HXTR-6105	Refer to AT-41410		
HXTR-6106	Refer to AT-41470		
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INA-03100*	MagIC Low Noise Silicon MMIC Amplifier		8-62
INA-03170*	MagIC Low Noise Silicon MMIC Amplifier		8-64
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ITA-06318	1.5 Gb/s MagIC Silicon MMIC Fiber Optic Transimpedance Amplifier		10-92
ITA-12300	0.8 Gb/s MagIC Silicon MMIC Fiber Optic Transimpedance Amplifier		10-94
ITA-12318	0.8 Gb/s MagIC Silicon MMIC Fiber Optic Transimpedance Amplifier		10-94
IVA-05118	MagIC Silicon MMIC Variable Gain Amplifier		10-98
IVA-05200	MagIC Silicon MMIC Variable Gain Amplifier		10-100
IVA-05208	MagIC Silicon MMIC Variable Gain Amplifier		10-102
IVA-05218	MagIC Silicon MMIC Variable Gain Amplifier		10-104
IVA-14208	MagIC Silicon MMIC Variable Gain Amplifier		10-106
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* Standard Hi-Rel version available, consult your local HP sales representative. ** Hi-Rel version available in package 35 only.

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MGA 62100	Low Noise GaAs MMIC Amplifier		9-31
MGA-63100	Medium Power GaAs FET Cascade		9-34
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MSA-0200*	MODAMP General Purpose Silicon MMIC Amplifier		8-82
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MSA-0235*	MODAMP General Purpose Silicon MMIC Amplifier		8-86
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MSA-0435*	MODAMP Medium Power Silicon MMIC Amplifier		8-115
MSA-0470*	MODAMP Medium Power Silicon MMIC Amplifier		8-117
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MSA-0500*	MODAMP Medium Power Silicon MMIC Amplifier		8-123
MSA-0504	MODAMP Medium Power Silicon MMIC Amplifier		8-126
MSA-0505	MODAMP Medium Power Silicon MMIC Amplifier		8-128
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MSA-0635*	MODAMP Low Noise Silicon MMIC Amplifier		8-136
MSA-0670*	MODAMP Low Noise Silicon MMIC Amplifier		8-138
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MSA-0686	MODAMP Low Noise Silicon MMIC Amplifier		8-142
MSA-0700*	MODAMP Low Noise Silicon MMIC Amplifier		8-144
MSA-0711	MODAMP Low Noise Silicon MMIC Amplifier		8-146
MSA-0735*	MODAMP Low Noise Silicon MMIC Amplifier		8-148
MSA-0770*	MODAMP Low Noise Silicon MMIC Amplifier		8-150

* Standard Hi-Rel version available, consult your local HP sales representative. ** Hi-Rel version available in package 35 only.

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MSA-0835*	MODAMP Low Noise Silicon MMIC Amplifier		8-158
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MSA-0900*	MODAMP High Frequency Silicon MMIC Amplifier		8-166
MSA-0910*	MODAMP High Frequency Silicon MMIC Amplifier		8-169
MSA-0986	MODAMP High Frequency Silicon MMIC Amplifier		8-171
MSA-1000*	MODAMP Medium Power Silicon MMIC Amplifier		8-173
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MSA-1100*	MODAMP High Dynamic Range Silicon MMIC Amplifier		8-178
MSA-1104	MODAMP High Dynamic Range Silicon MMIC Amplifier		8-181
MSA-1105	MODAMP High Dynamic Range Silicon MMIC Amplifier		8-183
MSA-1110*	MODAMP High Dynamic Range Silicon MMIC Amplifier		8-185
MSA-1120	MODAMP High Dynamic Range Silicon MMIC Amplifier		8-187
MSA-2011	MODAMP General Purpose Silicon MMIC Amplifier		8-189
MSA-2111	MODAMP General Purpose Silicon MMIC Amplifier		8-195
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10514B	Double Balanced Mixer 0.2-500 MHz (obsolete)		
10514C	Double Balanced Mixer 0.2-500 MHz (obsolete)		
10534A	Double Balanced Mixer 0.2-500 MHz (obsolete)		
10534B	Double Balanced Mixer 0.2-500 MHz (obsolete)		
10534C	Double Balanced Mixer 0.2-500 MHz (obsolete)		
1N5711	HV General Purpose Schottky Diode (5082-2800)	5082-0024	3-64
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1N5719	PIN Diode (Similar to 5082-3039)	5082-0012	4-37
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33005C	SRD Comb Generator Module 1000 MHz		11-4
33005D	SRD Comb Generator Module 1000 MHz		11-4
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33104A	SPST General Purpose Microwave Switch 0.1-18 GHz		11-12
33132A	SPST Low Loss Microwave Switch 0.1-18 GHz		11-18
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33142A	SPST Fast Microwave Switch 0.1-18 GHz		11-22
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33150A	Microwave Bias Network 0.1-18 GHz		11-26
33190B	Switch Driver for Fast SPST PIN Switches		11-28
33602A	General Purpose Microwave SPST Switch, DC-18 GHz (obsolete)		
33604A	General Purpose Microwave SPST Switch, DC-18 GHz (obsolete)		
33632A	Low Loss Microwave SPST Switch, DC-18 GHz (obsolete)		
33634A	Low Loss Microwave SPST Switch, DC-18 GHz (obsolete)		
33642A	Fast Microwave SPST Switch, DC-18 GHz (obsolete)		

* Standard Hi-Rel version available, consult your local HP sales representative. ** Hi-Rel version available in package 35 only.

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5082-0008	Step Recovery Diode Chip		5-4
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5082-0012*	PIN Switching Diode Chip		4-10
5082-0013	Low V_F Mixer/Zero Bias Detector Schottky Chip		3-12
5082-0015	Step Recovery Diode Chip		5-4
5082-0017	Step Recovery Diode Chip		5-4
5082-0018	Step Recovery Diode Chip		5-4
5082-0020	Step Recovery Diode Chip		5-4
5082-0021	Step Recovery Diode Chip (obsolete)		
5082-0023	X-Band Schottky Mixer Chip		3-12
5082-0024	High Voltage Switching Schottky Chip (Replaced by HSMS-0001)		
5082-0025	AGC PIN Chip (Replaced by HPND-0001)		
5082-0029	Ku Band Schottky Mixer Chip (obsolete)		
5082-0030*	PIN Switching Diode Chip		4-10
5082-0032	Step Recovery Diode Chip		5-4
5082-0034	VHF/UHF Switching PIN Chip (Replaced by HPND-0003)		
5082-0039	AGC PIN Chip (Replaced by HPND-0002)		
5082-0041	X-Band Schottky Mixer Chip (obsolete)		
5082-0047	PIN Switching Diode Chip		4-10
5082-0057	General Purpose Schottky Diode Chip (Replaced by HSMS-0002)		
5082-0087	General Purpose Schottky Chip (Replaced by HSMS-0001)		
5082-0090	Step Recovery Diode Chip (obsolete)		
5082-0097	General Purpose Schottky Chip		3-12
5082-0112	Step Recovery Diode	5082-0015	5-6
5082-0113	Step Recovery Diode		5-6
5082-0114	Step Recovery Diode		5-6
5082-0132	Step Recovery Diode	5082-0015	5-9
5082-0151	Step Recovery Diode	5082-0018	5-6
5082-0153	Step Recovery Diode	5082-0018	5-6
5082-0180*	Step Recovery Diode	5082-0032	5-6
5082-0241	Step Recovery Diode (obsolete)	5082-0032	
5082-0253	Step Recovery Diode	5082-0018	5-9
5082-0300	Step Recovery Diode	5082-0017	5-9
5082-0310	Step Recovery Diode (obsolete)	5082-0021	
5082-0320*	Step Recovery Diode	5082-0020	5-9
5082-0335	Step Recovery Diode		
5082-0800	Step Recovery Diode		5-9
5082-0803	Step Recovery Diode (obsolete)		
5082-0805	Step Recovery Diode (obsolete)		
5082-0810	Step Recovery Diode (obsolete)		
5082-0815	Step Recovery Diode (obsolete)		
5082-0820	Step Recovery Diode (obsolete)	5082-0090	
5082-0821	Step Recovery Diode (obsolete)	5082-0090	
5082-0825	Step Recovery Diode (obsolete)	5082-0090	
5082-0830	Step Recovery Diode	5082-0020	5-9
5082-0833	Step Recovery Diode	5082-0020	5-6
5082-0835	Step Recovery Diode	5082-0008	5-9
5082-0840	Step Recovery Diode	5082-0008	5-6
5082-0885	Step Recovery Diode	5082-0008	5-9
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5082-1002	High Conductance Diode		3-70
5082-1006	High Conductance Diode		3-70
5082-2080	Batch Matched 5082-2835 Schottky		3-64

* Standard Hi-Rel version available, consult your local HP sales representative. ** Hi-Rel version available in package 35 only.

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5082-2201	Batch Matched 5082-2200	HSCH-5317	3-74
5082-2202	Hermetic Stripline Schottky Diode	HSCH-5316	3-74
5082-2203	Batch Matched 5082-2202	HSCH-5317	3-74
5082-2207	Stripline Schottky Diode	HSCH-5316	3-74
5082-2208	Batch Matched 5082-2207	HSCH-5317	3-74
5082-2209	Stripline Schottky Diode	HSCH-5316	3-74
5082-2210	Batch Matched 5082-2209	HSCH-5317	3-74
5082-2231	Low V_F Hermetic Stripline Schottky Quad		†3-80
5082-2233	Low V_F Hermetic Stripline Schottky Quad	HSCH-5836	3-80
5082-2263	Hermetic Stripline Schottky Ring Quad	HSCH-5816	3-80
5082-2271	Low V_F Stripline Schottky Diode Quad		†3-80
5082-2272	Low V_F Stripline Schottky Diode Quad		†3-80
5082-2273	Ku Band Schottky Mixer Diode (obsolete)	5082-0029	
5082-2274	Matched Pair of 5082-2273 (obsolete)	5082-0029	
5082-2277	C-Band Stripline Schottky Ring Quad		†3-80
5082-2279	Low V_F Broadband Stripline Schottky Quad	HSCH-5832	3-80
5082-2280	Low V_F Broadband Stripline Schottky Quad	HSCH-5830	3-80
5082-2291	Stripline Schottky Ring Quad		†3-80
5082-2292	Stripline Schottky Ring Quad		†3-80
5082-2294	Stripline Schottky Ring Quad	HSCH-5810	3-80
5082-2295	X-Band Low V_F Schottky Diode (obsolete)	5082-0013	
5082-2296	Matched Pair of 5082-2295 (obsolete)	5082-0013	
5082-2297	X-Band Low V_F Schottky Diode (obsolete	5082-0013	
5082-2298	Matched Pair of 5082-2297 (obsolete)	5082-0013	
5082-2301	Schottky Barrier Diode		3-64
5082-2302	Schottky Barrier Diode		3-64
5082-2303	Schottky Barrier Diode		3-64
5082-2306	Matched Pair of 5082-2301		3-64
5082-2308	Matched Pair of 5082-2303		3-64
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5082-2356	Matched Encapsulated Bridge Quad		3-64
5082-2370	Matched Quad of 5082-2303 Unconnected		3-64
5082-2396	Matched Encapsulated Ring Quad		3-64
5082-2400	Schottky Barrier Diode		3-84
5082-2401	Matched Pair of 5082-2400		3-84
5082-2520	Schottky Barrier Diode (obsolete)		
5082-2521	Matched Pair of 5082-2520 (obsolete)		
5082-2565	Schottky Barrier Diode (obsolete)		
5082-2566	Matched Pair of 5082-2565 (obsolete)		
5082-2701	X-Band Schottky Mixer Diode (obsolete)	5082-0023	
5082-2702	X-Band Schottky Mixer Diode	5082-0023	3-84
5082-2706	Matched Pair of 5082-2701 (obsolete)	5082-0023	
5082-2707	Matched Pair of 5082-2702	5082-0023	3-84
5082-2711	X-Band Schotky Mixer Diode (obsolete)	5082-0023	
5082-2712	Matched Pair of 5082-2711 (obsolete)	5082-0023	
5082-2713	X-Band Schottky Mixer Diode (obsolete)	5082-0023	
5082-2714	Matched Pair of 5082-2713 (obsolete)	5082-0023	
5082-2723*	Ku Band Schottky Mixer Diode	5082-0029	3-84
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* Standard Hi-Rel version available, consult your local HP sales representative. ** Hi-Rel version available in package.
†Consult your local HP sales representative.

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5082-3170*	Hermetic Stripline PIN Diode	5082-0030	4-52
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* Standard Hi-Rel version available, consult your local HP sales representative. ** Hi-Rel version available in package.
†Consult your local HP sales representative.

Quality Assurance and High Reliability Screening



Quality Assurance Concepts and Methodology

Reliability/Quality Philosophy

Recognizing the increasing importance of microwave component reliability for the consumer, industrial, and military markets, the Communications Components Division (CMCD) of Hewlett-Packard has committed itself to achieve error free performance at all levels of manufacturing and to deliver the highest level of product quality and reliability performance. Three basic ingredients are integrated into the manufacture of reliable microwave components:

- The device must be designed with a technical understanding of the user's applications and quality requirements.
- The device must be manufactured with the optimum state-of-the-art technology for the application.
- Controls must be established in the manufacture of the device.

As a major manufacturer of microwave products, CMCD produces a broad family of many devices. Since it is not practical, technically necessary, nor cost effective to qualify each of these products via life and environmental testing, the logical approach has been to differentiate assembly/package related failure mechanisms from failure modes associated with the wafer fabrication process. This "die process" and "package product" approach to reliability has been a consideration in the new military standards for microelectronic testing/reliability and is used at the CMCD with the following definitions:

- **Die Process Family** consists of devices which have identical wafer processing. This premise recognizes that component geometry and layout of a product will have little impact on reliability because established design rules apply to all products fabricated by the same process.
- **Package/Assembly Family** are those of like construction and are assembled with identical materials, manufacturing controls and operations.

Component reliability estimation can therefore be achieved with a high confidence level from environmental and life testing data derived from various product families. Accelerated stress testing techniques are continuously employed to obtain definitive working knowledge of reliability performance, whereby the resulting information is used to predict long-term device reliability for the intended application.

In-process Control and Reliability Testing

The reliability performance of microwave components can be affected by numerous operations associated with device manufacturing; among these being:

- Wafer fabrication process/ technology
- Device design and layout
- Packaging design
- The manufacturing processes
  - — Wafer fabrication
  - — Package materials
  - — Assembly materials and procedures
- In-process controls
- Final electrical test procedures
- Quality Assurance inspection procedures
- Post-assembly reliability screening

One of the most important aspects of insuring quality and reliability is through adequate in-process controls of these operations. Wafer fabrication controls provide the assembly operation with a high quality and reliable chip, while the process controls associated with the assembly operation assure the optimum in package integrity. The main areas of Quality Assurance process controls may be summarized according to the fabrication and assembly operations:

Quality Assurance Process Controls

Wafer Fabrication	Assembly
Particle count, room and hood ambient Temperature/Humidity control Capacitance vs. Voltage plots Furnace tube cleaning Deionized water checks Metal thickness monitor Metal SEM monitor Inspection of starting material Plating bath in-process monitor Silox phosphorus content monitor	Die visual Die shear test Wire bond pull Incoming package evaluation Pre-seal visual Hermeticity Electrical test Molding compound evaluation

Life and Environmental Stress Tests

To ensure the highest product reliability commensurate with the intended use of the device, numerous life and environmental tests have been designed to assess device performance. The majority of these tests are designed to simulate more extreme operating conditions than would actually be encountered in most practical applications. This ensures the reliability performance of the device relative to its intended application. Typical device testing at CMCD generally comprises the following environmental and life tests:

Life Tests
High Temperature Reverse Bias (HTRB)
Operating Life
High Temperature Operating Life (HTOL)
High Temperature Storage (HTS)

Environmental Tests
Moisture Resistance
Hermeticity
Solderability
Mechanical Shock
Thermal Shock
Lead Fatigue
Temperature Cycling
Vibration Variable Frequency
Vibration Fatigue
Autoclave
Constant Acceleration
Terminal Strength
Salt Atmosphere
Marking Permanency

Specific methods and conditions of these tests are in compliance with MIL-STD-202, MIL-STD-750, and MIL-STD-883 test specifications, depending upon the nature of the device being tested and its functional classification. For more information on these testing programs please refer to the High Reliability section of this catalog.

Reliability Assessment and Prediction

Numerous concepts and mathematical models have been proposed to assess the reliability performance of semiconductor components. Of these, essentially three fundamental parameters are widely used in the industry for reliability assessment and prediction of failure rate:

- The failure rate equation, λ
- The probability of survival, P_S
- The activation energy, E_a

The **Failure Rate** is related to the population of units failed under life testing and the duration of the test as:

$$\lambda = \frac{N_F}{N_o t}$$

where
λ = assessed failure rate
N_F = quantity of failures occurring in a time interval t
N_0 = quantity of acceptable devices at zero hours
t = time interval or duration of test

Generally it is more meaningful to discuss failure rates in terms of the Mean Time To Failures or MTTF, which is the reciprocal of the failure rate and expressed as MTTF= $1/\lambda$. It is important to recognize that both λ and MTTF are statistical averages and apply only to the useful life of the product.

The **Probability of Survival** is the likelihood that a particular device will survive for a given period of operating time and may be expressed as:

$$P_S = e^{-\lambda t} = e^{-t(MTTF)}$$

where
t = operating time of the device
λ = failure rate = 1/MTTF

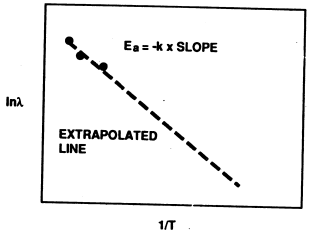
The third mathematical relationship of importance to reliability is expressed in a form of the Arrhenius Equation which relates the rate of a thermally accelerated process to temperature as:

$$\lambda = A \exp^{(-E_a/kT)}$$

or $$\ln\lambda = -E_a/kT + \ln A$$

where
E_a = Activation Energy
k = Boltzmann's Constant (8.62×10^{-5} eV/°K)
T = Temperature in Kelvin (°K)
λ = Failure Rate at Temperature T
A = Constant

A plot of Inλ versus 1/T will yield a straight line as illustrated:



The activation energy E_a can therefore be determined by

$$E_a = -k * (\text{slope})$$

For products which are extremely reliable, the failure rates are too low to be measured within a reasonable test duration. In that case, the failure rate can be determined by stressing parts at an elevated temperature and extrapolating along the straight line, on the plot illustrated above, to the temperature of interest. The temperature of interest can be the junction temperature, the ambient temperature, the case temperature, or whichever conditions the user is most concerned about. In practice, a simplified equation, with a known E_a, can be used for the prediction of failure rates at different temperatures, or for the determination of an acceleration factor, by changing the stress temperature from T1 to T2 expressed as:

$$\ln \frac{\lambda_2}{\lambda_1} = - \frac{E_a}{k} \left(\frac{T1 - T2}{T1 * T2} \right)$$

Reliability Monitor Program

The reliability monitor program is administered and executed by the Quality Assurance Department. The intent of this program is:

- To provide a periodic* evaluation of our product reliability on an on-going basis.
- To maintain a pulse on the fabrication and assembly processes.
- To identify, via long-term stress testing, the limitations of our products and thereby provide future direction for engineering design, development, and manufacturing improvements.

Fabrication and assembly variables were considered in the construction of the matrix to assure that these products would best represent all product families and their associated processes with meaningful volumes.

In addition to the following listed products, all new products must pass an extensive reliability test program prior to introduction. This ensures that the tradition of high quality is upheld in all new devices.

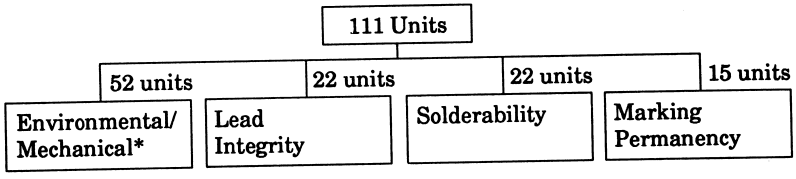
*Periodic is defined as somewhere between 2 and 4 months, depending upon current production volumes. New products will be added to the matrix once volume production is established.

Reliability Monitor Device Matrix

Fab Process	Package Process		Device[1]
GaAs			
Lifted Y Gate	Hermetic		ATF 1XX70
	Plastic		ATF 1XX84
Plated Y Gate	Plastic		ATF 2XX84
PHEMT	Hermetic		ATF 3XX70
	Non-Hermetic		ATF 3XX76
Si Bipolar			
ISOSAT	Hermetic		IAM 81018
	Plastic		IAM 81008
SAT	Hermetic		ATF 4XX70
	Plastic		ATF 4XX85 or MSA XX86
Diodes			
Schottky	Glass		5082-2800 5082-2810 5802-2835
	Plastic		HSMP-28XX HSMS-81XX
	Beam Lead	Hermetic	5082-2202
		Non-Hermetic	5082-2831
PIN	Glass		5082-3080 5082-2839
	Plastic		HSMP-38XX
	Ceramic	Hermetic	5082-3306
	Beam Lead	Hermetic	HPND-4005
High Conductance	Glass		5082-1001
Step Recovery	Glass		5082-0180

Notes:
1. Alternate devices from same fab process and/or package process may also be used.

Reliability Monitor Package Matrix



Hermetic Package:
Hermeticity → Thermal Shock → Mechanical Shock → Hermeticity (sequential)

Plastic Package:
Thermal Shock (or Temp. Cycling) → Autoclave (sequential)

Reliability Monitor Testing

Test	Conditions
Operating Life (O.L.)	1000 hrs. @ Max. Rated Power
High Temperature Reverse Bias (HTRB)[1]	1000 hrs. @ V_R = 80% V_{BR}, and Max. Rated Temperature
Thermal Shock	200 Cycle @ Min./Max. Storage Temperatures
Mechanical Shock*	1500 Gs Y_1, Y_2, X, 0.5 msec Pulse
Hermeticity*	Fine and Gross Leak
Autoclave	121°C, 15 PSIG, 100% RH, 96-hrs.
Solderability	16-hrs. Steam Aging, 245°C, 5 sec Dwell
Marking Permanency	Resistance to 3 Solvent Groups
Torque Test*	Glass-Frit Packages Only
Lead Integrity	Package Dependent

*Hermetic Packages Only.

Note:
1. Applicable only to discrete diodes and transistors.

High Reliability

Complete detail of HP/CMCD's High Reliability capabilities can be found in a separate catalog entitled, "High Reliability Handbook." Please contact your local Hewlett-Packard sales office to obtain a copy. The information that follows is a brief overview of HP/CMCD's capabilities.

The purpose of Hi-Rel testing is to demonstrate the ability of a device to meet electrical performance requirements over a specified lifetime, to a designated confidence level. This is especially critical in military and aerospace applications where the consequences of a device operating improperly could be catastrophic.

For over 20 years, the Communications Components Division (CMCD) of Hewlett-Packard has been extensively involved in providing High Reliability (Hi-Rel) tested devices for military and aerospace oriented programs. The inherent reliability and proven performance of our products has provided a vehicle with which we have built a strong reputation as the vendor of choice in meeting military and space program requirements. HP/CMCD devices are currently qualified for use on the following programs:

AMRAAM
CARA
DSCS III
FLEET SATCOM
GPS
HARM
HARPOON
INEWS
LANTIRN
INTELSAT
MILSTAR
MINUTEMAN
PATRIOT
PHALANX
PHOENIX
SINCGARS
SCOTT
SHUTTLE
STANDARD MISSILE
STINGER
TDRSS
TORNADO
TRIDENT

Hi-Rel Testing

There are numerous Hi-Rel testing specifications used to specify the test programs, methods, and conditions for semiconductors. MIL-S-19500 and MIL-STD-750 are the two most frequently used for discrete devices. MIL-S-19500 is the general specification and defines test sequences to achieve different levels of reliability. MIL-STD-750 defines the actual test methods, conditions, and pass/fail criteria as required by MIL-S-19500. For microelectronic/microcircuit devices, including monolithics and multichip/hybrid devices, MIL-M-38510 and MIL-STD-883 are the two most frequently used military standards. MIL-M-38510 is the general specification, while MIL-STD-883 defines the actual test methods, conditions, and pass/fail criteria as required by MIL-M-38510.

Since a specific test may be performed for a variety of reasons, the most frequently performed categories of testing are described below,

A. Quality Conformance Testing

The most common type of testing of semiconductors is quality conformance testing. This testing is performed on a sample of the lot to determine that the devices in the lot meet electrical and mechanical requirements. In MIL type specifications the essential electrical requirements (Group

A tests) are supplemented by various environmental tests (Group B, C, and D tests) with smaller sample sizes. These Group B and C and D tests measure the capability of the device to operate satisfactorily after exposure to environmental stresses such as mechanical shock, vibration, etc.

B. Qualification Testing
This type of testing is used to determine that the manufacturer of a device can supply devices that meet the full electrical and environmental capability requirements of the customer's specification. In MIL type specifications this testing is required before a device manufacturer is placed on a Qualified Products List (QPL). Periodic requalification may be required after interruptions in production or after specified time intervals. The actual tests performed are the same Group A, B, C, and D tests mentioned above in Quality Conformance Testing. However, the sample sizes are usually larger in qualification testing and some additional tests, not normally performed as part of Quality Conformance Testing, may be required.

C. Screening
The third basic type of testing is variously called screening, preconditioning, or reliability testing. Screening is a special form of 100% testing whose purpose is to eliminate marginal devices that might result in field failures. The assumptions behind screening tests are two-fold. The first assumption is that under normal operating conditions, there are a greater number of failures in the first few hours of operation as compared to the total number of failures over a long period of operation.

The second assumption behind screening tests is that the characteristics of a lot of devices will not be uniform. If the lot is subjected to an appropriate stress level for some screening test such as constant acceleration, a percentage of devices will fail. If the same screening test is then repeated at the same stress level, a much smaller percentage of devices will fail after the second test. The stress level chosen should represent the worst case condition to be experienced in the field. However, it is more usually chosen on the basis of experience with device capability. For example, it is known that well bonded semiconductor devices will withstand 20,000 Gs constant acceleration. Therefore, any device that fails this stress is not suitable for critical use.

The screening tests to be used for a particular device depend on its design and construction, the type of application and environmental conditions and the criticality of the device to mission success. For example, the screening tests used for a device intended for a non-redundant circuit in a long operating life unmanned space vehicle will be much more extensive than the screening tests used for a device intended for field replacement in ground based equipment.

HP/CMCD Hi-Rel Product Offerings

The Communications Components Division (CMCD) of Hewlett-Packard offers three types of Hi-Rel products: Standard Hi-Rel, which includes Standards with Adders; JAN qualified products; Specials; and Customs.

Standard Hi-Rel Products
Since the advantages of products tested to established reliability standards can be of significant value to customers requiring reliable devices, HP/CMCD offers a number of products that have been tested to the same screening level as JANTXV devices. These standard Hi-Rel programs are patterned after the requirements of MIL-S-19500 or MIL-M-38510, as applicable, and offer the following benefits:

1. Eliminate the costly requirement of the buyer's company to generate source control drawings.

2. Offer improved delivery.

3. Provide assistance to those customers required to generate procurement specifications.

The specific Hi-Rel screening tests performed on each device vary depending on its design and construction, complete details of which can be found in a separate CMCD High-Reliability Handbook. Contact your local Hewlett-Packard Sales Office to obtain a copy.

Available Hi-Rel Standard devices from HP/CMCD can be found in the alphanumeric index, at the front of this catalog.

JAN Qualified Products
Since a great number of reliability tested devices are

required for military programs, the JAN system was established by the U.S. Government to provide standardized levels of screening at a minimum cost to all users. There are three major advantages to the JAN type products:

1. First, the specification, and thus the reliability level of the device, is pre-specified for the buyer, thereby eliminating the need for the buyer's company to create special procurement specifications/documentation.

2. Second, JAN devices can be manufactured in large quantities which result in subsequent cost reductions.

3. Third, configuration control is administered by the U.S. Government.

Three levels of JAN Schottky and PIN diodes are offered by HP/CMCD:

1. JAN
   Each lot of these devices has successfully completed Groups A and B testing. Group C testing is performed each 6 months.

   Available JAN devices from HP/CMCD can be found in the alphanumeric index at the front of this brochure and are indicated by the "JAN" prefix.

2. JANTX
   Each lot of these devices has successfully completed 100% screening tests including delta limits. Each lot has also successfully completed Groups A and B testing. Group C testing is performed every 6 months.

   Available JANTX devices from HP/CMCD can be found in the alphanumeric index at the front of this brochure and are indicated by the "JANTX" prefix.

3. JANTXV
   Each lot of these devices has successfully completed a 100% pre-paint internal visual inspection and 100% screening tests including delta limits. Each lot has also successfully completed Groups A and B testing. Group C testing is performed every 6 months.

   Available JANTXV devices from HP/CMCD can be found in the alphanumeric index at the front of this brochure and are indicated by the "JANTXV" prefix.

Standard Hi-Rel Products with Adders

For many of our customers, our standard Hi-Rel device, with its inherent reliability and electrical performance is more than satisfactory for the intended application. These customers, however, may be prevented from purchasing these devices without first obtaining an HP/CMCD quotation, for several reasons:

1. The requirements of the military/aerospace program involved call for the generation of source control drawings.

2. The customer's procurement system calls for the generation of specific source control drawings.

3. The specific procurement documentation created invokes additional screening or administrative requirements above those performed on our Standard Hi-Rel devices.

To satisfy these customers/applications, HP/CMCD has established a family of "Adders" to our standard Hi-Rel devices. The available "Adders" range from Attributes Data to X-Ray and can be categorized as either added Administrative or added Screening requirements.

The available "Adders" offer:

1. Improved availability as the customer requested "Adders" are performed on finished goods inventory of the standard Hi-Rel device.

2. Greater flexibility in meeting the specific needs of the customer while still utilizing standard Hi-Rel devices.

3. The customer the ability to order HP/CMCD standard devices while specifying their own drawing/part number (if one exists).

The available "Adders" can be ordered in any combination as the "Adders" will be performed on devices which have already completed the standard HP/CMCD Hi-Rel processing. NOTE THAT NOT ALL "ADDERS" ARE AVAILABLE FOR EACH PART #.

In the separate CMCD High Reliability handbook you will find tables detailing which "Adders" are available by HP/CMCD part number followed by

a detailed description of each "Adder." and instructions on how to order these "Adders."

Hi-Rel Specials

At HP/CMCD we have a proven track record for handling customer specials. We recognize your special needs and welcome the opportunities provided by the military/aerospace industry. Our Hi-Rel department has extensive knowledge and experience in accommodating special testing, imposed quality levels, or other extra processing. We have a comprehensive drawing review procedure and emphasis is placed on compliance to all requirements of the latest revision of MIL-STD test methods and procedures. If the opportunity warrants, and we are able to satisfy the customer's requirements, HP/CMCD will offer a Hi-Rel Special.

The most common examples of customer requirements which would warrant a special include:

1. Selected electrical performance characteristics.

2. Additional screening tests such as extended burn-in, which are not standardly offered.

Opportunities such as these will be satisfied by utilizing devices which have been processed to the requirements of the generic Standard Hi-Rel part and upgrading it to the customer imposed requirements.

Hi-Rel Customs

In some instances, the customer's application and/or program requirements may require electrical performance or screening tests to be performed that cannot be satisfied with either an HP Standard or Special device type. In these instances, and when the CMCD Hi-Rel opportunity warrants, satisfaction of the customer's needs will be done with a Hi-Rel Custom.

Customer requirements which would warrant an HP custom include:

1. Unique packages and/or package orientations.

2. Unique chip/package combinations.

3. Wafer Selection/Qualification.

4. Unique/Out-of-Sequence Screening tests.

5. Unique burn-in conditions and/or delta limits.

6. S-Level Screening requirements.

7. In-process inspections.

Opportunities such as these are satisfied by building the devices to the detailed customer specifications/drawing.

Design Solutions



HEWLETT PACKARD

Design Solutions

Hewlett-Packard manufactures a wide variety of components to fit your communications design needs. From RF and microwave semiconductor discrete devices and integrated circuits, to subsystem level telecommunication components, HP offers design solutions, all built with the quality and reliability you expect from Hewlett-Packard.

The following section contains generic block diagrams for several applications. Each diagram also serves as a selection guide for components specifically designed or well suited for use in that application. Further information for the products listed on each page can be found within the product sections of this catalog.

These block diagrams represent only a handful of the design solutions HP can provide for you. Please contact your local field sales engineer for further information on these or any other products manufactured by Hewlett-Packard.

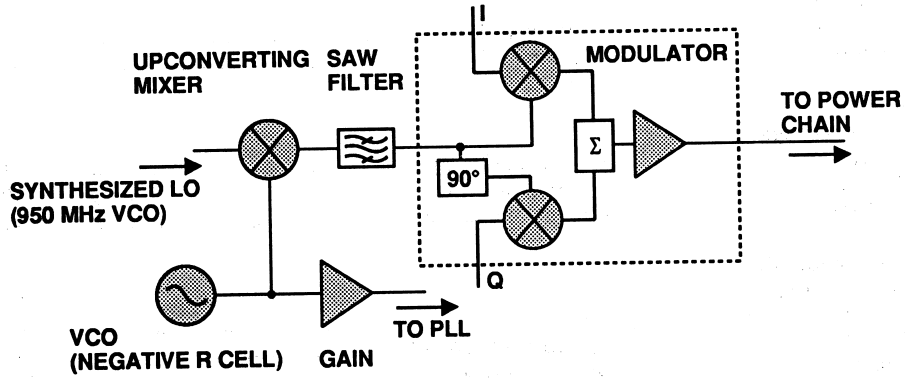
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Cellular Radio

Cellular Handsets put many demands on the high frequency semiconductors they use. Battery operation requires products capable of operating at 5 to 6 Volts for present systems and 3 to 4 Volts for future systems. Low current consumption is critical for extended talk time. Integration is needed for more compact handsets, while competitive price and surface-mount packaging are musts to meet cost targets in a consumer market. Hewlett-Packard provides a wide range of 900 MHz cellular solutions, from diodes and discrete transistors through high frequency Integrated Circuits. The following block diagrams detail significant offerings for cellular handsets.

Cellular Telephone Digital Transmitter

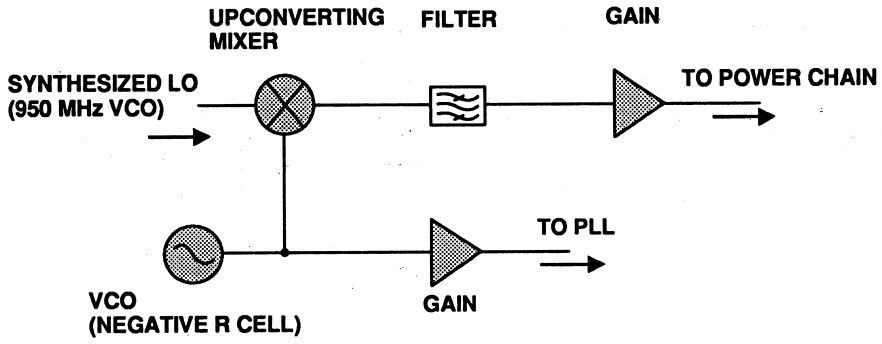


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Si Bipolar Transistors		
for gain, VCO negative R		
AT-60111	Low current, 3 & 6 V data	6-87
AT-60211	Low current, 3 & 6 V data	6-87
AT-00511	General purpose	6-14
AT-41411	General purpose	6-41
AT-41511	General purpose	6-58
AT-60585	General purpose	6-107

Cellular Radio (cont)

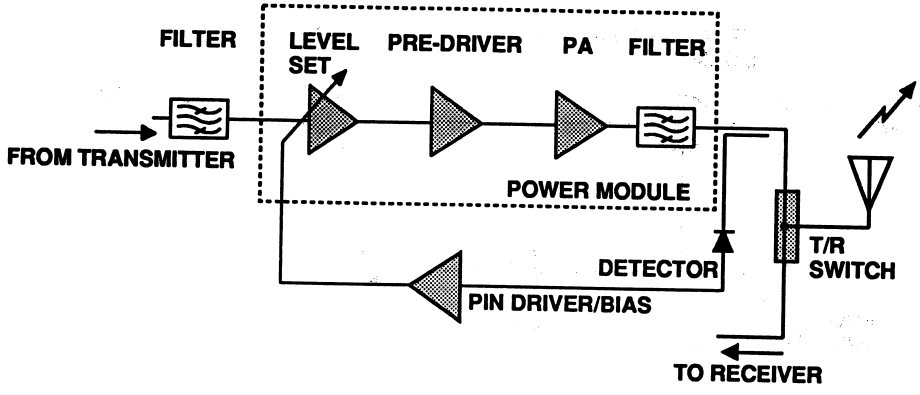
Cellular Telephone Analog Transmitter



		Page No.
Up Converting Mixers		
IAM-81008	5 V Gilbert cell mixer	8-35
IAM-82008	10 V Gilbert Cell @ 5 V	8-39
HSMS-2810	Schottky diode single	3-55
HSMS-2812	Schottky diode pair	3-55
HSMS-2817	Schottky diode quad	3-55
Gain Stage ICs		
INA-03184	22 dB gain, 3.5 V	8-66
MSA-0611	16 dB gain, 5 V	8-134
GaAs FETs		
for gain, VCO negative R		
ATF-21186	750 µm, SMT pkg	7-45
ATF-13284	250 µm, plastic pkg	7-26
ATF-13484	250 µm, plastic pkg	7-30
Si Bipolar Transistors		
for gain, VCO negative R		
AT-60111	Low current, 3 & 6 V data	6-87
AT-60211	Low current, 3 & 6 V data	6-87
AT-00511	General purpose	6-14
AT-41411	General purpose	6-41
AT-41511	General purpose	6-58
AT-60585	General purpose	6-107

Cellular Radio (cont)

Cellular Telephone Power Chain



		Page No.
Pre-Driver Transistors		
AT-42086	+20 dBm Si BJT	6-81
ATF-21186	+20 dBm GaAs FET	7-45
MMIC Drivers		
HPMX-3002	+23 dBm 30 dB gain with power control	8-30

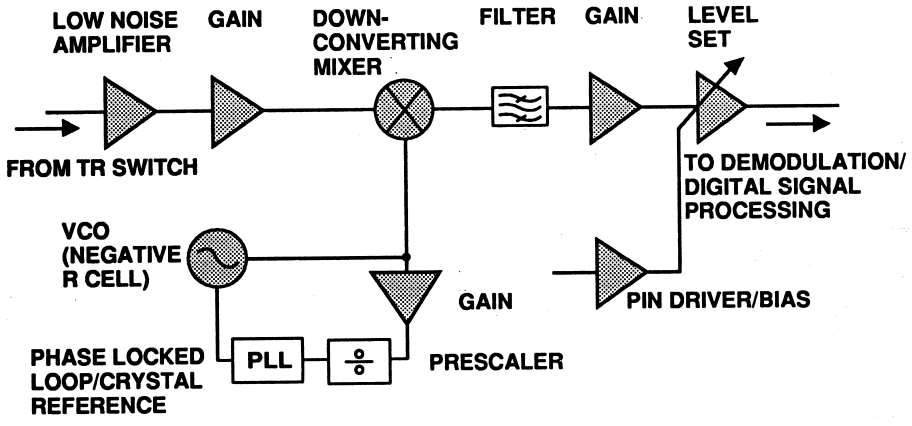
Power Modules

Please contact the factory for recent releases in high power discrete GaAs FET and bipolar Transistors, ICs, and Power Modules for Global System for Mobile communications (GSM), Japan Digital Cellular (JDC), and North American Digital Cellular (NADC) systems.

T\R Switch		
HSMP-3890	Low current PIN diodes	4-25
HSMP-3892	Low current PIN diodes	4-25
HSMP-3893	Low current PIN diodes	4-25
HSMP-3894	Low current PIN diodes	4-25
Level Set		
HSMP-3810	Surface mount PIN diodes	4-25
HSMP-3812	Surface mount PIN diodes	4-25
HSMP-3813	Surface mount PIN diodes	4-25
HSMP-3814	Surface mount PIN diodes	4-25
Detector		
HSMS-2810	Surface mount Schottky diodes	3-55

Cellular Radio (cont)

Cellular Telephone Receiver



Cellular Radio (cont)

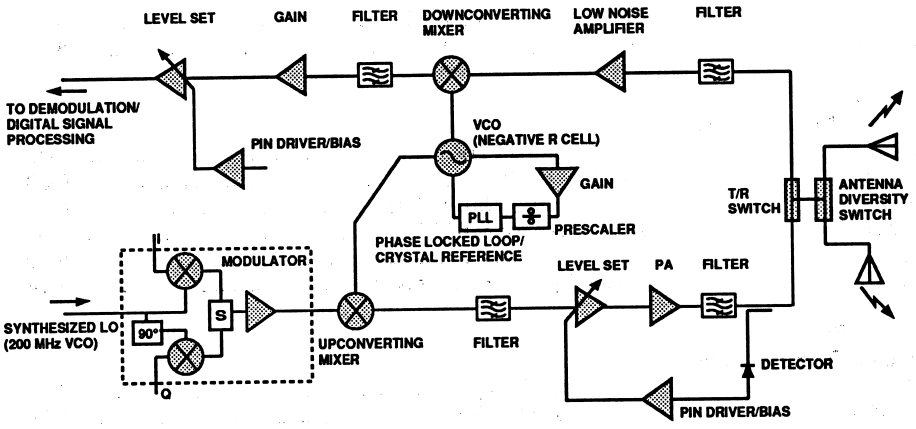
Cellular Telephone Receiver

		Page No.
Discrete BJTs		
for LNA, gain, VCO Negative R cell		
AT-41411	50Ω Γ_{opt} 1.5 dB NF	6-41
AT-41511	50Ω Γ_{opt} 1.5 dB NF	6-58
AT-60111	Low current, 3 & 6 V data	6-87
AT-60211	Low current, 3 & 6 V data	6-87
AT-60585	General purpose transistors	6-107
AT-00511	General purpose transistors	6-14
Discrete GaAs FETs		
for LNA, gain, VCO Negative R cell		
ATF-21186	750 µm SMT pkg	7-45
ATF-13284	250 µm plastic pkg	7-26
ATF-13484	250 µm plastic pkg	7-30
MMICs		
for LNA, gain		
MSA-0611	5 V, 16 dB	8-134
INA-03184	3.5 V, 22 dB	8-66
Down Converting Mixer		
IAM-81008	5 V Gilbert Cell	8-33
IAM-82008	10 V Gilbert Cell @ 5 V	8-39
HSMS-2810	Surface mount Schottky diodes	3-55
HSMS-2812	Surface mount Schottky diodes	3-55
HSMS-2817	Surface mount Schottky diodes	3-55
Level Set		
HSMP-3810	Surface mount PIN diodes	4-25
HSMP-3812	Surface mount PIN diodes	4-25
HSMP-3813	Surface mount PIN diodes	4-25
HSMP-3814	Surface mount PIN diodes	4-25

Personal Communications Systems

Personal Communications Systems (PCS, PCN, PHP, DCS-1800) have many of the same requirements as cellular telephones. Operating voltages and currents compatible with 6 or 3 volt batteries are a must: integrated circuits and surface mount packages are needed to keep handsets pocket-sized or smaller and to allow volume production. Additionally, the higher operating frequency around 1.9 GHz requires the use of significantly faster semiconductors. Hewlett Packard's high speed analog silicon bipolar and Gallium Arsenide processes are ideal vehicles for producing a full range of PCS products.

Personal Handy Phone (PHP)



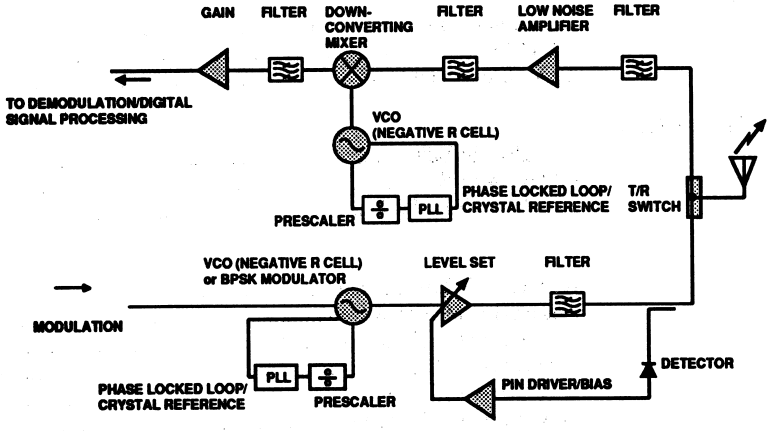
Personal Communications Systems (cont)

		Page No.
Modulators		
HPMX 2XXX series	Mixer pairs, direct and dual conversion Vector modulators	8-7 – 8-27
Up Converting and Down Converting Mixers		
IAM-81008	5 V Gilbert cell mixer	8-33
IAM-82008	10 V Gilbert cell @ 5 V	8-39
HSMS-28XX	Schottky diodes, pairs and quads	3-55
Gain Stage ICs		
INA-03184	22 dB gain, 3.5 V RF IC	8-66
MSA-0611	16 dB gain, 5 V, IF IC	8-134
Discrete BJTs		
for LNA, gain, Negative R cell		
AT-41411	50Ω Γ_{opt} 1.5 dB NF	6-41
AT-41511	50Ω Γ_{opt} 1.5 dB NF	6-58
AT-60111	Low current, 3 & 6 V data	6-87
AT-60211	Low current, 3 & 6 V data	6-87
AT-60585	General purpose Transistors	6-107
AT-00511	General purpose Transistors	6-14
Discrete GaAs FETs		
for LNA, gain, Negative R cell		
ATF-21186	750 µm SMT pkg	7-45
ATF-13284	250 µm plastic pkg	7-26
ATF-13484	250 µm plastic pkg	7-30
Power Amplifier Transistors		
AT-42086	+20 dBm Si BJT	6-81
ATF-21186	+20 dBm GaAs FET	7-45
T\R Switch		
antenna diversity switch		
MGS-70008	Reflective MMIC switch	9-45
MGS-71008	Absorptive MMIC switch	9-51
HSMP-3890	Low current PIN diodes	4-25
HSMP-3892	Low current PIN diodes	4-25
HSMP-4890	Low current PIN diodes	4-25
Gain Control/Level Set		
HSMP-3810	Surface mount PIN diodes	4-25
HSMP-3812	Surface mount PIN diodes	4-25
HSMP-4810	Surface mount PIN diodes	4-25
Detector		
HSMS-2810	Surface mount Schottky diodes	3-55

Cordless Telephones

The primary demand of the cordless telephone designer is performance at a very economical price. High performance discrete transistors are the best solution to this requirement. As new generation phones move to digital transmission and add features such as encryption for privacy, some of the cellular ICs also find their way into cordless telephones. Hewlett-Packard has a complete line of discrete transistors, both silicon bipolar and Galium Arsenide, that answer the needs of these systems.

Cordless Telephone



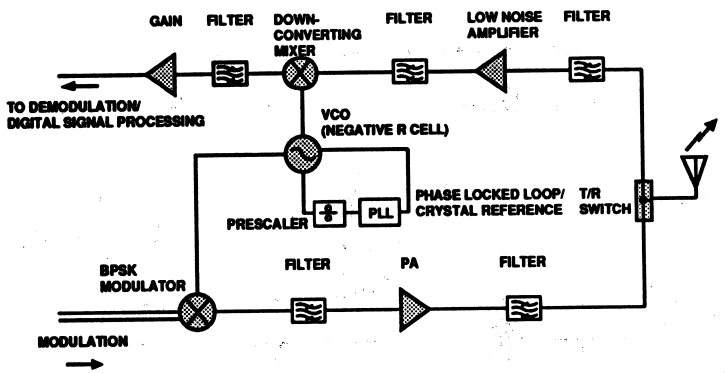
Cordless Telephones (cont)

		Page No.
Discrete BJTs		
for LNA, gain, mixer, VCO Negative R cell,		
AT-00511	Economic, general purpose transistors	6-14
AT-41511	Economic, general purpose transistors	6-58
Discrete GaAs FETs		
for LNA, gain, mixer, VCO Negative R cell		
ATF-21186	750 µm SMT pkge	7-45
BPSK/FSK Modulators		
HPMX 2001	High impedance mixer pair	8-7
IAM-81008	5 V Gilbert cell mixer	8-35
IAM-82008	10 V Gilbert cell @ 5 V	8-39
Power Amplifier Transistors		
AT-41486	+16 dBm Si BJT	6-55
AT-42086	+20 dBm Si BJT	6-81
ATF-21186	+20 dBm GaAs FET	7-45
T\R Switch		
MGS-70008	Reflective MMIC switch	9-45
MGS-71008	Absorptive MMIC switch	9-51
HSMP-3820	Low current PIN diodes	4-25
HSMP-3822	Low current PIN diodes	4-25
HSMP-3890	Low current PIN diodes	4-25
HSMP-3892	Low current PIN diodes	4-25
Gain Control/Level Set		
HSMP-3810	Surface mount PIN diodes	4-25
HSMP-3812	Surface mount PIN diodes	4-25
HSMP-3813	Surface mount PIN diodes	4-25
HSMP-3814	Surface mount PIN diodes	4-25
Detector		
HSMS-2800	Surface mount Schottky diodes	3-55
HSMS-2810	Surface mount Schottky diodes	3-55

Commercial Wireless/ Spread-Spectrum Transceivers

The deregulation of FCC part 15 has opened the marketplace to many different transceiver products, from remote meter readers to private information systems. There is also a growing interest in microwave "tags", for inventory control, remote toll paying, etc. The commodity nature of these applications once again focuses the designer on functionality at a very economic price. High performance discrete transistors plus select cost effective MMICs are the best solutions to these requirements. Many of the products used in these designs also find homes in cordless telephones or digital cellular systems. Hewlett-Packard's silicon bipolar and Gallium Arsenide technologies allow for a wide range of product offerings.

Spread-Spectrum Transceiver

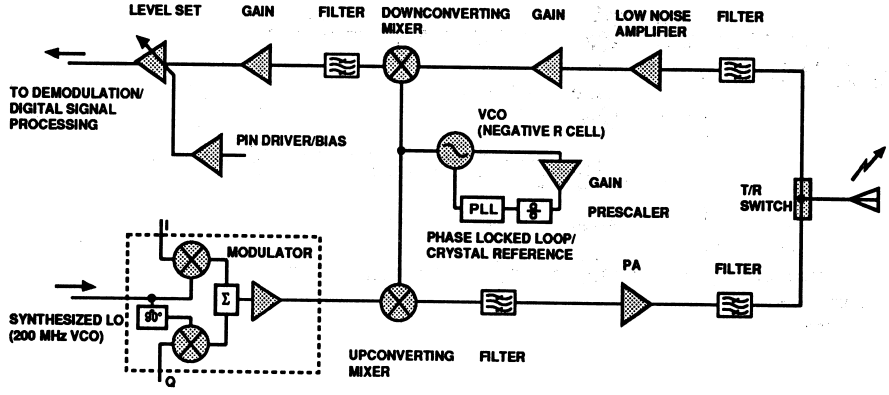


		Page No.
Discrete BJT		
for LNA, gain, mixer, VCO Negative R cell,		
AT-00511	Economic, general purpose transistors	6-14
AT-41511	Economic, general purpose transistors	6-58
Power Amplifier Transistors		
AT-41486	+16 dBm Si BJT	6-55
AT-42086	+20 dBm Si BJT	6-81
ATF-21186	+20 dBm GaAs FET	7-45
Discrete GaAs FETs		
for LNA, gain, mixer, VCO Negative R cell		
ATF-21186	750 µm SMT pkg	7-45
BPSK /FSK Modulators		
HPMX-2001	High impedance mixer pair	8-7
IAM-81008	5 V Gilbert cell mixer	8-35
IAM-82008	10 V Gilbert cell @ 5 V	8-39
T\R Switch		
MGS-70008	Reflective MMIC switch	9-45
MGS-71008	Absorptive MMIC switch HSMP-3890	9-51
HSMP-3892	Low current PIN diodes	4-25

Wireless Local Area Networks (LANs)

Wireless LANs require high performance semiconductors capable of processing gigabits of data each second with virtually non-existent error rates. Some LANs use licensed frequency bands, but the majority make use of the FCC part 15 ISM frequencies, especially in the 2.4 GHz band. The electrical functions are similar to those of a digital telephone, so many of the products used for PCS also work well for LAN designs, including LANs for laptops. Additionally, the designer of LANs for desktop computers can also take advantage of many high performance semiconductors that require higher operating voltages or currents than are acceptable in battery operated equipment.

2.4 GHz digital LAN



Wireless Local Area Networks (cont)

		Page No.
Modulators		
HPMX 2XXX series	Mixer pairs, direct and dual conversion Vector modulators	8-7 — 8-27
Up Converting and Down Converting Mixers		
IAM-81008	5 V Gilbert cell mixer	8-35
IAM-82008	10 V Gilbert cell mixer	8-39
HSMS-28XX	Schottky diodes, pairs and quads	3-55
Gain Stage ICs		
INA-XXX	Low noise, high gain ICs	8-62 – 8-68
MSA-XXXX	General purpose 50 Ω gain block	8-70 – 8-209
Discrete BJTs		
for LNA, gain, Negative R cell		
AT-60111	Low current, 3 & 6 V data	6-87
AT-60211	Low current, 3 & 6 V data	6-87
AT-60585	General purpose transistors	6-107
AT-00511	General purpose transistors	6-14
AT-41411	General purpose transistors	6-41
AT-41511	General purpose transistors	6-58
Discrete GaAs FETs		
for LNA, gain, Negative R cell		
ATF-21186	750 µm SMT pkg	7-45
ATF-13284	250 µm plastic pkg	7-26
ATF-13484	250 µm plastic pkg	7-30
Power Amplifier Transistors		
AT-42086	+20 dBm Si BJT	6-81
ATF-21186	+20 dBm GaAs FET	7-45
T\R Switch		
MGS-70008	Reflective MMIC switch	9-45
MGS-71008	Absorptive MMIC switch	9-51
HSMP-3890	Low current PIN diodes	4-25
HSMP-3892	Low current PIN diodes	4-25
Gain Control/Level Set		
HSMP-3810	Surface mount PIN diodes	4-25
HSMP-3812	Surface mount PIN diodes	4-25

Please contact the factory for other recent releases in high frequency transmitter and receiver products.

RF Components for RF/ID and RF Tags

- **Inventory Management**
- **Automotive Toll Debiting**
- **Security and Personnel Identification**
- **Retail Pricing and Inventory Control**
- **Factory Automation**
- **Automatic Identification**
- **IVHS & Vehicle Identification**
- **RF Data Communication (RF/DC)**
- **Remote Sensing**

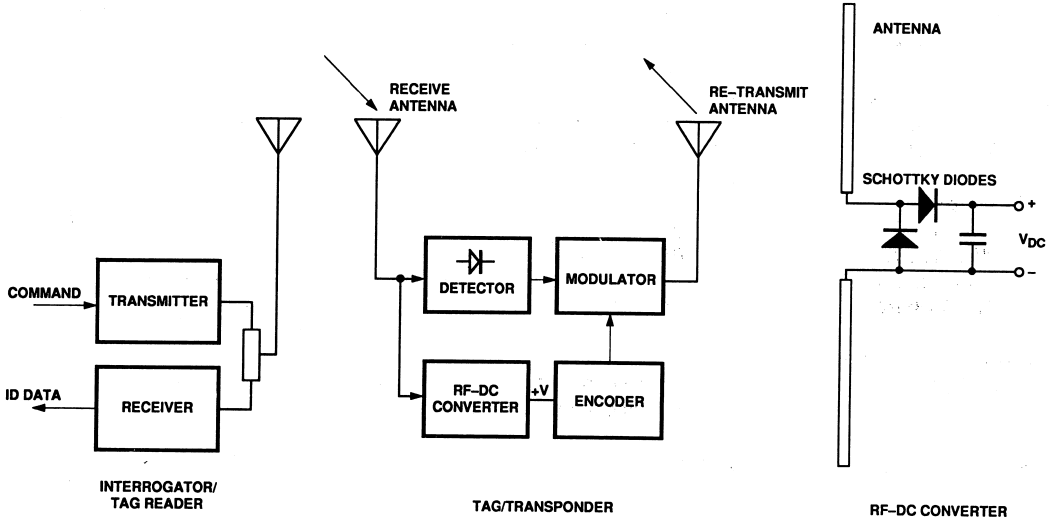
Radio Frequency/Identification (RF/ID) techniques and RF Tags are used for non-contact, wireless identification systems. These applications utilize a RF transmitter-receiver unit (interrogator) to query a transponder or tag located at distance. The tag detects the interrogating signal and transmits a response signal back to the interrogator's receiver. The response signal is encoded with data which may be as simple as 1-bit (tag is present or absent) to a serial stream of data. Operating frequencies are typically in the 900 MHz to 6 GHz range.

Batteryless transponders use Schottky diodes to detect an interrogating signal and re-transmit the fundamental or a harmonic directly back to the interrogator. Batteryless transponders may also use Schottky diodes to rectify a portion of the received RF to supply direct current bias to power transponder electronics. Schottky diodes with high rectification efficiency are essential for this function.

Transponders with batteries make use of high sensitivity Schottky diodes to detect and demodulate the interrogating signal and to activate transponder electronics from a power conserving standby mode.

Hewlett-Packard Schottky diodes are available in a wide range of electrical selections and package configurations to meet the requirements of all types of tag systems and operating frequencies. Options include multiple diode packaging for voltage multiplying RF rectifiers and detectors.

Hewlett-Packard also offers a complete line of product solutions for receivers and transmitters in Tag Readers and Interrogators.



RF Components for RF/ID and RF Tags (cont)

		Page No.
RF Detector		
HSMS-28XX	Schottky diodes, 900 MHz to 3 GHz	3-55
HSMS-8101	Schottky diode, 3 GHz to 16 GHz	3-61
HSCH-3486	Zero bias Schottky diode detector	3-46
RF to DC Converter		
HSMS-2800, 2810, 2820	Schottky diodes to 3 GHz	3-55
HSMS-2802, 2812, 2822	Schottky diode pairs for voltage doublers to 3 GHz	3-55
HSMS-8202	Schottky diode pairs for voltage doublers to 16 GHz	3-61
Interrogators & Tag Readers		
AT, ATF series	Silicon and GaAs low noise and medium power transistors	6-3, 7-4
MSA, INA, series	Silicon MMIC amplifiers	8-3 – 8-5
HSMS series	Schottky diodes for mixers and detectors	3-7 – 3-10
HSMP series	PIN diodes for T/R switches and AGC attenuators	4-25
MSF, IAM series	Silicon MMIC mixers	8-5

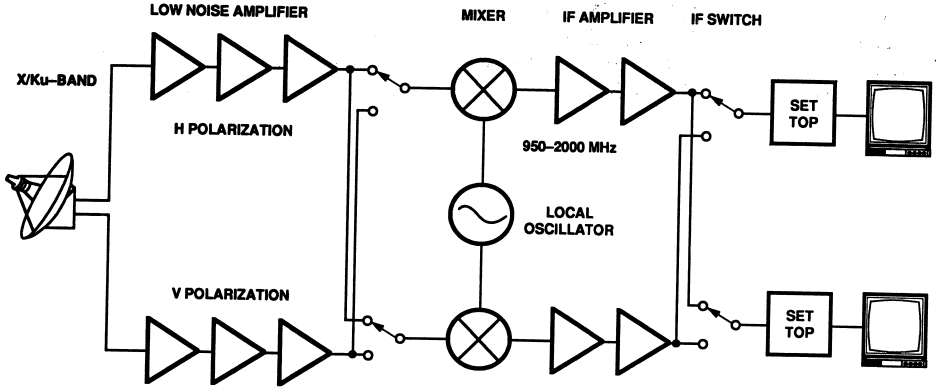
Ku-Band LNB Solutions for Direct Broadcast Satellite

The Low Noise Block (LNB) downconverter converts the DBS X/Ku-band signals to a lower intermediate frequency in the 950 to 2000 MHz range where the signals are then processed for TV viewing.

Low noise preamplification is accomplished by the use of low noise Gallium Arsenide PHEMT or MESFET devices. The mixer uses either matched Schottky diode pairs in a passive, balanced mixer or a MESFET as an active mixer that provides conversion gain. A GaAs FET dielectric resonator oscillator with parallel feedback provides a low phase noise source for the local oscillator.

IF amplification can be provided by either discrete bipolar transistors in a feedback amplifier configuration or by the use of silicon MMIC amplifiers.

PIN diodes or GaAs MMICs are used for IF switches in dual polarization designs.



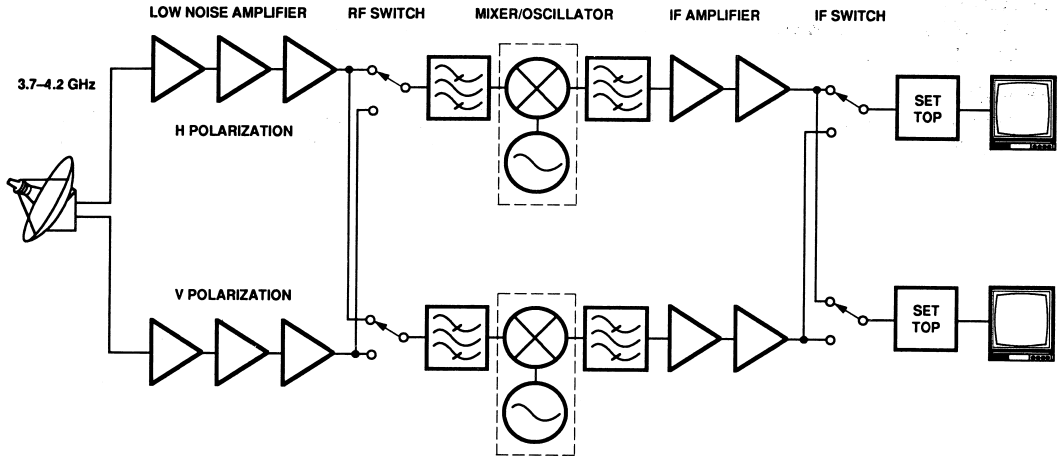
Ku-Band LNB Solutions for Direct Broadcast Satellite (cont)

		Page No.
Low Noise Amplifier		
ATF-35XXX	Low noise GaAs PHEMT, 0.75 dB NF @ 12 GHz	7-73
ATF-13XXX	Low noise GaAs FET	7-4
Mixer		
HSMS-8202	Matched Schottky diode pair for X /Ku-band mixers in SOT-23 package	3-61
ATF-13484, 137XX	GaAs FET for active mixer stage	7-4
Local Oscillator		
ATF-13786, 13484, 26884	GaAs FET for 10 GHz oscillator, +10 dBm P_{out}	7-4
IF Amplifier		
INA-10386, 03184; MSA-0886	25 dB gain silicon MMIC amplifiers	8-3, 8-4
AT-41511, 00511	2.5 dB NF bipolar transistor	6-58
IF Switch		
HSMP-382X, 389X	Surface mount PIN switching diodes	4-25
MGS-70008	DC-3 GHz GaAs MMIC SPDT switch	9-45

C-Band LNB Solutions for Television Receive Only

The Low Noise Block (LNB) downconverter of a Television Receive Only (TVRO) system converts C-band satellite signals to an intermediate frequency in the 950 to 1450 MHz range. The IF signal is further processed by a set top unit for viewing on a TV. Low noise preamplification is best accomplished by the use of low noise Gallium Arsenide PHEMT or MESFET devices. The mixers can use either matched Schottky diode pairs in a passive balanced mixer or a silicon MMIC self oscillating mixer. IF amplification can be provided by either discrete bipolar transistors in a feedback amplifier or by the use of silicon MMIC amplifiers.

PIN diodes or GaAs MMICs are used for RF and IF switching in dual polarization configurations.



C-Band LNB Solutions for Television Receive Only (cont)

		Page No.
Low Noise Amplifier		
ATF-35XXX	Low noise PHEMT, 0.3 dB NF at 4 GHz	7-73
ATF-13XXX	Low noise GaAs FET	7-4
RF Switch		
HSMP-389X, 489X	Surface mount PIN switching diodes	4-25
Mixer/Local Oscillator		
MSF-8885	Silicon MMIC self oscillating mixer	8-209
Mixer		
HSMS-8202	Matched Schottky diode pair, SOT-23 package	3-61
Local Oscillator		
ATF-13786, 13484, 26884	GaAs FET for 4 GHz oscillator	7-4
AT-41511	Silicon bipolar transistor	6-58
IF Amplifier		
INA-10386, 03184; MSA-0886	25 dB gain silicon IC amplifiers	8-3, 8-4
AT-00511	2.5 dB NF bipolar transistor	6-14
IF Switch		
HSMP-382X, 389X	Surface mount PIN switching diode pairs	4-25
MGS-70008	DC-3 GHz GaAs MMIC SPDT switch	9-45

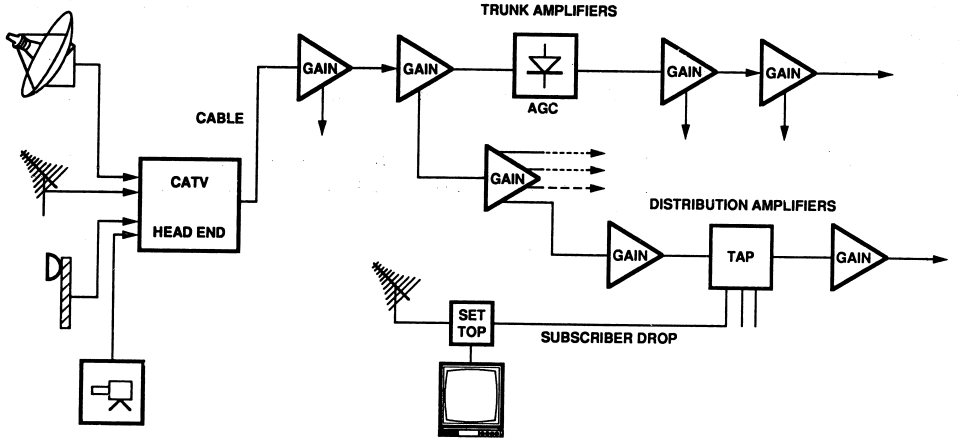
RF Solutions for CATV Distribution & Set Tops

Distribution

Television signals from multiple sources are combined by the head-end into a frequency band suitable for cable distribution. Typical cable bands are in the frequency ranges of 50 to 300/ 500 MHz and 30 to 870 MHz. From the head-end, the signals enter the distribution trunk where the amplifiers responsible for maintaining signal strength must have low noise and low distortion. Signal amplitude is controlled with AGC circuits using low distortion PIN attenuator diodes or variable gain silicon MMICs.

Signals from the trunk line are split and distributed by feeder lines with bridger, line extension, and active tap amplifiers before arriving at the subscriber drop.

The distribution amplifiers require wide bandwidth, cascadability, low noise, and low distortion to sustain high picture quality. These demands are best met with the MSA and INA series of silicon MMIC amplifiers.



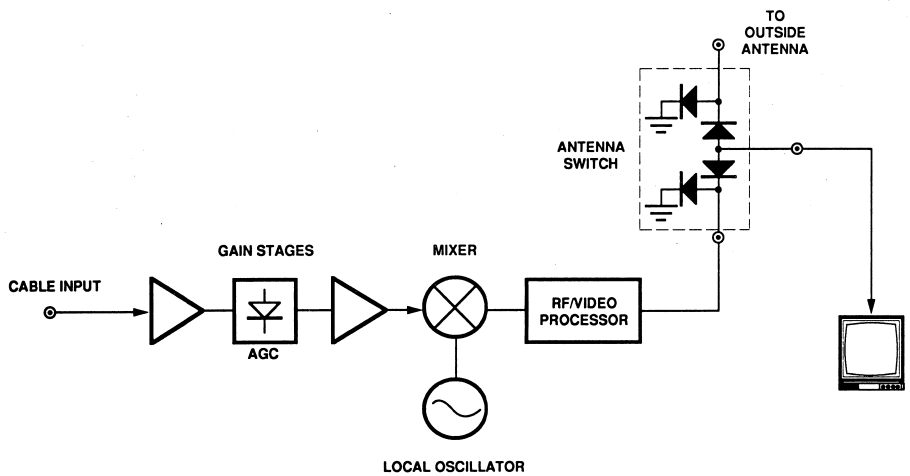
		Page No.
Distribution Amplifiers		
MSA-0886	Silicon MMIC amplifier, 300 MHz f_{3dB}, 32 dB gain, 61 dBmV P_{1dB}	8-164
INA-02186	Silicon MMIC amplifier, 800 MHz f_{3dB}, 30 dB gain, 60 dBmV P_{1dB}	8-58
MSA-1105	Silicon MMIC amplifier, 1300 MHz f_{3dB}, 12 dB gain, 66 dBmV P_{1dB}	8-183
INA-03184	Silicon MMIC amplifier, 2800 MHz f_{3dB}, 25 dB gain, 47 dBmV P_{1dB}	8-66
AGC		
HSMP-3810, 3812	Surface mount PIN attenuator diodes	4-25
IVA-05208	Variable gain silicon MMIC amplifier	10-102

RF Solutions for CATV Distribution & Set Tops (cont)

Set Top Converters

CATV set top heterodyne converters accept signals from the cable, downconvert, and process the signals for viewing with a television receiver.

Silicon MMICs provide effective solutions for gain stages and broadband mixers. Schottky diodes can be used in balanced mixers requiring wide dynamic range. AGC is accomplished by using either PIN attenuator diodes or a silicon MMIC variable gain amplifier. Silicon bipolar transistors are used in the local oscillator. PIN switching diodes provide a reliable means of switching the television receiver input between a TV broadcast antenna and the cable system.



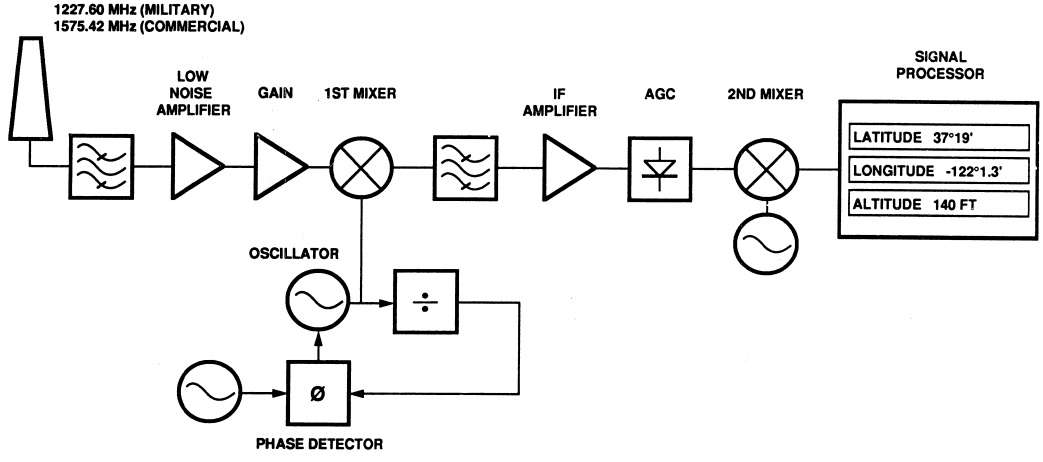
		Page No.
Gain Stage		
MSA-0104, 0204	Silicon MMIC amplifier, medium gain	8-72, 8-84
MSA-0885	Silicon MMIC amplifier, high gain	8-162
MSA-1105	Silicon MMIC amplifier, high IP_3	8-183
Mixer		
HSMS-2802, 2812	Matched Schottky diode pairs	3-55
HSMS-2807, 2817	Matched Schottky diode quads	3-55
IAM-81008	MMIC active mixer	8-35
MSF-8885	Self oscillating mixer	8-209
Oscillator		
AT-00511, 41511	Bipolar oscillator transistors	6-14, 6-58
AGC		
HSMP-3810, 3812	Surface mount PIN attenuator diodes	4-25
IVA-05208	Variable gain silicon MMIC amplifier	10-102
Antenna Switch		
HSMP-382X, 389X	Surface mount PIN switching diodes	4-25

RF Solutions for Global Positioning System

The RF front end of a Global Positioning System (GPS) converts the frequency of signals appearing at the antenna to a lower intermediate frequency where the data are digitally processed to accurately determine the user's geographic position.

Low noise preamplification is obtained by using either low noise Gallium Arsenide MESFETs, low noise bipolar transistors, or silicon MMICs. Very low current bipolar transistors are optimized for use in battery operated receivers.

Mixer functions can be accomplished by using silicon MMICs or Schottky diodes. Silicon MMICs or PIN attenuator diodes are used for the AGC. Bipolar transistors provide a low phase noise solution for the local oscillator.



RF Solutions for Global Positioning System (cont)

		Page No.
Low Noise Amplifier		
ATF-21186, 10136, 13284	Low noise GaAs FET	7-4
AT-41411	Low noise bipolar transistor	6-41
AT-60111	Low current, low noise bipolar transistor	6-87
Gain Stage		
INA-03184	Silicon MMIC amplifier	8-66
AT-60211	Low current, bipolar transistor	6-87
AT-41411	Low noise bipolar transistor	6-41
1st Mixer		
HSMS-2802, 2812	Matched Schottky diode pair	3-55
HSMS-2807, 2817	Matched Schottky diode quad	3-55
IAM-81008	Silicon MMIC active mixer	8-35
Oscillator		
AT-00511, AT-41411	Bipolar oscillator transistors	6-14, 6-41
Phase Detector		
HSMS-2802, 2807	Matched Schottky diode pairs, quads	3-55
IF Amplifier		
INA-03184; MSA-0611	25 dB gain silicon MMIC amplifiers	8-66, 8-134
AT-60211	Low current, bipolar transistor	6-87
AT-00511, 41511	Bipolar transistors	6-14, 6-58
AGC		
HSMP-3810, 3812	Surface mount PIN attenuator diode	4-25
IVA-05208	Variable gain silicon MMIC amplifier	10-102
2nd Mixer		
HSMS-2807, 2817	Matched Schottky diode pairs, quads	3-55
IAM-81008	Silicon MMIC active mixer	8-35

Millimeter Wave & RF Solutions for Collision Avoidance Radar

Vehicle collision warning/ avoidance features are based on FM-CW Doppler or pulse Doppler radars operating at typical frequencies of 24, 60, or 77 GHz.

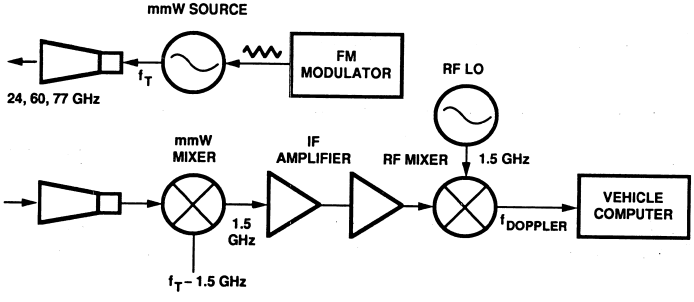
The simplest radar sensor approach uses a homodyne front end in which a portion of the transmitter power is used for the receiver local oscillator. This zero frequency IF design results in a direct output of the Doppler frequency shift.

Use of a heterodyne (non-zero IF) improves S/N ratio by reducing 1/f noise, thus reducing transmitter output power requirements. Typical IFs for heterodyne systems are in the 1 to 2 GHz range.

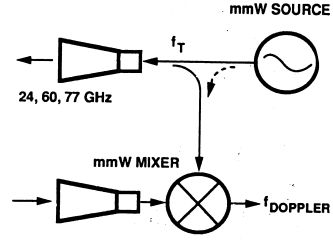
Hewlett-Packard's broad selection of millimeter wave GaAs Schottky diodes includes monolithic, matched pairs for use in balanced mixer down-converters and anti-parallel pairs for application in mixers with subharmonic local oscillators.

The f_{MAX} of Hewlett-Packard GaAs PHEMTs extend to 150 GHz and MESFETs to 100 GHz to meet the high frequency needs of radar sensors.

The IF signal of heterodyne type sensors is amplified by the use of either silicon bipolar transistors or silicon MMICs.



HETERODYNE FM–CW RADAR SENSOR



HOMODYNE FM–CW RADAR

Millimeter Wave & RF Solutions for Collision Avoidance Radar (cont)

		Page No.
mmWave Source		
ATF-35XXX	GaAs PHEMTs with 150 GHz f_{MAX}, 100 GHz f_T	7-73
ATF-131XX	GaAs MESFETs with 100 GHz f_{MAX}, 40 GHz f_T	7-4
mmWave Mixer		
HSCH-9201	Monolithic GaAs Schottky diode series pair for balanced mixers	3-39
HSCH-9251	Monolithic GaAs Schottky diode anti-parallel pair for subharmonic LO mixers	3-39
RF Local Oscillator		
AT-00511, 41511	Silicon bipolar transistor	6-14, 6-58
RF Mixer		
HSMS-28XX	Matched silicon Schottky diode pairs/quads	3-55
IF Amplifier		
INA-03184	25 dB gain silicon MMIC amplifiers	8-66
MSA-0611	25 dB gain silicon MMIC amplifiers	8-134
AT-41411	Low noise bipolar transistors	6-41
AT-41511	Low noise bipolar transistors	6-58
AT-00511	Low noise bipolar transistors	6-14

Silicon Bipolar IC Solutions for Gigabit Links

Workstations, mainframes, and supercomputers that require point-to-point Gigabit links can now be built using the HDMP-1000 Gigabit rate transmit/receive chip set.

Mux, demux, high speed clock generation, and clock recovery circuits are all included on-chip. The transmitter also includes a 50 Ω / 75 Ω coaxial line driver.

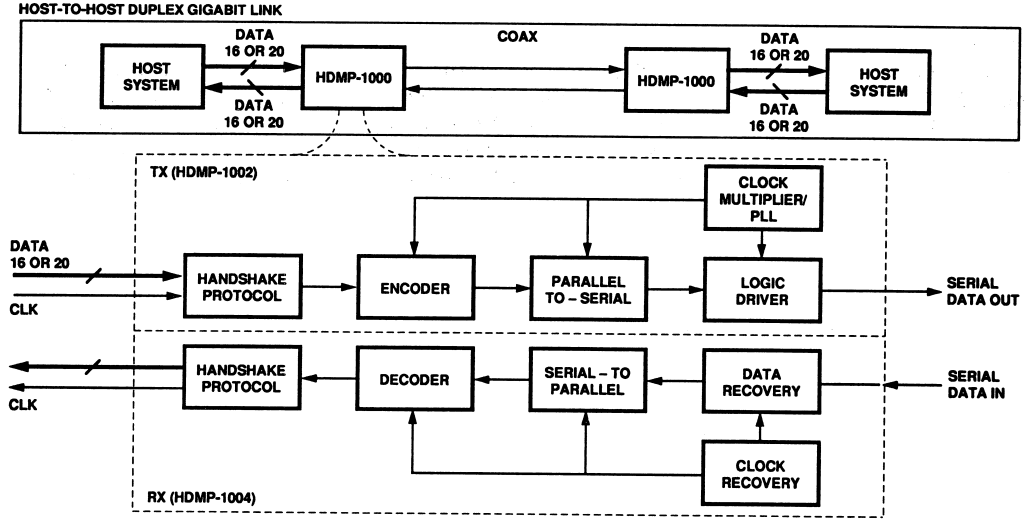
Link start-up and handshaking are functionally supported on-chip. User selectable data rates range from 110 MBaud to 1640 MBaud.

This chip set implements both the SCI-FI standard and serial HiPPI specification. The ICs can be used to design backplane extenders and ribbon cable replacements.

Simplex operation is also supported. This makes the HDMP-1000 attractive for applications such as image acquisition, digitized video distribution and transmission of high speed computer graphics which frequently requires simplex operation.

These Gigabit chips are manufactured using Hewlett-Packard 25-GHz f_T silicon bipolar process.

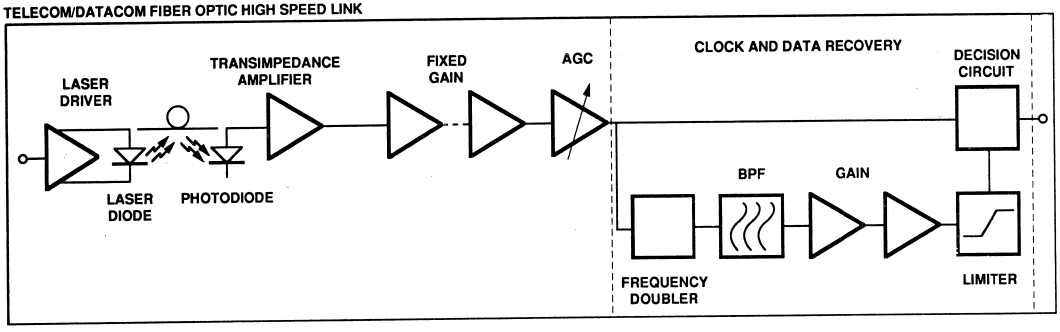
Refer to page 10-5 for more details.



Silicon Bipolar Solutions for High Speed Telecom/ Datacom Interface ICs

The design of high speed fiber optic links for telecom and datacom applications operating up to 2.8 Gb/s can be greatly simplified by using Hewlett-Packard's silicon bipolar MMIC products. Products range from a laser diode driver to a complete clock and data recovery circuit for 622 Mb/s SONET/ SDH applications (HDMP-2501).

TELECOM/DATACOM FIBER OPTIC HIGH SPEED LINK



Silicon Bipolar Solutions for High Speed Telecom/Datacom Interface ICs (cont)

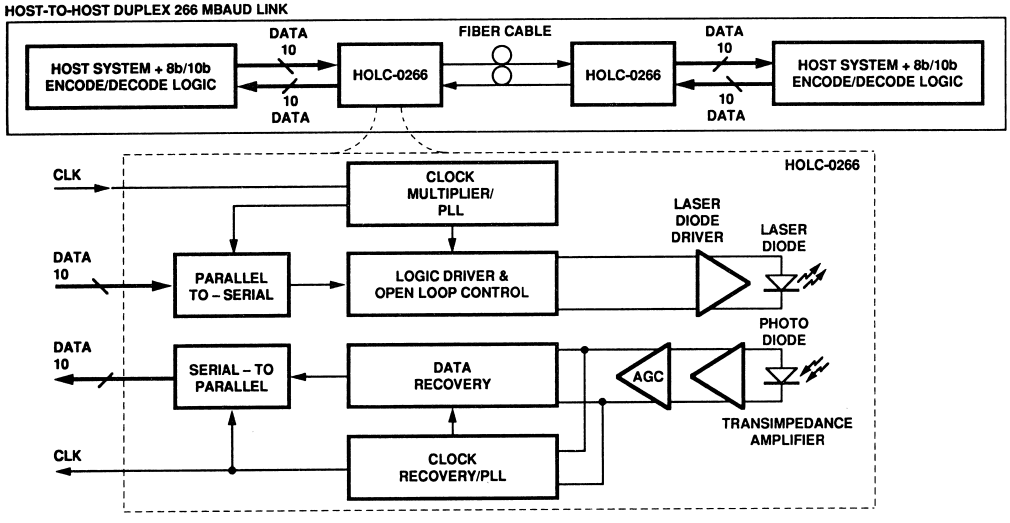
		Page No.
Laser Driver		
IDA-07318	MMIC laser diode driver (to 1.5 Gb/s)	10-86
Transimpedance Amplifiers		
ITA-123XX	MMIC transimpedance amplifier (to 800 Mb/s)	10-94
ITA-063XX	MMIC transimpedance amplifier (to 1.5 Gb/s)	10-92
Fixed Gain		
MSA-03XX	12 dB gain silicon MMIC amplifier	8-3
INA-03184	25 dB gain silicon MMIC amplifier	8-66
AGC Amplifier		
HPVA-0180	20 dB variable gain amplifier (to 2.5 GHz)	10-78
IVA-052XX	30 dB variable gain amplifier (to 1.5 GHz)	10-100, 10-102
IVA-142XX	24 dB variable gain amplifier (to 2.5 GHz)	10-106
Clock Recovery Circuit		
HDMP-2501	622 Mbit/s serial data and clock recovery circuit	10-54
Decision Circuit		
HDMP-2003	Decision circuit (comparator/D-FF to 2.0 Gb/s)	10-35
HDMP-2004	Decision circuit (comparator/D-FF to 2.8 Gb/s)	10-35
HDMP-2006	Decision circuit (comparator/D-FF to 1.5 Gb/s)	10-46
IDC-51418	Decision circuit (comparator/D-FF to 1.5 Gb/s)	10-88
Frequency Doubler		
IAM-810XX	5 GHz MMIC active double balanced mixer/IF amplifier	8-5
HSMP-3822	Surface mount PIN diode	4-25
Limiter		
IVA-052XX	30 dB variable gain amplifier (to 1.5 GHz)	10-100, 10-102
IVA-142XX	24 dB variable gain amplifier (to 2.5 GHz)	10-106

Modular Solutions for Fiber Channel Link

The HOLC-0266 Optical Link Card fills the need for a flexible low cost high data rate point-to-point connection between workstations, minicomputers, computer peripherals such as gigabyte disc arrays and high resolution graphic monitors.

The card includes both optical transmitter/receiver operating at 265.625 MBaud and conforms to the Fiber Standard physical layer FC-0 (ANSI X3T9.3).

The serializer, deserializer, clock recovery, laser driver, automatic power control, and laser safety functions are all located on a single daughter card that can be incorporated onto a system motherboard or adapter card. Input and outputs are industry standard TTL levels. Refer to page 10-63 for further details.



Silicon and GaAs Schottky Diodes



Characteristics of Schottky Barrier Diodes

A Schottky barrier diode contains a metal-semiconductor barrier formed by deposition of a metal layer on a semiconductor. The resulting non-linear diode is similar to point contact diodes and p-n junction diodes. The Schottky diode is more rugged than the point contact diode because the contact is not subject to change under vibration. The advantage over the p-n junction is the absence of minority carriers which limit the response speed in switching applications and the high frequency performance in mixing and detecting applications.

Types of Diode Construction

There are several assembly geometries used for Schottky barrier diodes. Three types used in this catalog are shown in Figure 1.

Mesh Diodes

Hewlett-Packard's patented mesh diode is made by depositing metal through a screen to the semiconductor surface. Many closely spaced diodes are created on the chip. The diode contacts are too small for thermocompression bonding. Contact is made by pressing a sharp metal point against one of the metal contacts on the diode. The large number of contacts on the chip provide a good yield to this operation.

Although the mesh contacts are too small for thermocompression bonding, they are not small enough for operation at high microwave frequencies. It is not possible to deposit reliable contact areas small enough for operation at frequencies above 7 GHz; in fact, the highest test frequency is 3 GHz. The mesh devices have model numbers in the series 5082-2300, 2400, and 2900.

Passivated Diodes

The problem of creating small area contacts was solved by the development of the passivated diode process. An oxide layer is formed over the entire silicon area. Then photolithographic techniques are used to open a small hole in the oxide.

The appropriate metal is deposited in the hole to make the small area Schottky barrier. Then gold is deposited to provide a larger surface for the thermocompression bond in ceramic packaged diodes (outlines 44 or 49) or for the pressure contact in glass packaged diodes (outline 15). (Silver is used for the 5082-2835.) Passivated diodes include the 5082-2835, the 5082-2700 series, and zero bias detectors. These devices are used at frequencies up to 40 GHz.

This passivation process is also used in our beam lead diodes. The final gold layer becomes the beam lead itself. Beam lead diodes contain a nitride layer on the oxide to provide immunity from contaminants that could otherwise lead to reverse current drift. There is also a platinum layer between the barrier metal and the gold. This

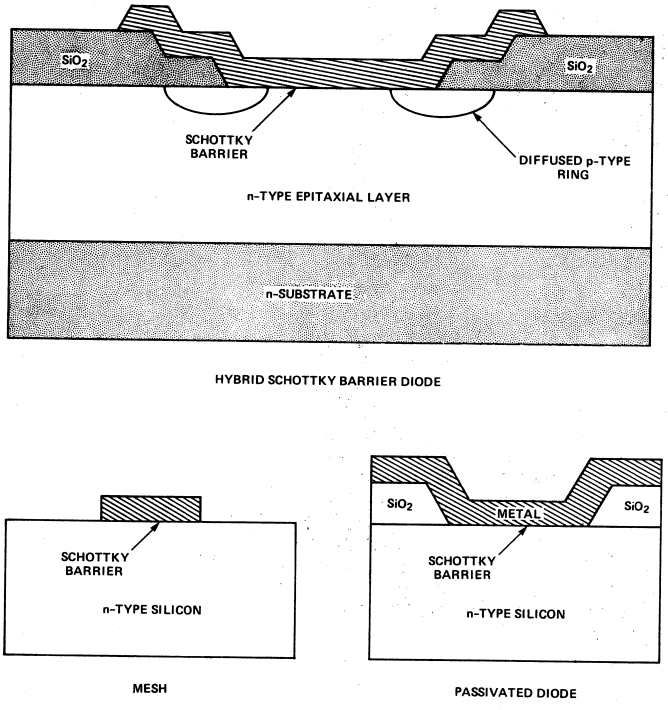


Figure 1. Three Types of Schottky Barrier Diodes.

layer permits reliable operation at higher temperatures. Breakdown voltage for passivated type beam lead diodes is 4 volts minimum at 10 microamps.

Beam lead single diodes are included in the HSCH-5300 series, pairs in the HSCH-5500 series, and quads in the HSCH-5800. These beam lead diodes are also available in package outlines C2, C4, E4, H2, H4, J2, J3, and J4.

Hybrid Diodes

The breakdown voltage limitation was solved with the invention of the hybrid process. Hewlett-Packard's patented process combines a Schottky diode with a p-n junction, eliminating the premature breakdown of the passivated diode without sacrificing the picosecond switching response of the Schottky barrier. Breakdown voltage specifications as high as 70 volts are available. Hybrid diodes are numbered from 5082-2800 to 2826 and also 5082-2836. The beam lead version is 5082-2837.

The dual nature of the hybrid diode limits the lowest capacitance to a picofarad. This limits the high frequency guaranteed performance of these diodes to 2 GHz.

Hybrid chips are assembled in an inexpensive glass package (outline 15) with a C-shaped spring contact.

The Offset Junction Schottky Diode

The increased preference of automatic wire bonding has driven the need for a Schottky chip that can withstand the stresses of thermosonic (vs. thermocompression) wire bonding. When the fragile Schottky barrier lies directly beneath the bond pad, as in conventional Schottky chips, cracking is likely to occur when sonic energy is applied directly above the active area. However, by offsetting the Schottky junction (see Figure 2), the bond pad will sit on a relatively thick oxide which acts as a stress dampener for the active area. This design, which keeps the bond pad symmetrically in the center of the chip, also allows much simpler pattern recognition when using automatic wire bonding.

The HSMS-0001 to HSMS-0013 Schottky diodes utilize this offset junction geometry and can replace most current center-junction hybrid chips. The offset-junction chip also has a larger gold bond pad (to 100 microns) and is silicon nitride-passivated to provide immunity to contaminants.

The Height of the Schottky Barrier

The current-voltage characteristic of Schottky barrier diodes at room temperature is described by the following equation:

$$I = I_S \left(\exp\left(\frac{V - IR_S}{0.026}\right) - 1\right)$$

For currents below 0.1 mA, the IRS term may be neglected. On semi-log graph paper, as plotted in this catalog, the current graph will be a straight line with inverse slope 2.3 x 0.026 = 0.060 volts per cycle. All curves have the same slope, but not necessarily the same value of current for a given voltage. This is determined by the saturation current, I_S, and is related to the type of metal deposited on the silicon and to the treatment of the silicon surface layer. The term "barrier height" is related to the voltage required for a given current. Low voltage corresponds to low barrier.

Study of the forward characteristics in this catalog shows that the lowest barrier diode is the HSCH-3486 family of zero bias

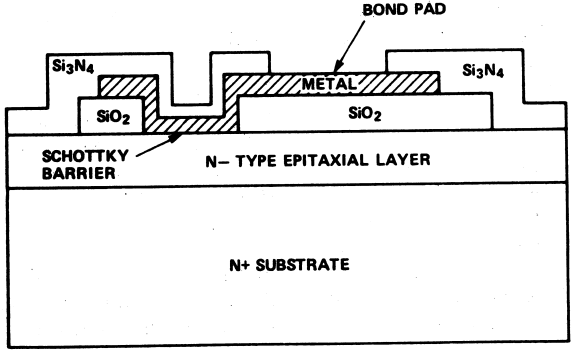


Figure 2. Offset-Junction Schottky Chip

detectors. Detection at zero bias is possible for a range of barrier heights, but the voltage sensitivity is best for high barrier diodes. The sensitivity degrades for barrier heights less than that of the HSCH-3486. The other extreme is represented by medium barrier mixer diodes such as the 5082-2702. However, this barrier height corresponds to a zero bias junction resistance that requires a load resistance above 10 megohms. Zero bias detection with these diodes is limited to single frequency applications.

Applications of Schottky Barrier Diodes

Schottky barrier diodes are useful in a wide variety of applications over a broad frequency range from digital to microwave.

Mixers

The most sensitive receivers using Schottky barrier diodes make use of the nonlinear properties of the diode to produce a difference frequency by mixing the received signal with a local oscillator. Although this can be done with a single diode, it is more common to use multiple diodes in balanced or double balanced mixers. Balanced circuits reduce the effect of a noisy local oscillator and also reduce the level of high order mixing products that are not related to the desired input frequency. For multiple diode mixers, batch matched devices or matched pairs are available.

The most important property of mixer diodes is the noise figure – a measure of how small a signal can be received. The noise level for a perfect receiver is -114 dBm per MHz of bandwidth. A 6 dB noise figure mixer will degrade the noise level to -108 dBm per MHz. If the bandwidth of the receiver is 4 MHz the noise level is raised to -102 dBm. If a 10 dB signal to noise level is required for proper operation of the receiver, the sensitivity is -92 dBm. In this section of the catalog there are several groups of single diodes characterized for mixer applications. For stripline circuits the hermetic H2, broadband C2, and beam lead outlines are available. The best diodes at the highest frequency are guaranteed to have a noise figure less than 7.2 dB at 44 GHz.

The other group of mixer diodes uses outline 15, glass package, for 2 GHz and outlines 44 and 49, ceramic packages, for 9.375 and 16 GHz. The best units have a 6 dB noise figure for 2 GHz and 6.5 dB for the highest frequency.

Applications such as Doppler radar involving intermediate frequencies below 1 MHz will benefit by using the 5082-2400 with its lower noise at these output frequencies. The additional noise (flicker noise) varies inversely with difference frequency and may differ as much as 20 dB from one diode type to another. Since the lowest capacitance (passivated) diodes (measured at 9.375 or 16 GHz) have the highest flicker noise, it is sometimes better to choose a Doppler mixer diode for lowest flicker noise rather than for lowest published noise figure.

Another type of mixer diode is the Schottky quad used for double balanced mixers. These quads are available in beam lead versions and in outlines E4, C4, and H4. These units contain a monolithic beam lead quad – four diodes connected in a ring configuration by gold deposited and plated on the wafer. Since the four diodes are made at the same time on the same portion of a wafer, they are nearly identical and ideally suited for double balanced mixers.

In most gallium arsenide cases both medium and low barrier silicon models are available. The low barrier units have an impedance closer to 50 Ω. These models give better performance in broad band untuned circuits, particularly in those applications with local oscillator power below normal.

Detector Applications

For system applications with relaxed requirements on sensitivity, the video detector receiver is a good alternative to the superheterodyne receiver. The sensitivity is degraded about 50 dB, but the circuitry is simplified and broad bandwidth is easily attained without the problem of tracking the local oscillator frequency.

The important parameters are tangential signal sensitivity (TSS) and voltage (γ). Both of these, as well as video resistance (R_V), are guaranteed for these detector diodes. Typical detector performance is shown for mixer diodes, but detector diodes are designed for superior performance for this application.

Tangential signal sensitivity measures the ability of the diode to distinguish a small

signal from noise. The name relates to a type of radar display with the bottom of the signal pulse tangent to the top of the noise level. There are subjective aspects to this measurement so that TSS measurement is now made with a voltmeter. The value depends on diode noise as well as detection capability.

In some applications, the detector is used as a monitor and the measurement level is well above the noise. For these applications, voltage sensitivity, voltage output for one microwatt input, is the important parameter.

The third specification, video resistance (R_V) is important for video amplifier and response time considerations. The video amplifier resistance, R_L, should be large compared to R_V because the maximum output voltage is degraded by the factor

$$\frac{R_L}{R_L + R_V}$$

However, response time is proportional to the RC product. If fidelity to pulse shape is important, the presence of pulses with steep edges requires a smaller value of load resistance. Sensitivity must be sacrificed for fidelity.

Zero bias Schottky detector diodes are available in the glass package (outline 15) and ceramic packages (outlines 44 and 49). Two types of metal to semiconductor junctions are used, resulting in two distinct ranges of junction resistance (video resistance). Since voltage sensitivity varies with resistance, the high resistance diodes have better voltage sensitivity. However, high resistance means higher noise so the TSS specifications are better for the low resistance diodes. All tests are done at 10 GHz.

The other type of detector (5082-2824 and -2750 series) requires a small forward bias. Production tests are made with 20 microamperes of bias which reduces the video resistance to about 1300 Ω. At zero bias the resistance is higher than for either one of the zero bias detectors. Although the statement has been made that high resistance corresponds to good sensitivity, the resistance is so high for these models (40 megohms for the 2750 series) that the sensitivity is degraded by normal load resistances. These diodes can be used without bias if the load resistance is comparable to the diode resistance. This is discussed in AN988 – All Schottky Diodes are Zero Bias Detectors.

The 5082-2824 diode is tested at 2 GHz. The 2750 series is supplied in outlines 15, 44, and 49 and tested at 10 GHz. The 5082-2787 is similar to the 2755 in outline 15 with the parameters sample tested to reduce cost.

Dynamic and Series Resistance

Schottky diode resistance may be expressed as series resistance, R_S, or as dynamic resistance, R_D. These two terms are related by the equation

$$R_D = R_S + R_j$$

where R_j is the resistance of the junction. Junction resistance of a diode with DC bias is quite accurately calculated by

$$R_j = 26/I_B \text{ where}$$

I_B is the bias current in milliamperes. The series resistance is independent of current.

The dynamic resistance is more easily measured. If series resistance is specified it is usually obtained by subtracting the calculated junction resistance form the measured dynamic resistance.

Surface Mount Schottky Diodes

Available Configurations

DIE	V_{BR}	GLASS	SOT-23					SOT-143		
			SINGLE	SINGLE	SERIES	COMMON ANODE	COMMON CATHODE	UNCON-NECTED PAIR	RING QUAD	BRIDGE QUAD
HSMS-0001	70 V	5082-2800 (1N5711)	HSMS-2800 **A0**	HSMS-2801 **A1**	HSMS-2802 **A2**	HSMS-2803 **A3**	HSMS-2804 **A4**	HSMS-2805 **A5**	HSMS-2807 **A7**	HSMS-2808 **A8**
HSMS-0002	20 V	5082-2810 (1N5712)	HSMS-2810 **B0**	HSMS-2811 **B1**	HSMS-2812 **B2**	HSMS-2813 **B3**	HSMS-2814 **B4**	HSMS-2815 **B5**	HSMS-2817 **B7**	HSMS-2818 **B8**
HSMS-0003	8 V	5082-2835	HSMS-2820 **C0**	HSMS-2821 **C1**	HSMS-2822 **C2**	HSMS-2823 **C3**	HSMS-2824 **C4**	HSMS-2825 **C5**	HSMS-2827 **C7**	HSMS-2828 **C8**

Note: SOT-23 and SOT-143 available in both standard and low profile. Low profile denoted in package marking code with suffix "L". For example, "A0" – standard profile; "A0L" – low profile.

RF Schottky Diodes

Silicon Schottky Mixer and Detector Diodes

Part Number	C_T Max. (pF)	V_{BR} Min. (V)	R_D Max. (Ω)	NF Max. (dB)	V_F Max. (mV)	V_F Max. (V)	T_{SS} (dBm) 20 mA Bias	T_{SS} (dBm) Zero Bias	Package	Page
5082-2301	1	30			1000	0.4			glass axial lead	3-64
5082-2302	1	30			1000	0.4			glass axial lead	3-64
5082-2303	1	20			1000	0.4			glass axial lead	3-64
5082-2900	1.2	10			1000	0.4			glass axial lead	3-64
JAN/TX/TXV/ 1N5711	2	70			1000	0.41			glass axial lead	3-64
5082-2800	2	70				0.41			glass axial lead	3-64
5082-2836	Batch matched 5082-2800								glass axial lead	3-64
JAN/TX/TXV/ 1N5712	1.2	20			1000	0.55			glass axial lead	3-64
5082-2810	1.2	20			1000	0.41			glass axial lead	3-64
5082-2811	1.2	15			1000	0.41			glass axial lead	3-64
5082-2826†	Batch matched 5082-2811								glass axial lead	3-64
5082-2835†	1	8			450	0.34			glass axial lead	3-64
5082-2080	Batch matched 5082-2835								glass axial lead	3-64
HSMS-0001†	1.7	70			1000	0.41			chip	3-12
HSMS-0002†	1.2	20			1000	0.41			chip	3-12
HSMS-0003†	0.8	8			500	0.34			chip	3-12
5082-0097	1.1	15			1000	0.41			chip	3-12
HSMS-2800	2.0	70	35			0.41			SOT-23 single	3-55
HSMS-2801	2.0	70	35			0.41			SOT-23 single	3-55
HSMS-2810	1.2	20	15			0.41			SOT-23 single	3-55
HSMS-2811	1.2	20	15			0.41			SOT-23 single	3-55
HSMS-2820	1.0	8	10			0.34			SOT-23 single	3-55
HSMS-2821	1.0	8	10			0.34			SOT-23 single	3-55
HSMS-2840	2.2	50				0.41			SOT-23 single	3-55
HSMS-2841	2.2	50				0.41			SOT-23 single	3-55
5082-2817	1*	15**		6.0					glass axial lead	3-84
5082-2400	0.7*	30**		6.0					glass axial lead	3-84
5082-2350	0.9*	30**		7.0					glass axial lead	3-84
5082-2824	1*	15**					-56		glass axial lead	3-90

Notes:
*C_j typical.
**V_{BR} typical.
†Standard Hi-Rel version available.
For reliability data see pages 3-94 – 3-118.

RF Schottky Diodes (cont.)

Silicon Schottky Mixer Diode Pairs

Part Number	C_T Max. (pF)	V_{BR} Min. (V)	R_D Max. Typ. @ 5 mA (Ω)	V_F Max. @ 1 mA (mV)	Package	Page
HSMS-2802	2.0	70	35	0.41	SOT-23, series	3-55
HSMS-2803	2.0	70	35	0.41	SOT-23, common anode	3-55
HSMS-2804	2.0	70	35	0.41	SOT-23, common cathode	3-55
HSMS-2805	2.0	70	35	0.41	SOT-143, unconnected pair	3-55
HSMS-2812	1.2	20	15	0.41	SOT-23, series	3-55
HSMS-2813	1.2	20	15	0.41	SOT-23, common anode	3-55
HSMS-2814	1.2	20	15	0.41	SOT-23, common cathode	3-55
HSMS-2815	1.2	20	15	0.41	SOT-143, unconnected pair	3-55
HSMS-2822	1.0	8	10	0.34	SOT-23, series	3-55
HSMS-2823	1.0	8	10	0.34	SOT-23, common anode	3-55
HSMS-2824	1.0	8	10	0.34	SOT-23, common cathode	3-55
HSMS-2825	1.0	8	10	0.34	SOT-143, unconnected pair	3-55
5082-2306	Matched pair 5082-2301				G-1	3-64
5082-2308	Matched pair 5082-2303				glass axial lead	3-64
5082-2912	Matched pair 5082-2900				glass axial lead	3-64
5082-2804	Matched pair 5082-2800				glass axial lead	3-84
5082-2818	Matched pair 5082-2817				glass axial lead	3-84
5082-2401	Matched pair 5082-2400				glass axial lead	3-84
5082-2351	Matched pair 5082-2350				glass axial lead	3-84

Silicon Schottky Mixer Diode Quads

Part Number	C_T Max. (pF)	V_{BR} Min. (V)	R_D Max. @ 5 mA (Ω)	V_F Max. @ 1 mA (mV)	Package	Page
HSMS-2807	2.0	70	35 Typ.	0.41	SOT-143, ring	3-55
HSMS-2808	2.0	70	35 Typ.	0.41	SOT-143, bridge	3-55
HSMS-2817	1.2	20	15 Typ.	0.41	SOT-143, ring	3-55
HSMS-2818	1.2	20	15 Typ.	0.41	SOT-143, bridge	3-55
HSMS-2827	1.0	8	10 Typ.	0.34	SOT-143, ring	3-55
HSMS-2828	1.0	8	10 Typ.	0.34	SOT-143, bridge	3-55
5082-2830	0.67 Typ.		12	0.40 Typ.	E-4 ring	3-80
5082-2831	0.67 Typ.		12	0.25 Typ.	E-4 ring	3-80
5082-2970	Matched quad 5082-2900				glass axial lead	3-64
5082-2997	Matched bridge quad 5082-2900				G-2	3-64
5082-2805	Matched quad 5082-2800				glass axial lead	3-64
5082-2815	Matched quad 5082-2811				glass axial lead	3-64
5082-2814	Matched ring quad 5082-2811				G-1	3-64
5082-2813	Matched bridge quad 5082-2811				G-2	3-64
5082-2370	Matched quad 5082-2303				glass axial lead	3-64
5082-2396	Matched ring quad 5082-2303				G-1	3-64
5082-2356	Matched bridge quad 5082-2303				G-2	3-64

Notes:
For reliability data see pages 3-94 – 3-118.

Microwave Schottky Diodes

Schottky Diode Chips

Part Number	C_T Max. (pF)	NF Typ. (dB)	T_{ss} Typ. (dBm)	Page
5082-0009	0.12	6.6[c]	-55	3-12
5082-0013	0.18	6.0[c]	-42	3-12
5082-0023	0.16	6.0[c]	-54	3-12

Silicon Schottky Mixer and Detector Diodes

Part Number	C_T Max. (pF)	V_{BR} Min. (V)	R_D Max. (Ω)	NF Max. (dB)	V_F Max. (mV)	T_{ss} (dBm)		Package	Page
						20 mA Bias	Zero Bias		
HSCH-5312* HSCH-5313*	0.15	4	16		500			beam lead	3-18 3-18
HSCH-5310* HSCH-5311*	0.10	4	20		500			beam lead	3-18 3-18
HSCH-5336* HSCH-5337*	0.25	4	12		375			beam lead	3-18 3-18
HSCH-5332* HSCH-5333*	0.15	4	16		375			beam lead	3-18 3-18
HSCH-5330* HSCH-5331*	0.10	4	20		375			beam lead	3-18 3-18
HSCH-5316* HSCH-5317*	0.25	4	12		500			beam lead	3-18 3-18
HSCH-5318* HSCH-5319*	0.25	4	12	6.2[c]	500	-54		beam lead	3-18 3-18
HSCH-5338* HSCH-5339*	0.25	4	12	6.2[c]	375	-54	-44	beam lead	3-18 3-18
5082-2207 5082-2208	0.18	4	12	6.0[c]	500	-54		C-2	3-74 3-74
5082-2209 5082-2210	0.18	4	12	6.5[c]	500	-54		C-2	3-74 3-74
5082-2774 5082-2775	0.18	4	12	6.0[c]	375	-54	-44	C-2	3-74 3-74
5082-2794 5082-2795	0.18	4	12	6.5[c]	375	-54	-44	C-2	3-74 3-74
HSCH-6312	0.27	4	12	6.2[c]	500	-54		J-2	3-50
HSCH-6332	0.27	4	12	6.2[c]	375	-54	-44	J-2	3-50
HSCH-5314* HSCH-5315*	0.15	4	16	7.2[b]	500			beam lead	3-18 3-18
HSCH-5334* HSCH-5335*	0.15	4	16	7.2[b]	375			beam lead	3-18 3-18
HSCH-6310	0.22	4	16	7.2[b]	500			J-2	3-50
HSCH-6330	0.22	4	16	7.2[b]	375			J-2	3-50
HSCH-5320* HSCH-5321*	0.10	4	20	7.5[a]	500			beam lead	3-18 3-18

Notes:
[a] 26 GHz
[b] 16 GHz
[c] 9.375 GHz
For reliability data see pages 3-94 – 3-118.

*Standard Hi-Rel Version Available

Microwave Schottky Diodes (cont.)

Silicon Schottky Mixer and Detector Diodes (Cont.)

Part Number	C_T Max. (pF)	V_{BR} Min. (V)	R_D Max. (Ω)	NF Max. (dB)	V_F Max. (mV)	T_{SS} (dBm)		Package	Page
						20 mA Bias	Zero Bias		
HSCH-5340*	0.10	4	20	7.5[a]	375			beam lead	3-18
HSCH-5341*									3-18
HSMS-8001	0.25	4	12	5.2[d]	350	-46		chip	3-15
HSMS-8011									3-15
HSMS-8002	0.16	4	14	5.5[d]	350	-46		chip	3-15
HSMS-8012									3-15
HSMS-8101	0.35	4	12	6.3[d]	350			SOT-23	3-61
HSMS-8202									3-61

Zero Bias Schottky Detector Diodes

Part Number	T_{SS} Max. (dBm)	γ Min. mV/μW	R_V		C_T (pF)	Package	Page
			Min. MΩ	Max. MΩ			
HSCH-3207	-42	8	80	300	0.30	44	3-46
HSCH-3206	-42	8	80	300	0.30	49	3-46
HSCH-3486	-54	7.2	2	8	0.30	15	3-46

Schottky Barrier Detector Diodes

Part Number	T_{SS} Max. (dBm)	γ Min. mV/μW	R_V		C_{jo} (pF)	Package	Page
			Min. MΩ	Max. MΩ			
5082-2787	-52	3.5	1.2	1.8	0.12	15	3-90
5082-2755	-55	5	1.2	1.6	0.10	15	3-90
5082-2751	-55	5	1.2	1.6	0.10	49	3-90
5082-2750	-55	5	1.2	1.6	0.10	44	3-90

Silicon Schottky Mixer Diode Pairs

Part Number	C_T Max. (pF)	V_{BR} Min. (V)	R_D Max. (Ω)	NF Max. (dB)	V_F Max. (mV)	Package	Page
HSCH-5514*	0.25	4	12	6.2[c]	500	beam lead	3-26
HSCH-5534*	0.25	4	12	6.2[c]	375	beam lead	3-26
HSCH-6512	0.27	4	12	6.2[c]	500	J-3	3-50
HSCH-6532	0.27	4	12	6.2[c]	375	J-3	3-50
HSCH-5518*	0.15	4	16	7.2[b]	500	beam lead	3-26
HSCH-5538*	0.15	4	16	7.2[b]	375	beam lead	3-26
HSCH-6510	0.22	4	16	7.2[b]	500	J-3	3-50
HSCH-6530	0.22	4	16	7.2[b]	375	J-3	3-50
HSCH-5520*	0.10	4	20	7.5[a]	500	beam lead	3-26
HSCH-5510*	0.10	4	20	7.0[b]	500	beam lead	3-26
HSCH-5540*	0.10	4	20	7.5[a]	375	beam lead	3-26
HSCH-5530*	0.10	4	20	7.0[b]	375	beam lead	3-26
HSCH-5511*	0.10	4	20		500	beam lead	3-26

Notes:
[a] 26 GHz
[b] 16 GHz
[c] 9.375 GHz
[d] Conversion Loss at 9.375 GHz
For reliability data see pages 3-94 – 3-118.

*Standard Hi-Rel version available.

Microwave Schottky Diodes (cont.)

Silicon Schottky Mixer Diode Pairs (cont.)

Part Number	C_T Max. (pF)	V_{BR} Min. (V)	R_D Max. (Ω)	NF Max. (dB)	V_F Max. (mV)	Package	Page
HSCH-5512*	0.15	4	16		500	beam lead	3-26
HSCH-5516*	0.25	4	12		500	beam lead	3-26
HSCH-5531*	0.10	4	20		375	beam lead	3-26
HSCH-5532*	0.15	4	16		375	beam lead	3-26
HSCH-5536*	0.25	4	12		375	beam lead	3-26
5082-2702 5082-2707	0.10	4		6.5[a]		44	3-84 3-84
5082-2723* 5082-2724	0.10	4		6.5[b]		49	3-84 3-84

Silicon Schottky Mixer Diode Quads

Part Number	C_T Max. (pF)	V_{BR} Min. (V)	R_D Max. (Ω)	NF Max. (dB)	V_F Max. (mV)	Package	Page
HSCH-5938*	0.50	4	10		350	beam lead bridge	3-35
HSCH-5918*	0.50	4	10		450	beam lead bridge	3-35
HSCH-5958*	0.50	4	10		650	beam lead bridge	3-35
5082-2292	0.40		15		350 typ.	C-4 ring	3-80
HSCH-5816*	0.25		12		500	beam lead ring	3-32
HSCH-5836*	0.25		12		375	beam lead ring	3-32
5082-2231	0.80		12		250	H-4 ring	3-80
5082-2233	0.54		16		300	H-4 ring	3-80
5082-2263	0.54		16		450	H-4 ring	3-80
5082-2271	0.80		12		250	C-4 ring	3-80
5082-2272	0.54		15		250	C-4 ring	3-80
5082-2279	0.25		16		300 typ.	C-4 ring	3-80
HSCH-6812	0.21		16		500	J-4 ring	3-50
HSCH-6832	0.21		16		375	J-4 ring	3-50
HSCH-5812	0.15		16		500	beam lead ring	3-32
HSCH-5832	0.15		16		375	beam lead ring	3-32
5082-2280	0.20		16		300 typ.	C-4 ring	3-80
5082-2294	0.20		16		450 typ.	C-4 ring	3-80
HSCH-6810	0.16		20		500	J-4 ring	3-50
HSCH-6830	0.16		20		375	J-4 ring	3-50
HSCH-5932	0.15	4	16		375	beam lead bridge	3-35
HSCH-5912	0.15	4	16		500	beam lead bridge	3-35
HSCH-5952	0.15	4	16		675	beam lead bridge	3-35
HSCH-5810	0.10		20		500	beam lead ring	3-32
HSCH-5830	0.10		20		375	beam lead ring	3-32

GaAs Schottky Mixer and Detector Diodes

Part Number	C_j† Max. (pF)	V_{BR} Min. (V)	R_D Max. (Ω)	NF Max. (dB)	V_F Max. (mV)	Package	Page
HSCH-9101*	0.04	4.5	12	6.7[c]	700	beam lead single	3-39
HSCH-9201*	0.04	4.5	12	6.7[c]	700	beam lead pair	3-39
HSCH-9251*	0.04	4.5	12	6.7[c]	700	beam lead anti-parallel pair	3-39
HSCH-9301*	0.04		12		700	beam lead ring quad	3-42
HSCH-9351*	0.04	4.5	12		700	beam lead bridge quad	3-42

Notes:
*Standard Hi-Rel version available.
[a] 9.375 GHz [c] 44 GHz
[b] 16 GHz
†C_j is determined by measuring total device capacitance and subtracting the calculated parasitic capacitance (0.035 pF).
For reliability data see pages 3-94 – 3-118.

HEWLETT PACKARD

Schottky Barrier Chips for Hybrid Integrated Circuits

Technical Data

5082-0009, 5082-0013, 5082-0023, 5082-0097, HSMS-0001, HSMS-0011, HSMS-0002, HSMS-0012, HSMS-0003, HSMS-0013

Features

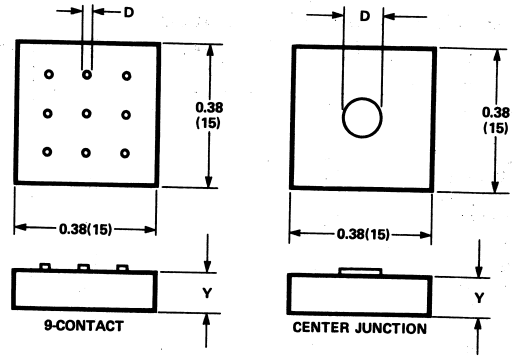
- **Thermocompression/ Thermosonically Bondable**
- **Gold Metallization**
- **Silicon Nitride Passivation**
- **Uniform Electrical Characteristics**
- **Batch Matched Versions Available**
- **Planar Construction**
- **Available in Many Electrical Selections**
- **Ideal for Hybrid Integrated Circuits**

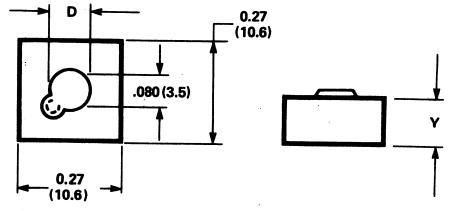
Description/ Applications

These Schottky chips are designed for hybrid applications at DC through K-band frequencies. The passivated planar construction of these Schottky chips provides a wide temperature range capability combined with broad bandwidth performance.

A variety of chips are provided which are optimized for various analog and digital applications. Typical applications of Schottky chips are mixing, detecting, switching, gating, sampling, and wave shaping.

The HSMS-00XX (offset junction) series Schottky diode chips





OFFSET JUNCTION

Dimension	Part Number		
	Center Junction		Offset Junction
	5082-0097	5082-0009 -0013 -0023	HSMS-000X -00XX
D	0.08 (3)	0.02 (0.80)*	0.10 (4)
Y	9.13 (5)	0.10 (4)	0.13 (5)

NOTES:
1. DIMENSIONS IN MILLIMETERS AND (1/1000 INCH).
2. DIMENSION TOLERANCE ±0.03 (1), EXCEPT * WHERE IT IS ±0.006 (0.2).
3. TOP CONTACT IS ANODE EXCEPT 5082-0009, WHERE TOP IS CATHODE.
4. ALL CONTACT METALLIZATION IS GOLD.

Outline 01B – Chip Dimensions

are specifically designed for analog and digital hybrid applications requiring thermosonic or thermocompression bonding techniques. The large bonding pad and offset junction allows easy bonding. The top metallization is a layer of gold deposited on adhesive metal layers for a tarnish-free surface that allows either thermosonic or thermocompression bonding techniques. The bottom metallization is also gold, suitable for epoxy or eutectic die attach methods.

Maximum Ratings

Junction Operating and Storage Temperature
5082-0097, HSMS-00XX ..... -65°C to +200°C
5082-0009, -0013, -0023 ..... -65°C to +150°C
Power Dissipation @ T_A = 25°C ..... 250 mW
Measured in an infinite heat sink derated linearly to zero at maximum rated temperature.
I_F max (1 µs pulse) ..... 1 Amp
Operation in excess of any one of these conditions may result in permanent damage.

Electrical Specifications at T_A = 25°C

Schottky Barrier Chips for General Purpose Applications Requiring Thermocompression Bonding Only

Part Number 5082- / Epoxy or Solder Die Attach[1]	Nearest Equivalent Packaged Part No. 5082-	Minimum Breakdown Voltage V_{BR} (V)	Maximum Forward Voltage V_F (mV)[2]	Maximum Forward Voltage V_F (V) @ I_F (mA)[2]	Maximum Capacitance C_T (pF)	Maximum Reverse Leakage Current I_R (nA) @ V_R (V)
0097	2811	15	410	1.0 20	1.1	100 8
Test Conditions		I_R = 10 µA	I_F = 1 mA		V_R = 0 V f = 1 MHz	

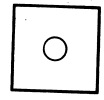
Notes:
1. Recommended methods. See "Assembling and Handling Procedures" for definitions.
2. V_F measured after proper die attach.

Schottky Barrier Chips for General Purpose Applications Requiring Thermosonic or Thermocompression Bonding Only



Part Number HSMS-		Nearest Equivalent Axial Lead Part No. 5082-	Minimum Breakdown Voltage V_{BR} (V)	Maximum Forward Voltage V_F (mV)[2]	Maximum Forward Voltage V_F (V) @ I_F (mV)	Maximum Capacitance C_T (pF)	Maximum Reverse Leakage Current I_R (nA) @ V_R (V)
Epoxy or Eutectic Die Attach[1]	Batch. Matched[1]						
0001	0011	2800	70	410	1.0 15	1.72	200 50
0002	0012	2810	20	410	1.0 35	1.2	50 15
0003	0013	2835	8*	340	0.5 10	0.8	100 1
Test Conditions	ΔV_F = 15 mV I_F = 1 mA		I_R = 10 μA *I_R = 100 μA	I_F = 1 mA		V_R = 0 V f = 1.0 MHz	

Notes:
1. Standard batch match size, 100 units.
2. V_F measured after proper die attach.



Schottky Barrier Chips for Mixing and Detecting

Part Number 5082-	Nearest Equivalent Packaged Part No. 5082-	Nearest Equivalent Beam Lead Part No. HSCH-	Maximum Junction Capacitance C_T (pF)	Typical Parameters	
				Noise Figure NF (dB)[1]	Tangential Sensitivity T_{SS} (dBm)
0023	2702, 2723	5316	0.16	6.0	-54
0013	HSCH-3206*	5332	0.18	6.0	-42**
0009	2750		0.12	6.6	-55
Test Conditions	*Zero Bias		V_R = 0 V f = 1.0 MHz	f = 9.375 GHz	f = 10 GHz BW = 2 MHz I_{BIAS} = 20 μA **Zero Bias

Notes:
1. NF includes 1.5 dB for the IF Amplifier.

Assembly and Handling Procedures for Schottky Chips

See page 3-17.

HEWLETT PACKARD

Schottky Diode Chips for X/Ku-Band Hybrid Integrated Circuits

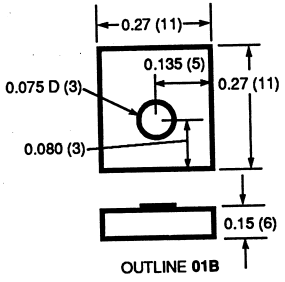
Technical Data

HSMS-8001
HSMS-8002
HSMS-8011
HSMS-8012

Features

- **Platinum Tri-metal System**
  - **— High Temperature Stability**
- **Offset Gold Bonding Pad**
  - **— Thermo (compression/ sonic) Bondability**
  - **— Ideal for Hybrid Integrated Circuits**
- **Silicon Nitride Passivation**
  - **— Stable, Reliable Performance**
- **Uniform Electrical Characteristics**
  - **— Batch Matched Versions Available**

Chip Outline



OUTLINE **01B**

NOTES;
1. DIMENSIONS IN MILLIMETERS AND (1/1000 INCH).
2. ALL CONTACT METALIZATION IS GOLD.

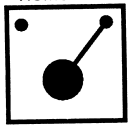
Description/ Applications

These Schottky chips are designed for hybrid applications at X / Ku - bands. Passivated planar construction provides a wide temperature range capability combined with broad bandwidth performance. Typical applications for these chips are mixing, detecting, switching, gating, sampling, and wave shaping.

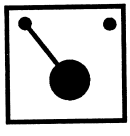
The top metalization is gold deposited on adhesive metal layers for a tarnish-free surface that allows either thermosonic or thermocompression bonding techniques. The bottom metalization is also gold and is suitable for epoxy or eutectic preform die attach methods.

Chip Identification

HSMS-8001



HSMS-8002



Absolute Maximum Ratings*

(T_A = 25°C)

Symbol	Parameters	Min.	Max.	Units
T_j	Junction Operating and Storage Temperature	-65	+150	°C
P_t	Power Dissipation @ T_A = 25°C(1)		75	mW
P_{IV}	Peak Inverse Voltage		4	V

* Operation in excess of any one of these parameters may result in permanent damage.

Note 1. Measured in an infinite heat sink. Derate linearly to zero at maximum rated temperature.

DC Electrical Specifications (T_A = 25°C)

Part Number HSMS-	Batch Matched[1]	Minimum Breakdown Voltage V_{BR}	Minimum Forward Voltage V_F (mV)	Maximum Forward Voltage V_F (mV)	Maximum Capacitance C_T (pF)	Maximum Dynamic Resistance R_D (Ω)
8001	8011	4	250	350	0.250	12
8002	8012	4	250	350	0.160	14
Test Conditions	ΔV_F =15 mV I_F = 1 mA	I_R = 10 μA	I_F = 1 mA		V_R = 0 V f = 1.0 MHz	I_F = 5 mA

Notes: 1. Standard batch match size, 100 units

RF Electrical Parameters, T_A = 25 °C

Part Number HSMS-	Typical			
	Conversion Loss L_C (dB)	IF Impedance Z_{IF} (Ω)	SWR (GHz)	Tangential Sensitivity T_{SS} (dBm)
8001	5.2[1]	150	1.2 [1]	-46
8002	5.5 [2]	150	1.2 [2]	-46
Test Conditions	DC load resistance = 0 Ω, LO power = 1 mW			f = 10 GHz BW = 2 MHz I_{BIAS}=20 μA

Notes: 1. Typical at f = 9.375 GHz. 2. Typical at f = 16.0 GHz.

Assembly and Handling Procedures for Schottky Chips

1. Storage

Devices should be stored in a dry nitrogen purged desiccator or equivalent.

2. Cleaning

If required, surface contamination may be removed with electronic grade solvents such as freon (T.F. or T.M.C.), acetone, deionized water, and methanol used singularly or in combinations. Typical cleaning times per solvent are one to three minutes. DI water and methanol should be used (in that order) in the final cleans. Final drying can be accomplished by placing the cleaned dice on clean filter paper and drying with an infrared lamp for 5 - 10 minutes. Acids such as hydrofluoric (HF) , nitric (HNO_3) and hydrochloric (HCl) must not be used.

The effects of cleaning methods / solutions should be verified on small samples prior to submitting the entire lot.

Following cleaning, dice should either be used in assembly (typically within a few hours) or stored in clean containers in an inert atmosphere or a vacuum chamber.

3. Die Attach

a. Eutectic-

Eutectic die attach can be accomplished by "scrubbing" the die with a preform on the header . (Note—times and temperature utilized vary depending on the type of preform.) For example, 310° C is suitable for a Au/Sn preform.

b. Epoxy

For epoxy die-attach, conductive silver-filler epoxies are recommended.This method can be used for all Hewlett-Packard Schottky chips.

4. Wire Bonding

Thermosonic or thermocompression wire bonding is recommended. Suggested wire is pure gold, 0.7 to 1.5 mil diameter.

HEWLETT PACKARD

Beam Lead Schottky Diodes for Mixers and Detectors (1-26 GHz)

Technical Data

HSCH-5300 Series

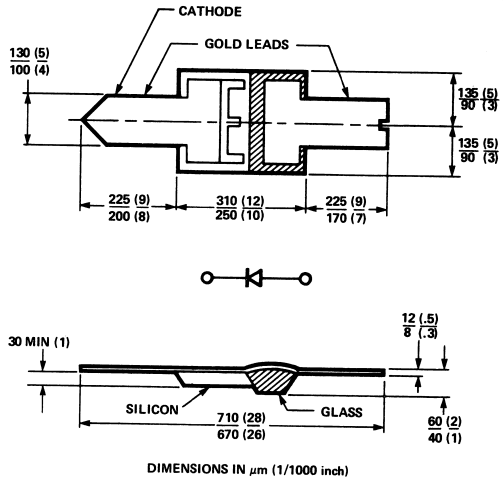
Features

- **Platinum Tri-Metal System**
  High Temperature Stability
- **Silicon Nitride Passivation**
  Stable, Reliable Performance
- **Low Noise Figure**
  Guaranteed 7.5 dB at 26 GHz
- **High Uniformity**
  Tightly Controlled Process Insures Uniform RF Characteristics
- **Rugged Construction**
  4 Grams Minimum Lead Pull
- **Low Capacitance**
  0.10 pF Max. at 0 V
- **Polyimide Scratch Protection**

Description

These beam lead diodes are constructed using a metal-semiconductor Schottky barrier junction. Advanced epitaxial techniques and precise process control insure uniformity and repeatability of this planar passivated microwave semiconductor. A nitride passivation layer provides immunity from contaminants which could otherwise lead to I_R drift.

The HP beam lead process allows for large beam anchor pads for rugged construction (typical 6 gram pull strength) without degrading capacitance.



Outline 07

Maximum Ratings

Pulse Power Incident at T_A = 25°C ..... 1 W
Pulse Width = 1 μs, Du = 0.001
CW Power Dissipation at T_A = 25°C ..... 150 mW
Measured in an infinite heat sink derated linearly to zero at maximum rated temperature
T_{OPR} – Operating Temperature Range ..... -65°C to +175 °C
T_{STG} – Storage Temperature Range ..... -65°C to +200°C
Minimum Lead Strength ..... 4 grams pull on any lead
Diode Mounting Temperature ..... +350°C for 10 sec. max.

These diodes are ESD sensitive. Handle with care to avoid static discharge through the diode.

Applications

The beam lead diode is ideally suited for use in stripline or microstrip circuits. Its small physical size and uniform dimensions give it low parasitics and repeatable RF characteristics through K-band.

The basic medium barrier devices in this family are DC tested HSCH-5310, -5312, and -5316. Batch matched versions are available as the HSCH-5311, -5313, and -5317. Equivalent low barrier devices are HSCH-5330, -5332, and -5336. Batch matched versions are available as HSCH-5331, -5333, and -5337.

For applications requiring guaranteed RF-tested performance up to 26 GHz, the HSCH-5320 is selected with batch match units available as the HSCH-5321. The HSCH-5318 is selected for 6.2 dB maximum noise figure at 9.375 GHz; with RF batch match units available as the HSCH-5319. The HSCH-5314 is rated at 7.2 dB maximum noise figure at 16 GHz with RF batch match units available as the HSCH-5315.

For guaranteed low-barrier RF-tested performance to 26 GHz, the HSCH-5340 is selected with batch match units available as the HSCH-5341. The HSCH-5338 and -5334 are selected for noise figure 6.2 dB maximum at 9.375 GHz and 7.2 dB maximum at 16 GHz respectively. Batch matched versions are available as the HSCH-5339 and -5335.

Bonding and Handling Procedures

See page 3-45.

Table IA. Electrical Specifications for RF Tested Diodes at $T_A = 25°C$

Part Number HSCH-	Batch* Matched HSCH-	Barrier	Max. Noise Figure NF (dB)	I_F Impedance Z_{IF} (Ω) Min.	I_F Impedance Z_{IF} (Ω) Max.	Max. SWR	Min. Breakdown Voltage V_{BR} (V)	Max. Dynamic Resistance R_D (Ω)	Max. Total Capacitance C_T (pF)	Max. Forward Voltage V_F (mV)	Max. Leakage Current I_R (nA)
5318	5319	Medium	6.2 at 9.375 GHz	200	400	1.5:1	4	12	0.25	500	100
5314	5315		7.2 at 16 GHz					16	0.15		
5320	5321		7.5 at 26 GHz					20	0.10		
5338	5339	Low	6.2 at 9.375 GHz	150	350	1.5:1	4	12	0.25	375	400
5334	5335		7.2 at 16 GHz					16	0.15		
5340	5341		7.5 at 26 GHz					20	0.10		
Test Conditions	ΔNF ≤ 0.3 dB $\Delta Z_{IF} \leq$ 25 Ω		DC Load Resistance - 0 Ω LO Power = 1 mW I_F = 30 MHz, 1.5 dB NF				$I_R \leq 10$ μA	I_F = 5 mA	V_R = 0 V f = 1 MHz	I_F = 1 mA	V_R = 1 V

*Minimum batch size 20 units.

Note:
1. $C_T = C_J + 0.02$ pF (fringing cap).

Table IB. Electrical Specifications for DC Tested Diodes at $T_A = 25°C$

Part Number HSCH-	Batch* Matched HSCH-	Barrier	Minimum Breakdown Voltage V_{BR} (V)	Maximum Dynamic Resistance R_D (Ω)	Maximum Total Capacitance C_T (pF)	Maximum Forward Voltage V_F (mV)	Maximum Leakage Current I_R (nA)
5316 5312 5310	5317 5313 5311	Medium	4	12 16 20	0.25 0.15 0.10	500	100
5336 5332 5330	5337 5333 5331	Low	4	12 16 20	0.25 0.15 0.10	375	400
Test Conditions	$\Delta V_F \leq 15$ mV @ 5 mA		$I_R \leq 10$ μA	$I_F = 5$ mA	$V_R = 0$ V f = 1 MHz	$I_F = 1$ mA	$V_R = 1$ V

*Minimum batch size 20 units.

Typical Detector Characteristics at $T_A = 25°C$

Medium Barrier and Low Barrier (DC Bias)

Parameter	Symbol	Typical Value	Units	Test Conditions
Tangential Sensitivity	TSS	-54	dBm	20 μA Bias, $R_L = 100$ kΩ Video Bandwidth = 2 MHz f = 10 GHz
Voltage Sensitivity	γ	6.6	mV/μW	
Video Resistance	R_V	1400	Ω	

Low Barrier (Zero Bias)

Parameter	Symbol	Typical Value	Units	Test Conditions
Tangential Sensitivity	TSS	-44	dBm	Zero Bias, $R_L = 10$ MΩ Video Bandwidth = 2 MHz f = 10 GHz
Voltage Sensitivity	γ	10	mV/μW	
Video Resistance	R_V	1.8	MΩ	

Typical Parameters

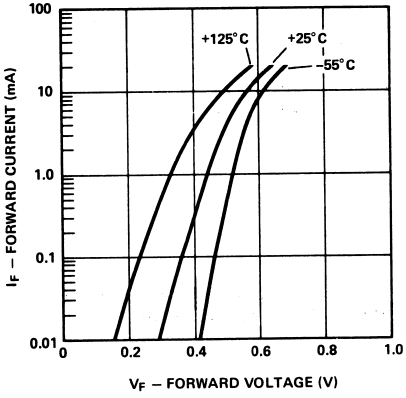


Figure 1. Typical Forward Characteristics for Medium Barrier Beam Lead Diodes. HSCH-5310, -5320 Series.

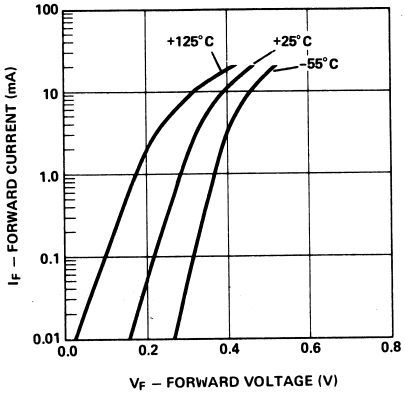


Figure 2. Typical Forward Characteristics for Low Barrier Beam Lead Diodes. HSCH-5330, -5340 Series.

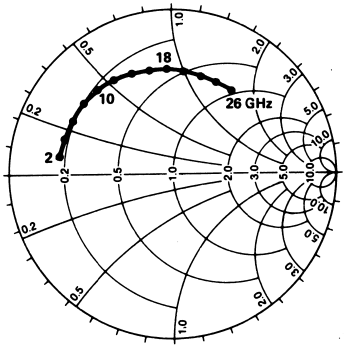


Figure 3. Typical Admittance Characteristics with 1 mA Self Bias. HSCH-5320, -5340, -5321, and -5341.

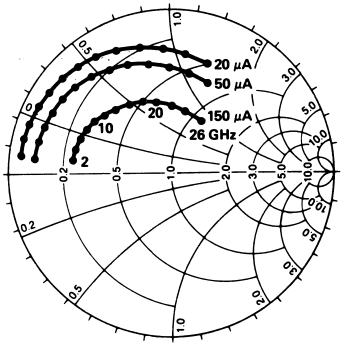


Figure 4. Typical Admittance Characteristics with External Bias. HSCH-5320, -5340, -5321, and -5341.

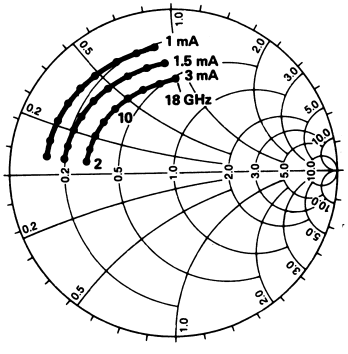


Figure 5. Typical Admittance Characteristics with Self Bias. HSCH-5314, -5315, -5334, and -5335.

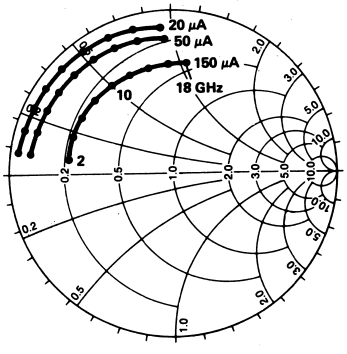


Figure 6. Typical Admittance Characteristics with External Bias. HSCH-5314, -5315, -5334, and -5335.

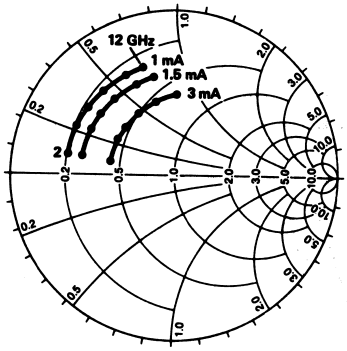


Figure 7. Typical Admittance Characteristics with Self Bias. HSCH-5318, -5319, -5338, and -5339.

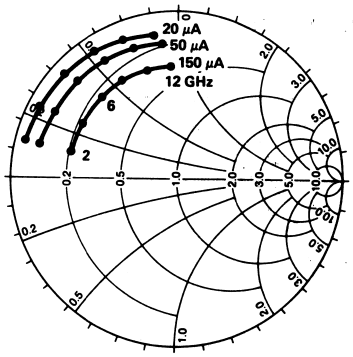


Figure 8. Typical Admittance Characteristics with External Bias. HSCH-5318, -5319, -5338, and -5339.

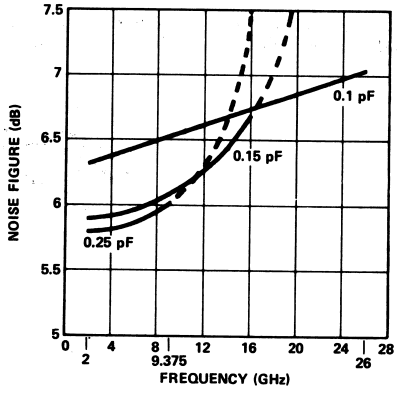
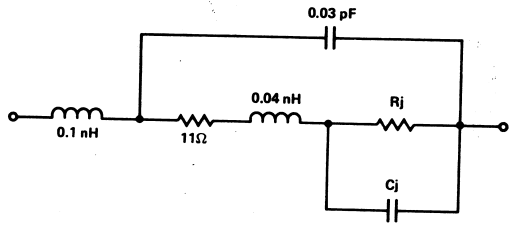


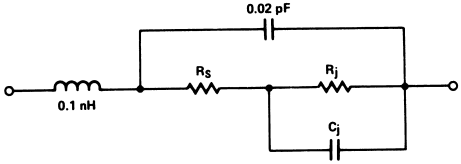
Figure 9. Typical Noise Figure vs. Frequency.

Models for Each Beam Lead Schottky Diode

HSCH-5320, -5321, -5340, -5341
1 mA Self Bias

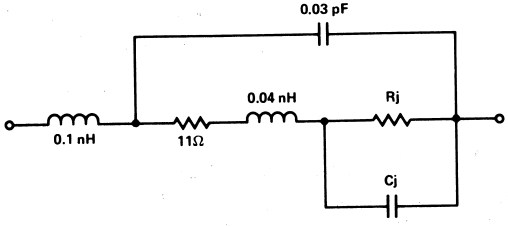


Other HSCH-53XX
Self Bias



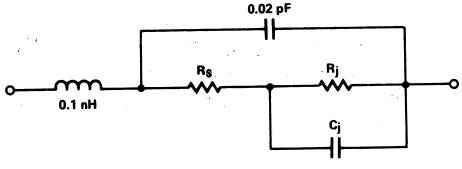
Part Numbers	1.0 mA Self Bias			1.5 mA Self Bias			3.0 mA Self Bias		
	R_S (Ω)	R_j (Ω)	C_j (pF)	R_S (Ω)	R_j (Ω)	C_j (pF)	R_S (Ω)	R_j (Ω)	C_j (pF)
HSCH-5314, -5315, -5334, -5335	5.0	393	0.11	5.2	232	0.11	5.0	150	0.12
HSCH-5318, -5319, -5338, -5339	5.1	244	0.16	5.0	178	0.16	5.0	109	0.19

HSCH-5320, -5321, -5340, -5341
External Bias



Part Numbers	20 μA DC Bias		50 μA DC Bias		150 μA DC Bias	
	R_j (Ω)	C_j (pF)	R_j (Ω)	C_j (pF)	R_j (Ω)	C_j (pF)
HSCH-5320, -5321, -5340, -5341	1400	0.09	560	0.09	187	0.10

Other HSCH-53XX
External Bias



Part Numbers	20 μADC Bias			50 μADC Bias			150 μADC Bias		
	R_S (Ω)	R_j (Ω)	C_j (pF)	R_S (Ω)	R_j (Ω)	C_j (pF)	R_S (Ω)	R_j (Ω)	C_j (pF)
HSCH-5314, -5315, -5334, -5335	2.8	1240	0.11	4.7	618	0.12	2.7	211	0.13
HSCH-5318, -5319, -5338, -5339	5.1	2050	0.18	3.9	665	0.19	4.7	242	0.20

HEWLETT PACKARD

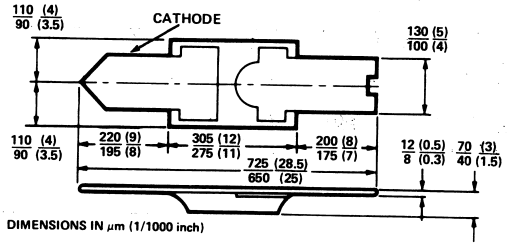
Beam Lead Schottky Diode

Technical Data

5082-2837

Features

- **Fast Switching**
- **High Breakdown**
- **Beam Lead Equivalent of 5082-2800**
- **Platinum Tri-Metal System**
- **Wide Temperature Range**
- **SiO_2 Passivation**



Outline 10B

Description

The HP 5082-2837 is an epitaxial planar passivated beam lead diode whose construction utilizes a unique combination of both a conventional PN junction and a Schottky barrier. This manufacturing process results in a device which has the high breakdown and temperature characteristics of silicon, the turn-on voltage of germanium and the speed of a Schottky diode majority carrier device.

This device is intended for high volume, low cost applications, and is the beam lead equivalent of the HP 5082-2800 glass packaged diode.

Applications

High level detection, switching, or gating; logarithmic or A-D converting; sampling or wave shaping are jobs the 5082-2837 will do better than conventional PN junction diodes. The low turn-on voltage and subnanosecond switching make it extremely attractive in digital circuits for DTL gates, pulse shaping circuits or other low level applications. Its high PIV allows wide dynamic range for fast high voltage sampling gates.

The 5082-2837 low turn-on voltage gives low offsets. The extremely low stored charge minimizes output offsets caused by the charge flow in the storage capacitor. At UHF, the diodes exhibit 95% rectification efficiencies. Both their low loss and their high PIV allow the diodes to be used in mixer and modulator applications which require wide dynamic ranges.

The combination of these technical features with the low price make these devices the prime consideration for any hybrid DC or RF circuit requiring nonlinear elements.

Maximum Ratings

Operating Temperature Range ..... -65°C to +175 °C
Storage Temperature Range ..... -65°C to +200°C
Minimum Lead Strength ..... 4 grams pull on either lead
Diode Mounting Temperature ..... 350°C for 10 sec. max.
CW Power Dissipation at T_A = 25°C ..... 300 mW
Measured in an infinite heat sink derated linearly to zero at maximum rated temperature.

Bonding and Handling Procedures

See page 3-45.

Note: Diode above is typically bonded with active area onto the circuit or silicon side up.

Electrical Specifications at $T_A = 25°C$

Specification	Symbol	Min.	Max.	Units	Test Conditions
Breakdown Voltage	V_{BR}	70	–	Volts	$I_R = 10\ \mu A$
Forward Voltage	V_{F1}	–	410	mV	$I_{F1} = 1$ mA
Forward Voltage	V_{F2}	–	1.0	V	$I_{F2} = 15$ mA
Reverse Leakage Current	I_R	–	200	nA	$V_R = 50$ V
Capacitance	C_O	–	2.0	pF	$V_R = 0$ V and f = 1 MHz
Effective Minority Carrier Lifetime	τ	–	100*	psec	$I_F = 5$ mA Krakauer Method

*Typical

Typical Parameters

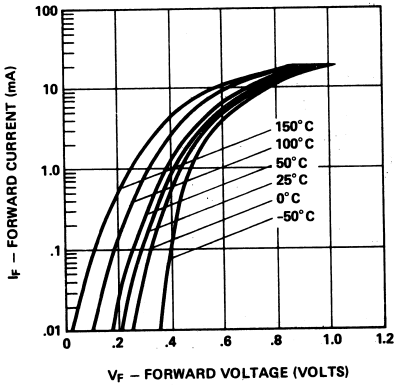


Figure 1. Typical Forward Characteristics.

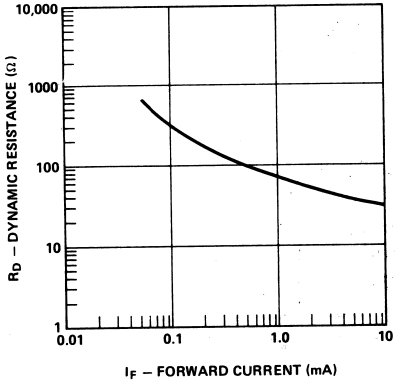


Figure 2. Typical Dynamic Resistance (R_D) vs. Forward Current (I_F).

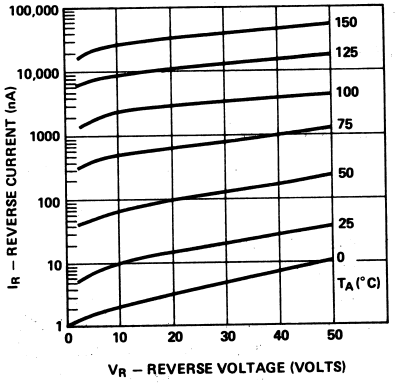


Figure 3. Typical Variation of Reverse Current (I_R) vs. Reverse Voltage (V_R) at Various Temperatures.

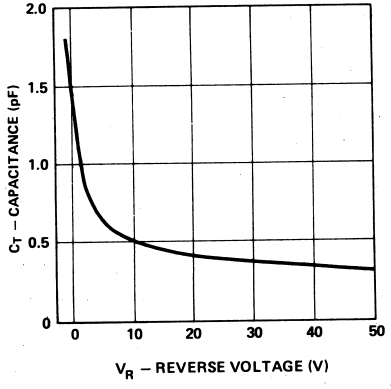


Figure 4. Typical Capacitance (C_T) vs. Reverse Voltage (V_R).

HEWLETT PACKARD

Beam Lead Schottky Diode Pairs for Mixers and Detectors

Technical Data

HSCH-5500 Series

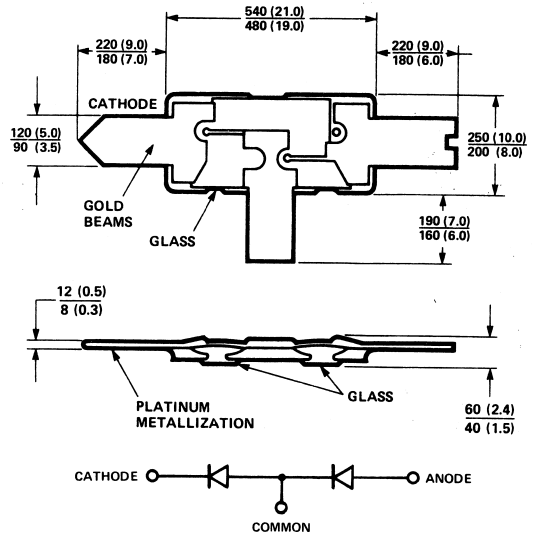
Features

- **Monolithic Pair**
  Closely Matched Electrical Parameters
- **Low Capacitance**
  0.1 pF Maximum at 0 Volts
- **Low Noise Figure**
  Guaranteed 7.5 dB at 26 GHz
- **Rugged Construction**
  4 Grams Minimum Lead Pull
- **Platinum Tri-Metal System**
  High Temperature Stability
- **Polyimide Scratch Protection**
- **Silicon Nitride Passivation**
  Stable, Reliable Performance

Description

These dual beam lead diodes are constructed using a metal-semiconductor Schottky barrier junction. Advanced epitaxial techniques and precise process control insure uniformity and repeatability of this planar passivated microwave semiconductor. A nitride passivation layer provides immunity from contaminants which could otherwise lead to I_R drift.

The HP beam lead process allows for large beam anchor pads for rugged construction (typical 6 gram pull strength) without degrading capacitance.



DIMENSIONS IN μm (1/1000 INCH)

Outline 04B

Maximum Ratings (for Each Diode)

Pulse Power Incident at T_A = 25°C ..... 1 W
Pulse Width = 1 µs, Du = 0.001
CW Power Dissipation at T_A = 25°C ..... 150 mW
Measured in an infinite heat sink derated linearly to zero at maximum rated temperature
T_{OPR} – Operating Temperature Range ..... -65°C to +175 °C
T_{STG} – Storage Temperature Range ..... -65°C to +200°C
Minimum Lead Strength ..... 4 grams pull on any lead
Diode Mounting Temperature ..... 350°C for 10 sec. max.

These diodes are ESD sensitive. Handle with care to avoid static discharge through the diode.

Applications

The beam lead diode is ideally suited for use in stripline or microstrip or coplanar waveguide circuits. Its small physical size and uniform dimensions give it low parasitics and repeatable RF characteristics through K-band.

These dual beam leads are intended for use in balanced mixers and in even harmonic anti-parallel pair mixers. By using several of these devices in the proper configuration it is easy to assemble bridge quads, star quads, and ring quads for Class I, II, or III type double balanced mixers.

Bonding and Handling Procedures

See page 3-45.

Table IA. Electrical Specifications for RF Tested Diodes at $T_A = 25°C$

Part Number HSCH-	Barrier	Max. Noise Figure NF (dB)	I_F Impedance Z_{IF} (Ω) Min.	I_F Impedance Z_{IF} (Ω) Max.	Max. SWR	Min. Breakdown Voltage V_{BR} (V)	Max. Dynamic Resistance R_D (Ω)	Max. ΔR_D (Ω)	Max. Total Capacitance C_T (pF)	Max. ΔC_T (pF)	Max. Forward Voltage V_F (mV)	Max. ΔV_F (mV)	Max. I_R (nA)
5520	Medium	7.5 at 26 GHz	200	400	1.5:1	4	20	3	0.10	0.02	500	10	100
5510		7.0 at 16 GHz					20		0.10				
5518		7.2 at 16 GHz					16	2	0.15	0.03			
5514		6.2 at 9.375 GHz					12		0.25				
5540	Low	7.5 at 26 GHz	150	350			20	3	0.10	0.02	375		400
5530		7.0 at 16 GHz					20		0.10				
5538		7.2 at 16 GHz					16	2	0.15	0.03			
5534		6.2 at 9.375 GHz					12		0.25				
Test Conditions		DC Load Resistance - 0 Ω LO Power = 1 mW I_F = 30 MHz, 1.5 dB NF				I_R = 10 μA	I_F = 5 mA		V_R = 0 V f = 1 MHz		I_F = 1 mA		V_R = 1 V
						Measured across adjacent leads.							

Table IB. Electrical Specifications for DC Tested Diodes at $T_A = 25°C$

Part Number HSCH-[1]	Barrier	Minimum Breakdown Voltage V_{BR} (V)	Maximum Dynamic Resistance R_D (Ω)	Max. ΔR_D (Ω)	Maximum Total Capacitance C_T (pF)	Max. ΔC_T (pF)	Maximum Forward Voltage V_F (mV)	Max. ΔV_F (mV)	Max. I_R (nA)
5511	Medium	4	20	3	0.10	0.02	500	10	100
5512			16	2	0.15	0.03			
5516			12		0.25				
5531	Low		20	3	0.10	0.02	375		400
5532			16	2	0.15	0.03			
5536			12		0.25				
Test Conditions		I_R = 10 μA	I_F = 5 mA		V_R = 0 V f = 1 MHz		I_F = 1 mA		V_R = 1 V

Note:
1. Standard Hi-Rel program available on HSCH-5511 and HSCH-5531. (See Tables II, III, and IV.) Others are available upon request.

Typical Detector Characteristics at T_A = 25°C

Medium Barrier and Low Barrier (DC Bias)

Parameter	Symbol	Typical Value	Units	Test Conditions
Tangential Sensitivity	TSS	-55	dBm	20 μA Bias, Zero Bias, P_{in} = -40 dBm, R_L = 100 kΩ Video Bandwidth = 2 MHz f = 10 GHz
Voltage Sensitivity	γ	9.0	mV/μW	
Video Resistance	R_V	1350	Ω	

Low Barrier (Zero Bias)

Parameter	Symbol	Typical Value	Units	Test Conditions
Tangential Sensitivity	TSS	-46	dBm	Zero Bias, Zero Bias, P_{in} = -30 dBm, R_L = 10 MΩ Video Bandwidth = 2 MHz f = 10 GHz
Voltage Sensitivity	γ	17	mV/μW	
Video Resistance	R_V	1.4	MΩ	

Typical Parameters

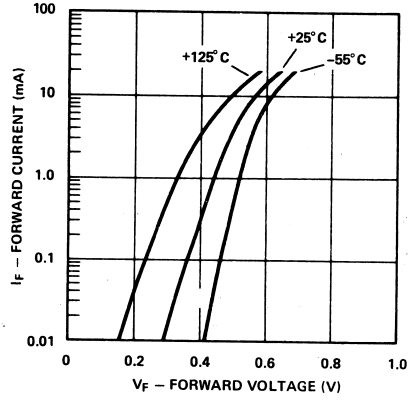


Figure 1. Typical Forward Characteristics for Medium Barrier Beam Lead Diodes. HSCH-5520 and HSCH-551X Series.

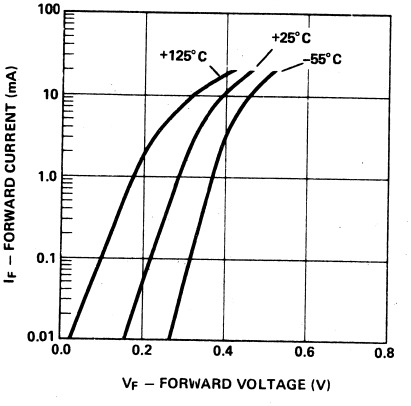


Figure 2. Typical Forward Characteristics for Low Barrier Beam Lead Diodes. HSCH-5540 and HSCH-553X Series.

Typical Parameters (cont.)

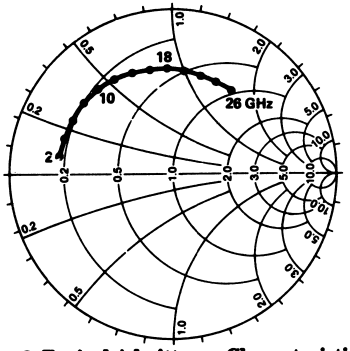


Figure 3. Typical Admittance Characteristics with 1 mA Self Bias. HSCH-5510, -5520, -5530, and -5340.

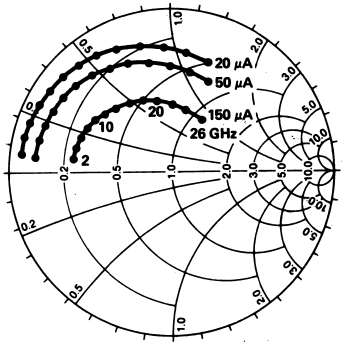


Figure 4. Typical Admittance Characteristics with External Bias. HSCH-5510, -5520, -5530, and -5540.

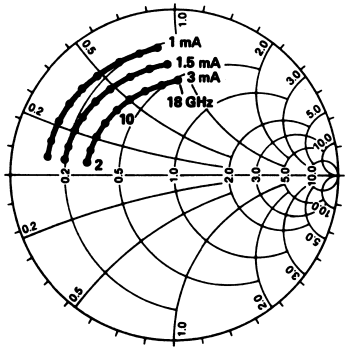


Figure 5. Typical Admittance Characteristics with Self Bias. HSCH-5518, -5538.

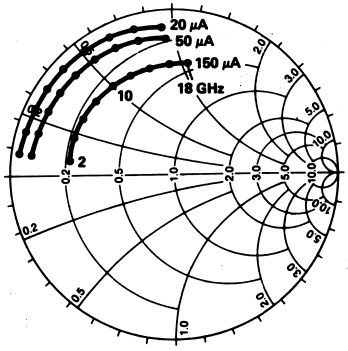


Figure 6. Typical Admittance Characteristics with External Bias. HSCH-5518, -5538.

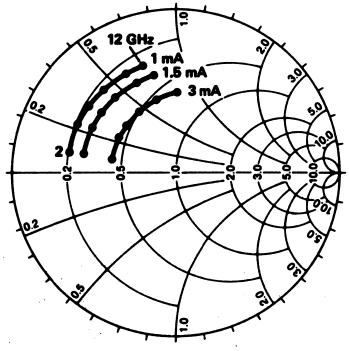


Figure 7. Typical Admittance Characteristics with Self Bias. HSCH-5514, -5534.

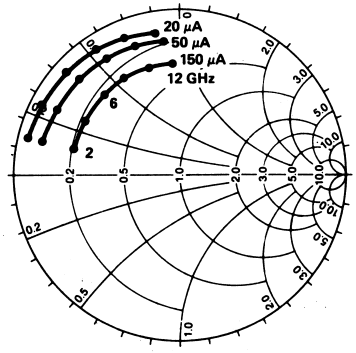


Figure 8. Typical Admittance Characteristics with External Bias. HSCH-5514, -5534.

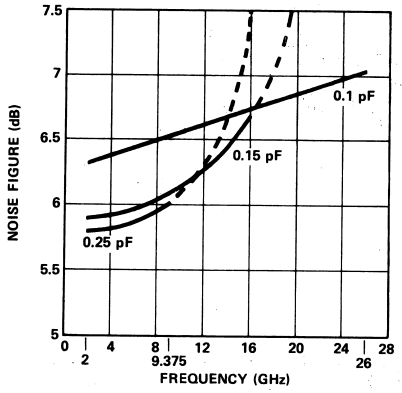
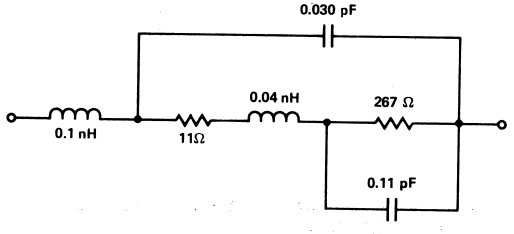


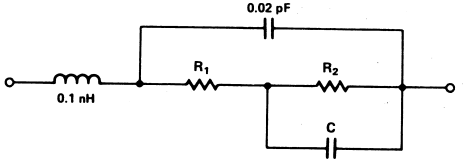
Figure 9. Typical Noise Figure vs. Frequency.

Models for Each Beam Lead Schottky Diode

HSCH-5510, -5520, -5530, -5540
1 mA Self Bias

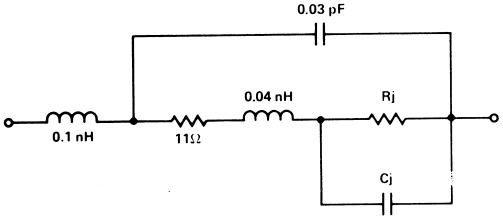


HSCH-5514, -5518, -5534, -5538
Self Bias



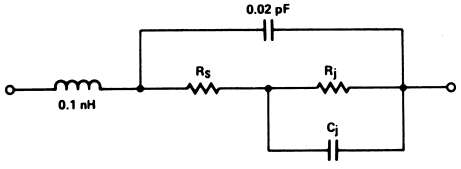
Part Numbers	1.0 mA Self Bias			1.5 mA Self Bias			3.0 mA Self Bias		
	R_1 (Ω)	R_2 (Ω)	C (pF)	R_1 (Ω)	R_2 (Ω)	C (pF)	R_1 (Ω)	R_2 (Ω)	C (pF)
HSCH-5518, -5538	5.0	393	0.11	5.2	232	0.11	5.0	150	0.12
HSCH-5514, -5534	5.1	244	0.16	5.0	178	0.16	5.0	109	0.19

HSCH-5510, -5520, -5530, -5540
External Bias



Part Numbers	20 μA DC Bias		50 μA DC Bias		150 μA DC Bias	
	R_j (Ω)	C_j (pF)	R_j (Ω)	C_j (pF)	R_j (Ω)	C_j (pF)
HSCH-5510, -5520, -5530, -5540	1400	0.09	560	0.09	187	0.10

HSCH-5518, -5538, -5514, -5534
External Bias



Part Numbers	20 μA DC Bias			50 μA DC Bias			150 μA DC Bias		
	R_S (Ω)	R_j (Ω)	C_j (pF)	R_S (Ω)	R_j (Ω)	C_j (pF)	R_S (Ω)	R_j (Ω)	C_j (pF)
HSCH-5518, -5538	2.8	1240	0.11	4.7	618	0.12	2.7	211	0.13
HSCH-5514, -5534	5.1	2050	0.18	3.9	665	0.19	4.7	242	0.20

HEWLETT PACKARD

Beam Lead Schottky Diode Ring Quads for Double Balanced Mixers Operating to 26 GHz

Technical Data

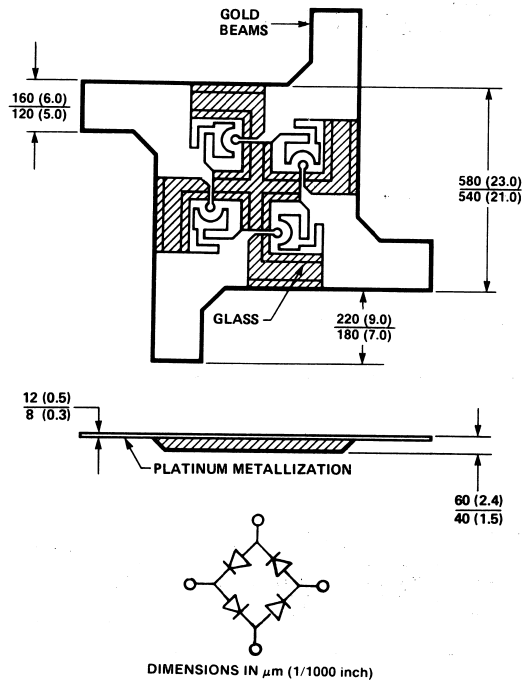
HSCH-5800 Series

Features

- **Monolithic Ring Quads** Closely Matched Electrical Parameters
- **Low Capacitance** 0.10 pF Max. at 0 V
- **Planar Surface** Easier Bonding, Stronger Leads
- **Platinum Tri-Metal System** High Temperature Stability
- **Polyimide Scratch Protection**
- **Silicon Nitride Passivation** Stable, Reliable Performance

Description

These beam lead diode quads are constructed using a metal-semiconductor Schottky barrier junction. Advanced epitaxial techniques and precise process control insure uniformity and repeatability of this planar passivated microwave semiconductor. A nitride passivation layer provides immunity from contaminants which could otherwise lead to I_R drift.



Outline 03

Maximum Ratings

CW Power Dissipation at T_{LEAD} = 25°C ..... 150 mW/junction
Derated linearly to zero at maximum rated temperature.
T_{OPR} – Operating Temperature Range ..... -65°C to +175 °C
T_{STG} – Storage Temperature Range ..... -65°C to +200°C
Minimum Lead Strength ..... 6 grams pull on any lead
Diode Mounting Temperature ..... 350°C for 10 sec. max.

These diodes are ESD sensitive. Handle with care to avoid static discharge through the diode.

Applications

These diodes are designed for use in double balanced mixers, phase detectors, AM modulator, and digital modulators requiring wideband operation and small size. The outline geometries are designed to balance the internal lead inductance for optimal performance at higher frequencies. The monolithic construction results in inherently low parasitics and extremely tight uniformity. The low barrier diodes allow for optimum mixer noise figure at lower than conventional local oscillator level. The wider dynamic range of the medium barrier diodes allows for better distortion performance.

Bonding and Handling Procedures

See page 3-45.

Electrical Specifications at $T_A = 25°C$

Part Number HSCH-	Frequency Band	Barrier	Maximum Capacitance C_M (pF)	Maximum Measured Capacitance Difference ΔC_M (pF)	Maximum Dynamic Resistance R_D (Ω)	Maximum Resistance Difference ΔR_D (Ω)	Maximum Forward Voltage V_F (mV)	Maximum V_F Difference ΔV_F (mV)
5816	X 12 GHz	Medium	0.25	0.03	12	2	500	15
5836		Low					375	
5812	Ku 18 GHz	Medium	0.15		16		500	
5832		Low					375	
5810	K 26 GHz	Medium	0.10	0.02	20	3	500	
5830		Low					375	
Test Conditions			$V_R = 0$ V f = 1 MHz		$I_F = 5$ mA		$I_F = 1$ mA	
					Measured across adjacent leads			

Dynamic and Series Resistance

Schottky diode resistance may be expressed as series resistance, R_S, or as dynamic resistance, R_D. These two terms are related by the equation

$$R_D = R_S + R_j$$

where R_j is the resistance of the junction. Junction resistance of a diode with DC bias is quite accurately calculated by

$$R_j = 26/I_B$$

where I_B is the bias current in milliamperes. The series resistance is independent of current.

The dynamic resistance is more easily measured. If series resistance is specified it is usually obtained by subtracting the calculated junction resistance from the measured dynamic resistance.

Quad Capacitance

Capacitance of Schottky diode quads is measured using an HP4271 LCR meter. This instrument effectively isolates individual diode branches from the others, allowing accurate capacitance measurement of each branch or each diode. The conditions are: 20 mV R.M.S. voltage at 1 MHz. HP defines this measurement as "C_M," and it is equivalent to the capacitance of the diode by itself. The equivalent diagonal and adjacent capacitances can then be calculated by the formulas given below.

In a quad, the diagonal capacitance is the capacitance between points A and B as shown in Figure 2. The diagonal capacitance is calculated using the following formula:

$$C_{DIAGONAL} = \frac{C_1 \times C_2}{C_1 + C_2} + \frac{C_3 \times C_4}{C_3 + C_4}$$

The equivalent adjacent capacitance is the capacitance between points A and C in Figure 2. This capacitance is calculated using the following formula:

$$C_{ADJACENT} = C_1 + \frac{1}{\frac{1}{C_2} + \frac{1}{C_3} + \frac{1}{C_4}}$$

Typical Characteristics

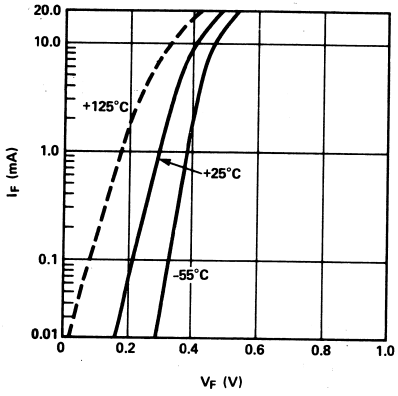


Figure 1. Typical Forward Characteristics for Low Barrier Diodes. HSCH-583X Series.

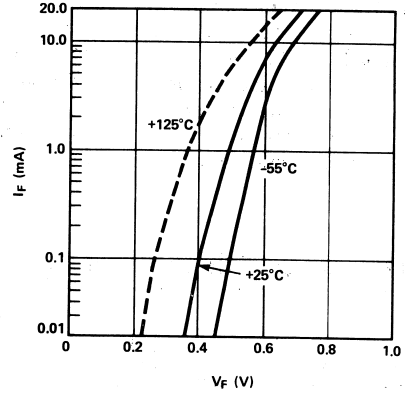


Figure 2. Typical Forward Characteristics for Medium Barrier Diodes. HSCH-581X Series.

HEWLETT PACKARD

Beam Lead Schottky Diode Bridge Quads for Double-Balanced Mixers and Samplers

Technical Data

HSCH-5900 Series

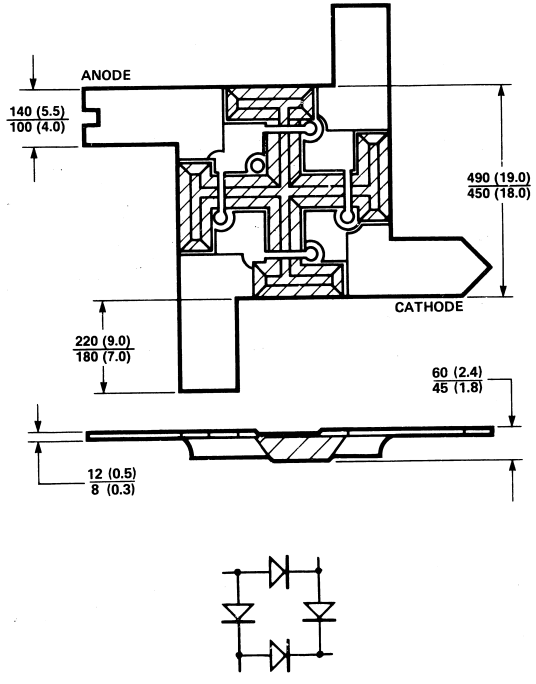
Features

- **Monolithic Bridge Quads**
  Closely Matched Electrical Parameters
  Low, Medium, High Barrier
- **Planar Surface**
  Easier Bonding
- **Platinum Tri-Metal System**
  High Temperature Stability
- **Polyimide Scratch Protection**
- **Silicon Nitride Passivation**
  Stable, Reliable Performance

Description/ Applications

These beam lead diode quads are constructed using a metal-semiconductor Schottky barrier junction. Advanced epitaxial techniques and precise process control ensure uniformity and repeatability of this planar passivated microwave semiconductor. A nitride passivation layer provides immunity from contaminants which could otherwise lead to I_R drift.

These diodes are designed for use in double balanced mixers and sampling circuits requiring wideband operation and small size. The monolithic construction results in inherently low parasitics and extremely tight uniformity. The wide dynamic range of medium barrier diodes allows for good distortion performance.



DIMENSIONS IN μm (1/1000 inch)

Outline 08B

Assembly Techniques

Thermocompression bonding is recommended. Welding, ultrasonic bonding, solder, or conductive epoxy may also be used. For additional information see Application Note 979, "The Handling and Bonding of Beam Lead Devices Made Easy", or Application Note 992, "Beam Lead Attachment Methods", or Application Note 993, "Beam Lead Device Bonding to Soft Substrates".

Bonding and Handling Procedures

See page 3-45.

Maximum Ratings

CW Power Dissipation at T_{LEAD} = 25°C ..... 150 mW/junction
Derated linearly to zero at maximum rated temperature.
T_{OPR} – Operating Temperature Range ..... -65°C to +175°C
T_{STG} – Storage Temperature Range ..... -65°C to +200°C
Minimum Lead Strength ..... 6 grams pull on any lead
Diode Mounting Temperature ..... 350°C for 10 sec. max.

These diodes are ESD sensitive. Handle with care to avoid static discharge through the diode.

Electrical Specifications at T_A = 25°C

Part Number HSCH-	Frequency Band	Barrier	Maximum Capacitance C_M (pF)	Maximum Measured Capacitance Difference ΔC_M (pF)	Maximum Dynamic Resistance R_D (Ω)	Minimum Breakdown Voltage V_{BR} (V)	Maximum Forward Voltage V_F (mV)	Maximum V_F Difference ΔV_F (mV)
5938 5918 5958	C 6 GHz	Low Medium High	0.50	0.05	10	4	350 450 650	20
5932 5912 5952	Ku 18 GHz	Low Medium High	0.15	0.03	16	4	375 500 675	20
Test Conditions			V_R = 0 V	V_R = 0 V f = 1 MHz	I_F = 5 mA	$I_R \leq 10$ µA	I_F = 1 mA	I_F = 5 mA
				Measured across adjacent leads				

Dynamic and Series Resistance

Schottky diode resistance may be expressed as series resistance, R_S, or as dynamic resistance, R_D. These two terms are related by the equation

$$R_D = R_S + R_j$$

where R_j is the resistance of the junction. Junction resistance of a diode with DC bias is quite accurately calculated by

$$R_j = 26/I_B$$

where I_B is the bias current in milliamperes. The series resistance is independent of current.

The dynamic resistance is more easily measured. If series resistance is specified it is usually obtained by subtracting the calculated junction resistance from the measured dynamic resistance.

Quad Capacitance

Capacitance of Schottky diode quads is measured using an HP4271 LCR meter. This instrument effectively isolates individual diode branches from the others, allowing accurate capacitance measurement of each branch or each diode. The conditions are: 20 mV R.M.S. voltage at 1 MHz. HP defines this measurement as "C_M," and it is equivalent to the capacitance of the diode by itself. The equivalent diagonal and adjacent capacitances can then be calculated by the formulas given below.

In a quad, the diagonal capacitance is the capacitance between points A and B as shown in Figure 2. The diagonal capacitance is calculated using the following formula:

$$C_{DIAGONAL} = \frac{C_1 \times C_2}{C_1 + C_2} + \frac{C_3 \times C_4}{C_3 + C_4}$$

The equivalent capacitance is the capacitance between points A and C in Figure 2. This capacitance is calculated using the following formula:

$$C_{ADJACENT} = C_1 + \frac{1}{\frac{1}{C_2} + \frac{1}{C_3} + \frac{1}{C_4}}$$

Typical Parameters

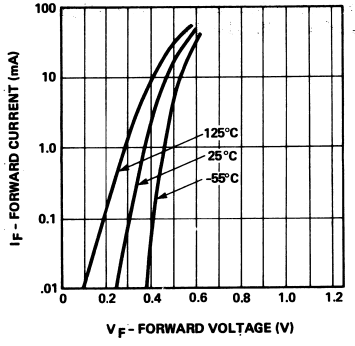


Figure 1. Typical Forward Characteristics for Medium Barrier Beam Lead Diode, HSCH-5918.

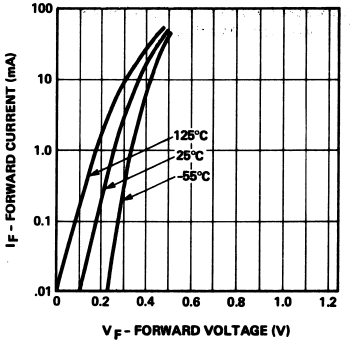


Figure 2. Typical Forward Characteristics for Low Barrier Beam Lead Diode, HSCH-5938.

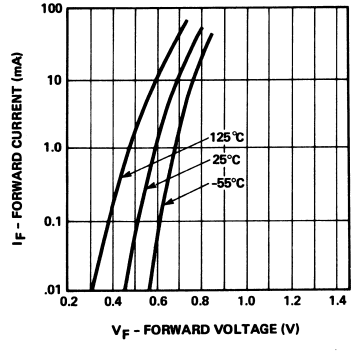


Figure 3. Typical Forward Characteristics for High Barrier Beam Lead Diode, HSCH-5958.

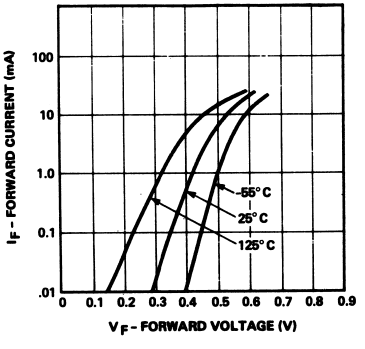


Figure 4. Typical Forward Characteristics for Medium Barrier Beam Lead Diode, HSCH-5912.

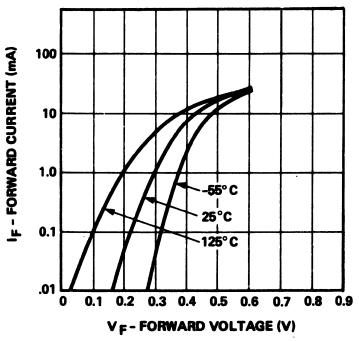


Figure 5. Typical Forward Characteristics for Low Barrier Beam Lead Diode, HSCH-5932.

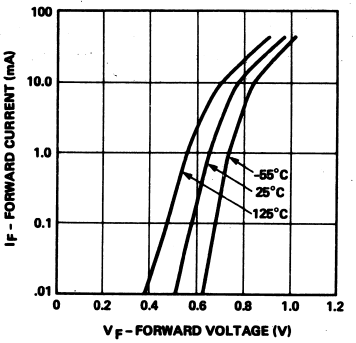


Figure 6. Typical Forward Characteristics for High Barrier Beam Lead Diode, HSCH-5952.

HEWLETT PACKARD

GaAs Beam Lead Schottky Barrier Diodes

Technical Data

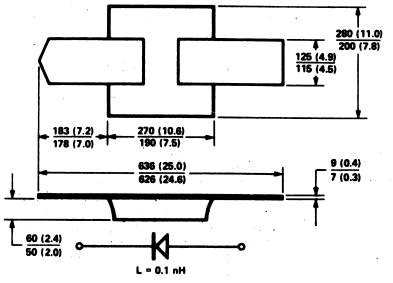
HSCH-9101
HSCH-9201
HSCH-9251

Features

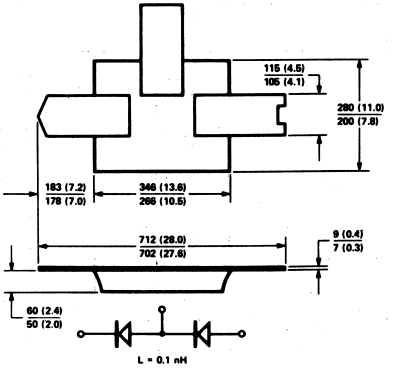
- **Gold Tri-Metal System**
  For Improved Reliability
- **Low Capacitance**
- **Low Series Resistance**
- **High Cutoff Frequency**
- **Polyimide Passivation**
- **Low Noise Figure Through K_a Band**
  Guaranteed at 44 GHz
- **Multiple Configurations**

Description

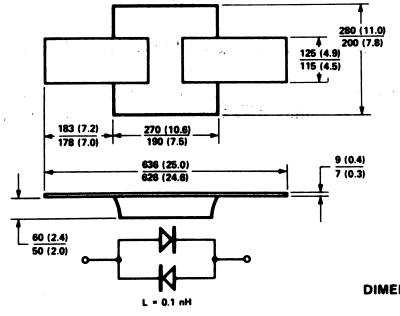
The HSCH-9101 single, the HSCH-9201 series pair, and the HSCH-9251 anti-parallel pair are advanced gallium arsenide Schottky barrier diodes. These devices are fabricated utilizing molecular beam epitaxy (MBE) manufacturing techniques and feature rugged construction and consistent electrical performance. A polyimide coating provides scratch protection and resistance to contamination.



HSCH-9101



HSCH-9201



HSCH-9251
Junction Side Up

DIMENSIONS IN μm (1/1000 inch)

Applications

This line of Schottky diodes is optimized for use in mixer applications at millimeter wave frequencies. Some suggested mixer types are single ended and single balanced for the single and series pair. The anti-parallel pair is ideal for harmonic mixers.

Assembly Techniques

Thermocompression bonding is recommended. Welding, ultrasonic bonding, solder, or conductive epoxy may also be used. For additional information see Application Note 979, "The Handling and Bonding of Beam Lead Devices Made Easy," or Application Note 992, "Beam Lead Attachment Methods," or Application Note 993, "Beam Lead Device Bonding to Soft Substrates."

GaAs diodes are ESD sensitive. Proper precautions should be used when handling these devices.

Maximum Ratings

Power Dissipation at T_{LEAD} = 25°C ..... 75 mW per junction
Measured in an infinite heat sink derated linearly to zero at maximum rated temperature
Operating Temperature ..... -65°C to +150°C
Storage Temperature ..... -65°C to +150°C
Mounting Temperature ..... 235°C for 10 seconds
Minimum Lead Strength ..... 6 grams

Bonding and Handling Procedures

See page 3-45.

Electrical Specifications at T_A = 25°C

Part Number			HSCH-9101			HSCH-9201			HSCH-9251		
Symbol	**Parameters and Test Conditions**	**Units**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
C_j[1]	Junction Capacitance V_R = 0 V, f = 1 MHz	pF		0.040	0.050		0.040	0.050		0.040	
ΔC_j[1]	Junction Capacitance Difference V_R = 0 V, f = 1 MHz	pF					0.005	0.010			
R_S[2]	Series Resistance	Ω			6			6			6
V_{F1}	Forward Voltage I_F = 1 mA	mV		700	800		700	800		700	800
V_{F10}	Forward Voltage I_F = 10 mA	mV		800	850		800	850		800	850
ΔV_F	Forward Voltage Difference I_F = 1 mA and 10 mA	mV						15			15
V_{BR}	Reverse Breakdown Voltage $V_R = V_{BR}$ measure $I_R \leq 10$ μA (per junction)	V	4.5			4.5					
NF[3]	Noise Figure at 44 GHz	dB		6.7	7.2		6.7	7.2		6.7	
SWR	Standing Wave Ratio at Noise Figure			1.35	1.5		1.35	1.5			
Z_{IF}	IF Impedance at Noise Figure	Ω	125	200	325	125	200	325			

Notes:
1. Junction capacitance is determined by measuring total device capacitance and subtracting the calculated parasitic capacitance (0.035 pF).
2. Series resistance is determined by measuring the dynamic resistance and subtracting the calculated junction resistance of 6 Ω.
3. Noise figure is determined by lot sampling (LTPD = 15), LO power = 6 dBm, IF = 90 MHz, and the IF noise figure (1.5 dB) is included.

Typical Parameters

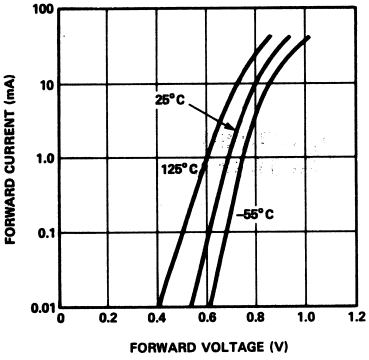


Figure 1. Typical Forward Characteristics for HSCH-9101, HSCH-9201, and HSCH-9251.

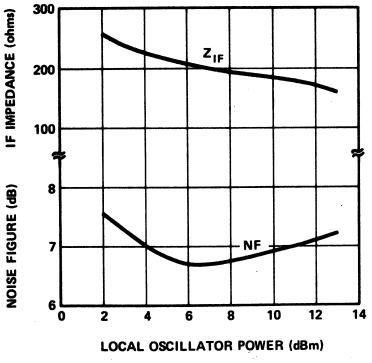


Figure 2. Typical Noise Figure and I.F. Impedance vs. Local Oscillator Power, for HSCH-9101 and HSCH-9201.

HEWLETT PACKARD

GaAs Beam Lead Schottky Barrier Ring and Bridge Diodes

Technical Data

HSCH-9301
HSCH-9351

Features

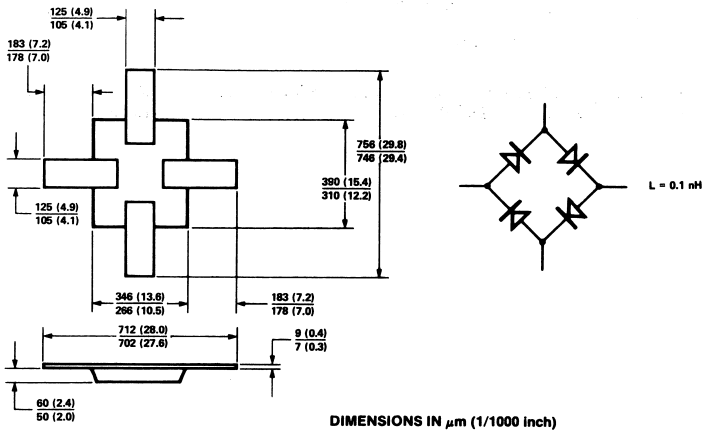
- **Gold Tri-Metal System** For Improved Reliability
- **Low Capacitance**
- **Low Series Resistance**
- **High Cutoff Frequency**
- **Polyimide Passivation**

Description

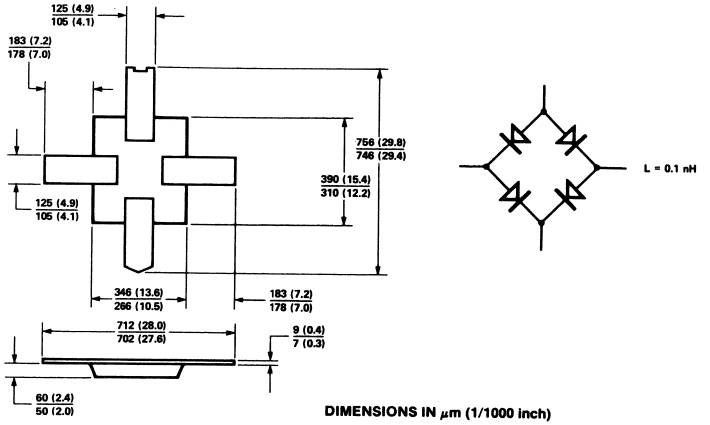
The HSCH-9301 ring quad and the HSCH-9351 bridge quad are advanced gallium arsenide Schottky barrier diodes. These devices are fabricated utilizing molecular beam epitaxy (MBE) manufacturing techniques and feature rugged construction and consistent electrical performance. A polyimide coating provides scratch protection and resistance to contamination.

Applications

This line of Schottky diodes is optimized for use in mixer applications at millimeter wave frequencies. Some suggested mixer types are double balanced for the ring quad and biased double balanced for the bridge quad. The bridge quad can also be used in sampling circuits.



HSCH-9301



HSCH-9351
Junction Side Up

Assembly Techniques

Thermocompression bonding is recommended. Welding, ultrasonic bonding, solder, or conductive epoxy may also be used. For additional information see Application Note 979, "The Handling and Bonding of Beam Lead Devices Made Easy," or Application Note 992, "Beam Lead Attachment Methods," or Application Note 993, "Beam Lead Device Bonding to Soft Substrates."

GaAs diodes are ESD sensitive. Proper precautions should be used when handling these devices.

Maximum Ratings

Power Dissipation at T_{LEAD} = 25°C ..... 75 mW per junction
Measured in an infinite heat sink derated linearly to zero at maximum rated temperature
Operating Temperature ..... -65°C to +150°C
Storage Temperature ..... -65°C to +150°C
Mounting Temperature ..... 235°C for 10 seconds
Minimum Lead Strength ..... 6 grams

Electrical Specifications at T_A = 25°C

Part Number			HSCH-9301			HSCH-9351		
Symbol	**Parameters and Test Conditions**	**Units**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
C_M	Measured Capacitance V_R = 0 V, f = 1 MHz	pF		0.075	0.100		0.075	0.100
C_{TA}	Total Adjacent Capacitance V_R = 0 V, f = 1 MHz	pF		0.110			0.110	
C_{TD}	Total Diagonal Capacitance V_R = 0 V, f = 1 MHz	pF		0.075			0.075	
ΔC_M	Measured Capacitance Difference V_R = 0 V, f = 1 MHz	pF		0.003	0.010		0.003	0.010
R_S	Series Resistance	Ω			6			6
V_F	Forward Voltage I_F = 1 mA	mV		700	800		700	800
ΔV_F	Forward Voltage Difference I_F = 1 mA	mV			20			20
V_{BR}	Reverse Breakdown Voltage $V_R = V_{BR}$ measure $I_R \leq 10\ \mu A$ (per junction)	V				4.5		

Typical Parameters

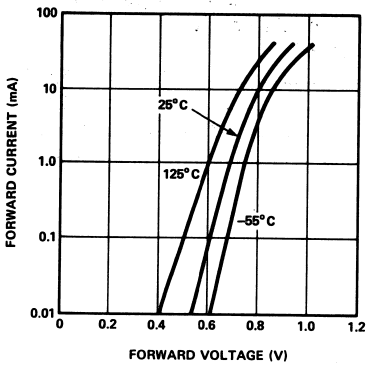


Figure 1. Typical Forward Characteristics for HSCH-9301, HSCH-9351.

Dynamic and Series Resistance

Schottky diode resistance may be expressed as series resistance, R_S, or as dynamic resistance, R_D. These two terms are related by the equation

$$R_D = R_S + R_j$$

where R_j is the resistance of the junction. Junction resistance of a diode with DC bias is quite accurately calculated by

$$R_j = 26/I_B$$

where I_B is the bias current in milliamperes. The series resistance is independent of current.

The dynamic resistance is more easily measured. If series resistance is specified it is usually obtained by subtracting the calculated junction resistance from the measured dynamic resistance.

Quad Capacitance

Capacitance of Schottky diode quads is measured using an HP4271 LCR meter. This instrument effectively isolates individual diode branches from the others, allowing accurate capacitance measurement of each branch or each diode. The conditions are: 20 mV R.M.S. voltage at 1 MHz. HP defines this measurement as "C_M," and it is equivalent to the capacitance of the diode by itself. The equivalent diagonal and adjacent capacitances can then be calculated by the formulas given below.

In a quad, the diagonal capacitance is the capacitance between points A and B as shown in Figure 2. The diagonal capacitance is calculated using the following formula

$$C_{DIAGONAL} = \frac{C_1 \times C_2}{C_1 + C_2} + \frac{C_3 \times C_4}{C_3 + C_4}$$

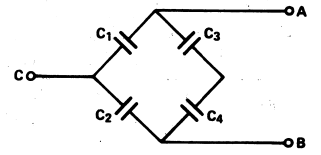


Figure 2.

The equivalent capacitance is the capacitance between points A and C in Figure 2. This capacitance is calculated using the following formula

$$C_{ADJACENT} = C_1 + \frac{1}{\frac{1}{C_2} + \frac{1}{C_3} + \frac{1}{C_4}}$$

Bonding and Handling Procedures for Beam Lead Diodes

1. Storage

Under normal circumstances, storage of beam lead diodes in HP supplied waffle/gel packs is sufficient. In particularly dusty or chemically hazardous environments, storage in an inert atmosphere desiccator is advised.

2. Handling

In order to avoid damage to beam lead devices, particular care must be exercised during inspection, testing, and assembly. Although the beam lead diode is designed to have exceptional lead strength, its small size and delicate nature requires that special handling techniques be observed so that the devices will not be mechanically or electrically damaged. A vacuum pickup is recommended for picking up beam lead devices, particularly larger ones, e.g., quads. Care must be exercised to assure that the vacuum opening of the needle is sufficiently small to avoid passage of the device through the opening. A #27 tip is recommended for picking up single beam lead devices. A 20X magnification is needed for precise positioning of the tip on the device. Where a vacuum pickup is not used, a sharpened wooden Q-tip dipped in isopropyl alcohol is very commonly used to handle beam lead devices.

3. Cleaning

For organic contamination use a warm rinse of trichloroethane followed by a cold rinse in acetone and methanol. Dry under infrared heat lamp for 5-10 minutes on clean filter paper. Freon degreaser may replace trichloroethane for light organic contamination.

- Ultrasonic cleaning is not recommended.
- Acid solvents should not be used.

4. Bonding

See Application Note 992, "Beam Lead Attachment Methods", for a general description of the various methods for attaching beam lead diodes to both hard and soft substrates.

Thermocompression: See Application Note 979 "The Handling and Bonding of Beam Lead Devices Made Easy". This method is good for hard substrates only.

Wobble: This method picks up the device, places it on the substrate and forms a thermocompression bond all in one operation. This is described in MIL-STD-883, Method 2017 and is intended for hard substrates only. Equipment specifically designed for beam lead wobble bonding is available from KULICKE and SOFFA in Horsham, PA.

Ultrasonic: Not recommended.

Resistance Welding or Parallel-GAP Welding: To make welding on soft substrates easier, a low pressure welding head is recommended. Suitable equipment is available from HUGHES, Industrial Products Division in Carlsbad, CA.

For more information, see Application Note 993, "Beam Lead Diode Bonding to Soft Substrates".

Epoxy: With solvent free, low resistivity epoxies (available from ABLESTIK in Gardena, CA, MICON in Lexington, MA, and many others) and improvements in dispensing equipment, the quality of epoxy bonds is sufficient for many applications. Equipment is available from ADVANCED SEMICONDUCTOR MATERIALS AMERICA, INC., Assembly Products Group in Chandler, AZ (Automatic), and WEST BOND in Orange, CA (Manual).

Reflow: By preparing the substrate with tin or solder plating, reflow soldering can be suitably performed using a modified wire bonder. The probe is used as a soldering tip. WEST BOND or UNITEK bonders make suitable bonds.

HEWLETT PACKARD

Zero Bias Schottky Diodes for Mixers and Detectors

Technical Data

HSCH-3206/07
HSCH-3486

Features

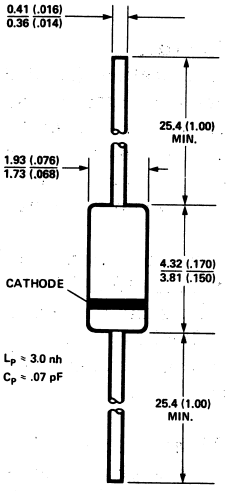
- **High Voltage Sensitivity**
- **No Bias Required**
- **Choice of High or Low Video Impedance**

Description/ Applications

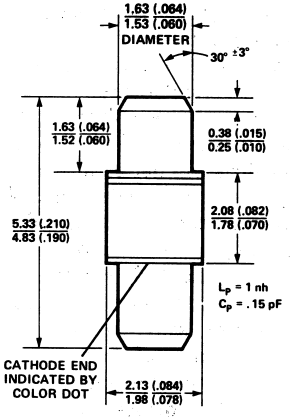
The high zero bias voltage sensitivity of these Schottky barrier diodes makes them ideally suited for narrow bandwidth video detectors, ECM receivers, and measurement equipment. These diodes also make excellent mixers for use with low power LO.

Package Characteristics

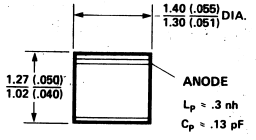
The HP Outline 15 package has a glass hermetic seal with gold plated Dumet leads which should be restricted so that the bend starts at least 1/16" (1.6 mm) from the glass body. With this restriction, it will meet MIL-STD-750, Method 2036, Condition A (4 lb. [1.8 kg] tension for 30 minutes). The maximum soldering temperature is 230°C for 5 seconds. Marking is by digital coding with a cathode band.



Outline 15



Outline 49



DIMENSIONS IN MILLIMETERS AND (INCHES).

Outline 44

The HP Outline 49 package has a metal-ceramic hermetic seal. The anode and cathode studs are gold-plated Kovar. The maximum soldering temperature is 230°C for 5 seconds. Stud-stud TIR is 0.010" max.

The HP Outline 44 package is a hermetically sealed ceramic package. The anode and cathode are gold-plated Kovar. The maximum soldering temperature is 230°C for 5 seconds.

Maximum Ratings

Operating and Storage Temperature Range ..... -65°C to +150 °C
CW Power Dissipation at T_{CASE} = 25°C
HSCH-3206, -3207 ..... 200 mW
HSCH-3486 ..... 300 mW
Derate Linearly to 0 W at 150°C
Pulse Power Dissipation at T_{CASE} = 25°C
Peak power incident.
1 μs pulse, Du = 0.001 ..... 1 W

These diodes are ESD sensitive. Handle with care to avoid static discharge through the diode.

Electrical Specifications at T_A = 25°C

Part Number	Package Outline	Maximum Tangential Sensitivity TSS (dBm)	Minimum Voltage Sensitivity γ (mV/μW)	Video Resistance R_V (KΩ) Min.	Max.	Typical Total Capacitance C_T (pF)
HSCH-3207	44	-42	8	80	300	0.30
HSCH-3206	49	-42	8	80	300	0.30
HSCH-3486	15	-54	7.5	2	8	0.30
Test Conditions		Video Bandwidth = 2 MHz f_{test} = 10 GHz	Power in = -30 dBm f_{test} = 10 GHz R_L = 10 MΩ, I_{bias} = 0			V_R = 0 V f = 1 MHz

Typical Characteristics

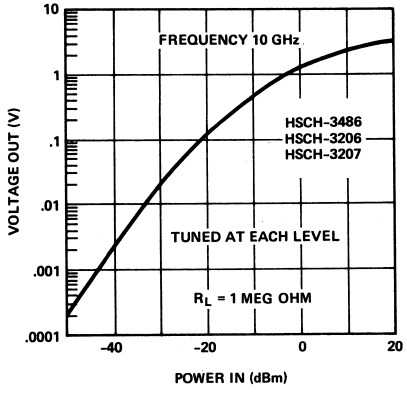


Figure 1. Typical Dynamic Transfer Characteristics.

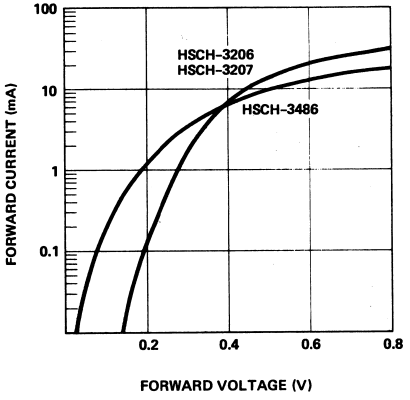


Figure 2. Typical Forward Characteristics at T_A = 25°C.

Typical Characteristics (cont.)

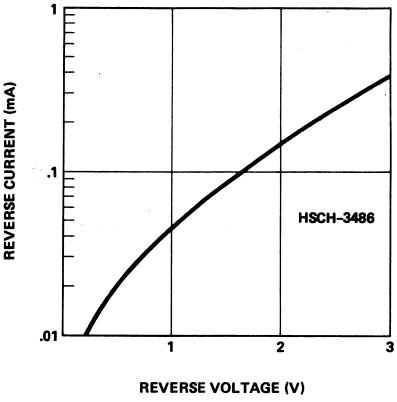


Figure 3. Typical Reverse Characteristics at T_A = 25°C.

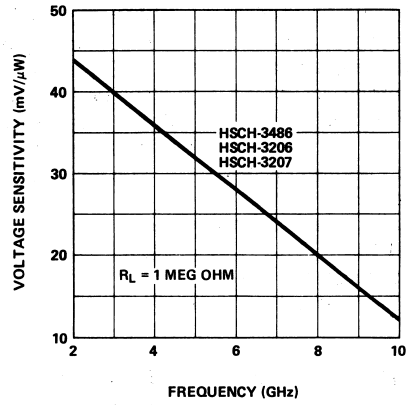


Figure 4. Typical Voltage Sensitivity vs. Frequency.

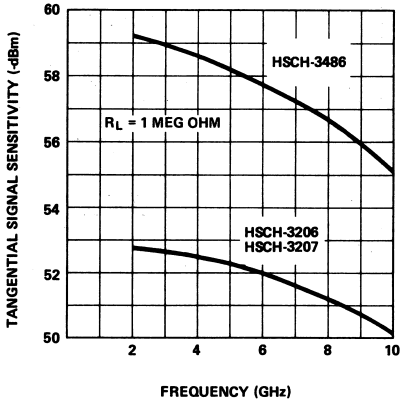


Figure 5. Typical Tangential Sensitivity vs. Frequency.

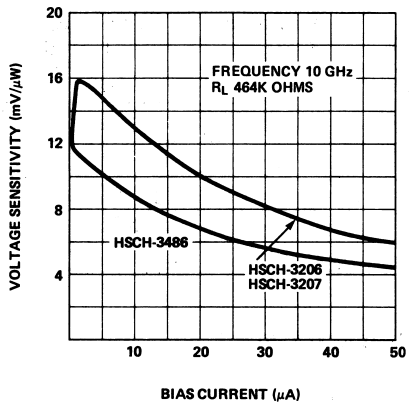


Figure 6. Typical Voltage Sensitivity vs. Bias Current.

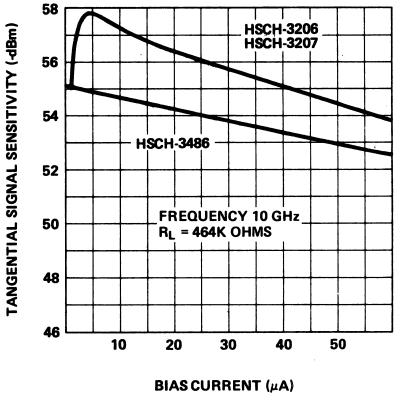


Figure 7. Typical Tangential Sensitivity vs. Bias Current.

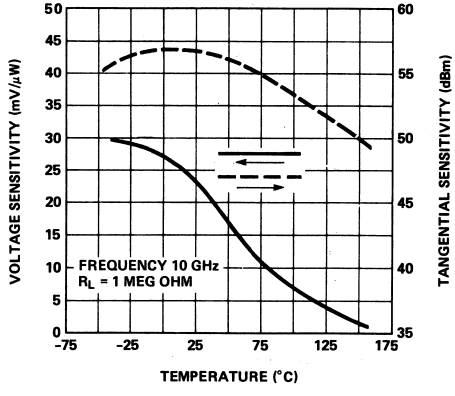


Figure 8. Effect of Temperature on HSCH-3486.

Typical Characteristics (cont.)

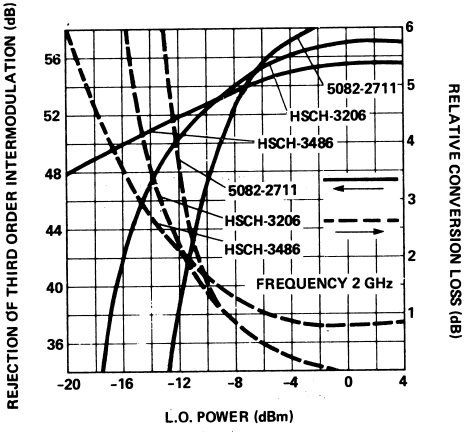


Figure 9. Mixer Performance.

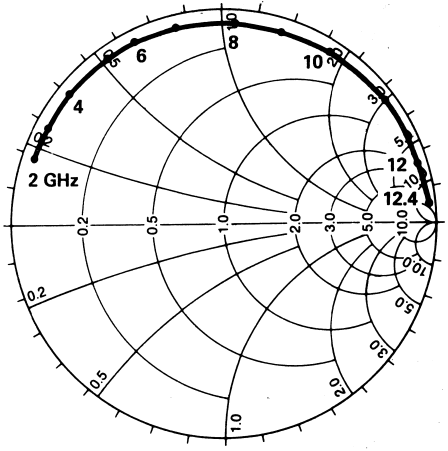


Figure 10. Typical Admittance Characteristics, HSCH-3206.

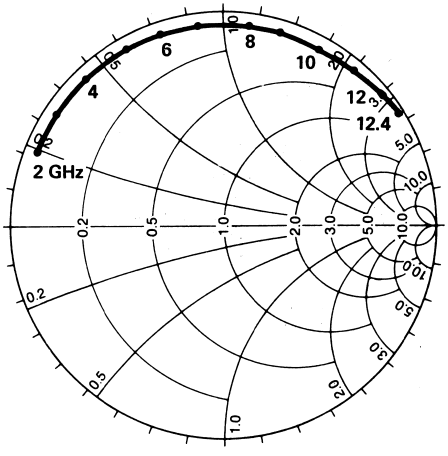


Figure 11. Typical Admittance Characteristics, HSCH-3207.

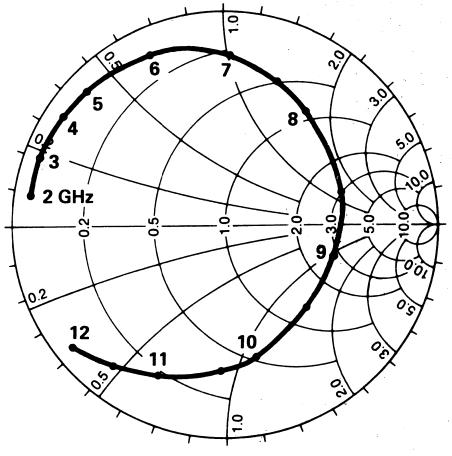


Figure 12. Typical Admittance Characteristics, HSCH-3486.

HEWLETT PACKARD

Hermetic Schottky Diodes for Mixers and Detectors (1-18 GHz)

Technical Data

HSCH-6000 Series

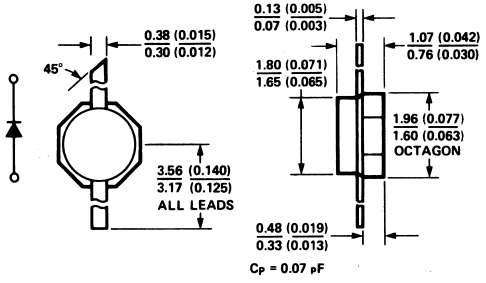
Features

- **Low Parasitic Hermetic Package**
  - –High Frequency Performance
  - –Meets Performance Standards of Space Level Testing
- **Lead Forming Option**
  No Board Drilling Required
- **Rugged Construction**
  MIL-STD-750 Compliance
- **High Uniformity**
  Tightly Controlled Process Insures Consistent Performance
- **Silicon Nitride Passivation, Tri-Metallization**
  Stable High Temperature Performance

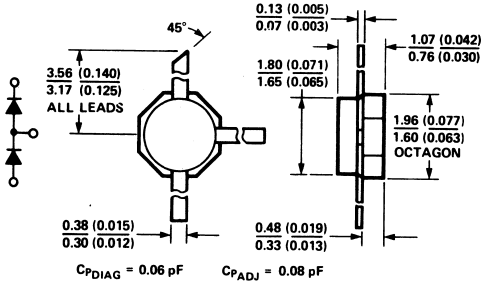
Description

These Schottky barrier diodes are fabricated by advanced epitaxial techniques. Precise process control insures uniformity and repeatability of this planar beam lead microwave semiconductor. A nitride passivation layer provides immunity from contaminants which could otherwise lead to I_R drift.

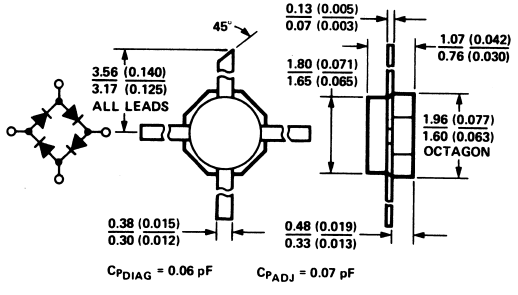
These diodes are packaged in the hermetic J package. Advanced design and assembly



Outline J-2



Outline J-3



Outline J-4

DIMENSIONS IN MILLIMETERS AND (INCHES)

processes minimize package parasitics resulting in optimum performance.

The body of the package is alumina, while the leads are gold-plated over nickel-plated Kovar. The solder glass seal and rugged construction meet the stringent requirements of space-level testing and are capable of meeting the environmental tests of MIL-STD-750.

Applications

These hermetic devices are designed for stripline and microstrip use. The design features extremely low package parasitics. The package outline also maximizes lead strength while reducing overall body size. This design is especially useful in environments requiring high frequency and/or wide band operation.

The single diode can be used in either mixer or detector applications. The pairs can be used in balanced mixers and can be configured to assemble bridge, star, and ring quads for Class I, II, or III type double balanced mixers. The quads are used as double balanced mixers, phase detectors, and AM and digital modulators.

Maximum Ratings

Pulse Power Incident at T_{CASE} = 25°C
(1 µs pulse, DC = 0.001) ..... 1 W
CW Power Dissipation at T_{CASE} = 25°C
Derate Linearly to Zero at 175°C ..... 150 mW/junction
Operating Temperature Range ..... -65°C to +175°C
Storage Temperature Range ..... -65°C to +200°C
Soldering Temperature ..... 290°C Max. for 10 sec.

These diodes are ESD sensitive. Handle with care to avoid static discharge through the diode.

Electrical Specifications at T_{CASE} = 25°C

Single Diode in J-2 Package

Part Number HSCH-	Barrier	Maximum Noise Figure NF (dB)	IF Impedance Z_{IF} (Ω) Min.	Max.	Maximum SWR	Minimum Breakdown Voltage V_{BR} (V)	Maximum Dynamic Resistance R_D (Ω)	Maximum Forward Voltage V_F (mF)	Maximum Total Capacitance C_T (pF)
6310	Medium	7.2 at 16 GHz	200	400	1.5:1	4	16	500	0.22
6312		6.2 at 9.375 GHz					12		0.27
6330	Low	7.2 at 16 GHz	150	350			16	375	0.22
6332		6.2 at 9.375 GHz					12		0.27
Test Conditions		DC Load Resistance = 0 Ω L.O. Power = 1 mW I_F = 30 MHz, 1.5 dB NF				$I_R \leq 10$ µA	I_F = 5 mA	I_F = 1 mA	V_R = 0 V f = 1 MHz

Diode Pairs in J-3 Package

Part Number HSCH-	Barrier	Max. Noise Figure NF (dB)	IF Impedance Z_{IF} (Ω) Min.	Max.	Max. SWR	Min. Breakdown Voltage V_{BR} (V)	Max. Dynamic Resistance R_D (Ω)	Max. ΔR_D (Ω)	Max. Total Capacitance C_T (pF)	Max. ΔC_T (pF)	Max. Forward Voltage V_F (mV)	Max. ΔV_F (mV)
6510	Medium	7.2 at 16 GHz	200	400	1.5:1	4	16	3	0.22	0.02	500	10
6512		6.2 at 9.375 GHz					12		0.27			
6530	Low	7.2 at 16 GHz	150	350			16		0.22		375	
6532		6.2 at 9.375 GHz					12		0.27			
Test Conditions		DC Load Resistance = 0 Ω L.O. Power = 1 mW I_F = 30 MHz, 1.5 dB NF				$I_R \leq 10$ μA	I_F = 5 mA		V_R = 0 V f = 1 MHz		I_F = 1 mA	
						Measured between adjacent leads.						

Diode Quads in J-4 Package

Frequency Band	Part Number HSCH-	Barrier	Maximum Capacitance C_M (pF)	Maximum Measured Capacitance Difference ΔC_M (pF)	Maximum Dynamic Resistance R_D (Ω)	Maximum Resistance Difference ΔR_D (Ω)	Maximum Forward Voltage V_F (mF)	Maximum V_F Difference ΔV_F (mV)
Ku	6810	Medium	0.22	0.03	20	3	500	15
18 GHz	6830	Low					375	
X	6812	Medium	0.27		16	2	500	
12 GHz	6832	Low					375	
Test Conditions			V_R = 0 V f = 1 MHz		I_F = 5 mA		I_F = 1 mA	
					Measured between adjacent leads.			

Typical Parameters

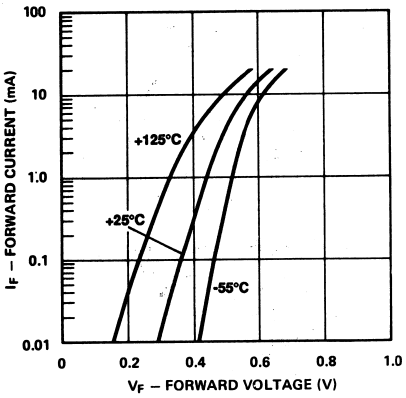


Figure 1. Typical Forward Characteristics for Medium Barrier Diodes.

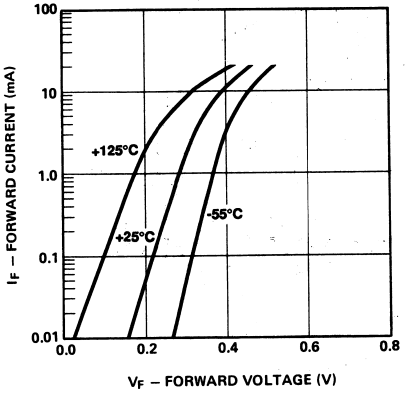


Figure 2. Typical Forward Characteristics for Low Barrier Diodes.

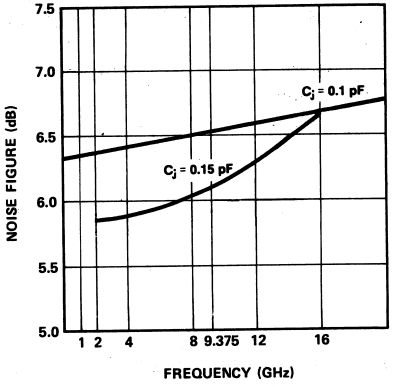


Figure 3. Typical Noise Figure vs. Frequency for J-Packages.

Typical Parameters (cont.)

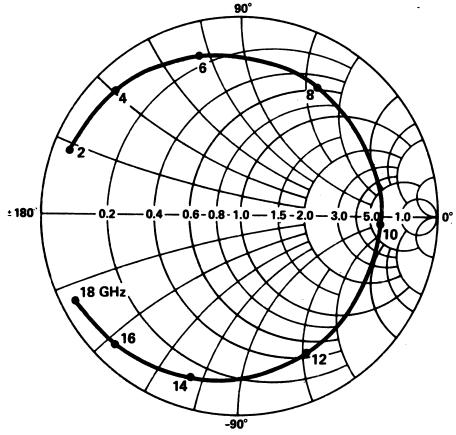


Figure 4. Typical Admittance Characteristics with 20 μA External Bias. HSCH-6310, -6330.

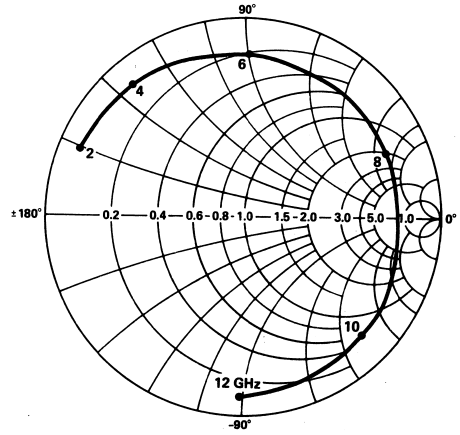
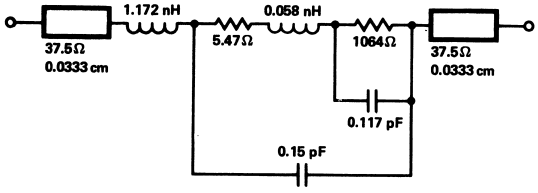
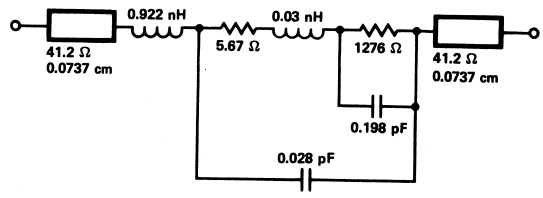


Figure 5. Typical Admittance Characteristics with 20 μA External Bias. HSCH-6312, -6332.

MODEL FOR J-2 PACKAGE SCHOTTKY DIODES AT 20 μA EXTERNAL BIAS HSCH-6310, -6330

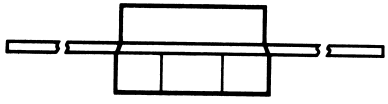
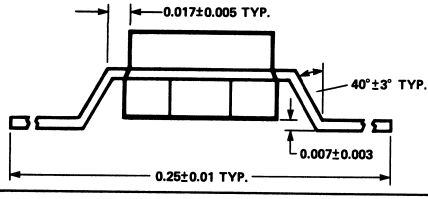


MODEL FOR J-2 PACKAGE SCHOTTKY DIODES AT 20 μA EXTERNAL BIAS HSCH-6312, -6332



Special Order Information

In the event that mounting these diodes in the circuit requires leads formed as shown below, this lead configuration can be ordered directly. Please refer to the following table for order information.

	**Straight Lead Order Information** Specify: Part Number (HSCH-6XXX) No Option Required
	**Formed Lead Order Information** Specify: Part Number (HSCH-6XXX) Option Number F01 All electrical tests are made prior to lead forming

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Surface Mount RF Schottky Barrier Diodes

Technical Data

HSMS-28XX Series

Features

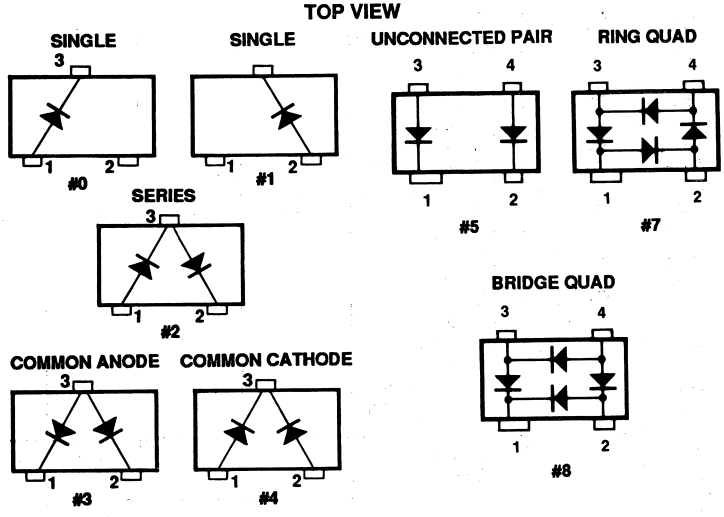
- **Surface Mount SOT-23/ SOT-143 Package**
- **Low Turn-On Voltage** (As Low as 0.34 V at 1 mA)
- **Low FIT (Failure in Time) Rate***
- **Six-sigma Quality Level**
- **Single, Dual and Quad Versions**
- **High and Low Profile Versions**
- **Tape and Reel Options Available**

*For more information see the Surface Mount Schottky Reliability Data Sheet.

Description/ Applications

These Schottky diodes are specifically designed for analog and digital applications requiring devices in the SOT-23 and SOT-143 surface mount packages. This series offers a wide range of specifications and package configurations to give the designer wide flexibility. Typical applications of these Schottky diodes are mixing, detecting, switching, sampling, clamping, and wave shaping.

Package Lead Code Identification



Absolute Maximum Ratings* T_A = 25°C

Symbol	Parameter	Value
I_f	Forward Current (1 µs Pulse)	1 Amp
P_t	Total Device Dissipation	250 mW[1]
PIV	Peak Inverse Voltage	Same as V_{BR}
T_j	Junction Temperature	150°C
T_{stg}	Storage Temperature	-65 to 150°C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

Note:

1. CW Power Dissipation at T_{LEAD} = 25°C. Derate to zero at maximum rated temperature.

Ordering Information

See page 14-14.

Electrical Specifications T_A = 25°C, Single Diode[4]

Part Number HSMS[5]	Package Marking Code[3]	Lead Code	Configuration	Nearest Equivalent Axial Lead Part No. 5082-	Minimum Breakdown Voltage V_{BR} (V)	Maximum Forward Voltage V_F (mV)	Maximum Forward Voltage V_F (V) @ I_F (mA)	Maximum Reverse Leakage I_R (nA) @ V_R (V)	Maximum Capacitance C_T (pF)	Typical Dynamic Resistance R_D (Ω)
2800	A0	0	Single	2800 (1N5711)	70	410	1.0 15	200 50	2.0	35
2801	A1	1	Single							
2802	A2	2	Series							
2803	A3	3	Common Anode							
2804	A4	4	Common Cathode							
2805	A5	5	Unconnected Pair							
2807	A7	7	Ring Quad[6]							
2808	A8	8	Bridge Quad[6]							
2810	B0	0	Single	2810 (1N5712)	20	410	1.0 35	200 15	1.2	15
2811	B1	1	Single							
2812	B2	2	Series							
2813	B3	3	Common Anode							
2814	B4	4	Common Cathode							
2815	B5	5	Unconnected Pair							
2817	B7	7	Ring Quad[6]							
2818	B8	8	Bridge Quad[6]							
2820	C0	0	Single	2835	8*	340	0.5 1.0	100 1	1.0	10
2821	C1	1	Single							
2822	C2	2	Series							
2823	C3	3	Common Anode							
2824	C4	4	Common Cathode							
2825	C5	5	Unconnected Pair							
2827	C7	7	Ring Quad[6]							
2828	C8	8	Bridge Quad[6]							
2840	J0	0	Single		50	410	1.2 10	200 40	2.2	
2841	J1	1	Single							
Test Conditions					I_R = 10 μA *I_R = 100 μA	I_F = 1 mA[1]			V_F = 0 V f = 1.0 MHz[2]	I_F = 5 mA

Notes:

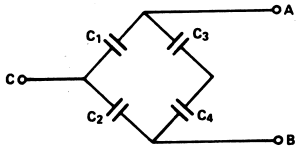
1. ΔV_F for diodes in pairs and quads in 15 mV maximum at 1 mA.
2. ΔC_{TO} for diodes in pairs and quads is 0.2 pF maximum.
3. Package marking code is in white. Package marking codes for low profile are designated by a suffix "L".
4. Effective Carrier Lifetime (τ) for all these diodes is 100 ps maximum measured with Krakauer method at 5 mA, except HSMS-282X which is measured at 20 mA.
5. Batch Matching available upon request.
   ΔV_F = 10 mV at 10 mA;
   ΔC_T = 0.1 pF at 0 V.
   Minimum batch size = 100.
6. See section titled "Quad Capacitance."

Quad Capacitance

Capacitance of Schottky diode quads is measured using an HP4271 LCR meter. This instrument effectively isolates individual diode branches form the others, allowing accurate capacitance measurement of each branch or each diode. The conditions are: 20 mV R.M.S. voltage at 1 MHz. HP defines this measurement as "CM", and it is equivalent to the capacitance of the diode by itself. The equivalent diagonal and adjacent capacitances can then be calculated by the formulas given below.

In a quad, the diagonal capacitance is the capacitance between points A and B as shown in figure below. The diagonal capacitance is calculated using the following formula

$$C_{DIAGONAL} = \frac{C_1 \times C_2}{C_1 + C_2} + \frac{C_3 \times C_4}{C_3 + C_4}$$



The equivalent adjacent capacitance is the capacitance between points A and C in figure below. This capacitance is calculated using the following formula

$$C_{ADJACENT} = C_1 + \frac{1}{\frac{1}{C_2} + \frac{1}{C_3} + \frac{1}{C_4}}$$

Typical Parameters at T_A = 25°C (unless otherwise noted), Single Diode

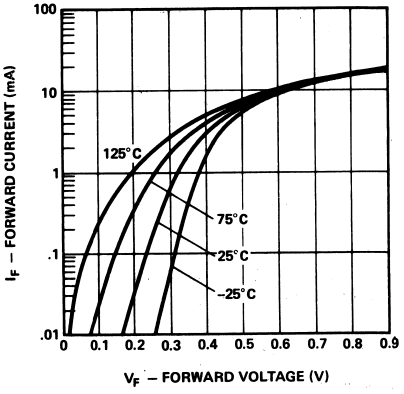


Figure 1. Forward Current vs. Forward Voltage at Temperatures – HSMS-2800 Series.

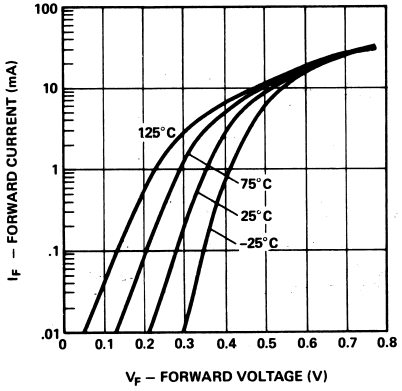


Figure 2. Forward Current vs. Forward Voltage at Temperatures – HSMS-2810 Series.

Typical Parameters (cont'd.)

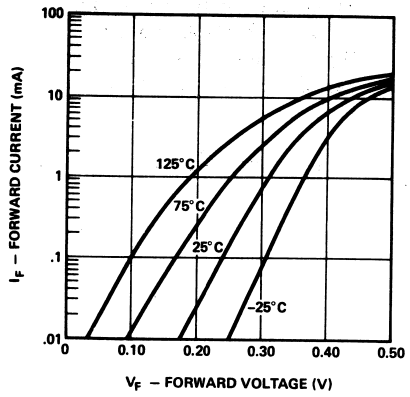


Figure 3. Forward Current vs. Forward Voltage at Temperatures – HSMS-2820 Series.

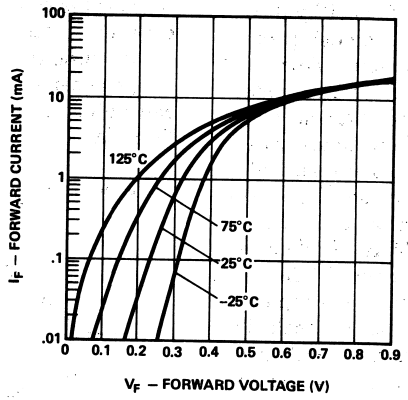


Figure 4. Forward Current vs. Forward Voltage at Temperatures – HSMS-2840 Series.

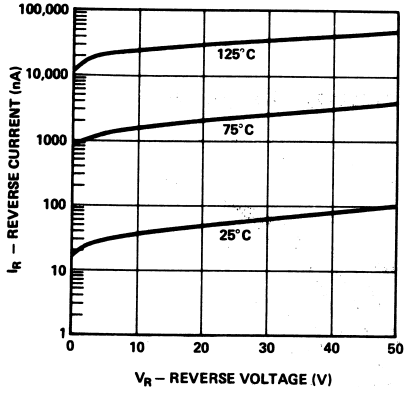


Figure 5. Reverse Current vs. Reverse Voltage at Temperatures – HSMS-2800 Series.

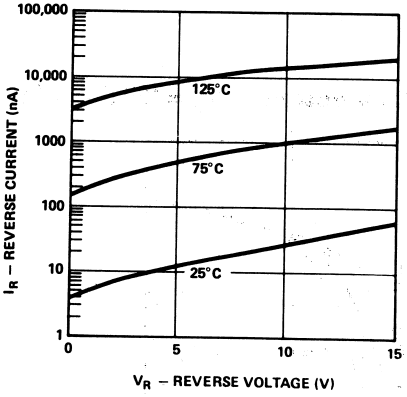


Figure 6. Reverse Current vs. Reverse Voltage at Temperatures – HSMS-2810 Series.

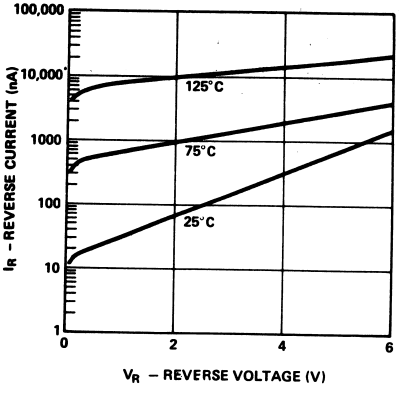


Figure 7. Reverse Current vs. Reverse Voltage at Temperatures – HSMS-2820 Series.

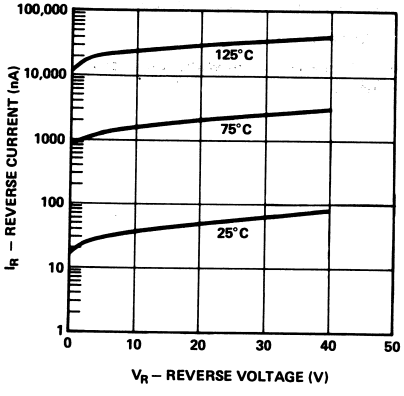


Figure 8. Reverse Current vs. Reverse Voltage at Temperatures – HSMS-2840 Series.

Typical Parameters (cont'd.)

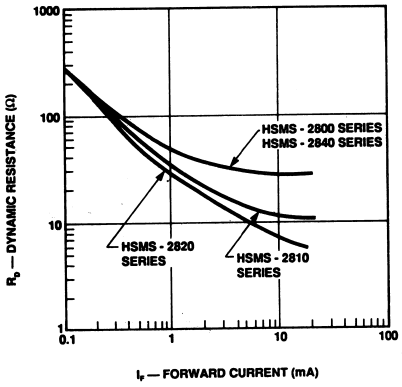


Figure 9. Dynamic Resistance vs. Forward Current – HSMS-2800 Series.

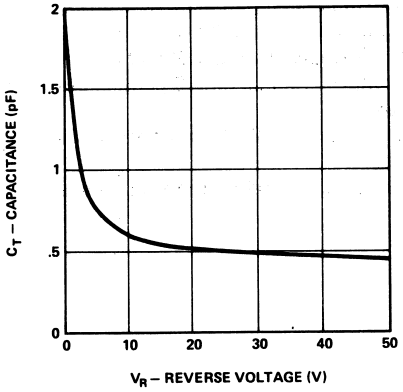


Figure 10. Total Capacitance vs. Reverse Voltage – HSMS-2800 Series.

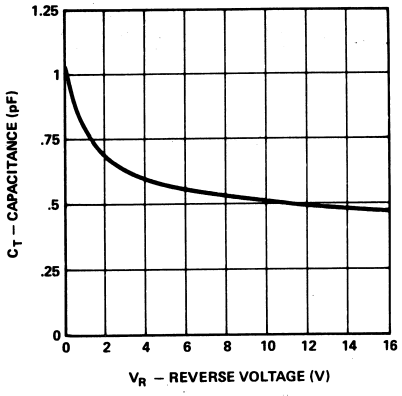


Figure 11. Total Capacitance vs. Reverse Voltage – HSMS-2810 Series.

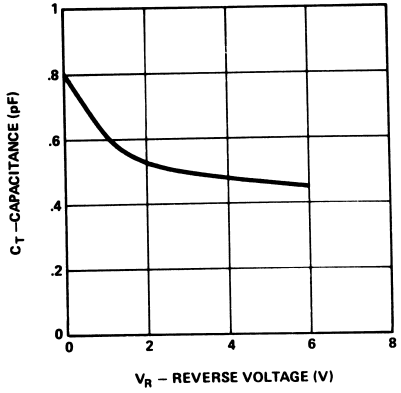


Figure 12. Total Capacitance vs. Reverse Voltage – HSMS-2820 Series.

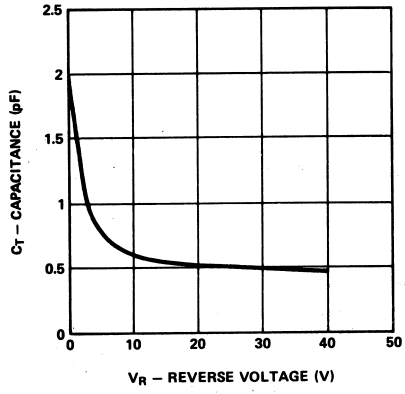
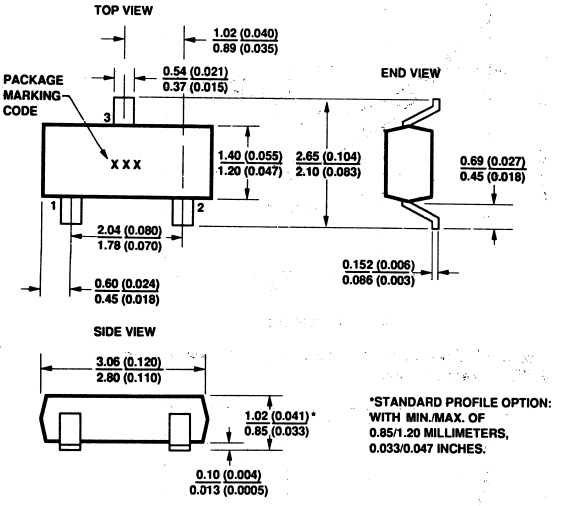


Figure 13. Total Capacitance vs. Reverse Voltage – HSMS-2840 Series.

Package Characteristics

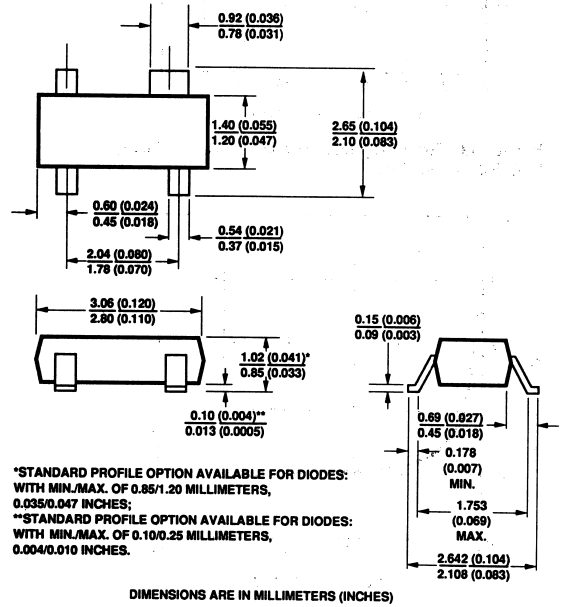
Lead Material ..... Alloy 42
Lead Finish ..... Tin-Lead, 60-40%
Max. Soldering Temperature ... 260°C for 5 sec
Min. Lead Strength ..... 2 pounds pull
Typical Package Inductance ..... 2 nH (opposite leads)
Typical Package Capacitance ..... 0.08 pF (opposite leads)

Package Dimensions



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Outline 23 (SOT-23)



*STANDARD PROFILE OPTION AVAILABLE FOR DIODES: WITH MIN./MAX. OF 0.85/1.20 MILLIMETERS, 0.035/0.047 INCHES;
**STANDARD PROFILE OPTION AVAILABLE FOR DIODES: WITH MIN./MAX. OF 0.10/0.25 MILLIMETERS, 0.004/0.010 INCHES.

DIMENSIONS ARE IN MILLIMETERS (INCHES)

Outline 143 (SOT-143)

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Surface Mount Microwave SOT-23 Schottky Diodes

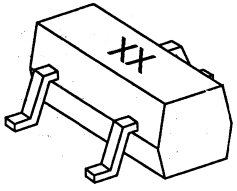
Technical Data

HSMS-8101 Single
HSMS-8202 Pair

Features

- **Optimized for use at 10-14 GHz**
- **Low Capacitance**
- **Low Conversion Loss**
- **Low R_D**
- **Low Cost Surface Mount Plastic Package**

Plastic SOT-23 Package



Description/ Applications

These low cost microwave Schottky diodes are specifically designed for use at X/Ku-bands and are ideal for DBS and VSAT downconverter applications. They are available as a single or a series pair in SOT-23 standard package configurations.

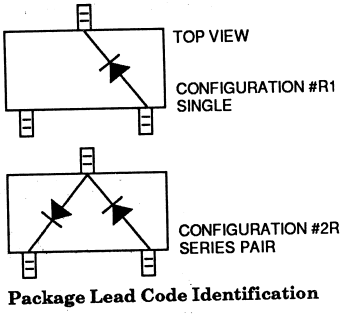
Absolute Maximum Ratings*

(T_A = 25°C)

Symbol	Parameters	Min.	Max.	Units
P_T	Total Device Dissipation(1)		75	mW
P_{IV}	Peak Inverse Voltage		4	V
T_j	Junction Temperature		+150	°C
T_{stg} & T_{op}	Storage & Operating Temperature	-65	+150	°C

* Operation in excess of any one of these parameters may result in permanent damage.

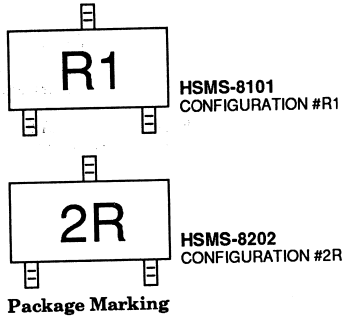
Note 1. Measured in an infinite heat sink at T_{case} = 25°C. Derate linearly to zero at 150°C per diode.



Package Lead Code Identification

Package Characteristics

Lead Material ..... Alloy 42
Lead Finish ..... Tin-Lead
Max. Soldering Temp. ..... 260°C for 5 sec.
Min. Lead Strength ..... 2 pounds pull
Typical Package Inductance ..... 2 nH
Typical Package Capacitance ..... 0.08 pF (opposite leads)



Package Marking

Ordering Information

See page 14-14.

DC Electrical Specifications (T_A = 25°C)

Symbol	Parameters	Test Conditions	Units	HSMS-8101		HSMS-8202	
				Min.	Max.	Min.	Max.
V_{BR}	Breakdown Voltage	I_R = 10 μA	V	4		4	
C_T	Total Capacitance	V_R = 0 V, f = 1 MHz	pF		0.35		0.26
ΔC_T	Capacitance Difference	V_R = 0 V, f = 1 MHz	pF				0.04
R_D	Dynamic Resistance	I_F = 5 mA	Ω		12		14
ΔR_D	Dynamic Resistance Difference	I_F = 5 mA	Ω				2
V_F	Forward Voltage	I_F = 1 mA	mV	250	350	250	350
ΔV_F	Forward Voltage Difference	I_F = 1 mA	mV				20

RF Electrical Parameters, (T_A = 25°C)

Symbol	Parameters	Units	HSMS-8101	HSMS-8202
			Typ.	Typ.
L_c	Conversion Loss at 12 GHz	dB	6.3	6.1
Z_{IF}	IF Impedance	Ω	150	150
SWR	SWR at 12 GHz		1.2	1.2

Note:

DC Load resistance = 0 Ω; LO power = 1 mW.

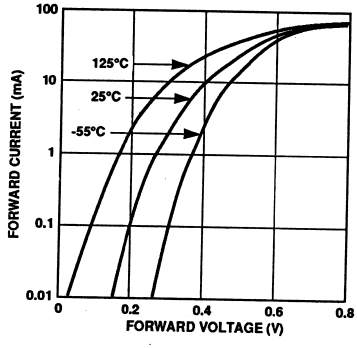


Figure 1. Typical Forward Current vs. Forward Voltage at Three Temperatures

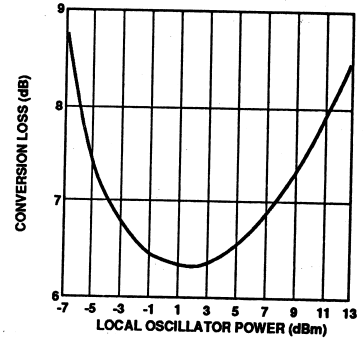
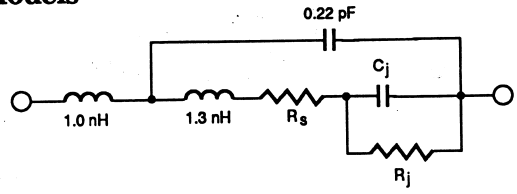


Figure 2. Typical Conversion Loss vs. Local Oscillator Power

Equivalent Circuit Models

HSMS-8101



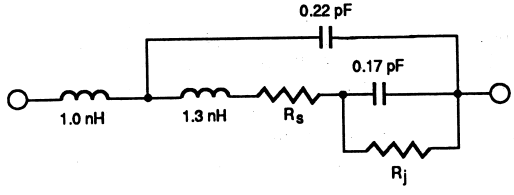
Self Bias

	1 mA	2.5 mA
R_s	15	12.3
R_j	286	139
C_j	0.23	0.26

Spice Parameters:

IS = 9 E-8	EG = 0.69	TT = 0
RS = 4	CJO = 0.23 E-12	
N = 1.08	VJ = 0.5	
BV = 5.5	M = 0.5	
IBV = 1 E-5	FC = 0.5	

HSMS-8202



Self Bias

	1 mA	2.5 mA
R_s	6.8	1.4
R_j	263	142

Spice Parameters:

IS = 4.6 E-8	EG = 0.69	TT = 0
RS = 6	CJO = 0.18 E-12	
N = 1.09	VJ = 0.5	
BV = 7.3	M = 0.5	
IBV = 1 E-5	FC = 0.5	

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Schottky Barrier Diodes for General Purpose Applications

Technical Data

1N5711,
JAN1N5711/TX/TXV
1N5712,
JAN1N5712/TX/TXV
5082-2300 Series
5082-2800 Series
5082-2900 Series

Features

- **Low Turn-On Voltage**
  As Low as 0.34 V at 1 mA
- **Pico Second Switching Speed**
- **High Breakdown Voltage**
  Up to 70 V
- **Matched Characteristics Available**

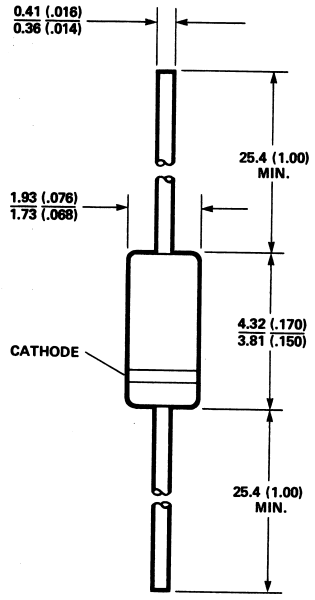
Description/ Applications

The 1N5711, 1N5712, 5082-2800/10/11 are passivated Schottky barrier diodes which use a patented "guard ring" design to achieve a high breakdown voltage. Packaged in a low cost glass package, they are well suited for high level detecting, mixing, switching, gating, log or A-D converting, video detecting, frequency discriminating, sampling, and wave shaping.

The 5082-2835 is a passivated Schottky diode in a low cost glass package. It is optimized for low turn-on voltage. The 5082-2835 is particularly well suited for the UHF mixing needs of the CATV marketplace.

The 5082-2300 and 2900 Series devices are unpassivated Schottky diodes in a glass package. These diodes have extremely low 1/f noise and are ideal for low noise mixing, and high sensitivity detecting. They are particularly well suited for use in Doppler or narrow band video receivers.

Note: The JAN Series 1N5711 and the JAN Series 1N5712 devices are well suited for applications that require the high reliability of a JAN/TX/TXV device. The TX and TXV devices have solder dipped leads. Both the JAN Series 1N5711 and 1N5712 undergo testing per MIL-STD-750. More information about these devices can be obtained through your local Hewlett-Packard field sales engineer.



DIMENSIONS IN MILLIMETERS AND (INCHES).

Outline 15

Maximum Ratings

Junction Operating and Storage Temperature Range
- 5082-2301, -2302, -2303, -2900 ..... -60°C to +100°C
- 1N5711, 1N5712, 5082-2800/10/11 ..... -65°C to +200°C
- 5082-2835 ..... -60°C to +150°C

DC Power Dissipation
(Measured in an infinite heat sink at T_{CASE} = 25°C)
Derate linearly to zero at maximum rated temperature
- 5082-2301, -2302, -2303, -2900 ..... 100 mW
- 1N5711, 1N5712, 5082-2800/10/11 ..... 250 mW
- 5082-2835 ..... 150 mW

Peak Inverse Voltage ..... V_{BR}

Package Characteristics

	Outline 15
Lead Material	Dumet
Lead Finish	95-5% Tin-Lead
Max. Soldering Temperature	260°C for 5 sec
Min. Lead Strength	4 pounds pull
Typical Package Inductance	
1N5711, 1N5712:	2.0 nH
2800 Series:	2.0 nH
2300, 2900 Series:	3.0 nH
Typical Package Capacitance	
1N5711, 1N5712:	0.2 pF
2800 Series:	0.2 pF
2300, 2900 Series:	0.07 pF

The leads on the Outline 15 package should be restricted so that the bend starts at least 1/16 inch from the glass body.

Outline 15 diodes are available on tape and reel. The tape and reel specification is patterned after RS-296-D.

Electrical Specifications at T_A = 25°C

General Purpose Diodes

Part Number	Package Outline	Min. Breakdown Voltage V_{BR} (V)	Max. Forward Voltage V_F (mV)	V_F = 1 V Max. at Forward Current I_F (mA)	Max. Reverse Leakage Current I_R (nA) at V_R (V)		Max. Capacitance C_T (pF)
5082-2800	15	70	410	15	200	50	2.0
1N5711	15	70	410	15	200	50	2.0
5082-2810	15	20	410	35	100	15	1.2
1N5712	15	20	550	35	150	16	1.2
5082-2811	15	15	410	20	100	8	1.2
5082-2835	15	8*	340	10**	100	1	1.0
Test Conditions		I_R = 10 μA *I_R = 100 μA	I_F = 1 mA	*V_F = 0.45 V			V_R = 0 V f = 1.0 MHz

Note: Effective Carrier Lifetime (τ) for all these diodes is 100 ps maximum measured with Krakauer method at 5 mA except for 5082-2835 which is measured at 20 mA.

Low 1/f (Flicker) Noise Diodes

Part Number 5082-	Package Outline	Min. Breakdown Voltage V_{BR} (V)	Max. Forward Voltage V_F (mV)	V_F = 1 V Max. at Forward Current I_F (mA)	Max. Reverse Leakage Current I_R (nA) at V_R (V)		Max. Capacitance C_T (pF)
2301	15	30	400	50	300	15	1.0
2302	15	30	400	35	300	15	1.0
2303	15	20	400	35	500	15	1.0
2900	15	10	400	20	100	5	1.2
Test Conditions		I_R = 10 μA	I_F = 1 mA				V_R = 0 V f = 1.0 MHz

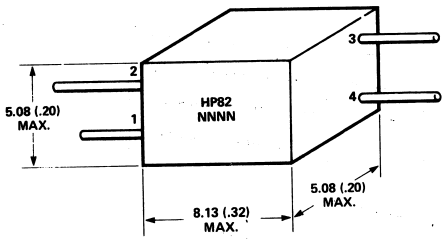
Note: Effective Carrier Lifetime (τ) for all these diodes is 100 ps maximum measured with Krakauer method at 20 mA.

Matched Pairs and Quads

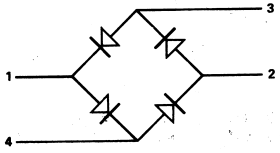
Basic Part Number 5082-	Matched Pair Un-connected	Matched Quad Un-connected	Matched Ring Quad Encapsulated G-1 Outline	Matched Bridge Quad Encapsulated G-2 Outline	Batch Matched[1]	Test Conditions
2301	5082-2306 ΔV_F = 20 mV ΔC_O = 0.2 pF					ΔV_F at I_F = 0.75, 20 mA ΔC_O at f = 1.0 MHz
2303	5082-2308 ΔV_F = 20 mV ΔC_O = 0.2 pF	5082-2370 ΔV_F = 20 mV ΔC_O = 0.2 pF	5082-2396 ΔV_F = 20 mV ΔC_O = 0.2 pF	5082-2356 ΔV_F = 20 mV ΔC_O = 0.2 pF		ΔV_F at I_F = 0.75, 20 mA ΔC_O at f = 1.0 MHz
2900	5082-2912 ΔV_F = 30 mV	5082-2970 ΔV_F = 30 mV		5082-2997 ΔV_F = 30 mV		ΔV_F at I_F = 1.0, 10 mA
2800	5082-2804 ΔV_F = 20 mV	5082-2805 ΔV_F = 20 mV			5082-2836* ΔV_F = 20 mV ΔC_O = 0.1 pF	ΔV_F at I_F = 0.5, 5 mA *I_F = 10 mA ΔC_O at f = 1.0 MHz
2811		5082-2815 ΔV_F = 20 mV ΔC_O = 0.2 pF	5082-2814 ΔV_F = 20 mV ΔC_O = 0.2 pF	5082-2813 ΔV_F = 20 mV ΔC_O = 0.2 pF	5082-2826 ΔV_F = 10 mV ΔC_O = 0.1 pF	ΔV_F at I_F = 10 mA ΔC_O at f = 1.0 MHz
2835					5082-2080 ΔV_F = 10 mV ΔC_O = 0.1 pF	ΔV_F at I_F = 10 mA ΔC_O at f = 1.0 MHz

Note:
1. Batch matched devices have a minimum batch size of 50 devices.

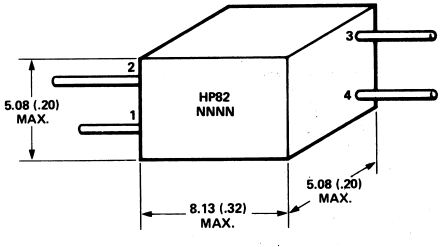
Outline G-1



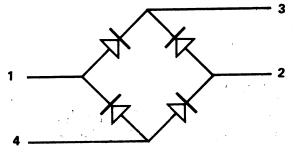
LEAD LENGTH 19.05 (0.75) MIN.



Outline G-2



LEAD LENGTH 19.05 (0.75) MIN.



LEAD FINISH – GOLD

ALL DIMENSIONS IN MILLIMETERS (INCHES).

Typical Parameters

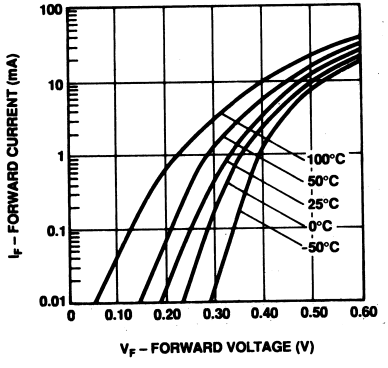


Figure 1. I-V Curve Showing Typical Temperature Variation for 5082-2300 and 5082-2900 Series Schottky Diodes.

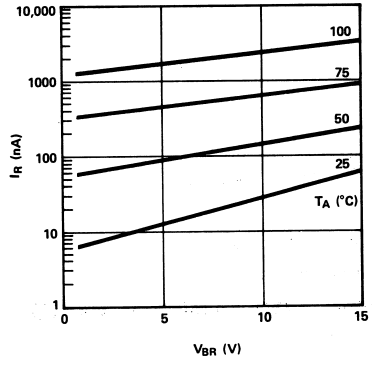


Figure 2. 5082-2300 Series Typical Reverse Current vs. Reverse Voltage at Various Temperatures.

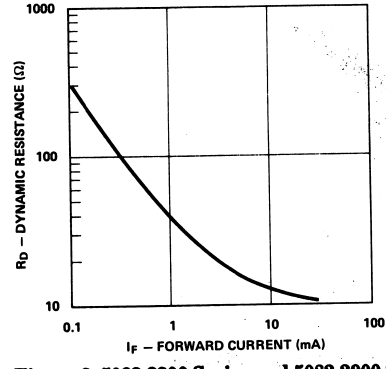


Figure 3. 5082-2300 Series and 5082-2900 Series Typical Dynamic Resistance (R_D) vs. Forward Current (I_F).

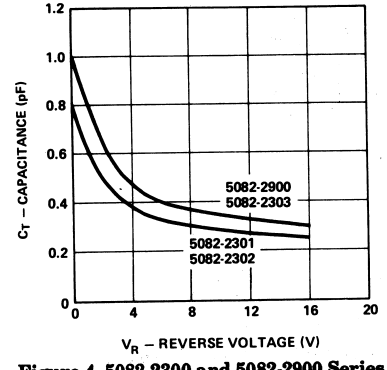


Figure 4. 5082-2300 and 5082-2900 Series Typical Capacitance vs. Reverse Voltage.

Typical Parameters (continued)

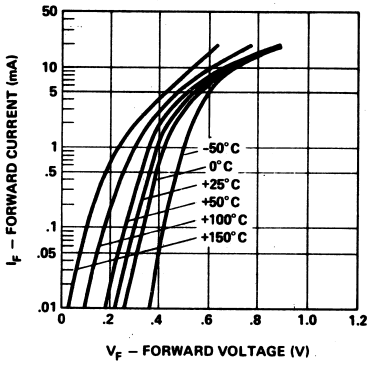


Figure 5. I-V Curve Showing Typical Temperature Variation for 5082-2800 or 1N5711 Schottky Diodes.

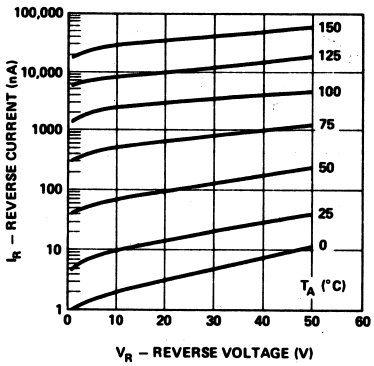


Figure 6. (5082-2800 or 1N5711) Typical Variation of Reverse Current (I_R) vs. Reverse Voltage (V_R) at Various Temperatures.

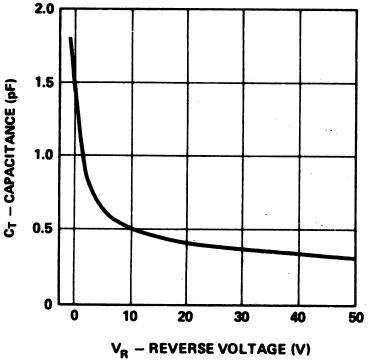


Figure 7. (5082-2800 or 1N5711) Typical Capacitance (C_T) vs. Reverse Voltage (V_R).

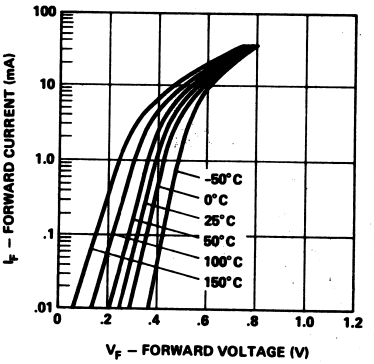


Figure 8. I-V Curve Showing Typical Temperature Variation for the 5082-2810 or 1N5712 Schottky Diode.

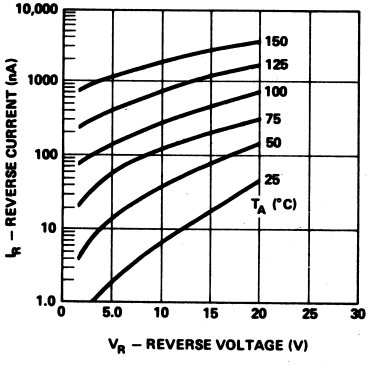


Figure 9. (5082-2810 or 1N5712) Typical Variation of Reverse Current (I_R) vs. Reverse Voltage (V_R) at Various Temperatures.

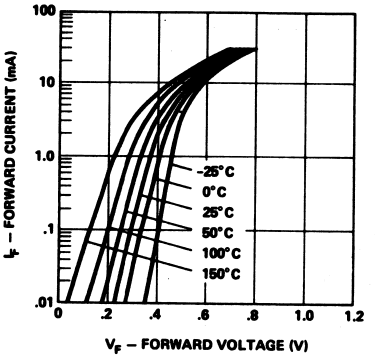


Figure 10. I-V Curve Showing Typical Temperature Variation for the 5082-2811 Schottky Diode.

Typical Parameters (continued)

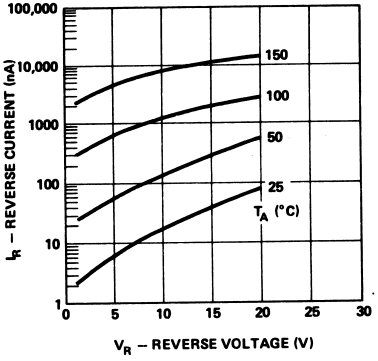


Figure 11. (5082-2811) Typical Variation of Reverse Current (I_R) vs. Reverse Voltage (V_R) at Various Temperatures.

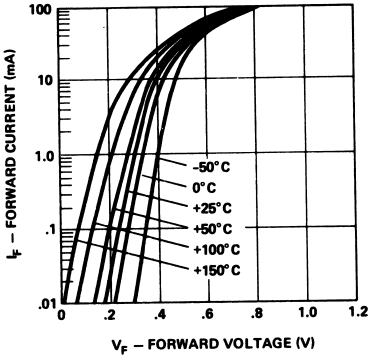


Figure 12. I-V Curve Showing Typical Temperature Variations for 5082-2835 Schottky Diode.

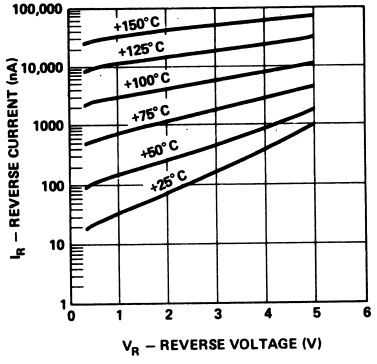


Figure 13. (5082-2835) Typical Variation of Reverse Current (I_R) vs. Reverse Voltage (V_R) at Various Temperatures.

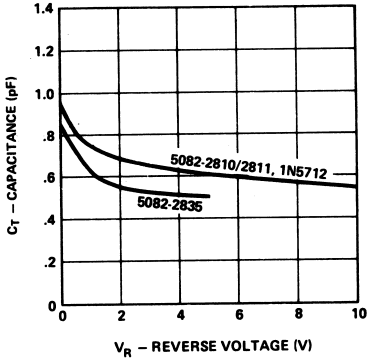


Figure 14. Typical Capacitance (C_T) vs. Reverse Voltage (V_R)

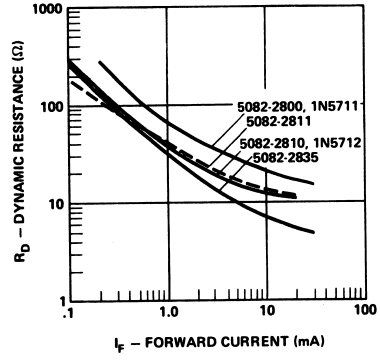


Figure 15. Typical Dynamic Resistance (R_D) vs. Forward Current (I_F).

HEWLETT PACKARD

High Conductance Diodes

Technical Data

5082-1001
5082-1002
5082-1006
(1N4456)

Features

- **Fast Switching**
- **Low Capacitance**
- **High Current Capability**

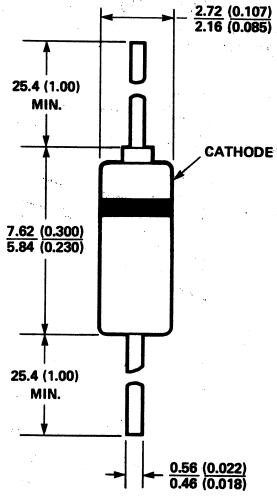
Description/ Applications

The 5082-1000 series of diodes feature planar silicon epitaxial construction to provide high conductance, low capacitance, and nanosecond turn-on and turn-off. Turn-on time and voltage overshoot are minimized in these diodes of low conductivity modulation.

These diodes are ideally suited for applications such as core drivers, pulse generators, input gates, or wherever high conductance without loss of speed is required.

Mechanical Specifications

The HP Outline 11 package has a glass hermetic seal with dumet leads. The package will meet MIL-STD-750, Method 2036, Conditions A (2 lbs. tension for 15 sec.), and E. The maximum soldering temperature is 230°C for 5 seconds. Outline 11 package capacitance and inductance are typically 0.15 pF and 4 nH respectively.



DIMENSIONS IN MILLIMETERS AND (INCHES)

Outline 11B

Maximum Ratings

WIV – Working Inverse Voltage
1001/1002 ..... 30 V
1006 ..... 40 V
I_F (Surge) – Forward Current Surge,
1.0 Sec. Duration ..... 0.75 Amp
I_F (Surge) – Forward Current Surge,
1.0 Microsec. Duration ..... 7.50 Amp
Power Dissipation[1] at T_{CASE} = 25°C ..... 500 mW
Junction Temperature Range ..... -65°C to +175°C
Storage Temperature Range ..... -65°C to +200°C

Electrical Specifications at $T_A = 25°C$

Part Number 5082-	Minimum Breakdown Voltage V_{BR} (V)	Minimum Forward Current I_F (mA)	Minimum Forward Current I_F (mA)	Maximum Reverse Leakage Current I_R (nA)	Maximum Reverse Leakage Current I_R (μA)	Maximum Total Capacitance C_T (pF)	Maximum Reverse Recovery Time t_{rr} (ns)	Maximum Turn-On Time t_{on} (ns)
1001	35	150	500	200	200	1.5	1.5	2.5
1002	35	300	800	200	200	3.0	2.0	2.5
1006	50	150	500	200	200	1.1	1.5	–
Test Conditions	I_R = 10 μA	V_F = 1.0 V [2]	V_F = 1.4 V [2]	[3]	150°C[3]	V_R = 0 V, f = 1.0 MHz	(Figure 9)	(Figure 10)

Notes:
1. Mounted on a printed circuit board in still air.
2. Measured at a repetition rate not to exceed the power dissipation.
3. V_R = 35 V for 1006; V_R = 30 V for 1001, 1002.
4. Inductance measured at the edge of the glass package seal is typically 4.0 nH for all devices.
5. Rectification Efficiency is typically 65% for all devices (Figure 8).
6. 1N4456 has same specs as 5082-1001.

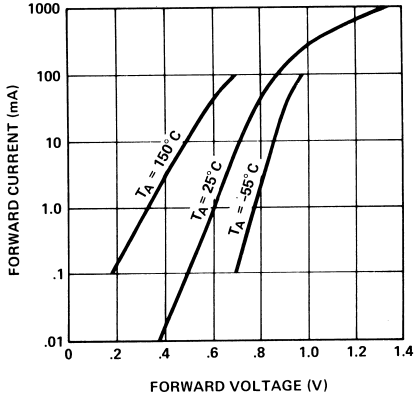


Figure 1. Typical Forward Conduction Characteristics. 5082-1001 and 1006.

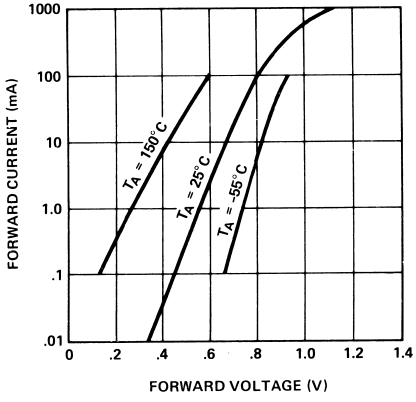


Figure 2. Typical Forward Conduction Characteristics. 5082-1002.

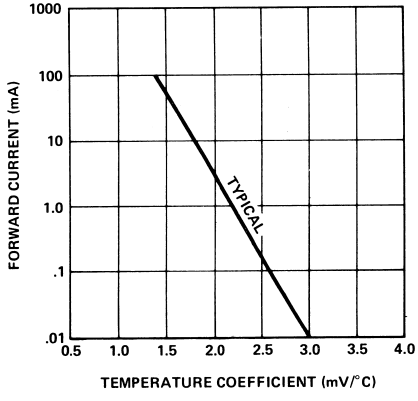


Figure 3. Typical Forward Current Temperature Coefficient.

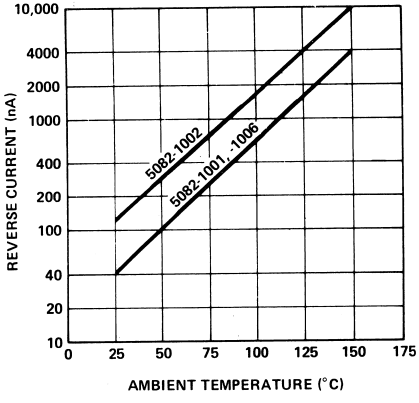


Figure 4. Typical Reverse Current at Specified V_R vs. Increasing Temperature.

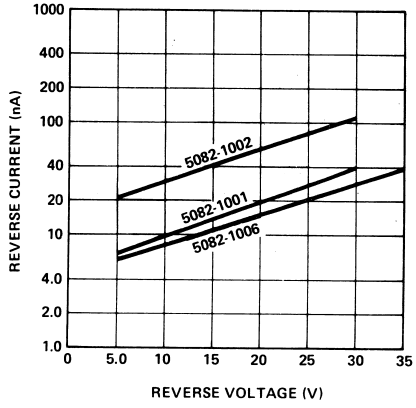


Figure 5. Typical Reverse Current vs. Reverse Voltage.

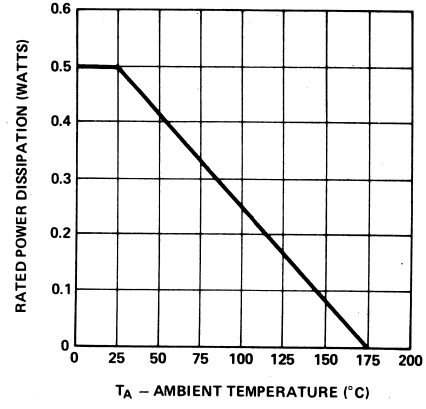


Figure 6. Power Dissipation Derating Characteristics.

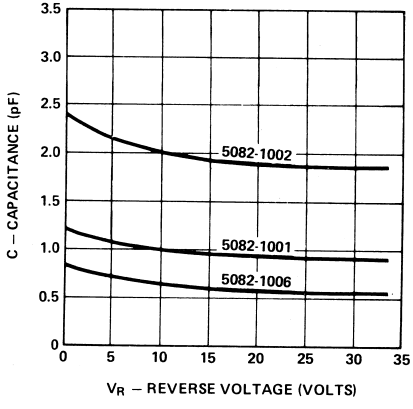


Figure 7. Typical Capacitance vs. Reverse Voltage Characteristics.

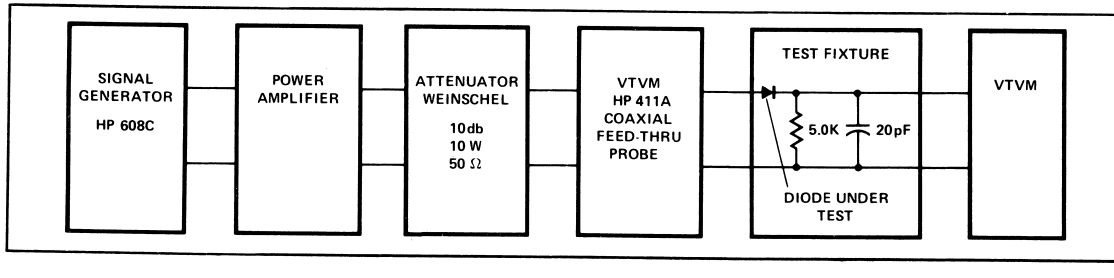


Figure 8. Test Circuit for Measuring the Rectification Efficiency. Signal source is adjusted to 100 MHz and 2 V RMS as read on the 411A. The rectification efficiency calculated from the DC output voltage by RE = V_{DC}/2.83 is typically 65% for all devices.

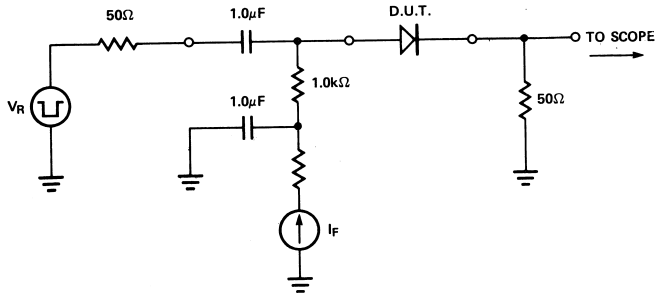


Figure 9. Test Circuit for Measuring Reverse Recovery Time. I_F is set at 20 mA and V_R at 2 V.

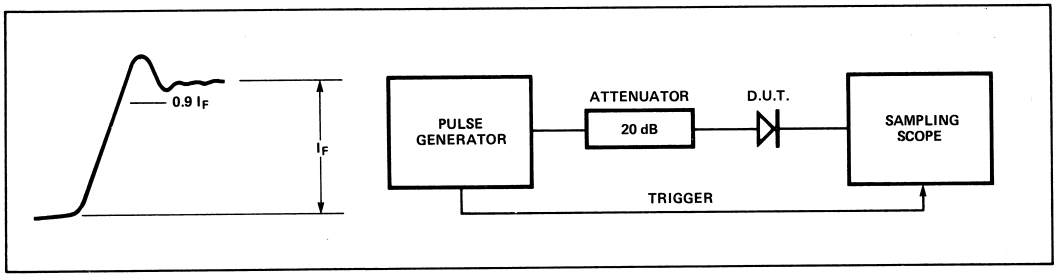


Figure 10. Test Circuit for Measuring Turn-On Time. I_F is adjusted for 10 mA after applying the step voltage. t_{ON} is measured as the time required to reach 0.9 I_F from initial application of the step voltage. For high excitation levels the t_{ON} value is significantly lower than the value specified, i.e., at 100 mA t_{ON} is typically less than 1.0 ns.

HEWLETT PACKARD

Schottky Barrier Diodes for Stripline, Microstrip Mixers and Detectors

Technical Data

5082-2200/01/02/03
5082-2207/08/09/10
5082-2765/66
5082-2774/75
5082-2785/86
5082-2794/95

Features

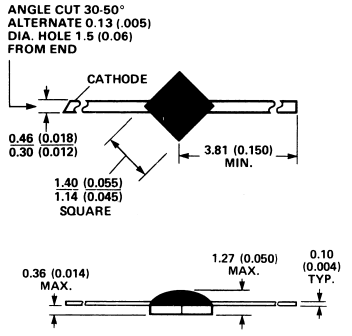
- **Small Size**
- **Low Noise Figure**
  6 dB Typical at 9 GHz
- **Rugged Design**
- **High Uniformity**
- **High Burnout Rating**
  1 W RF Pulse Power Incident
- **Both Medium and Low Barrier Available**

Description/ Applications

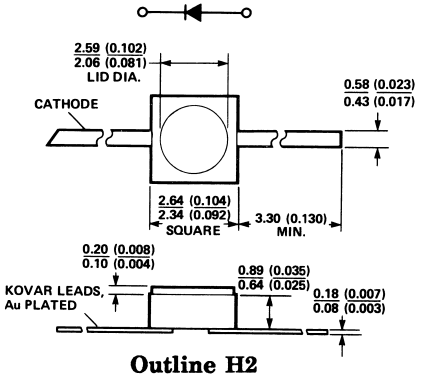
This family consists of medium barrier and low barrier beam lead diodes mounted in easily handled carrier packages. Low barrier diodes provide optimum noise figure at low local oscillator drive levels. Medium barrier diodes provide a wider dynamic range for lower distortion mixer designs. Application Note 976 presents impedance matching techniques for an X-Band mixer.

Package Characteristics

These diodes are designed for microstrip and stripline use. The kovar leads provide good continuity of transmission line impedance to the diode. Outline C2 is a plastic on ceramic package. Outline H2 has a metal ceramic hermetic seal.



Outline C2
C_P = 0.055 pF



Outline H2
C_P = 0.175 pF

DIMENSIONS IN MILLIMETERS AND (INCHES).

The ceramic is alumina. Metal parts are gold plated kovar.

The hermetic package, outline H2, is capable of passing many of the environmental tests of MIL-STD-750. The applicable solderability test is reference 2031.1: 260°C, 10 seconds.

Maximum Ratings

Operating and Storage Temperature Range
C2 Packaged Diodes ..... -65°C to +150 °C
H2 Packaged Diodes ..... -65°C to +175 °C
Pulse Power Incident at T_{CASE} = 25°C ..... 1 W
(1 μs pulse, Du = 0.001)
CW Power Dissipation at T_{CASE} = 25°C
(Measured in an infinite heat sink) ..... 125 mW
Derate linearly to zero at maximum operating temperature.
Diode Mounting Temperature in Packages
C2 ..... 235°C for 10 sec max.
H2 ..... 260°C for 10 sec max.
Peak Inverse Voltage ..... 4 V

These diodes are ESD sensitive. Handle with care to avoid static discharge through the diode.

RF Electrical Specifications at T_A = 25°C

Part Number 5082-	Batch Matched* 5082-	Test Freq. (GHz)	Barrier	Maximum Noise Figure NF (dB)	IF Impedance Z_{IF} (Ω) Min.	IF Impedance Z_{IF} (Ω) Max.	Maximum SWR	Package	Typical Junction Capacitance C_j (pF)
2200 2202	2201 2203	9.375	Medium Medium	6.0 6.5	200	400	1.5:1 2.0:1	Hermetic H2	0.18
2765 2785	2766 2786		Low Low	6.0 6.5	150	350	1.5:1 2.0:1		
2207 2209	2208 2210		Medium Medium	6.0 6.5	200	400	1.5:1 2.0:1	Broadband C2	
2774 2794	2775 2795		Low Low	6.0 6.5	150	350	1.5:1 2.0:1		
Test Conditions	ΔNF ≤ 0.3 dB ΔZ_{IF} ≤ 25 Ω			DC Load Resistance = 0 Ω L.O. Power = 1 mW IF = 30 MHz, 1.5 dB NF					V = 0

*Minimum batch size 20 units.

Typical Detector Characteristics at T_A = 25°C

Medium Barrier and Low Barrier (DC Bias)

Parameter	Symbol	Typical Value	Units	Test Conditions
Tangential Sensitivity	T_{SS}	-54	dBm	20 μA Bias, R_L = 100 kΩ P_{in} = - 40 dBm Video Bandwidth = 2 MHz f = 10 GHz
Voltage Sensitivity	γ	6.6	mV/μW	
Video Resistance	R_V	1400	Ω	

Low Barrier (Zero Bias)

Parameter	Symbol	Typical Value	Units	Test Conditions
Tangential Sensitivity	T_{SS}	-44	dBm	Zero Bias, R_L = 10 MΩ P_{in} = - 30 dBm Video Bandwidth = 2 MHz f = 10 GHz
Voltage Sensitivity	γ	10	mV/μW	
Video Resistance	R_V	1.8	MΩ	

Typical Parameters

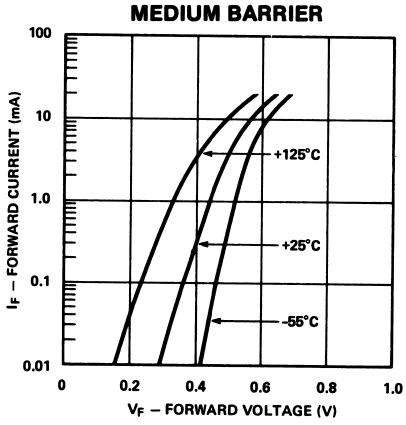


Figure 1. Typical Forward Characteristics.

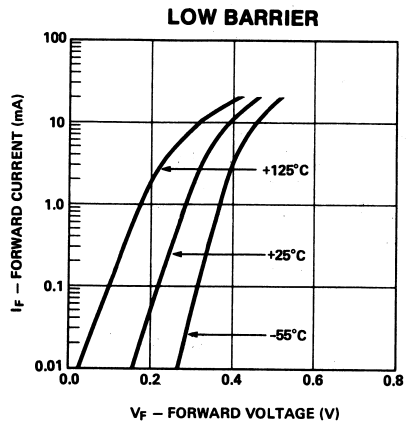


Figure 2. Typical Forward Characteristics.

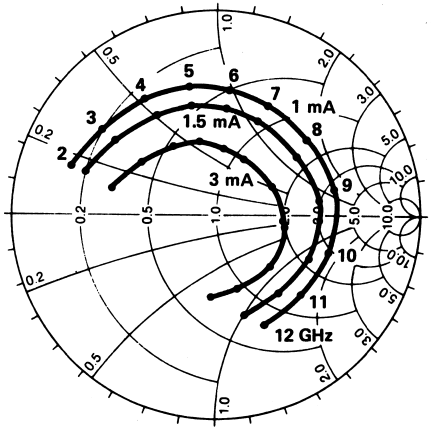


Figure 3. Typical Admittance Characteristics, 5082-2200 and 5082-2765 with Self Bias.

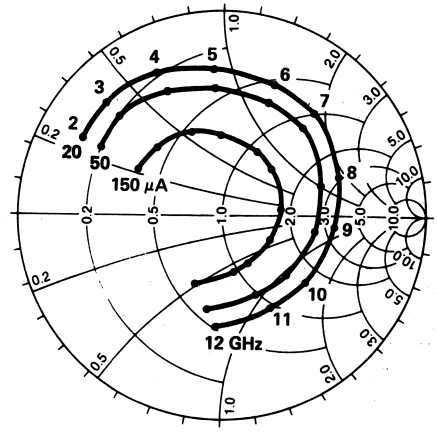


Figure 4. Typical Admittance Characteristics, 5082-2200 and 5082-2765 with External Bias.

Typical Parameters (cont.)

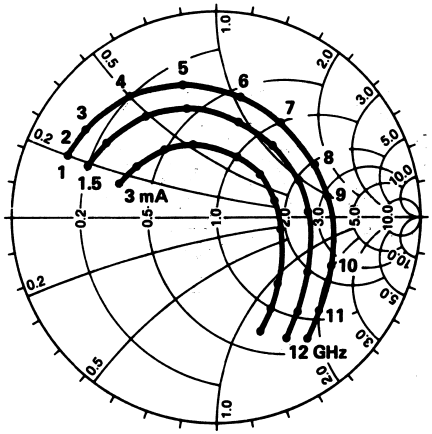


Figure 5. Typical Admittance Characteristics, 5082-2202 and 5082-2785 with Self Bias.

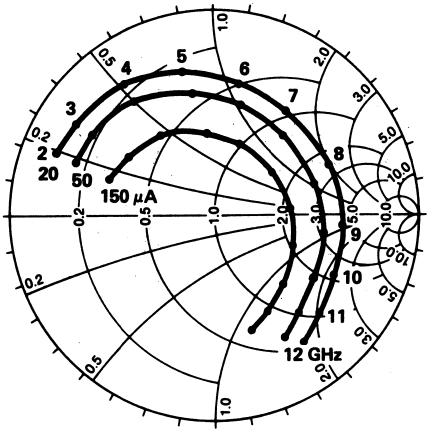


Figure 6. Typical Admittance Characteristics, 5082-2202 and 5082-2785 with External Bias.

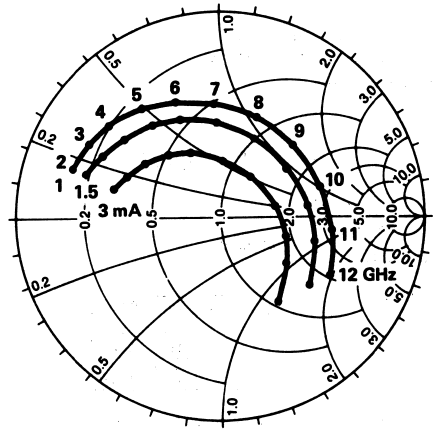


Figure 7. Typical Admittance Characteristics, 5082-2207 and 5082-2774 with Self Bias.

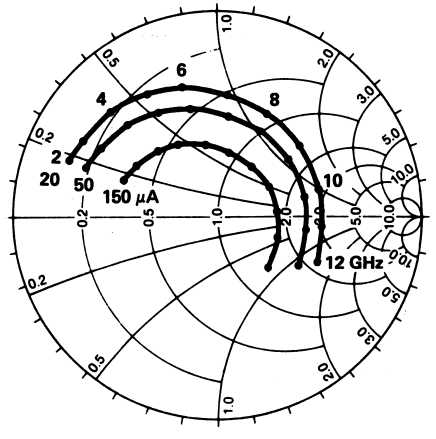


Figure 8. Typical Admittance Characteristics, 5082-2207 and 5082-2774 with External Bias.

Typical Parameters (cont.)

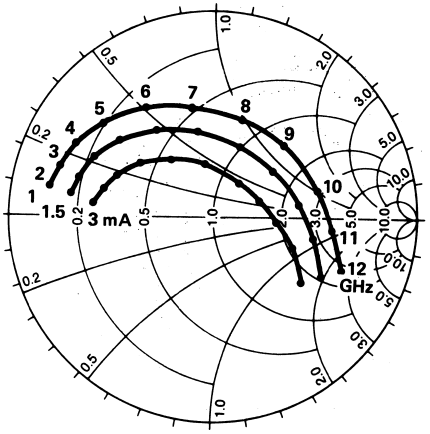


Figure 9. Typical Admittance Characteristics, 5082-2209 and 5082-2794 with Self Bias.

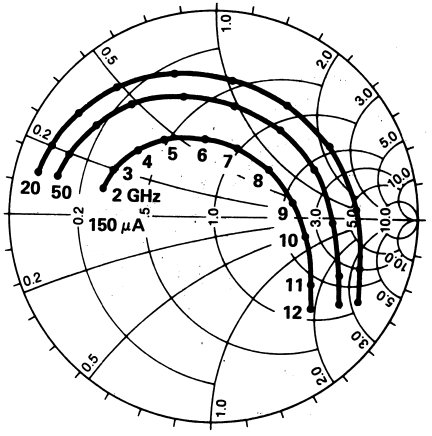


Figure 10. Typical Admittance Characteristics, 5082-2209 and 5082-2794 with External Bias.

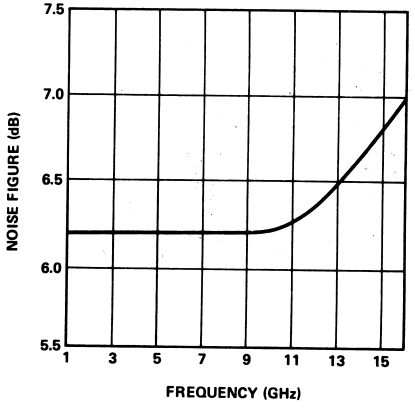
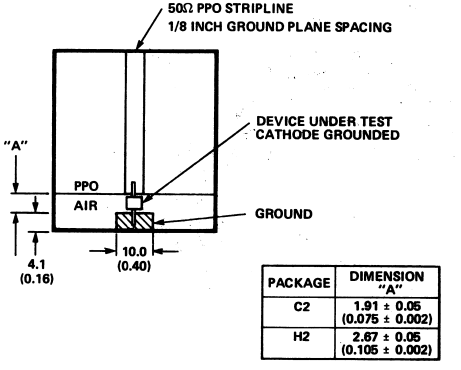


Figure 11. Typical Noise Figure vs. Frequency for 5082-2209, -2794.

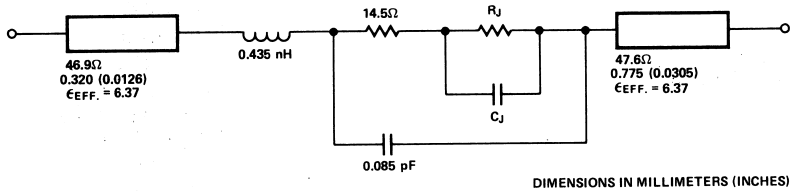


PACKAGE	DIMENSION "A"
C2	1.91 ± 0.05 (0.075 ± 0.002)
H2	2.67 ± 0.05 (0.105 ± 0.002)

DIMENSIONS IN MILLIMETERS (INCHES)

Figure 12. Admittance Test Circuit.

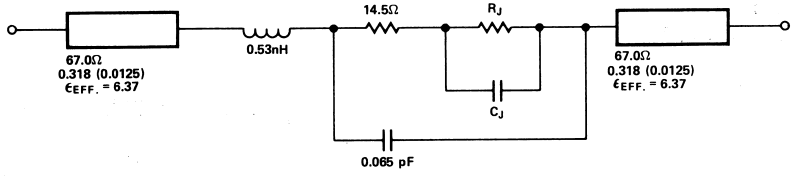
MODEL FOR H2 DIODES



DIMENSIONS IN MILLIMETERS (INCHES)

Parameter	Symbol	1 mA Rect. Current 5082-2200, 5082-2765	20 μA Ext. Bias 5082-2200, 5082-2765	Units
Junction Resistance	R_J	258	545	Ω
Junction Capacitance	C_J	0.255	0.302	pF

MODEL FOR C2 DIODES



DIMENSIONS IN MILLIMETERS (INCHES)

Parameter	Symbol	1 mA Rect. Current 5082-2207, 5082-2774	20 μA Ext. Bias 5082-2207, 5082-2774	Units
Junction Resistance	R_J	338	421	Ω
Junction Capacitance	C_J	0.189	0.195	pF

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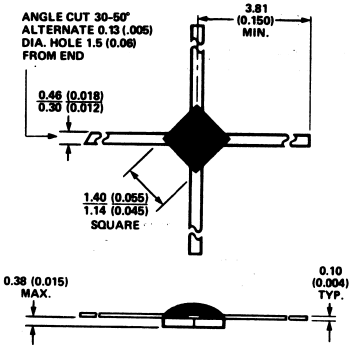
Schottky Barrier Diode Quads for Double Balanced Mixers

Technical Data

5082-2231
5082-2233
5082-2263
5082-2271/72
5082-2277
5082-2279/80
5082-2291/92
5082-2294
5082-2830/31

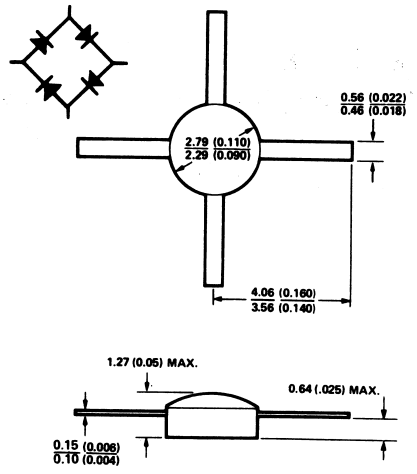
Features

- **Small Size**
  Eases Broad Band Designs
- **Tight Match**
  Improves Mixer Balance
- **Improved Balance over Temperature**
- **Rugged Design**
- **Both Medium and Low Barrier Diodes Available**



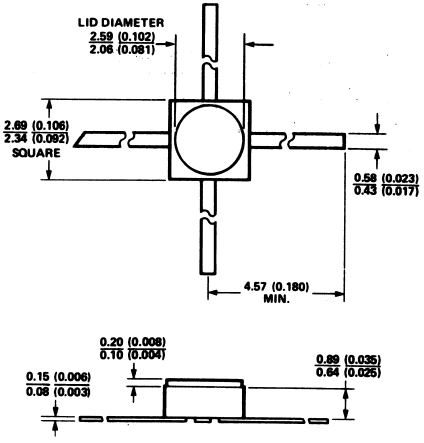
Outline C4

C_P = 0.05 pF diagonal **C_P = 0.07 pF adjacent**



Outline E4

C_P = 0.07 pF diagonal **C_P = 0.09 pF adjacent**



Outline H4

C_P = 0.16 pF diagonal **C_P = 0.20 pF adjacent**

DIMENSIONS IN MILLIMETERS (INCHES)

Description/ Applications

These matched diode quads use a monolithic array of Schottky diodes interconnected in ring configuration. The relative proximity of the diode junction on the wafer assures uniform electrical characteristics and temperature tracking.

These diodes are designed for use in double balanced mixers, phase detectors, AM modulators, and pulse modulators requiring wideband operation and small size. The low barrier diodes allow for optimum mixer noise figure at lower than conventional local oscillator levels. The wider dynamic range of the medium barrier diodes allows for better distortion performance.

Maximum Ratings

Junction Operating and Storage Temperature Range
- H4 Packaged Diodes ..... -65°C to +150°C
- E4 ..... -65°C to +125°C
- C4 Packaged Diodes ..... -65°C to +150°C

DC Power Dissipation ..... 75 mW per Junction
Derated linearly to zero at maximum rated temperatures (measured in infinite heat sink at T_{CASE} = 25°C).

Soldering Temperature
- H4 ..... 260°C for 10 sec.
- C4 ..... 235°C for 10 sec.
- E4 ..... 220°C for 10 sec.

These diodes are ESD sensitive. Handle with care to avoid static discharge through the diode.

Selection Guide

Package Outline \ Frequency	Barrier	To 2 GHz	2-4 GHz	4-8 GHz	8-12 GHz	12-18 GHz
E4 Low Cost	Medium Low	5082-2830 5082-2831	5082-2277	5082-2277		
H4 Hermetic	Medium Low	5082-2263 5082-2231	5082-2263 5082-2231	5082-2263 5082-2233		
C4 Broadband	Medium Low	5082-2291 5082-2271	5082-2291 5082-2271	5082-2292 5082-2272	5082-2294 5082-2279	5082-2294 5082-2280

Electrical Characteristics at $T_A = 25°C$

Part Number 5082-	Package	Barrier	Maximum Capacitance C_M (pF)	Maximum Measured Capacitance Difference ΔC_M (pF)	Maximum V_F Difference ΔV_F (mV)	Maximum Dynamic Resistance R_D (Ω)	Typical Parameters: Forward Voltage V_F (V)
2231	H4	Low	0.60	0.10	20	12	0.25
2233			0.40	0.05		16	0.30
2263		Medium	0.40	0.05		16	0.45
2830	E4		0.5 Typ.	0.20		12	0.40
2831		Low	0.5 Typ.	0.20		12	0.25
2277		Medium	0.50	0.10		15	0.35
2271	C4	Low	0.60	0.10		12	0.25
2272			0.40	0.10		15	0.25
2279			0.25	0.05		16	0.30
2280			0.20	0.05		16	0.30
2291		Medium	0.60	0.10		12	0.35
2292			0.40	0.10		15	0.35
2294			0.20	0.05		16	0.45
Test Conditions			$V_R = 0$, f = 1 MHz		$I_F = 5$ mA between Adjacent Leads		$I_F = 1$ mA Measured between Adjacent Leads

Package Characteristics

The HP outline E4 package is designed for MIC, Microstrip, and Stripline use from dc through X-Band. The leads provide a good continuity of transmission line impedance to the monolithic diode array. The leads are tin plated copper.

The C4 subminiature package is a ceramic carrier whose gold plated kovar leads are brazed to the substrate for maximum package ruggedness. If the leads are to be formed, they should be restricted so the bend starts at least 0.25 mm (0.01 inch) from the package body. The semiconductor is protected from mechanical abrasion by epoxy. The H4 miniature package is a hermetic metal-ceramic device, which makes it ideal for applications requiring high reliability. The leads are gold plated kovar. Outline H4 is capable of passing many of the environmental tests of MIL-STD-750. The applicable solderability test is reference 2031.1: 260°C, 10 seconds.

Dynamic and Series Resistance

Schottky diode resistance may be expressed as series resistance, R_S, or as dynamic resistance, R_D. These two terms are related by the equation

$$R_D = R_S + R_j$$

where R_j is the resistance of the junction. Junction resistance of a diode with DC bias is quite accurately calculated by

$$R_j = 26/I_B$$

where I_B is the bias current in milliamperes. The series resistance is independent of current.

The dynamic resistance is more easily measured. If series resistance is specified it is usually obtained by subtracting

the calculated junction resistance from the measured dynamic resistance.

Quad Capacitance

Capacitance of Schottky diode quads is measured using an HP4271 LCR meter. This instrument effectively isolates individual diode branches from the others, allowing accurate capacitance measurement of each branch or each diode. The conditions are: 20 mV R.M.S. voltage at 1 MHz. HP defines this measurement as "C_M," and it is equivalent to the capacitance of the diode by itself. The equivalent diagonal and adjacent capacitances can then be calculated by the formulas given below.

In a quad, the diagonal capacitance is the capacitance between points A and B as shown in Figure 1. The diagonal capacitance is calculated using the following formula:

$$C_{DIAGONAL} = \frac{C_1 \times C_2}{C_1 + C_2} + \frac{C_3 \times C_4}{C_3 + C_4}$$

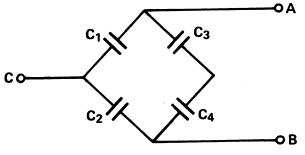


Figure 1.

The equivalent adjacent capacitance is the capacitance between points A and C in Figure 1. This capacitance is calculated using the following formula:

$$C_{ADJACENT} = C_1 + \frac{1}{\frac{1}{C_2} + \frac{1}{C_3} + \frac{1}{C_4}}$$

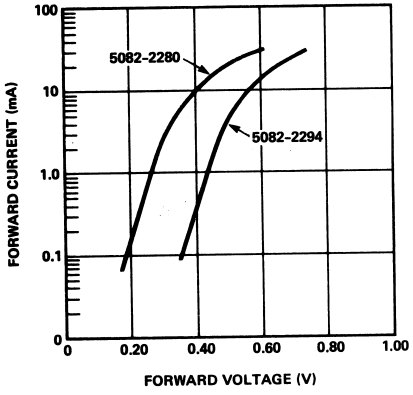


Figure 2. Typical Forward Characteristics at T_A = 25°C.

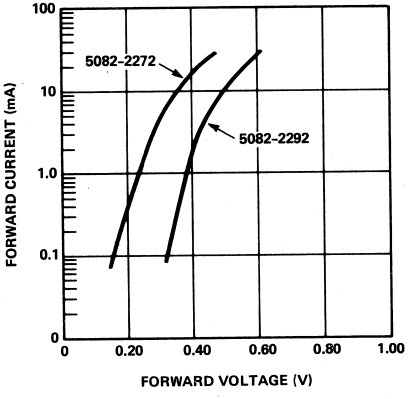


Figure 3. Typical Forward Characteristics at T_A = 25°C.

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Schottky Barrier Diodes for Mixers and Detectors

Technical Data

5082-2350/51
5082-2400/01
5082-2702/07
5082-2723/24
5082-2817/18

Features

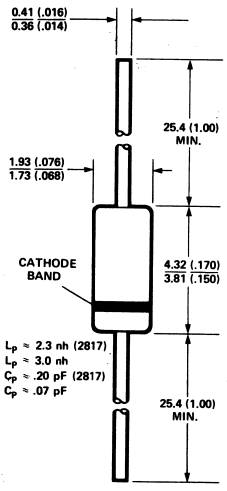
- **Low Noise Figure**
- **High Burnout Rating**
  1 W RF Pulse Power Absorbed
- **Rugged Design**
- **High Uniformity**
- **Both Medium and Low Barrier Diodes Available**

Description/ Applications

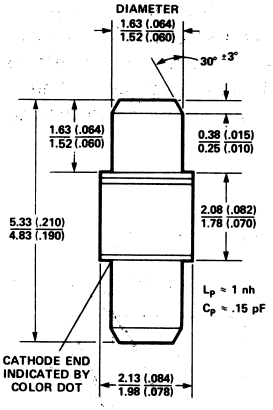
These Schottky diodes are optimized for use in broad band and narrow band microstrip, coaxial, or waveguide mixer assemblies operating to 18 GHz. The low barrier diodes give optimum noise figure performance at low local oscillator drive levels. Medium barrier diodes provide a wider dynamic range for lower distortion mixer designs. The 5082-2350, -2400, -2520, and -2565 have extremely low 1/f noise, making them ideal for use as Doppler mixers.

Package Characteristics

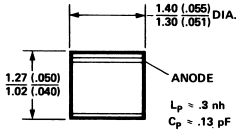
The HP Outline 15 package has a glass hermetic seal with plated Dumet leads which should be restricted so that the bend starts at least 1/16" (1.6 mm) from the glass body. With this



Outline 15



Outline 49



Outline 44

DIMENSIONS IN MILLIMETERS AND (INCHES)

restriction, it will meet MIL-STD-750, Method 2036, Conditions A (4 lb. [1.8 kg] tension for 30 minutes]. The maximum soldering temperature is 230°C for 5 seconds. Marking is by digital coding with a cathode band.

The HP Outline 49 package has a metal-ceramic hermetic seal. The anode and cathode studs are gold-plated Kovar. The maximum soldering temperature is 230°C for 5 seconds. Stud-stud TIR is 0.010" max.

The HP Outline 44 package is a hermetically sealed ceramic package. The anode and cathode are gold-plated Kovar. The maximum soldering temperature is 230°C for 5 seconds.

Maximum Ratings

Junction Operating and Storage Temperature Range
- 5082-2400, -2401, -2350, -2351 ..... -60°C to +100°C
- 5082-2817, -2818 ..... -60°C to +200°C
- All other diodes ..... -60°C to +150°C

CW Power Dissipation

Derated linearly to 0 W at maximum rated temperatures (measured in infinite heat sink at T_{CASE} = 25°C).
- 5082-2300, -2400 Series ..... 100 mW
- 5082-2817, -2818 ..... 250 mW
- Others ..... 200 mW

Pulse Power Dissipation

Peak power absorbed by the diode at T_{CASE} = 25°C
- 1 µs pulse, Du = 0.001 ..... 1 W

Soldering Temperature ..... 260°C for 5 sec.

Note: The 5082-2200, -2500, and -2700 series are ESD sensitive. Handle with care to avoid static discharge through the diode.

Electrical Specifications at T_A = 25°C

Typical Parameters

Part Number 5082-	Matched Pair 5082-	Barrier	LO Test Frequency (GHz)	Maximum SSB Noise Figure NF (dB)	IF Impedance Z_{IF} (Ω) Min.	IF Impedance Z_{IF} (Ω) Max.	Maximum SWR	Package Outline	Junction Capacitance C_{JO} (pF)	Breakdown Voltage V_{BR} (V)
2817	2818	Medium	2.0	6.0	250	400	1.5:1	15	1.0	15
2400	2401	Medium	2.0	6.0	150	250	1.3:1		0.7	30
2350	2351	Medium	2.0	7.0	150	250	1.5:1		0.9	30
2702	2707	Medium	9.375	6.5	200	400	1.5:1	44	0.10	4
2723	2724	Medium	16	6.5	200	400	1.5:1	49		3
Test Conditions	$\Delta NF \le 0.3$ dB $\Delta Z_{IF} \le 25$ Ω		LO Power = 1 mW IF = 30 MHz, 1.5 dB NF Zero DC Load Resistance (100 Ω for 5082-2817)		Same as for NF except IF = 10 KHz		Same as for NF		V = 0	I_R = 10 µA

Typical Parameters

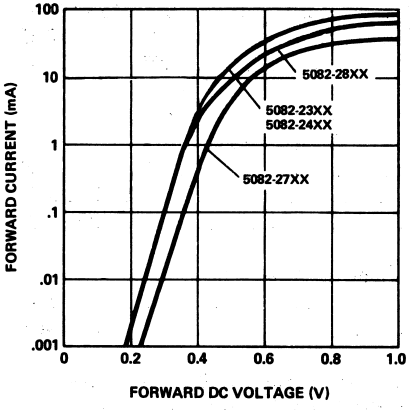


Figure 1. Typical Forward Characteristics at T_A = 25°C.

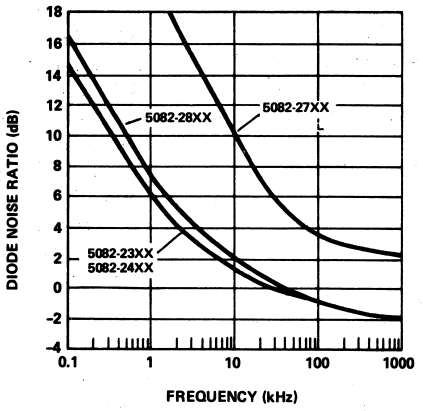


Figure 2. Typical Diode Noise Ratio vs. Frequency at 1 mA Current.

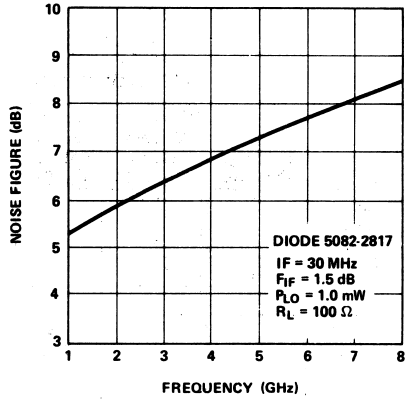


Figure 3. Typical Noise Figure vs. Frequency. (The Mount is tuned for Minimum Noise Figure at each Frequency.)

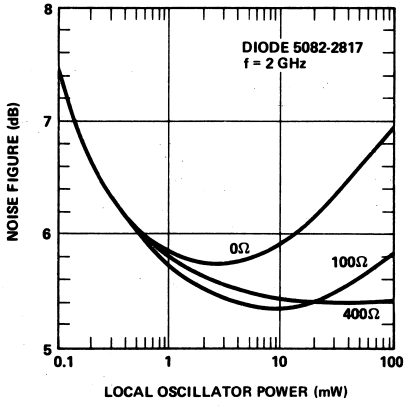


Figure 4. Single Sideband Noise Figure (including an IF-amplifier noise figure of 1.5 dB) vs. Incident LO Power for Various DC-load Resistances R_L. (The Mount is tuned for Minimum Noise Figure at each LO Power Level.)

Typical Parameters (cont.)

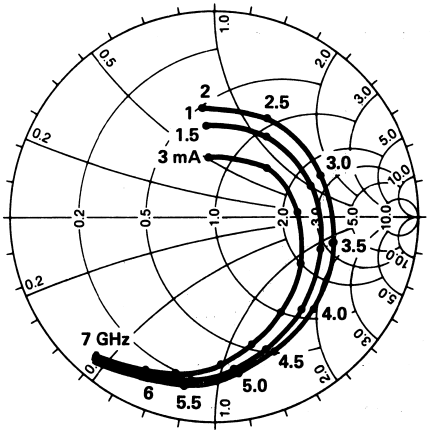


Figure 5. Typical Admittance Characteristics, 5082-2817 with Self Bias.

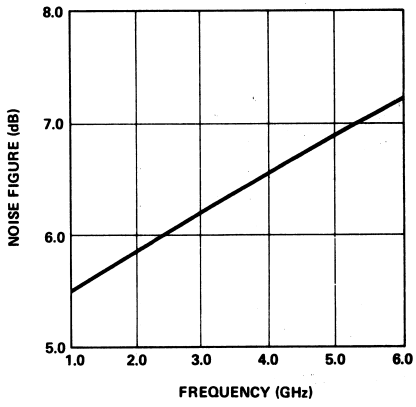


Figure 6. Typical HP 5082-2400 Noise Figure vs. Frequency with P_{LO} = 1.0 mW, IF = 30 MHz, and NF_{IF} = 1.5 dB. (Mount Tuned at Each Frequency.)

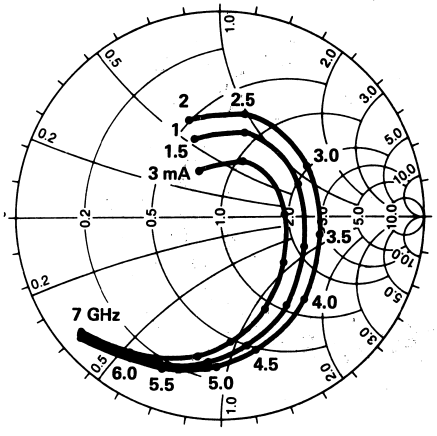


Figure 7. Typical Admittance Characteristics, 5082-2400 with Self Bias.

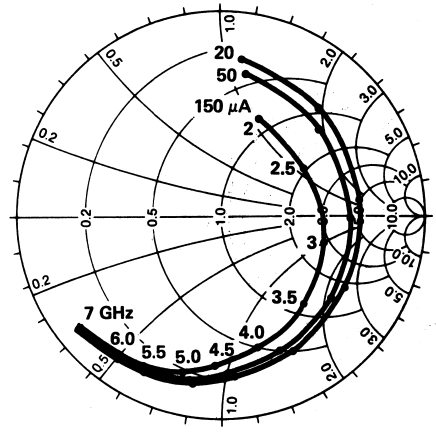


Figure 8. Typical Admittance Characteristics, 5082-2400 with External Bias.

Typical Parameters (cont.)

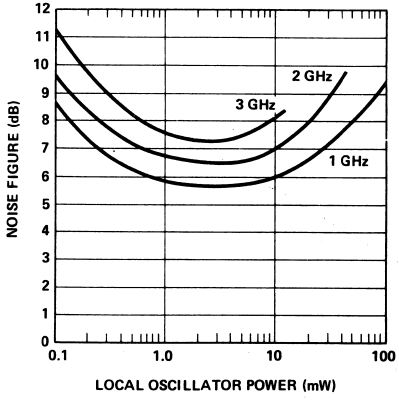


Figure 9. Typical HP 5082-2350 Noise Figure vs. Local Oscillator Power at 1.0, 2.0, and 3.0 GHz with IF = 30 MHz and NF_{IF} = 1.5 dB. (The Mount is tuned for Minimum Noise Figure at each LO Level).

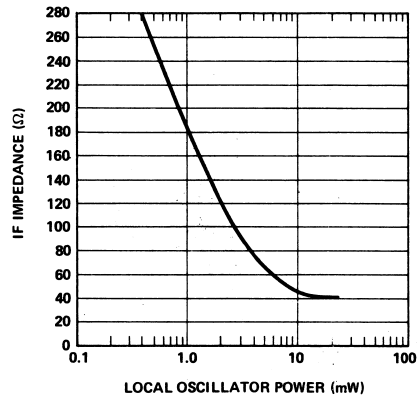


Figure 10. Typical HP 5082-2300 and 2400 Series IF Impedance vs. Local Oscillator Power with f_{LO} = 2.0 GHz and IF = 30 MHz. (The Mount is tuned for Minimum Noise Figure at each LO Level.)

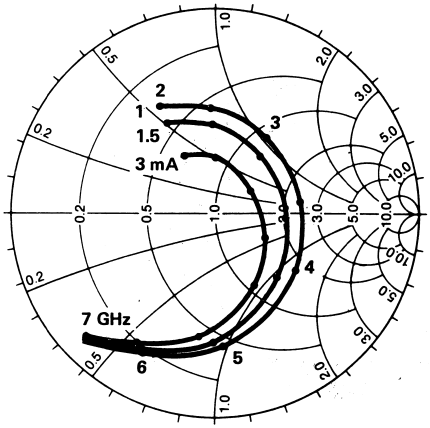


Figure 11. Typical Admittance Characteristics, 5082-2350 with Self Bias.

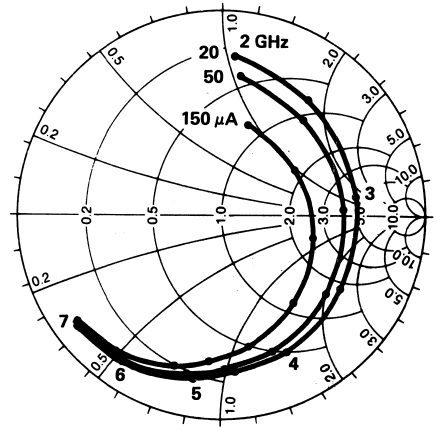


Figure 12. Typical Admittance Characteristics, 5082-2350 with External Bias.

Typical Parameters (cont.)

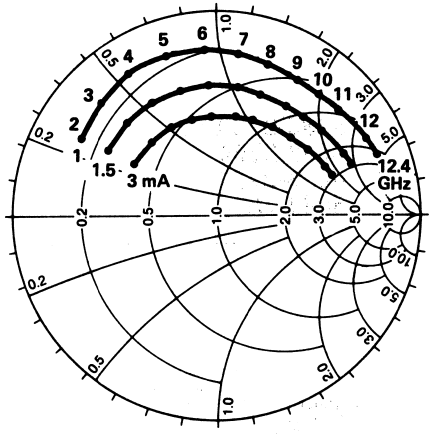


Figure 13. Typical Admittance Characteristics, 5082-2702 with Self Bias.

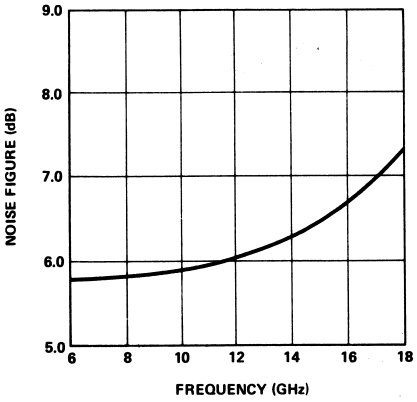


Figure 14. Typical Noise Figure vs. Frequency. IF = 30 MHz, NF_{IF} = 1.5 dB, P_{LO} = 1 mW. Diode tuned at each frequency (5082-2700 series).

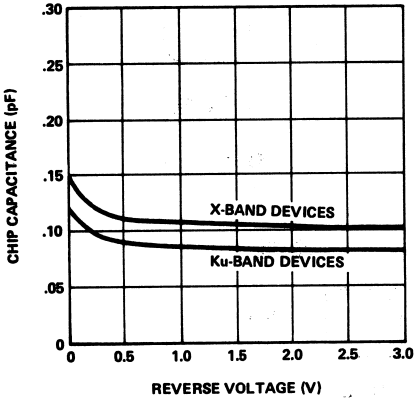


Figure 15. Typical Chip Capacitance vs. Reverse Voltage (5082-2700 Series).

HEWLETT PACKARD

Schottky Barrier Diodes for Detectors

Technical Data

5082-2750/51
5082-2755
5082-2787
5082-2824

Features

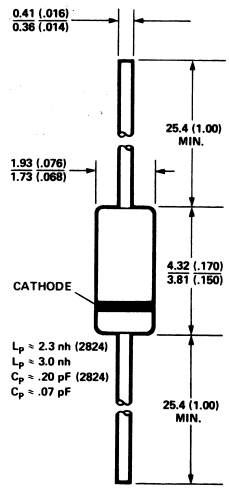
- **Improved Detection Sensitivity**
  TSS of -55 dBm at 10 GHz
- **Low 1/f Noise**
  Typical Noise-Temperature Ratio = 4 dB at 1 kHz
- **High Peak Power Dissipation**
  4.5 W RF Peak Pulse Power

Description/ Applications

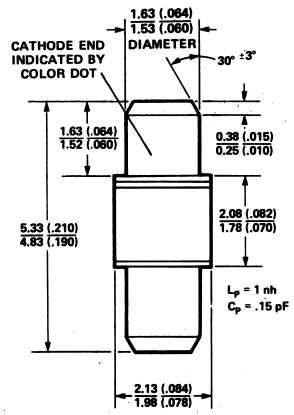
The low 1/f noise and high voltage sensitivity make these Schottky barrier diodes ideally suited for narrow bandwidth video detectors, and Doppler mixers as required in Doppler radar equipment, ECM receivers, and measurement equipment.

Package Characteristics

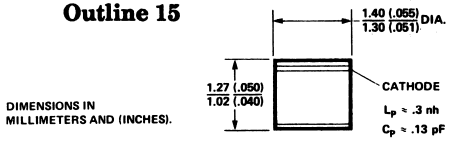
The HP Outline 15 package has a glass hermetic seal with plated Dumet leads which should be restricted so that the bend starts at least 1.16" (1.6 mm) from the glass body. With this restriction, it will meet MIL-STD-750, Method 2036, Condition A (4 lb. [1.8 kg] tension for 30 minutes). The maximum soldering temperature is 230°C for 5 seconds. Marking is by digital coding with a cathode band.



Outline 15



Outline 49



Outline 44

The HP Outline 49 package has a metal-ceramic hermetic seal. The anode and cathode studs are gold-plated Kovar. The maximum soldering temperature is 230°C for 5 seconds. Stud-stud TIR is 0.010" max.

The HP Outline 44 package is a hermetically sealed ceramic package. The anode and cathode are gold-plated Kovar. The maximum soldering temperature is 230°C for 5 seconds.

Maximum Ratings

Junction Operating and Storage Temperature Range
- 5082-2824 ..... -65°C to +200 °C
- All Others ..... -60°C to +150 °C

DC Power Dissipation – Power Absorbed by Diode
- *Derate Linearly to Zero at Maximum Temperature*
- 5082-2824 ..... 250 mW
- All Others ..... 100 mW

Soldering Temperature ..... 260°C for 5 sec.

RF Peak Pulse Power at T_{CASE} = 25°C (Pulse Width = 1 μs, Du = 0.001)
- 5082-2824 (Power Absorbed by Diode) ..... 4.5 W
- All Others (Power Incident) ..... 2.0 W

Maximum Peak Inverse Voltage (PIV) ..... V_{BR}

Note: The 2700 series diodes are ESD sensitive. Handle with care to avoid static discharge through the diode.

Electrical Specifications at T_A = 25°C

Typical Parameters

Part Number 5082-	Package Outline	Maximum Tangential Sensitivity TSS (dBm)	Voltage Sensitivity Minimum γ (mV/μW)	Video Resistance R_V (kΩ) Min.	Video Resistance R_V (kΩ) Max.	Minimum Breakdown Voltage V_{BR} (V)	Noise Temperature Ratio at f (dB)	Junction Capacitance C_{JO} (pF)
2824	15	-56	6.0	1.2	1.5	15	2 at 20 kHz 8 at 1 kHz	1.0
2787*		-52	3.5		1.8	4	5.0 at 20 kHz 15.0 at 1 kHz	12
2755		-55	5		1.6			1
2751	49							
2750	44							
Test Conditions		Video Bandwidth = 2 MHz f_{RF} = 2 GHz for 5082-2824, 10 GHz for all others I_{BIAS} = 20 μA; Video Amp. Eq. Noise, R_A = 500 Ω.	Same as for TSS at RF Signal Power Level of -40 dBm. Load Resistance = 100 kΩ			I_R = 10 μA	R_V = 50 Ω	V = 0

*RF Parameters for the 5082-2787 are sample tested only.

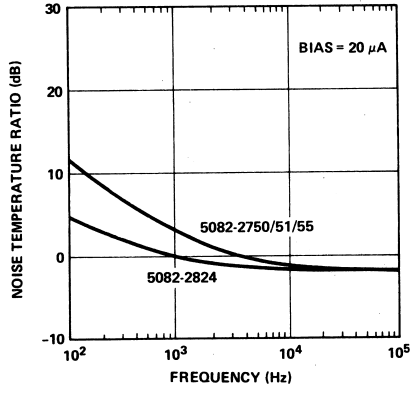


Figure 1. Typical Flicker (1/f) Noise vs. Frequency.

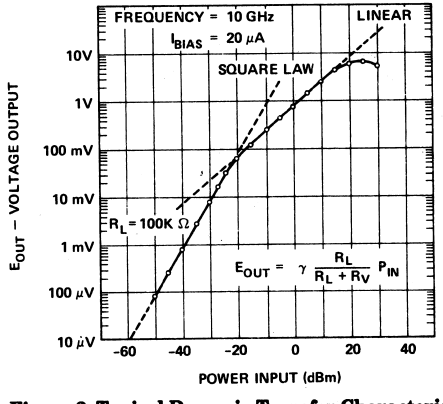


Figure 2. Typical Dynamic Transfer Characteristic. (5082-2750 Series).

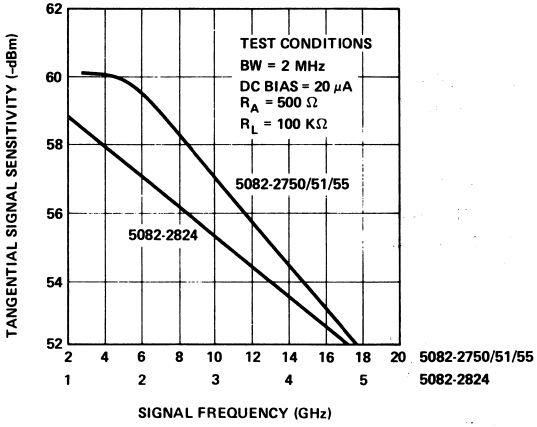


Figure 3. Typical TSS vs. Frequency.

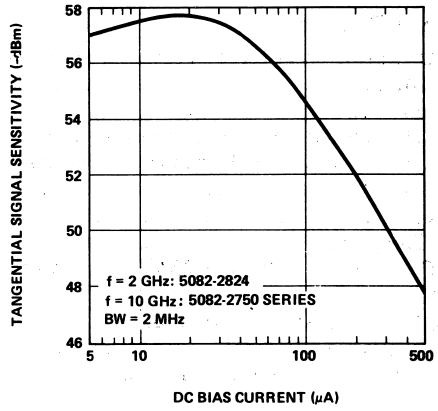


Figure 4. Typical TSS vs. Bias.

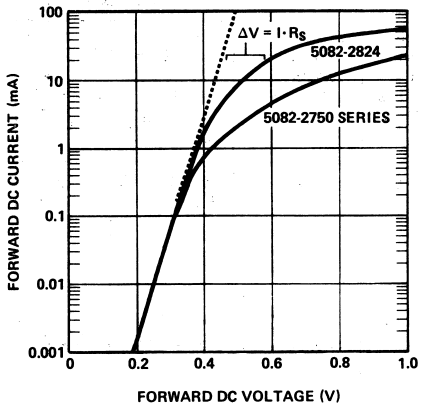


Figure 5. Typical Forward Characteristics at T_A = 25°C.

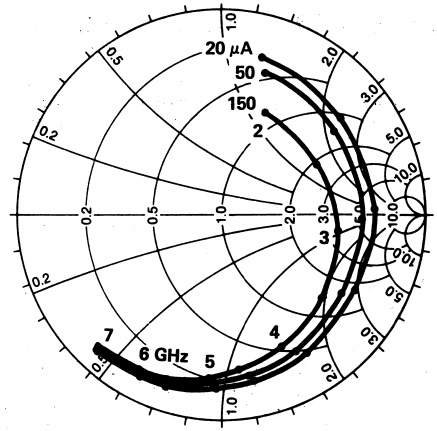


Figure 6. Typical Admittance Characteristics, 5082-2824 with External Bias.

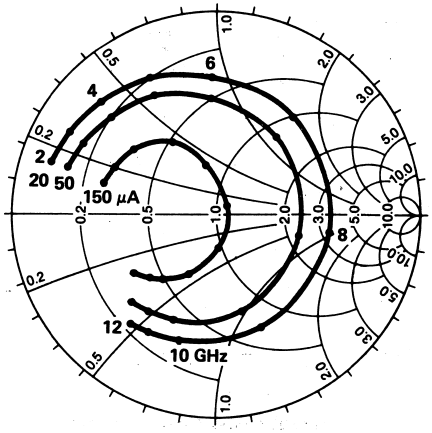


Figure 7. Typical Admittance Characteristics, 5082-2755 with External Bias.

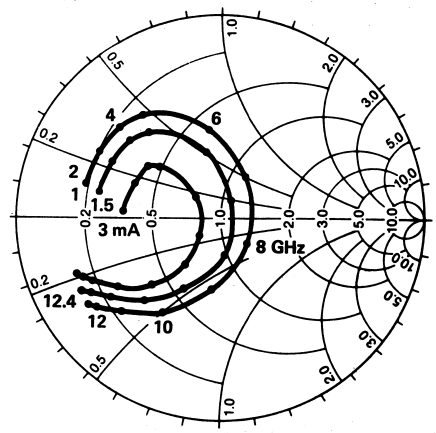


Figure 8. Typical Admittance Characteristics, 5082-2755 with Self Bias.

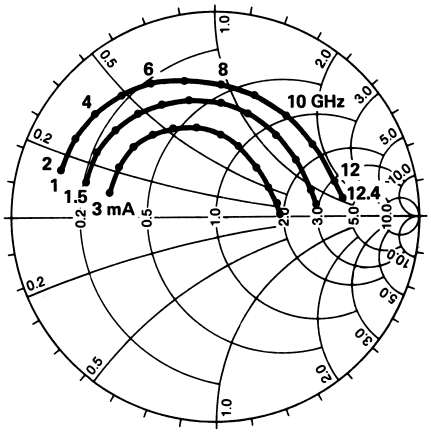


Figure 9. Typical Admittance Characteristics, 5082-2751 with Self Bias.

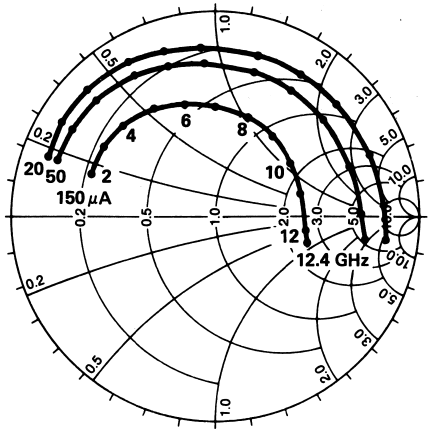


Figure 10. Typical Admittance Characteristics, 5082-2751 with External Bias.

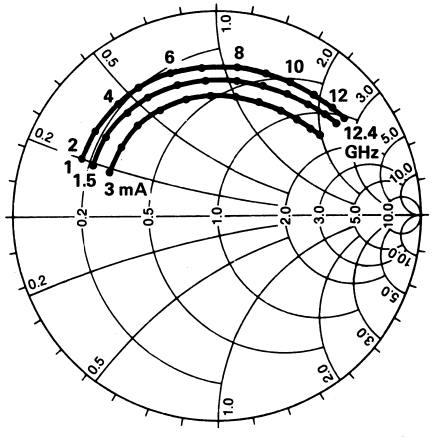


Figure 11. Typical Admittance Characteristics, 5082-2750 with Self Bias.

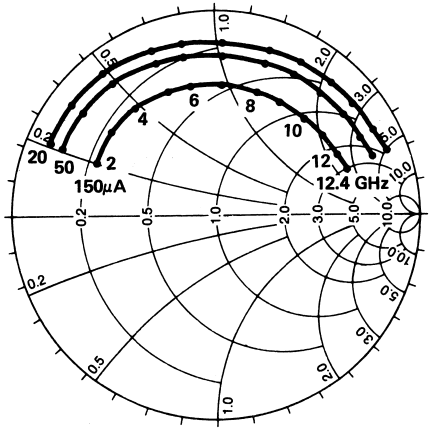


Figure 12. Typical Admittance Characteristics, 5082-2750 with External Bias.

HEWLETT PACKARD

GaAs Schottky Diode

Reliability Data

HSCH-9XXX

The following cumulative test results have been obtained from testing performed at Hewlett-Packard Communications Components Division in accordance with the latest revision of MIL-STD-750. Data was gathered from the product qualification, reliability monitor, and engineering evaluation.

For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in this catalog.

1. Life Test

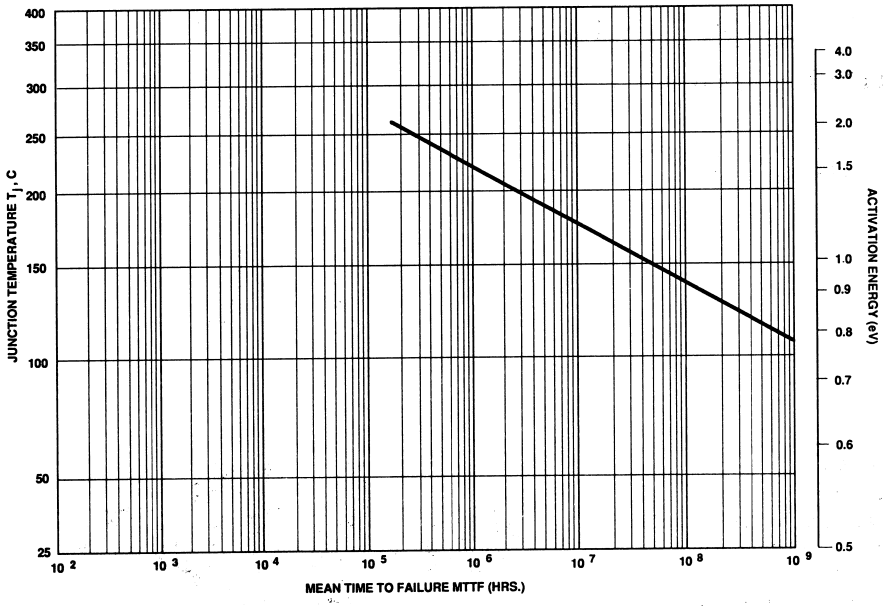
A. Demonstrated Performance

Test	Test Conditions	Units Tested	Total Device Hrs.	Total Failed	Failure Rate 1%/1K Hrs.
High Temp Reverse Bias (HTRB)	80% of V_{BR} @ T_A = 150°C	128	128,000	0	
Operating Life (O.L.)	I_f = 55 mA D.C @ T_A = 55°C	134	122,150	0	

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 1.0 ev, and listed in the following table.

Junction Temp. Tj (°C)	Point[1]		90% Confidence Level[2]	
	MTTF (hours)	FIT[3]	MTTF (hours)	FIT[3]
150	$5x10^7$	25	$2.2 x 10^7$	45
125	$2.5x10^8$	4	$1.1x10^8$	9
100	$2.0x10^9$	0.50	$9x10^8$	1.10
75	$1.5x10^{10}$	0.07	$6.5x10^9$	0.15
50	$2.0x10^{11}$	0.005	$9x10^{10}$	0.01



Notes:

1. The point MTTF is extrapolated from High Temperature Storage at 150, 200, 250°C.
2. This MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows: FIT = 10^9/(MTTF).

C. Example of Failure Rate Calculation

At 50°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hrs/day x 5 days/wk) ÷ 168 hrs/wk = 25%

Then the point failure rate per year is:

($5x10^{-12}$ hrs.) x (25%) x (8760 hrs/yr) = $1.1x10^{-6}$% per year

Likewise, the 90% confidence level failure rate per year is:

($1x10^{-11}$%/1000 hrs. x (25%) x (8760 hrs/yr) = $2x10^{-6}$% per year

II. Environmental and Mechanical Tests

Test	MIL-STD-750 Reference	Test Conditions	Units Tested	Total Failed
Moisture Resistance		80-98% RH @ -10/+65°C, 10 Days	22	0
Salt Atmosphere	1041	10-50 gr/m^2 @ 35°C, 24 hrs.	22	0

III. DOD-HDBK-1686 ESD Classification:

HSCH-9XXX – Class I

HEWLETT PACKARD

Tri Metal Beam Lead Schottky Diodes

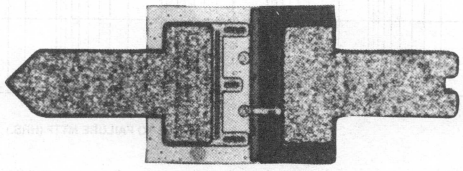
Reliability Data

Conclusion

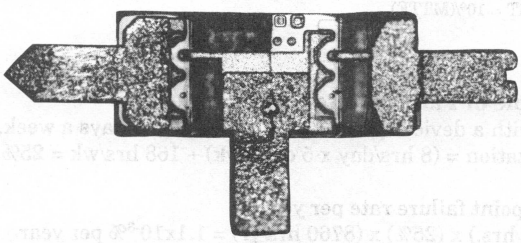
Hewlett-Packard's beam lead diodes have successfully passed stringent environmental testing. Hewlett-Packard beam lead diodes may be used in military and space applications without the necessity of hermetically sealed packaging.

General

For applications requiring component reliability estimation, Hewlett-Packard provides reliability data for all families of devices. Data is compiled from reliability tests run to demonstrate that a product meets the specified design criteria. All Schottky beam lead families have fulfilled the standard requirements of reliability qualification, and the results of these tests are shown on pages 3-98 and 3-101.



SINGLE



PAIR

Typical Beam Lead Outlines

Program Description

The purpose of this program is to qualify all beam lead diodes for operation in extreme environmental conditions which may be encountered during military and space operations.

The following test sequence has been designed to assess the endurance of beam lead diodes through relevant environmental stresses such as heat and humidity. To qualify a device as hermetic, the conventional procedure is to perform dye-penetrant and Radiflo tests. However, because of the absence of an enclosed cavity in the unique design of the beam lead diode, these tests are not directly applicable. Therefore, this program utilizes reliability tests such as moisture resistance, salt atmosphere, and immersion to verify that the passivation layer on the beam lead acts as a seal to protect the active area of the diode.

To perform these tests, various Schottky diodes were mounted in non-hermetic, open packages and tested as exposed beam lead devices.

Applicable Part Numbers

Schottky Beam Leads

5082-2837
HSCH-5300 Series
HSCH-5500 Series
HSCH-5800 Series
HSCH-5900 Series
HSCH-6000 Series

Test Sequence

Test	MIL-STD-750	Tests Condition	Units Tested	Failed	LTPD
Moisture Resistance[1,2]	1021	98% R.H. -10°C to 65°C, 10 days			
Temperature Cycling	1051	-65°C to 200°C, 100 cyc.	80	0	<7
Constant Acceleration	2006	20 KG, 1 min. each axis	(40 per lot)		
Salt Atmosphere[2]	1041	35° fog, 24 hours	25	0	<10
Salt Water Immersion[2]	(MIL-STD-883, M1002B)	65°C saturated NaCl solution, 2 cycles	25	0	<10

Notes:

1. The sequence of moisture resistance and temperature cycling followed by constant acceleration assures a thorough evaluation of the effect of exposure to high humidity and heat conditions. End points were taken after each test.
2. End points were: Visual at 100X magnification and D.C. testing to MIL-STD-19500.

Results

As demonstrated by these tests, Hewlett-Packard's beam lead diodes exhibit superior performance when subjected to severe environmental conditions. This proven reliability is achievable because of Hewlett-Packard's unique beam lead design. These beam lead diodes are made of tri-metal (Ti-Pt-Au or NiCr-Pt-Au) which extends both the operating and storage temperature range. In addition, a nitride passivation layer acts as a sealant and provides immunity from contaminants which could lead to I_R drift. Conductive particle protection is provided by a layer of polyimide, which also functions as scratch protection. Therefore, it is recommended that Hewlett-Packard beam lead diodes be used in military and space applications without the necessity of hermetically sealed packaging.

HEWLETT PACKARD

Tri Metal Beam Lead Schottky Diodes and Hermetic Packaged Devices

Reliability Data

HSCH-5300 Series
HSCH-5500 Series
HSCH-5800 Series
HSCH-6000 Series
5082-2200
5082-2202/03
5082-2231
5082-2233
5082-2263
5082-2765/66
5082-2785/86
5082-2837

The following cumulative test results have been obtained from testing performed at Hewlett-Packard Communications Components Division in accordance with the latest revision of MIL-STD-750. Data was gathered from the product qualification, reliability monitor, and engineering evaluation.

For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in this catalog.

1. Life Test

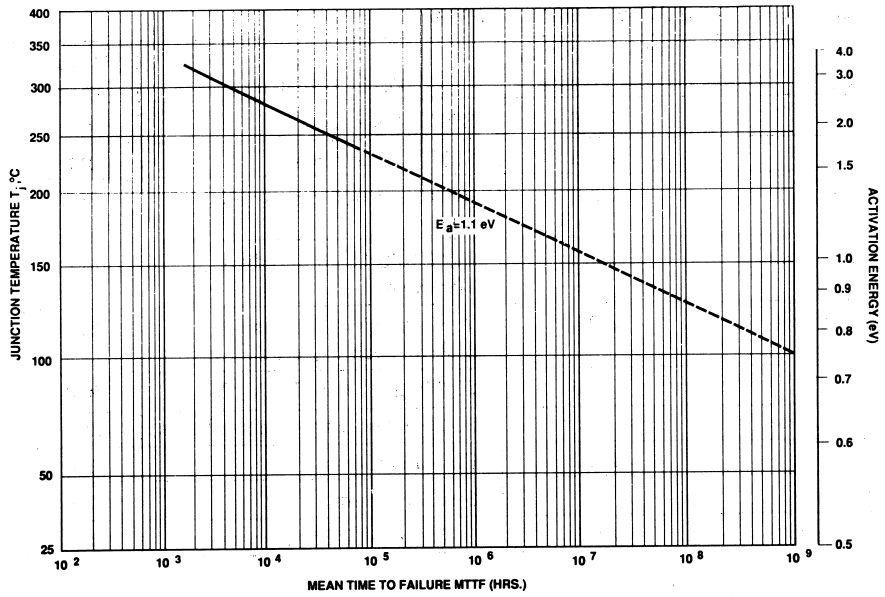
A. Demonstrated Performance

Test	Test Conditions	Units Tested	Total Device Hrs.	Total Failed	Failure Rate 1%/1K Hrs.
High Temp. Rev. Bias (HTRB)	V_R = 80% V_{BR}, T_A = 150°C	482	482,000	0	0
Operating Life (OL)	I_P = 50 mA A-C, T_A = 125°C	1052	1,050,000	0	0
Room Temp. Operating Life (RTOL)	P_{fm} = 125 mW, T_A = 25°C V_R = 80% V_{BR}, 60 Hz	297	297,000	0	0
High Temp. Operating Life (HTOL)	10 mA DC, T_A = 150°C	287	287,500	0	0
High Temp. Storage (HTS)	T_A = 200°C	191	191,000	0	0

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 1.1 eV, and listed in the following table.

Junction Temp. T_J (°C)	Point[1]		90% Confidence Level[2]	
	MTTF (Hours)	FIT[3]	MTTF (Hours)	FIT[3]
200°C	5.0×10^5	2000.0	2.2×10^5	4545.0
175°C	2.3×10^6	435.0	1.0×10^6	1000.0
150°C	1.2×10^7	83.0	5.2×10^6	192.0
125°C	6.5×10^7	15.0	2.8×10^7	35.0
100°C	7.0×10^8	1.4	3.0×10^8	3.3
75°C	8.2×10^9	0.12	3.6×10^9	0.27



Notes:

1. The point MTTF is simply the total device hours divided by the number of failures which can only be generated at elevated temperature. Data in the above table is obtained by extrapolation to lower temperature.
2. The MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows: FIT = 10^9/(MTTF).

C. Example of Failure Rate Calculation

At 75°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hrs/day x 5 days/wk) ÷ 168 hrs/wk = 25%

Then the point failure rate per year is:

(1.2 x 10^{-10}/hr.) x (25%) x (8760 hrs/yr) = 2.6 x 10^{-5}% per year

Likewise, the 90% confidence level failure rate per year is:

(2.7 x 10^{-10}/hrs.) x (25%) x (8760 hrs/yr) = 5.9 x 10^{-5}% per year

2. Environmental and Mechanical Tests

Test	MIL-STD-750 Reference	Test Conditions	Units Tested	Total Failed
Solderability	2026	260°C, 5 seconds	50	0
Solder Heat	2031	260°C, 10 seconds	22	0
Thermal Shock	1056	-65°C/150°C, 5 min dwell, 200 cycles	281	0
Temperature Cycle	1051	-65°C/150°C, 10 min dwell, 200 cycles	40	0
Mechanical Shock	2016	1500 gs, 0.5 msec pulse 5 blows each X_1, Y_1, Y_2	316	0
Acceleration	2006	20,000 gs, 1 min, X_1, Y_1, Y_2	273	0
Vibration Variable Freq.	2056	20-2000 Hz, 20 g, 4 min all axis	221	0
Hermeticity	1017	Fine and Gross	256	1
Lead Integrity		3 oz Minimum	25	0
Salt Atmosphere	1041	10-50 gr/m² @ 35°C, 24 hrs.	22	0

3. DOD-HDBK-1686 ESD Classification:

HSCH-53XX	Class I
HSCH-55XX	Class I
HSCH-63XX	Class I
HSCH-65XX	Class I
5082-2XXX	Class I
HSCH-5800	Class III
HSCH-68XX	Class III
5082-223X	Class III
5082-2263	Class III

HEWLETT PACKARD

Tri Metal Beam Lead Schottky Diodes (Non-Hermetic Packaged)

Reliability Data

5082-2207/08/09/10
5082-2271/72
5082-2277
5082-2279/80
5082-2291/92
5082-2294
5082-2774/75
5082-2794/95
5082-2831

The following cumulative test results have been obtained from testing performed at Hewlett-Packard Communications Components Division in accordance with the latest revision of MIL-STD-750. Data was gathered from the product qualification, reliability monitor, and engineering evaluation.

For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in this catalog.

1. Life Test

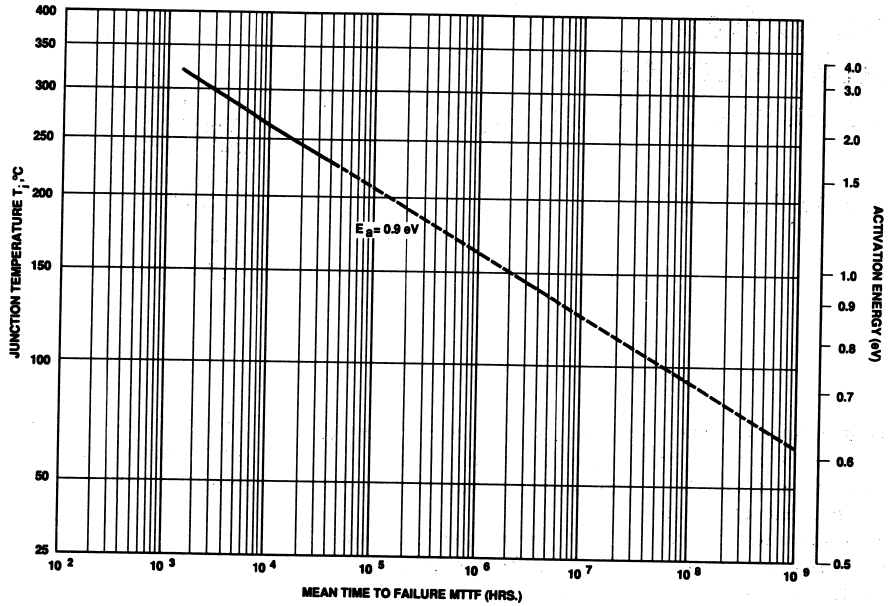
A. Demonstrated Performance

Test	Test Conditions	Units Tested	Total Device Hrs.	Total Failed	Failure Rate 1%/1K Hrs.
High Temp. Reverse Bias (HTRB)	$V_R = 80\%\ V_{BR}$, $T_A = 150°C$	482	482,000	0	0
High Temp. Operating Life (OL)	$I_P = 50$ mA AC, $T_A = 125°C$	1052	1,050,000	0	0
Room Temp. Operating Life (OL)	$P_{fm} = 125$ mW, 25°C $V_R = 80\%\ V_{BR}$, 60 Hz	297	297,000	0	0
High Temp. Storage (HTS)	$T_A = 125°C$	319	319,000	0	0

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 0.9 eV, and listed in the following table.

Junction Temp. T_J (°C)	Point[1]		90% Confidence Level[2]	
	MTTF (Hours)	FIT[3]	MTTF (Hours)	FIT[3]
150°C	1.7×10^6	588.0	7.4×10^5	1351.0
140°C	3.1×10^6	322.0	1.3×10^6	769.0
130°C	5.7×10^6	175.0	2.5×10^6	402.0
120°C	1.1×10^7	91.0	5.0×10^6	200.0
100°C	4.7×10^7	21.0	2.0×10^7	50.0
75°C	3.5×10^8	2.8	1.5×10^8	6.7
50°C	3.6×10^9	0.28	1.56×10^9	0.64



Notes:

1. The point MTTF is simply the total device hours divided by the number of failures which can only be generated as elevated temperature. Data in the above table is obtained by extrapolation at low temperatures.
2. The MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows: FIT = 10^9/(MTTF).

C. Example of Failure Rate Calculation

At 50°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hrs/day x 5 days/wk) ÷ 168 hrs/wk = 25%

Then the point failure per year is:

(2.8 x 10^{-10}/hr) x (25%) x (8760 hrs/yr) = 6.1 x 10^{-5}% per year

Likewise, the 90% confidence level failure rate per year is:

(6.4 x 10^{-10}/hr) x (25%) x (8760 hrs/yr) = 1.4 x 10^{-4}% per year

2. Environmental and Mechanical Tests

Test	MIL-STD-750 Reference	Test Conditions	Units Tested	Total Failed
Solderability	2026	260°C, 5 seconds	144	0
Solder Heat	2031	260°C, 10 seconds	115	0
Moisture Resistance		85°C/85% RH, biased, 1000 hrs.	845	0
Thermal Shock	1056	-65°C/125°C, 5 min. dwell, 200 cycles	744	0
Temperature Cycle	1051	-65°C/125°C, 10 min. dwell, 200 cycles	1784	0
Lead Integrity		>3 oz	214	0

3. DOD-HDBK-1686 ESD Classification

5082-220X Class I
5082-2210 Class I
5082-27XX Class I
5082-22XX Class III

HEWLETT PACKARD

Surface Mount Schottky Diodes

Reliability Data

HSMS-000X
HSMS-001X
HSMS-280X
HSMS-281X
HSMS-282X
HSMS-284X

The following cumulative test results have been obtained from testing performed at Hewlett-Packard Communications Components Division in accordance with the latest revision of MIL-STD-750. Data was gathered from the product qualification, reliability monitor, and engineering evaluation.

For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in this catalog.

1. Life Test

A. Demonstrated Performance

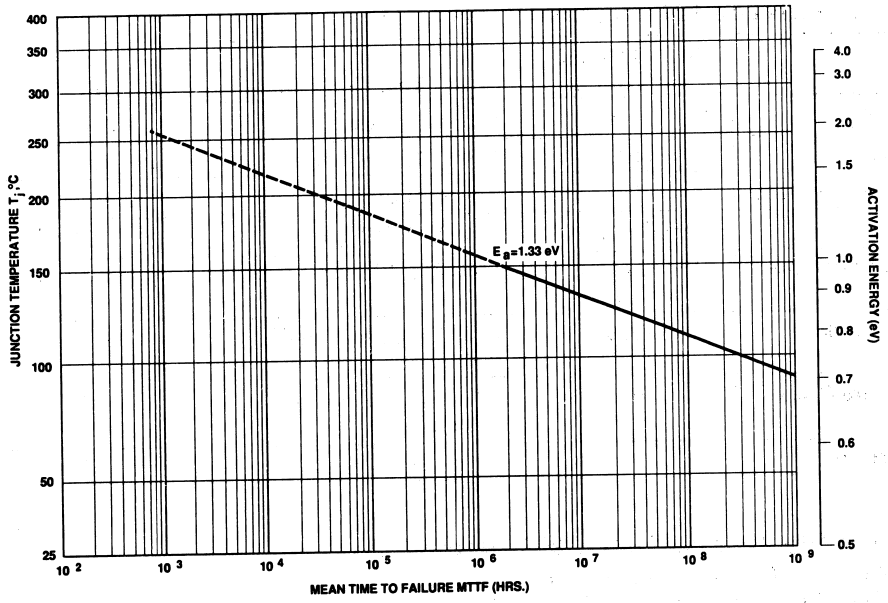
Test	Test Conditions	Units Tested	Total Device Hrs.	Total Failed	Failure Rate 1%/1K Hrs.
High Temp. Rev. Bias (HTRB)	V_R = 80% V_{BR}, T_A = 150°C	804	828,045	0	0
Operating Life (O.L.)	T_A = 25°C, P_{FM} = 250 mW V_R = 80% V_{BR}, 60 Hz	1,068	999,884	0	0
High Temp. Operating Life (HTOL)	10 mA DC, T_A = 150°C	250	251,900	0	0
High Temp. Storage (HTS)	T_A = 150°C	2,917	1,836,660	0	0

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 1.33 eV, and listed in the following table.

Junction Temp. T_J** (°C)	Point[1]		90% Confidence Level[2]	
	MTTF* (Hours)	FIT[3]	MTTF (Hours)	FIT[3]
150°C	1.8×10^6	556.0	7.8×10^5	1282.0
140°C	4.4×10^6	227.0	1.9×10^6	526.0
130°C	1.1×10^6	91.0	4.8×10^6	208.0
120°C	2.9×10^7	34.0	1.3×10^7	77.0
100°C	2.4×10^8	4.0	1.0×10^8	10.0
75°C	4.8×10^9	0.20	2.1×10^9	0.48
50°C	1.5×10^{11}	0.007	6.5×10^{10}	0.015

*MTTF data collected in Hermetic and Plastic Packages.
**T_J was calculated using a θ_{JA} of 500°C/W.
(Notes on reverse side.)



Notes:

1. The point MTTF is simply the total device hours divided by the number of failures.
2. The MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows: FIT = 10^9/(MTTF).

C. Example of Failure Rate Calculation

At 50°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hrs/day x 5 days/wk) ÷ 168 hrs/wk ≡ 25%

Then the point failure rate per year is:

$(7.0 \times 10^{-12}/\text{hr}) \times (25\%) \times (8760\ \text{hrs/yr}) = 1.5 \times 10^{-6}\%$ per year

Likewise, the 90% confidence level failure rate per year is:

$(1.5 \times 10^{-11}/\text{hr}) \times (25\%) \times (8760\ \text{hrs/yr}) = 3.3 \times 10^{-6}\%$ per year

2. Environmental and Mechanical Tests

Test	MIL-STD-750 Reference	Test Conditions	Units Tested	Total Failed
Solderability	2026	215°C, 5 seconds	500	0
Solder Heat	2031	260°C, 10 seconds	426	0
Resistance to Solvent	1022	4 Solvent Groups	98	0
Autoclave	HP GSS 12-109	121°C, 15 PSIG, 96 hrs.	1204	0
Moisture Resistance	HP GSS 12-107, Method B	85°C/85% RH, biased, 1000 hrs.	311	0
Thermal Shock	1056	-65/150°C, 5 min dwell, 200 cycles	615	0
Temperature Cycle	1051	-65/150°C, 10 min dwell, 200 cycles	637	0
Lead Integrity		2.0 pounds minimum	140	0

3. Flammability Test (MIL-STD-202, Method 111):

Meets Needle Flame Test per UL Category D
(Flaming Time <3 sec.) under material classification 94V0.

4. DOD-HDBK-1686A ESD Classification:

HSMS-00XX	Class I
HSMS-280X/281X/282X	Class I

Surface Mount Schottky Diodes

Reliability Data

HSMS-8001
HSMS-8002
HSMS-8101
HSMS-8011
HSMS-8012
HSMS-8202

The following cumulative test results have been obtained from testing performed at Hewlett-Packard Communications Components Division in accordance with the latest revision of MIL-STD-750. Data was gathered from the product qualification, reliability monitor, and engineering evaluation.

For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in this catalog.

1. Life Test

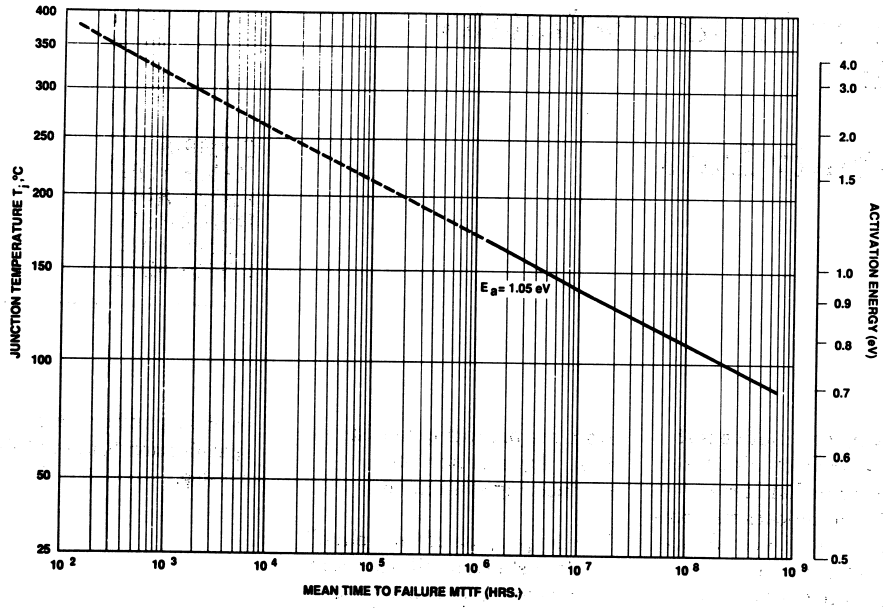
A. Demonstrated Performance

Test	Test Conditions	Units Tested	Total Device Hrs.	Total Failed	Failure Rate 1%/1K Hrs.
High Temp. Rev. Bias (HTRB)	V_R = 80% V_{BR}, T_A = 150°C	127	127,000	0	0
High Temp. Operating Life (HTOL)	P_{fm} = 75 mW, T_A = 65°C V_R = 80% V_{BR}	129	129,000	0	0
High Temp. Storage (HTS)	T_A = 150°C	129	129,000	0	0

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 1.05 eV, and listed in the following table.

Junction Temp. T_J (°C)	Point[1]		90% Confidence Level[2]	
	MTTF (Hours)	FIT[3]	MTTF (Hours)	FIT[3]
150°C	3.6×10^6	278.0	1.6×10^6	625.0
140°C	7.3×10^6	137.0	3.2×10^6	312.0
130°C	1.5×10^7	67.0	6.5×10^6	153.0
120°C	3.2×10^7	31.0	1.4×10^7	71.0
100°C	1.7×10^8	6.0	7.4×10^7	14.0
75°C	1.8×10^9	0.56	7.8×10^8	1.3
50°C	2.6×10^{10}	0.04	1.1×10^{10}	0.09



Notes:

1. The point MTTF is simply the total device hours divided by the number of failures.
2. The MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows: FIT = 10^9/(MTTF).

C. Example of Failure Rate Calculation

At 50°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hrs/day x 5 days/wk) ÷ 168 hrs/wk = 25%

Then the point failure rate per year is:

$(4.0 \times 10^{-11}/1000 \text{ hrs.}) \times (25\%) \times (8760 \text{ hrs/yr}) = 8.76 \times 10^{-6}\%$ per year

Likewise, the 90% confidence level failure rate per year is:

$(9.0 \times 10^{-11}/1000 \text{ hrs.}) \times (25\%) \times (8760 \text{ hrs/yr}) = 1.97 \times 10^{-5}\%$ per year

2. Environmental and Mechanical Tests

Test	MIL-STD-750 Reference	Test Conditions	Units Tested	Total Failed
Solderability	2026	215°C, 5 seconds	500	0
Solder Heat	2031	260°C, 10 seconds	426	0
Resistance to Solvent	1022	4 solvent groups	98	0
Autoclave		121°C, 15 PSIG, 96 hrs.	116	0
Moisture Resistance		85°C/85% RH, biased, 1000 hrs.	118	0
Thermal Shock	1056	-65/150°C, 5 min dwell, 200 cycles	163	0
Temperature Cycle	1051	-65/150°C, 10 min dwell, 200 cycles	169	0
Lead Integrity			140	0

3. Flammability Test:

Meets Needle Flame Test Category D (Flaming Time <3 sec.) under material classification 94V0.

4. DOD-HDBK-1686A ESD Classification:

HSMS-8001/8002/8011/8012/8101/8202 Class I

HEWLETT PACKARD

Passivated General Purpose Schottky Diodes

Reliability Data

1N5711, -5712
5082-0024
5082-0087
5082-0097
5082-2080
5082-2800
5082-2804/05
5082-2810/11
5082-2813/14/15
5082-2817/18
5082-2824
5082-2826
5082-2835/36

The following cumulative test results have been obtained from testing performed at Hewlett-Packard Communications Components Division in accordance with the latest revision of MIL-STD-750. Data was gathered from the product qualification, reliability monitor, and engineering evaluation.

For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in this catalog.

1. Life Test

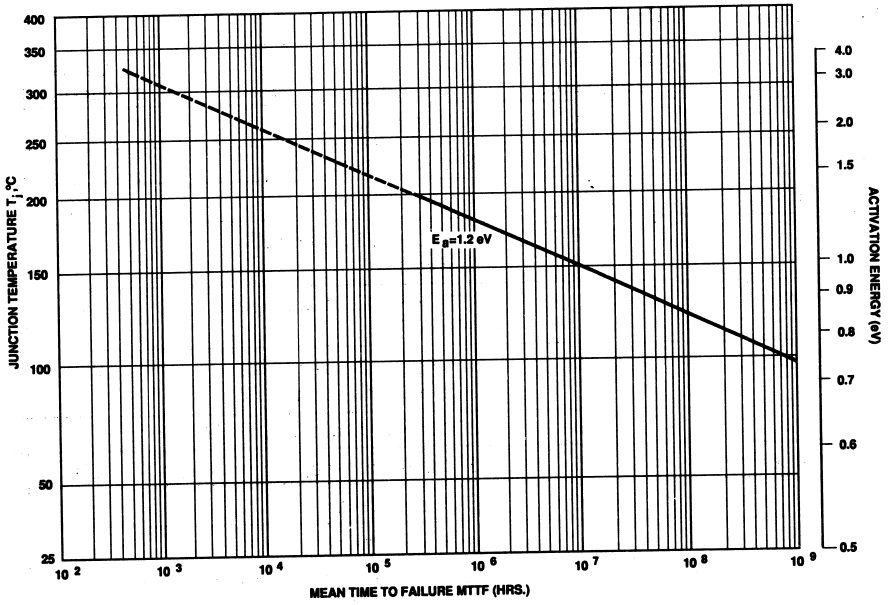
A. Demonstrated Performance

Test	Test Conditions	Units Tested	Total Device Hrs.	Total Failed	Failure Rate 1%/1K Hrs.
High Temp. Rev. Bias (HTRB)	V_R = 80% V_{BR}, T_A = 200°C	676	598,000	0	0
Room Temp. Operating Life (RTOL)	P_{fm} = 250 mW, T_A = 25°C V_R = 80% V_{BR}, 60 Hz	364	364,000	0	0
High Temp. Storage (HTS)	T_A = 200°C	367	271,000	0	0

B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 1.2 eV, and listed in the following table.

Junction Temp. T_J (°C)	Point[1]		90% Confidence Level[2]	
	MTTF (Hours)	FIT[3]	MTTF (Hours)	FIT[3]
200°C	2.7×10^5	3704.0	1.2×10^5	8333.0
175°C	1.4×10^6	714.0	6.1×10^5	1639.0
150°C	8.9×10^6	112.0	4.0×10^6	250.0
125°C	7.1×10^7	14.0	3.1×10^7	32.0
100°C	7.4×10^8	1.3	3.2×10^8	3.1
75°C	1.0×10^{10}	0.10	4.3×10^9	2.3



Notes:

1. The point MTTF is simply the total device hours divided by the number of failures.
2. The MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows: FIT = 10^9/(MTTF).

C. Example of Failure Rate Calculation

At 75°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hrs/day x 5 days/wk) ÷ 168 hrs/wk = 25%

Then the point failure rate per year is:

(1.0 x 10^{-10}/hr.) x (25%) x (8760 hrs/yr) = 2.2 x 10^{-5}% per year

Likewise, the 90% confidence level failure rate per year is:

(2.3 x 10^{-10}/hrs.) x (25%) x (8760 hrs/yr) = 5.1 x 10^{-5}% per year

2. Environmental and Mechanical Tests

Test	MIL-STD-750 Reference	Test Conditions	Units Tested	Total Failed
Solderability	2026	260°C, 5 seconds	198	0
Solder Heat	2031	260°C, 10 seconds	44	0
Resistance to Solvent	1022	4 solvent groups	126	0
Thermal Shock	1056	-65/200°C, 5 min dwell, 200 cycles	116	0
Temperature Cycle	1051	-55°C/100°C, 10 min dwell, 200 cycles	416	0
Mechanical Shock	2016	1500 g's, 0.5 msec pulse 5 blows each X1, Y1, Y2	272	0
Acceleration	2006	20,000 g's, 1 min, X1, Y, Y2	116	0
Vibration Variable Freq.	2056	20-2000 Hz, 20 g, 4 min all axis	116	0
Hermeticity	1017	Fine and Gross	416	0
Lead Integrity		4 lbs Minimum	176	0
Salt Atmosphere	1041	10-50 gr/m² @ 35°C, 24 hrs.	45	0

3. DOD-HDBK-1686 ESD Classification:

5082-28XX Class I

HEWLETT PACKARD

Passivated P-Type Microwave Schottky Diodes

Reliability Data

Description

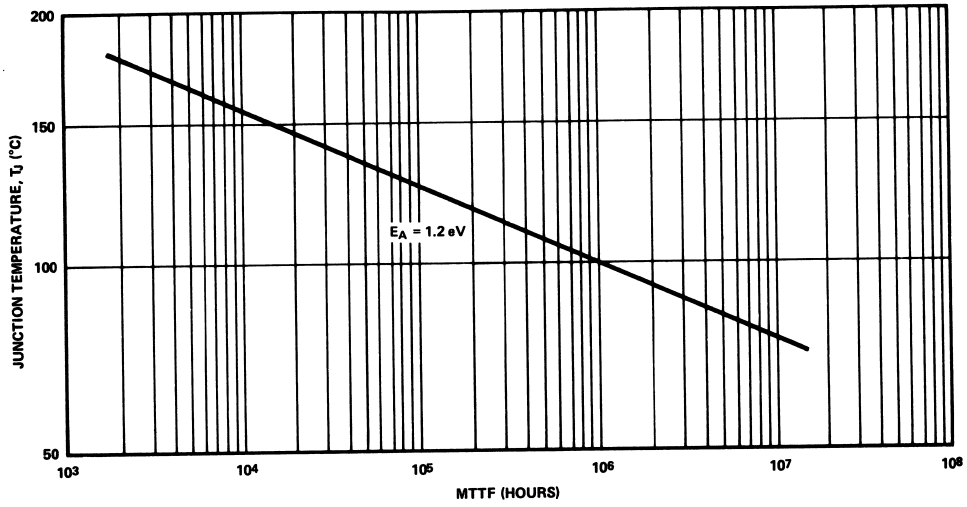
For applications requiring component reliability estimation, Hewlett-Packard provides reliability data for all families of devices. Data is compiled from reliability tests run to demonstrate that a product meets the specified design criteria. Periodically, additional tests are run. The data on this sheet represents the latest review of accumulated test results. All data recorded here is for P-type passivated microwave Schottky diodes mounted in non-hermetic sealed unsealed 44 packages.

Applications

This information represents the capabilities of the generic device. Failure rate and MTTF values presented here are achievable with normal MIL-S-19500 test screening. Reliability can be guaranteed only under specified conditions and LTPD levels.

Applicable Part Numbers

5082-0009
5082-2750
5082-2751
5082-2755
5082-2787
5082-9891
HSCH-3486



Mean Time to Failure vs. Junction Temperature

Burn-In and Storage

Test	Test Conditions[1]	LTPD per 1000 Hours
High Temperature Life	Storage at 125°C	4.0
Steady State Operating Life	P_{FM} = 100 mW V_{RM} = 80% of V_{BR} T_A = 25°C f = 60 Hz	3.0

Note:
1. 1000 hours minimum on all life tests.

Environmental

Test	MIL-STD-750	Test Conditions	LTPD
Temperature Cycling	1051C	10 cycles from -65°C to 200°C, 5 hrs. at extremes, 5 min. transfer	10
Thermal Shock	1056	10 cycles from 0°C to 100°C, 3 sec. transfer	10
Mechanical Shock	2016	5 blows each at X_1, X_2, Y, 1500 G, 0.5 msec. pulse	10
Vibration Fatigue	2046	20 G min., 60 Hz	10
Vibration Variable Frequency	2056	four 4 min. cycles each X, Y, Z at 20 G min., 100 to 2000 Hz	10
Moisture Resistance	1021	240 hours, 90-98% relative humidity	10
Salt Atmosphere	1041	35°C fog for 24 hours	12

HEWLETT PACKARD

Passivated N-Type Microwave Schottky Diodes

Reliability Data

Description

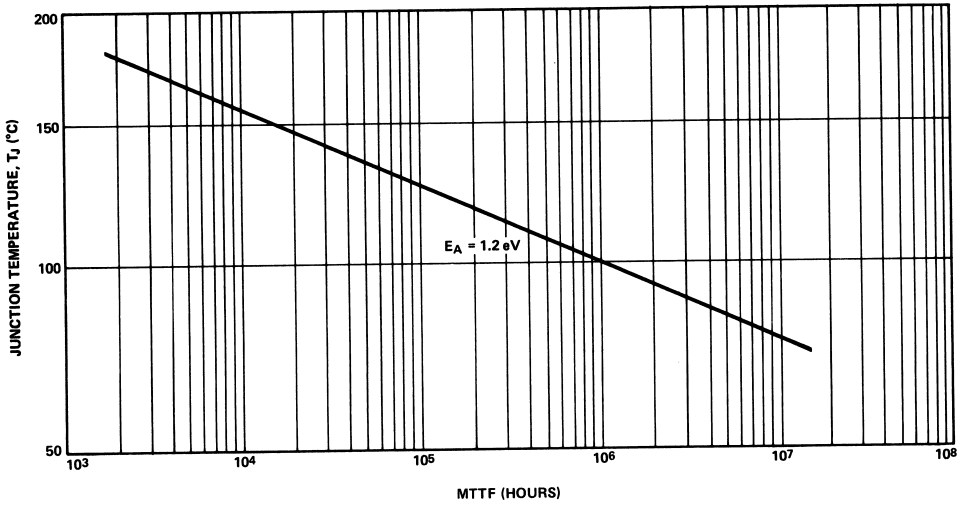
For applications requiring component reliability estimation, Hewlett-Packard provides reliability data for all families of devices. Data is compiled from reliability tests run to demonstrate that a product meets the specified design criteria. Periodically, additional tests are run. The data on this sheet represents the latest review of accumulated test results. All data recorded here is for N-type passivated microwave Schottky diodes mounted in non-hermetic sealed unsealed 44 packages.

Applications

This information represents the capabilities of the generic device. Failure rate and MTTF values presented here are achievable with normal MIL-S-19500 test screening. Reliability can be guaranteed only under specified conditions and LTPD levels.

Applicable Part Numbers

5082-0013	5082-2702
5082-0023	5082-2706
5082-0029	5082-2707
5082-0041	5082-2711
5082-2273	5082-2712
5082-2274	5082-2713
5082-2295	5082-2714
5082-2296	5082-2723
5082-2297	5082-2724
5082-2298	HSCH-3206
5082-2701	HSCH-3207



Mean Time to Failure vs. Junction Temperature

Burn-In and Storage

Test	Test Conditions[1]	LTPD per 1000 Hours
High Temperature Life	Storage at 125°C	3.0
Steady State Operating Life	P_{FM} = 75 mW V_{RM} = 80% of V_{BR} T_A = 25°C f = 60 Hz	4.0

Note:
1. 1000 hours minimum on all life tests.

Environmental

Test	MIL-STD-750	Test Conditions	LTPD
Temperature Cycling	1051C	10 cycles from -65°C to 125°C, 5 hrs. at extremes, 5 min. transfer	10
Thermal Shock	1056	10 cycles from 0°C to 100°C. 3 sec. transfer	10
Mechanical Shock	2016	5 blows each at X_1, X_2, Y, 1500 G, 0.5 msec. pulse	10
Vibration Fatigue	2046	20 G min., 60 Hz	10
Vibration Variable Frequency	2056	four 4 min. cycles each X, Y, Z at 20 G min., 100 to 2000 Hz	10
Constant Acceleration	2006	20 KG, 1 minute per axis	10
Moisture Resistance	1021	240 hours, 90-98% relative humidity	10
Salt Atmosphere	1041	35°C fog for 24 hours	12

HEWLETT PACKARD

Mesh Schottky Diodes

Reliability Data

Description

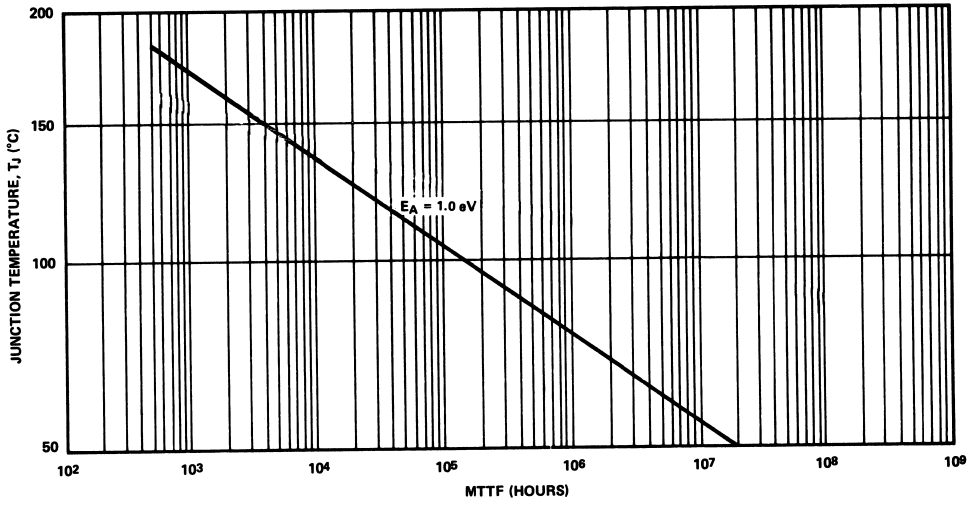
For applications requiring component reliability estimation, Hewlett-Packard provides reliability data for all families of devices. Data is compiled from reliability tests run to demonstrate that a product meets the design criteria. Periodically, additional tests are run. The data on this sheet represents the latest review of accumulated test results. All data recorded here is for mesh Schottky diodes mounted in hermetically sealed glass packages.

Applications

This information represents the capabilities of the generic device. Failure rate and MTTF values presented here are achievable with normal MIL-S-19500 test screening. Reliability can be guaranteed only under specified conditions and LTPD levels.

Applicable Part Numbers

5082-2301	5082-2401
5082-2302	5082-2520
5082-2303	5082-2521
5082-2306	5082-2565
5082-2308	5082-2566
5082-2350	5082-2900
5082-2351	5082-2912
5082-2356	5082-2970
5082-2370	5082-2997
5082-2396	HSCH-3486
5082-2400	



Mean Time to Failure vs. Junction Temperature

Burn-In and Storage

Test	Test Conditions[1]	LTPD per 1000 Hours
High Temperature Life	Storage at 100°C	2.0
Steady State Operating Life	P_{FM} = 125 mW V_{RM} = 80% of V_{BR} T_A = 25°C f = 60 Hz	2.0
High Temperature Reverse Bias	V_R = 80% of V_{BR} T_A = 100°C	8.0

Note:
1. 1000 hours minimum on all life tests.

Environmental

Test	MIL-STD-750	Test Conditions	LTPD
Temperature Cycling	1051C	10 cycles from -65°C to 100°C, 5 hrs. at extremes, 5 min. transfer	10
Thermal Shock	1056	10 cycles from 0°C to 100°C, 3 sec. transfer	10
Mechanical Shock	2016	5 blows each at X_1, X_2, Y, 1500 G, 0.5 msec. pulse	10
Vibration Variable Frequency	2056	four 4 min. cycles each X, Y, Z at 20 G min, 100 to 2000 Hz	10
Moisture Resistance	1021	240 hours, 90-98% relative humidity	10
Terminal Strength	2036	Condition A	10
Solderability	2026	Sn 95, Pb 5, 260°C	10

PIN Diodes



Characteristics of PIN Diodes

The most important feature of the PIN diode is its basic property of being an almost pure resistor at RF frequencies, whose resistance value can be varied from approximately 10,000 Ω to less than 1 Ω by the control current flowing through it. Most diodes exhibit this characteristic to some degree, but the PIN diode is optimized in design to achieve a relatively wide resistance range, good linearity, low distortion, and low current drive. The characteristics of the PIN diode make it suitable for use in switches, attenuators, modulators, limiters, phase shifters, and other signal control circuits.

Device Characteristics

The principal parameters of a PIN diode which play major roles in determining the performance of a circuit include the following:

RF Resistance

The PIN diode structure consists of an I (Intrinsic) layer of very high resistivity material sandwiched between regions of highly doped P (positively charged) material and N (negatively charged) material. With reverse or zero bias, the I-layer is depleted of charges and the PIN diode exhibits very high resistance. When forward bias is applied across the PIN diode, positive charge from the P region and negative charge from the N region are injected into the I-layer, therefore increasing its conductivity and lowering its resistance. The high off resistance and low on resistance make the PIN diode attractive for switching applications.

At RF frequencies, the PIN diode with forward bias behaves essentially as a pure resistor. The resistance of the PIN diode is related to the bias current, the geometry of the I-layer and the properties of the carriers. For a given type of PIN diode with uniform characteristics, resistance is inversely proportional to the forward bias current. Whereas, only high off resistance and low on resistance are important in switching applications, the resistance characteristics in the entire dynamic range are of concern in attenuator applications. Linearity of resistance with bias makes the PIN diode useful for attenuator applications.

Carrier Lifetime

An important parameter of the PIN diode is the carrier lifetime, τ, which is useful for defining the low frequency limit, $f_o = 1/2\pi\tau$, for linear performance of the diode. For RF signal frequencies below f_o, the PIN diode rectifies the signal much like an ordinary PN junction diode, and considerable output distortion results. (See Application Note 957-3 for additional discussion on rectification causes and effects). At frequencies above f_o, less rectification occurs with increasing frequency, allowing the PIN diode to appear more linear, approaching a pure resistor.

For applications requiring good linearity and low distortion the minimum signal frequency should be ten times f_o, i.e., $f_{min} = 10/2\pi\tau, = 1.6/\tau$. This restriction is not important in switching applications, where the diode is normally biased either completely OFF or ON. In those states, since most of the power is either reflected or transmitted, the effect of RF current on the total charge is small and distortion is not a problem.

Capacitance

Diode capacitance limits switch and attenuator performance at high frequencies in the form of isolation rolloff and increased insertion loss. Optimum performance can be achieved by one of several alternatives available. Using a low capacitance diode would be one solution. Since the junction capacitance of a PIN diode is related to the geometry and electrical properties of the I-layer similar to the case of RF resistance, an R-C trade-off may be feasible. Special techniques can be employed to minimize capacitive (and other parasitic) effects, and in some cases even to take advantage of them. (Some of the techniques for improving high frequency performance are discussed in Application Notes 922 and 957-2.)

Reverse Recovery Time

Reverse recovery time is a measure of switching time, and is dependent on the forward and reverse bias applied. With forward bias current, charge is stored in the I-layer. When a reverse pulse is applied, reverse current will flow for a short period of time, known as delay time, t_d. When a sufficient number of carriers have been removed, the current begins to decrease. The time required for the reverse current to decrease from 90% to 10% is called the transition time, t_t. The sum, $t_d + t_t$, is the reverse recovery time, which is a measure of the

time it takes to switch the diode from ON to OFF.

Reverse Breakdown Voltage

The reverse breakdown voltage defines the maximum signal level which may be applied to the diode. Operation at signal levels above the reverse breakdown voltage may result in degradation of diode characteristics or in permanent damage to the diode.

Applications of PIN Diodes

PIN diodes are used principally for the control of RF and microwave signals. Applications include switching, attenuating, modulating, limiting and phase shifting. Certain diode requirements are common to all these control functions, while others are more important in a particular type of usage.

Switching Applications

The performance of a PIN diode circuit is directly related to the basic characteristics of the diode. As an illustrative example, the performance of a PIN diode switch can be simply approximated by treating the PIN diode essentially as a resistor in the forward biased state and a capacitor in the reverse biased state. Switch performance can then be analyzed as follows:

Insertion Loss

The loss of signal attributed to the diode when the switch is on (transmission state) is insertion loss. For low insertion loss, low resistance is needed in a series switch (Figure 1). Low capacitance (particularly at high frequencies) is needed in a shunt switch (Figure 2).

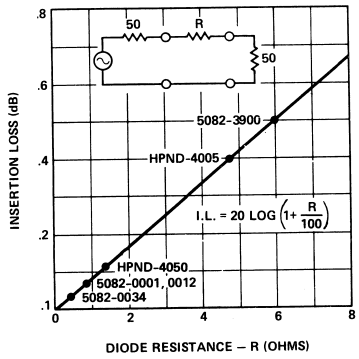


Figure 1. Typical Insertion Loss of Series Diode Switch.

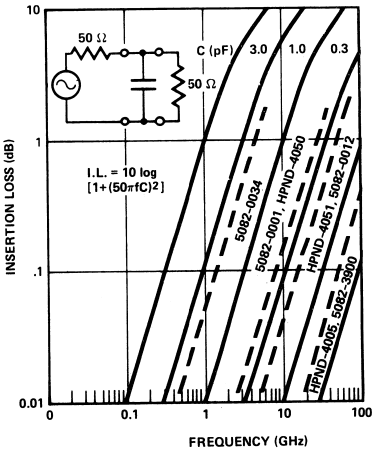


Figure 2. Typical Insertion Loss of Shunt Diode Switch.

Isolation

Isolation is the measure of RF leakage between the input and output when the switch is off. For high isolation (low transmission) low capacitance is required in a series switch especially at high frequencies (Figure 3). Low resistance is required in a shunt switch (Figure 4).

Switching Speed

In many applications, switching time is very important. Reverse

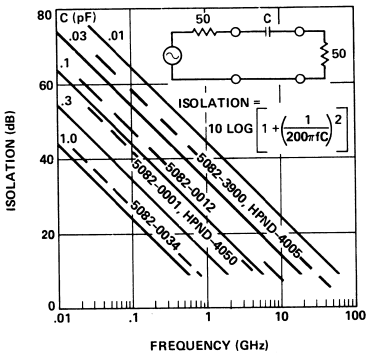


Figure 3. Typical Isolation of Series Diode Switch.

recovery time is a measure of the switching time of a PIN diode, the time required to switch the diode from ON to OFF. The time needed to switch the diode from OFF to ON is shorter. (See Application Note 929 for details.)

Power Handling Capability

The RF power (CW or pulse) that can be handled safely by a diode switch is limited by two factors – the breakdown voltage of the diode, and thermal considerations, which involve the maximum junction temperature and the thermal resistance of the diode and packaging. Other factors affecting power handling capability are ambient temperatures, frequency, attenuation level (which is related to diode resistance), pulse width and duty cycle. (See Application Note 922 for details.)

Attenuators

Whereas a switch is used only in its maximum ON or OFF state, an attenuator is operated throughout its dynamic range (or resistance range in the case of a diode attenuator). Although a single diode series or shunt switch can be used as an attenuator, it cannot offer in its entire

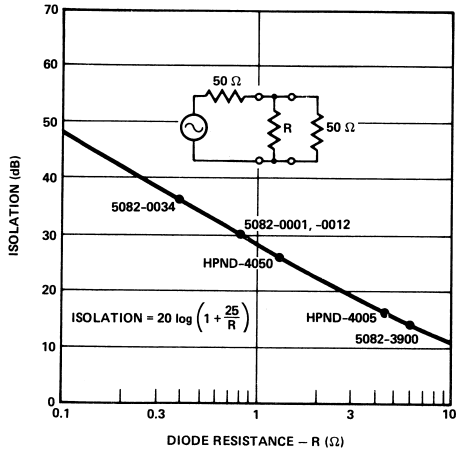


Figure 4. Typical Isolation of Shunt Diode Switch.

dynamic range constant input and output impedance, which is required for optimum source and load matching in most attenuator applications. By using a multiple diode circuit such as a π, T, or bridged-T attenuator, constant input and output impedance can be achieved throughout the attenuation range.

An additional requirement in most attenuator applications is low distortion. Distortion can be kept at a minimum, if the carrier lifetime of the PIN diode used is greater than the inverse of the signal frequency, preferably $\tau > 1.6/f$, where τ is the carrier lifetime and f is the signal frequency.

Limiters

Sensitive amplifiers, mixers, and detectors in microwave systems can be protected against damage by high level signals with the use of a PIN diode limiter shunting the transmission line.

A PIN diode limiter is essentially an attenuator that uses self bias rather than externally applied bias. As the RF input increases the rectified current generated by the PIN diode (in some limiter circuits by an auxiliary Schottky diode) biases the diode to a low resistance state. Most of the input power is then attenuated, allowing very little to be transmitted. The sensitive equipment that follows is thus protected.

For a limiter circuit to be efficient, it is essential that the PIN diode has fast switching time. Without an auxiliary diode, a PIN diode with good rectification efficiency is needed to achieve low resistance. Another diode requirement is good heat transfer characteristics (low thermal resistance).

Phase Shifters

The high speed switching capabilities and low ON and high OFF resistance states of the PIN diode make it also very useful for many types of high speed, current controlled phase shifter applications. Another important requirement for these application is the uniformity of diode characteristics such as capacitance and resistance, particularly in systems where a large number of elements are involved.

Pin Diode Selection Guide

Hewlett-Packard PIN diodes are available in chip form and several types of packages, which lend themselves more suitable for particular applications.

For switching, attenuating, and other general purpose applications particularly in the VHF/UHF range, the low cost glass package (Outline 15) and new surface mount, SOT-23 package are suitable. Due to their low parasitics, ceramic packages (Outlines 31 and 38) are suited for broadband circuits up to 1 GHz and for resonated narrowband circuits up to 8 GHz. In addition, they have medium power handling capability.

Stripline Packages (Outlines 60 and 61) containing built-in low pass matching circuits, can be used in broadband designs up to 10 GHz for Outline 60, and 18 GHz for Outline 61. Because of good heat sinking, they can handle high power in switching, attenuating and limiting applications.

The beam lead devices with low parastics are designed for use in stripline or microstrip circuits using welding or thermocompression bonding techniques.

Surface Mount PIN Diodes

Available Configurations

DIE	APPLICATION	GLASS	SOT-23						
			SINGLE	SINGLE	SERIES	COMMON ANODE	COMMON CATHODE	LOW INDUCTANCE	LOW INDUCTANCE
HPND-0001	Attenuator 50 Ω	5082-3080	HSMP-3800 D0	HSMP-3801 D1	HSMP-3802 D2	NOT AVAILABLE	HSMP-3804 D4	–	–
HPND-0002	Attenuator 75 Ω	5082-3081	HSMP-3810 E0	HSMP-3811 E1	HSMP-3812 E2	HSMP-3813 E3	HSMP-3814 E4	–	HSMP-4810 EB
HPND-0003	Switch	5082-3188	HSMP-3820 F0	HSMP-3821 F1	HSMP-3822 F2	HSMP-3823 F3	HSMP-3824 F4	HSMP-4820 FA	–
5082-0012	General Purpose	5082-3077	HSMP-3830 K0	HSMP-3831 K1	HSMP-3832 K2	HSMP-3833 K3	HSMP-3834 K4	–	–
	Switch Low Distortion		HSMP-3880 S0	HSMP-3881 S1				–	–
	Switch Low Capacitance		HSMP-3890 G0	HSMP-3891 G1	HSMP-3892 G2	HSMP-3883 G3	HSMP-3894 G4	HSMP-4890 GA	–

Note: SOT-23 available in both standard and low profile. Low profile denoted in package marking code with suffix "L". For example, "A0" – standard profile; "A0L" – low profile.

RF PIN Diodes

Part Number	C_T Max. (pF)	R_S Max. at 100 mA (Ω)	V_{BR} Min. (V)	t_{rr} Typ. (ns)	Lifetime τ Typ. (ns)[a]	Package	Page
5082-3002	0.25	1	300	100	100	glass axial lead	4-37
5082-3001†	0.25	1	200	100	100	glass axial lead	4-37
5082-3039	0.25	1.25	150	100	100	glass axial lead	4-37
JAN/TX/1N5719	0.3	1.25	150	100	100	glass axial lead	4-37
5082-3077	0.3	1.5	200	100	100	glass axial lead	4-37
5082-3188	1	0.6*	35	12	70***	glass axial lead	4-37
5082-3168†	2	0.5*	35	12	70***	glass axial lead	4-37
5082-3080†	0.4	2.5	100		1300	glass axial lead	4-37
1N5767	0.4	2.5	100		1000	glass axial lead	4-37
5082-3379	0.4		50		1300	glass axial lead	4-37
5082-3081†	0.4	3.5	100		2500	glass axial lead	4-37
HSMP-3800	0.35	2.5	100	500	1800	SOT-23, single	4-25
HSMP-3801	0.35	2.5	100	500	1800	SOT-23, single	4-25
HSMP-3802	0.35	2.5	100	500	1800	SOT-23, series	4-25
HSMP-3804	0.35	2.5	100	500	1800	SOT-23, common cathode	4-25
HSMP-3810	0.35	4.0	100	300	1500	SOT-23, single	4-25
HSMP-3811	0.35	4.0	100	300	1500	SOT-23, single	4-25
HSMP-3812	0.35	4.0	100	300	1500	SOT-23, series	4-25
HSMP-3813	0.35	4.0	100	300	1500	SOT-23, common anode	4-25
HSMP-3814	0.35	4.0	100	300	1500	SOT-23, common cathode	4-25
HSMP-3820	1.0	0.6*	35	7	70***	SOT-23, single	4-25
HSMP-3821	1.0	0.6*	35	7	70***	SOT-23, single	4-25
HSMP-3822	1.0	0.6*	35	7	70***	SOT-23, series	4-25
HSMP-3823	1.0	0.6*	35	7	70***	SOT-23, common anode	4-25
HSMP-3824	1.0	0.6*	35	7	70***	SOT-23, common cathode	4-25
HSMP-3830	0.3	1.5	200	80	500	SOT-23, single	4-25
HSMP-3831	0.3	1.5	200	80	500	SOT-23, single	4-25
HSMP-3832	0.3	1.5	200	80	500	SOT-23, series	4-25
HSMP-3833	0.3	1.5	200	80	500	SOT-23, common anode	4-25
HSMP-3834	0.3	1.5	200	80	500	SOT-23, common cathode	4-25
HSMP-3880	0.4	6.5**	100	550	2500	SOT-23, single	4-25
HSMP-3881	0.4	6.5**	100	550	2500	SOT-23, single	4-25
HSMP-3890	0.3	2.5**	35	–	200***	SOT-23, single	4-25
HSMP-3891	0.3	2.5**	35	–	200***	SOT-23, single	4-25
HSMP-3892	0.3	2.5**	35	–	200***	SOT-23, series	4-25
HSMP-3893	0.3	2.5**	35	–	200***	SOT-23, common anode	4-25
HSMP-3894	0.3	2.5**	35	–	200***	SOT-23, common cathode	4-25
HPND-0001†	0.2	2	100	500	1800	chip	4-8
HPND-0002†	0.2	3.5	100	300	1500	chip	4-8
HPND-0003†	1	0.4*	35	7	70***	chip	4-8

*R_S Max. at 10 mA
**R_S Max. at 5 mA
***I_F = 10 mA, I_R = 6 mA.
†Standard Hi-Rel version available.
[a] Lifetime measured at I_F = 50 mA, I_R = 250 mA.
For reliability data see pages 4-60 – 4-68.

Microwave PIN Diodes

Silicon PIN Diodes

Part Number	C_T Typ. (pF)	R_S Typ. (Ω)	V_{BR} Min. (V)	t_{rr} Min. (ns)	Lifetime, τ Typ. (ns)	Package	Page
5082-0001**	0.10	0.8	705	5	35**	chip	4-10
5082-0047	0.10	0.6	150	100	400	chip	4-10
HPND-4050**	0.12	1.3	40	2	25**	beam lead	4-20
HPND-4018**	0.22	4.3	60	2	26**	beam lead	4-14
5082-3900	0.02	6.0	200		150	beam lead	4-22
5082-3305	0.40	1.0	70	5	35	38	4-57
5082-3306	0.45	1.0	70	5	35	31	4-57
HPND-4005**	0.02	4.7	120		400***	beam lead	4-12
5082-0012**	0.10	1.0	150	100	400	chip	4-10
5082-0030***	0.10	1.0	150	100	400	chip	4-10
5082-3101	0.32	2.0	200	100	400	*38	4-49
5082-3102	0.30	1.0	300	100	400	*38	4-49
5082-3201	0.35	1.0	200	100	400	*31	4-49
5082-3202	0.32	1.0	300	100	400	*31	4-49
5082-3203	0.40	1.0	200	100	400	31	4-49
5082-3204	0.32	1.0	250	100	400	31	4-49
HPND-4028**	0.04	2.6	60	2.6	37***	beam lead	4-14
HPND-4038**	0.06	1.7	60	2.4	45***	beam lead	4-14
5082-3042**	0.40	1.0	70	5 (max)	35	15	4-37
5082-3043	0.40	1.5	50	10 (max)	35	15	4-37
HSMP-4810	0.30	4.0	100	300	1500	SOT-23	4-25
HSMP-4820	1.0	1.0**	35	7	70***	SOT-23	4-25
HSMP-4890	0.35	2.5**	35	–	200***	SOT-23	4-25

Silicon Stripline PIN Diodes

Part Number	Isolation Min. (dB)	Insertion Loss Max. (dB)	SWR Max.	Lifetime, τ Typ. (ns)	Package	Page
5082-3140	20	0.5	1.5	400	60*	4-52
5082-3141†	20	1.0	1.5	35	60	4-52
5082-3170†	20	0.5	1.5	400	60	4-52
5082-3040	20	0.5	1.5	400	61*	4-44
5082-3041	20	1.0	1.5	35	61	4-44
5082-3340	20	0.5	1.5	400	61	4-44
5082-3071		1.2	2		61	4-42

*Denotes anode heat sink; all other parts are cathode heat sink.
**R_S Max. at 5 mA.
***I_F = 10 mA, I_R = 6 mA.
†Standard Hi-Rel version available.
For reliability data see pages 4-60 – 4-68.

HEWLETT PACKARD

Small Signal RF PIN Diode Chips for Hybrid Integrated Circuits

Technical Data

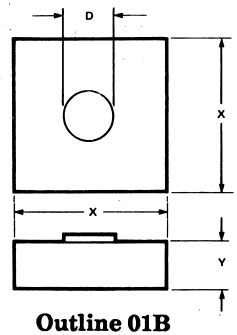
HPND-0001
HPND-0002
HPND-0003

Features

- **Thermocompression/ Thermosonically Bondable**
- **Ideal for Hybrid Integrated Circuits**
- **Gold Metallization**
- **Silicon Nitride Passivation**
- **Uniform Electrical Characteristics**
- **Batch Matched Versions Available**
- **Planar Construction**

Description

These PIN/NIP diode chips are specifically designed for hybrid applications requiring thermosonic or thermocompression bonding techniques. The top metallization is a layer of gold for a tarnish free surface that allows either thermosonic or thermocompression bonding techniques. The bottom metallization is also gold, suitable for epoxy or eutectic die attach method.



Outline 01B
Chip Dimensions

DIMENSIONS	FOR EPOXY OR EUTECTIC DIE ATTACH PART NO. HPND-		
	-0001	-0002	-0003
D (0.03) (1)	0.25 (10)	0.20 (8)	0.10 (4)
X (0.05) (2)	0.51 (20)	0.38 (15)	0.30 (12)
Y (0.03) (1)	0.15 (6)	0.15 (6)	0.13 (5)
TOP CONTACT	CATHODE	CATHODE	ANODE
BOTTOM CONTACT	ANODE	ANODE	CATHODE

DIMENSIONS IN MILLIMETERS (1/1000 INCH).

Applications

These small signal, general purpose PIN/NIP diode chips are optimized for various analog and digital applications such as switches, digital phase shifters, pulse and amplitude modulators, limiters, leveling, and attenuating.

Maximum Ratings

Junction Operating and Storage Temperature Range ..... -65°C to +150°C

T_A = 25°C

P_D Power Dissipation ..... 250 mW
(Measured in an infinite heat sink derated linearly to zero at 150°C.)

Operation in excess of any one of these conditions may result in permanent damage to this device.

Electrical Specifications at T_A = 25°C

Chip for Epoxy or Eutectic Die Attach HPND-	Nearest Equivalent Surface Mount Part No. HSMP-	Nearest Equivalent Axial Lead Part No. 5082-	Minimum Breakdown Voltage V_{BR} (V)	Maximum Capacitance C_j (pF)	Typical Parameters		
					Series Resistance R_S (Ω)	Typical Carrier Lifetime τ (ns)	Typical Reverse Recovery Time t_{rr} (ns)
0001	3800	3080	100	0.20	2.0	1800	500
0002	3810	3081	100	0.20	3.5	1500	300
0003	3820	3188	35	1.0*	0.4*	70*	7
Test Conditions			$V_R = V_{BR}$ Measure $I_R \leq 10$ μA	V_R = 50 V *V_R = 20 V f = 1.0 MHz	I_F = 100 mA *I_F = 10 mA	I_F = 50 mA I_R = 250 mA *I_F = 10 mA *I_R = 6 mA	I_F = 20 mA V_R = 10 V 90% Recovery

Assembly and Handling Procedures for PIN Chips

1. Storage

Devices should be stored in a dry nitrogen purged dessicator or equivalent.

2. Cleaning

If required, surface contamination may be removed with electronic grade solvents such as freon (T.F. or T.M.C.), acetone, deionized water, and methanol used singularly or in combinations. Typical cleaning times per solvent are one to three minutes. DI water and methanol should be used (in that order) in the final cleans. Final drying can be accomplished by placing the cleaned dice on clean filter paper and drying with an infrared lamp for 5-10 minutes. Acids such as hydrofluoric (HF), nitric (HNO_3), and hydrochloric (HCl) should not be used.

The effects of cleaning methods/solutions should be verified on small samples prior to submitting the entire lot.

Following cleaning, dice should be either used in assembly (typically within a few hours) or stored in clean containers in a reducing atmosphere or a vacuum chamber.

3. Die Attach

a. Eutectic

Eutectic die attach can be accomplished by "scrubbing" the die with/without a preform on the header to combine with the silicon in the die. Temperature is approximately 400°C, with heating times of 5-10 seconds. (Note–times and temperature utilized may vary depending on the type, composition, and heat capacity of the header or substrate used.) This method is recommended for the HPND-000X series.

b. Epoxy

For epoxy die-attach, conductive silver-filled epoxies are recommended. This method can be used for all Hewlett-Packard PIN chips.

4. Wire Bonding

Either ultrasonic, thermosonic or thermocompression bonding techniques can be employed. Suggested wire is pure gold, 0.7 to 1.5 mil diameter.

HEWLETT PACKARD

PIN Diode Chips for Hybrid MIC Switches/Attenuators

Technical Data

5082-0001
5082-0012
5082-0030
5082-0047

Features

- **Low Series Resistance**
  0.8 Ω Typical
- **Nitride Passivated**

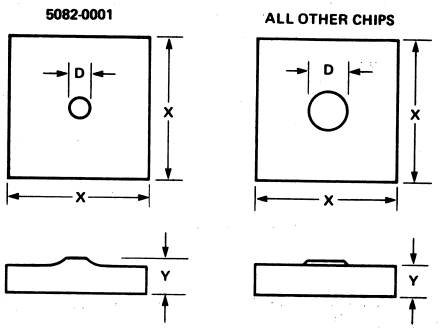
Description

These PIN diode chips are silicon dioxide or nitride passivated. The 5082-0001 has a mesa construction and the 5082-0012, -0030, and -0047 have a pitted planar construction that includes a pit etched into the backside of the chip. The fabrication processes are optimized for long term reliability and tightly controlled for uniformity in electrical performance.

Applications

These general purpose PIN diodes are intended for low power switching applications such as duplexers, antenna switching matrices, digital phase shifters, time multiplex filters, TR switches, pulse and amplitude modulators, limiters, leveling circuits, and attenuators.

The 5082-0001 is optimized for applications requiring fast switching.



Outline 01B

Dimension	HP Part Number 5082-		
	0012 0047	0030	0001
D ±0.03 (1)	0.10 (4)	0.13 (5)	0.06 (2.5)
X ±0.05 (2)	0.38 (15)		
Y ±0.03 (1)	0.10 (4.0)		0.11 (4.5)
Top Contact	Au. Cathode	Au. Anode	
Bottom Contact	Au. Anode	Au. Cathode	

Dimensions in millimeters (1/1000 inch)

Maximum Ratings

Junction Operating and Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature
5082-0001 ..... +300°C for 1 min. max.
5082-0012, -0030, -0047 ..... +425°C for 1 min. max.

Electrical Specifications at $T_A = 25°C$

Typical Parameters

Chip Part Number 5082-	Nearest Equivalent Packaged Part No. 5082-	Minimum Breakdown Voltage V_{BR} (V)	Maximum Junction Capacitance C_j (pF)	Typical Series Resistance R_S (Ω)	Typical Lifetime τ (ns)	Typical Reverse Recovery Time t_{rr} (ns)
0001	3041	70	0.16*	0.8*	35*	5
0012	3001	150	0.12	1.0	400	100
0030	3303	150	0.12	1.0	400	100
0047		150	0.15	0.6	400	100
Test Conditions		$V_R = V_{BR}$ Measure $I_R \leq 10\ \mu A$	$V_R = 50$ V *$V_R = 20$ V f = 1 MHz	$I_F = 100$ mA *$I_F = 20$ mA f = 100 MHz	$I_F = 50$ mA $I_R = 250$ mA *$I_R = 6$ mA *$I_F = 10$ mA	$I_F = 20$ mA $V_R = 10$ V 90% Recovery

Assembly and Handling Procedures for PIN Chips

1. Storage

Devices should be stored in a dry nitrogen purged dessicator or equivalent.

2. Cleaning

If required, surface contamination may be removed with electronic grade solvents such as freon (T.F. or T.M.C.), acetone, deionized water, and methanol used singularly or in combinations. Typical cleaning times per solvent are one to three minutes. DI water and methanol should be used (in that order) in the final cleans. Final drying can be accomplished by placing the cleaned dice on clean filter paper and drying with an infrared lamp for 5-10 minutes. Acids such as hydrofluoric (HF), nitric (HNO_3) and hydrochloric (HCl) should not be used.

The effects of cleaning methods/solutions should be verified on small samples prior to submitting the entire lot.

Following cleaning, dice should be either used in assembly (typically within a few hours) or stored in clean containers in a reducing atmosphere or a vacuum chamber.

3. Die Attach

a. Eutectic

5082-0001
AuSn preform with stage temperature of 300°C for one minute max.

5082-0012, 5082-0030, and 5082-0047
AuSn preform with stage temperature of 310°C for one minute max. AuGe preform with stage temperature of 390°C for one minute max.

b. Epoxy

For epoxy die-attach, conductive silver-filled or gold-filled epoxies are recommended. This method can be used for all Hewlett-Packard PIN chips.

4. Wire Bonding

Either ultrasonic, or thermocompression bonding techniques can be employed. Suggested wire is pure gold, 0.7 to 1.5 mil diameter. Ultrasonic bonding method should be avoided for the 5082-0001 diode chip.

HEWLETT PACKARD

Beam Lead PIN Diode

Technical Data

HPND-4005

Features

- **High Breakdown Voltage**
  120 V Typical
- **Low Capacitance**
  0.017 pF Typical
- **Low Resistance**
  4.7 Ω Typical
- **Rugged Construction**
  4 Grams Minimum Lead Pull
- **Nitride Passivated**

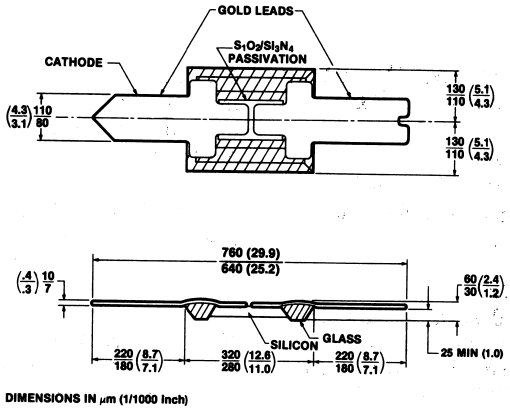
Description

The HPND-4005 planar beam lead PIN diode is constructed to offer exceptional lead strength while achieving excellent electrical performance at high frequencies. High beam strength offers users superior assembly yield, while extremely low capacitance allows high isolation to be realized.

Nitride passivation and polyimide coating provide reliable device protection.

Applications

The HPND-4005 beam lead PIN diode is designed for use in stripline or microstrip circuits. Applications include switching, attenuating, phase shifting, limiting, and modulating at microwave frequencies. The extremely low capacitance of the HPND-4005 makes it ideal for circuits requiring high isolation in a series diode configuration.



Outline 21

Maximum Ratings

Operating Temperature ..... -65°C to +175°C
Storage Temperature ..... -65°C to +200°C
Power Dissipation at T_{CASE} = 25°C ..... 250 mW
(Derate linearly to zero at 175°C.)
Minimum Lead Strength ..... 4 grams pull on either lead
Diode Mounting Temperature ..... 220°C for 10 sec. max.

Bonding and Handling Procedures

See page 4-24.

Electrical Specifications at $T_A = 25°C$

Part Number HPND-	Breakdown Voltage V_{BR} (V)		Series Resistance R_S (Ω)[2]		Capacitance C_T (pF)[1,2]		Forward Voltage V_F (V)	Reverse Current I_R (nA)	Minority Carrier Lifetime τ (ns)[2]	
	Min.	Typ.	Typ.	Max.	Typ.	Max.	Max.	Max.	Min.	Typ.
4005	100	120	4.7	6.5	0.017	0.02	1.0	100	50	100
Test Conditions	I_R = 10 μA		I_F = 20 mA I_F = 100 MHz		V_R = 10 V f = 10 GHz		I_F = 20 mA	V_R = 30 V	I_F = 10 mA I_R = 6 mA	

Notes:
1. Total capacitance calculated from measured isolation value in a series configuration.
2. Test performed on packaged samples.

Typical Parameters

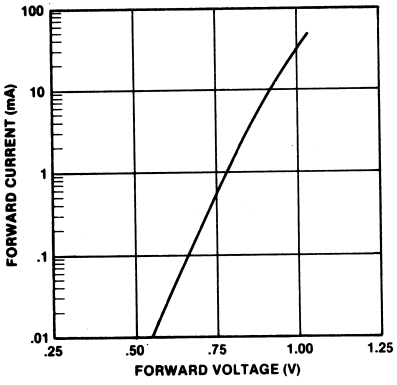


Figure 1. Typical Forward Conduction Characteristics.

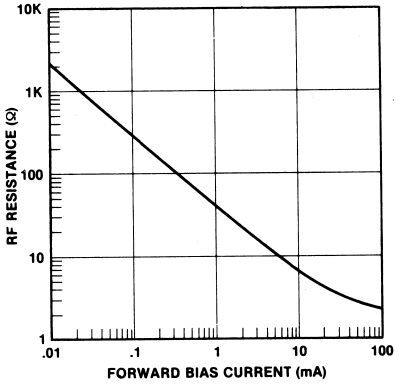


Figure 2. Typical RF Resistance vs. Forward Bias Current.

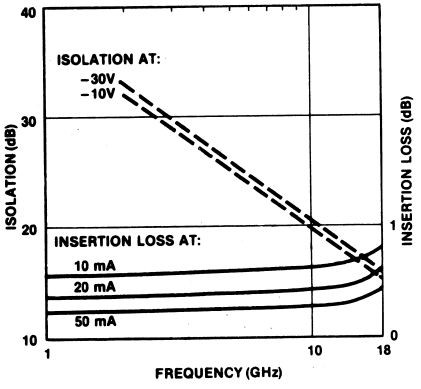


Figure 3. Typical Isolation and Insertion Loss in the Series Configuration (Z_o = 50 Ω).

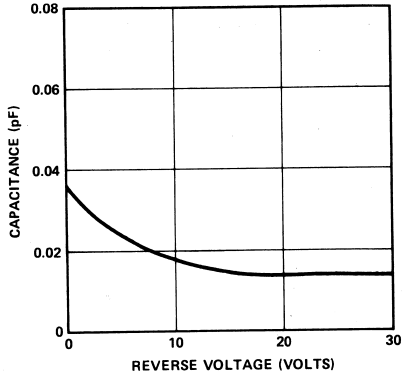


Figure 4. Typical Capacitance at 10 GHz vs. Reverse Bias.

HEWLETT PACKARD

Beam Lead PIN Diodes for Phased Arrays and Switches

Technical Data

HPND-4018
HPND-4028
HPND-4038

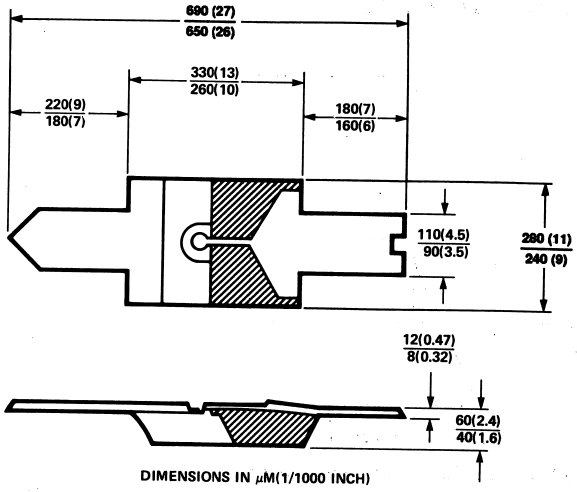
Features

- **Low Capacitance**
  0.025 pF Maximum at 1 MHz
  Guaranteed Min./Max.
- **Fast Switching**
  2.0 nsec
- **Low Resistance at Low Bias**
  1.5 Ω at I_F = 10 mA
- **Rugged Construction**
  Typical 10 Gram Lead Pull
- **Silicon Nitride Passivation**

Description

The HPND-4018, 4028, and 4038 beam lead PIN diodes are designed for low capacitance, low resistance, and fast switching at microwave frequencies. These characteristics are achieved at low bias levels for minimal power consumption. Advanced processing techniques ensure uniform and consistent electrical performance, allowing guaranteed capacitance windows. This translates to improved performance in phased array applications.

Rugged construction and strong beams ensure high assembly yields while nitride passivation and polyimide coating ensure reliability. Standard Hi-Rel programs are available for all three devices.



Outline 83

Maximum Ratings

Operating Temperature ..... -65°C to +150°C
Storage Temperature ..... -65°C to +200°C
Power Dissipation at T_{CASE} = 25°C ..... 250 mW
(Derate linearly to zero at 150°C.)
Minimum Lead Strength ..... 4 grams pull on either lead per MIL-S-19500, LTPD = 20

Applications

These beam lead PIN diodes are designed for use in stripline, coplanar waveguide, or microstrip circuits. Applications include phase shifting and switching. The guaranteed capacitance windows ensure uniform performance in phased array radar. The low capacitance makes them ideal for circuits requiring high isolation in the series configuration. These devices have been fully characterized and S-parameters have been provided.

Bonding and Handling Procedures

See page 4-24.

Electrical Specifications at $T_A = 25°C$

Part Number HPND-	Capacitance (pF)		Series Resistance R_S (Ω)		Break-down Voltage V_{BR} (V)	Reverse Current I_R (nA)	Forward Voltage V_F (V)	Carrier Lifetime τ (ns)	Reverse Recovery t_{rr} (ns)	Series Resistance R_S (Ω)
	Min.	Max.	Typ.	Max.	Min.	Max.	Max.	Typ.	Typ.	Typ.
4018	0.015	0.025	4.0	4.6	60	100	1.1	26	2.0*	2.5
4028	0.025	0.045	2.3	3.0	60	100	1.1	36	2.6	2.0
4038	0.045	0.065	1.5	2.0	60	100	1.1	45	2.4	1.0
Test Conditions	V_R = 30 V f = 1 MHz		I_F = 10 mA f = 100 MHz		$V_R = V_{BR}$ Measure $I_R \leq 10$ μA	V_R = 50 V	I_F = 20 mA	I_F = 10 mA I_R = 6 mA	*I_F = 10 mA I_F = 5 mA V_R = 10 V 90% recovery	I_F = 50 mA f = 100 MHz

Typical Parameters

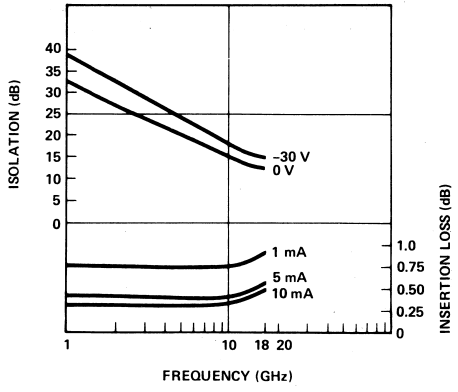


Figure 1. Typical Isolation and Insertion Loss. HPND-4018.

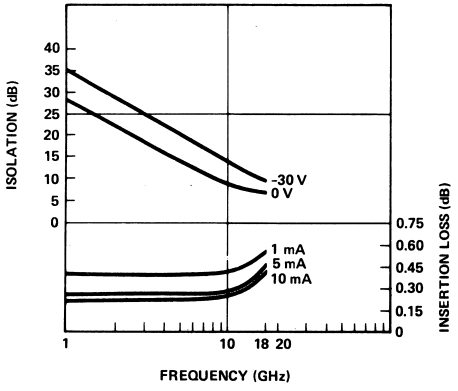


Figure 2. Typical Isolation and Insertion Loss. HPND-4028.

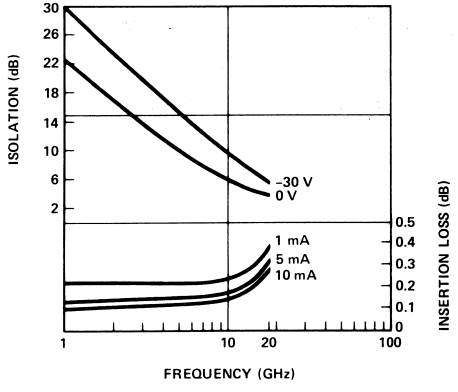


Figure 3. Typical Isolation and Insertion Loss. HPND-4038.

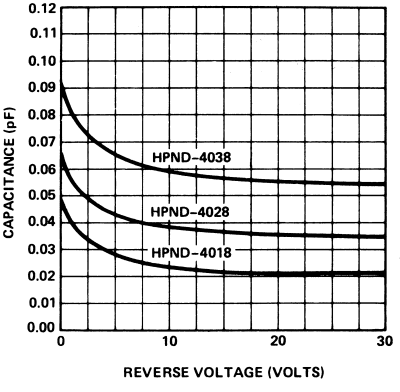


Figure 4. Typical Capacitance vs. Reverse Voltage (at 1 MHz).

Typical Parameters (cont.)

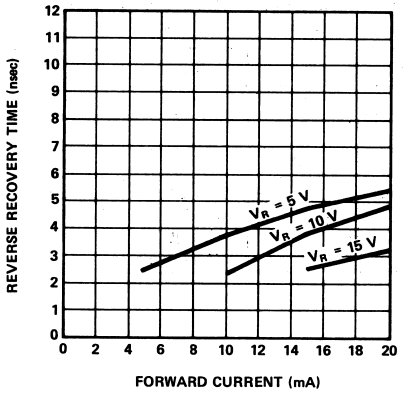


Figure 5. Typical Reverse Recovery Time vs. Forward Current (Series Configuration). HPND-4018.

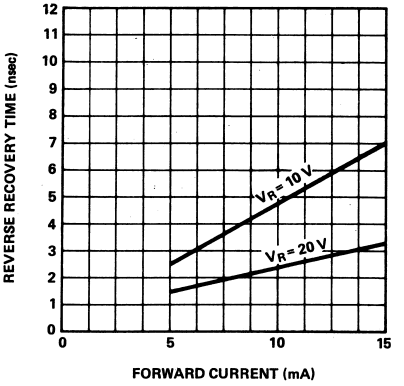


Figure 6. Typical Reverse Recovery Time vs. Forward Current (Series Configuration). HPND-4028, HPND-4038.

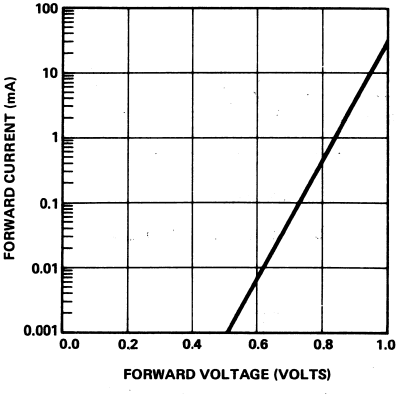


Figure 7. Typical Forward Characteristics.

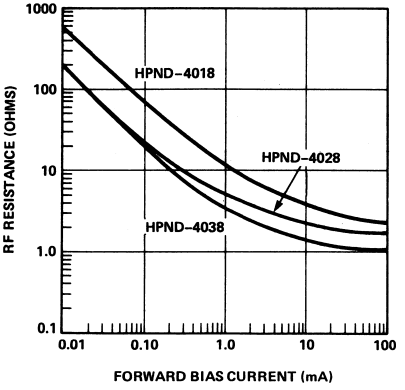


Figure 8. Typical RF Resistance vs. Forward Bias Current (at 100 MHz).

Typical S-Parameters (in series configuration)

HPND-4018

Freq. (MHz)	I_F = 1 mA					I_F = 5 mA					I_F = 10 mA				
	S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}		
	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.
1000	0.086	-1	-0.76	0.917	-1	0.046	8	-0.38	0.958	-1	0.037	11	-0.30	0.967	-1
2000	0.085	5	-0.76	0.917	-2	0.047	17	-0.40	0.957	-2	0.040	23	-0.32	0.965	-2
3000	0.085	10	-0.76	0.918	-4	0.051	25	-0.40	0.957	-4	0.043	32	-0.32	0.966	-4
4000	0.088	14	-0.74	0.919	-5	0.056	31	-0.40	0.957	-5	0.049	38	-0.32	0.966	-5
5000	0.090	18	-0.76	0.918	-6	0.060	36	-0.40	0.956	-6	0055	43	-0.32	0.965	-6
6000	0.093	20	-0.76	0.918	-7	0.066	39	-0.40	0.956	-7	0.061	46	-0.32	0.965	-7
7000	0.096	22	-0.76	0.918	-8	0.071	42	-0.40	0.957	-8	0.066	48	-0.32	0.965	-8
8000	0.100	24	-0.76	0.918	-10	0.076	43	-0.40	0.955	-10	0.072	50	-0.32	0.965	-10
9000	0.103	26	-0.76	0.918	-11	0.081	45	-0.40	0.955	-11	0.078	51	-0.32	0.965	-11
10000	0.106	27	-0.76	0.918	-12	0.086	46	-0.40	0.955	-12	0.083	51	-0.32	0.964	-12
11000	0.109	28	-0.74	0.919	-13	0.090	47	-0.40	0.956	-13	0.087	52	-0.32	0.965	-13
12000	0.114	28	-0.76	0.918	-14	0.096	46	-0.40	0.956	-14	0.093	52	-0.32	0.965	-15
13000	0.117	29	-0.76	0.917	-16	0.100	47	-0.40	0.956	-16	0.097	52	-0.32	0.965	-16
14000	0.121	30	-0.78	0.916	-17	0.105	48	-0.42	0.953	-17	0.103	53	-0.34	0.962	-17
15000	0.125	30	-0.80	0.913	-18	0.111	48	-0.42	0.953	-18	0.109	53	-0.34	0.963	-18
16000	0.129	31	-0.80	0.914	-19	0.116	49	-0.42	0.953	-19	0.114	53	-0.34	0.962	-19
17000	0.134	31	-0.80	0.914	-21	0.122	48	-0.44	0.952	-21	0.120	53	-0.36	0.961	-21
18000	0.140	32	-0.84	0.909	-22	0.130	49	-0.46	0.950	-22	0.129	53	-0.36	0.960	-22

HPND-4018

Freq. (MHz)	V_R = 0 V					V_R = 10 V					V_R = 30 V				
	S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}		
	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.
1000	0.995	-3	-33.16	0.022	84	0.999	-2	-39.18	0.011	93	1.000	-2	-39.18	0.011	93
2000	0.990	-5	-27.54	0.042	76	0.998	-4	-32.78	0.023	85	0.998	-4	-33.16	0.022	87
3000	0.983	-7	-24.30	0.061	71	0.996	-6	-29.12	0.035	83	0.997	-6	-29.64	0.033	84
4000	0.975	-10	-22.28	0.077	68	0.993	-8	-26.76	0.046	81	0.995	-8	-27.14	0.044	82
5000	0.967	-12	-20.74	0.092	64	0.991	-10	-24.90	0.057	78	0.992	-10	-25.36	0.054	79
6000	0.959	-14	-19.50	0.106	62	0.987	-12	-23.24	0.069	76	0.988	-12	-23.76	0.065	77
7000	0.950	-16	-18.42	0.120	59	0.982	-14	-21.84	0.081	73	0.985	-14	-22.28	0.077	74
8000	0.942	-18	-17.60	0.132	57	0.979	-16	-20.74	0.092	71	0.982	-16	-21.22	0.087	72
9000	0.933	-21	-16.84	0.144	54	0.972	-18	-19.84	0.102	68	0.975	-18	-20.28	0.097	69
10000	0.924	-23	-16.32	0.153	52	0.966	-20	-19.10	0.111	67	0.969	-20	-19.50	0.106	68
11000	0.915	-25	-15.56	0.167	49	0.959	-23	-18.14	0.124	63	0.960	-22	-18.58	0.118	64
12000	0.904	-27	-15.00	0.178	48	0.951	-25	-17.40	0.135	62	0.953	-24	-17.80	0.129	63
13000	0.896	-29	-14.66	0.185	45	0.944	-27	-16.96	0.142	59	0.946	-26	-17.34	0.136	60
14000	0.886	-31	-14.04	0.199	43	0.936	-29	-16.20	0.155	55	0.940	-29	-16.60	0.148	56
15000	0.876	-33	-13.86	0.203	41	0.925	-31	-15.92	0.160	53	0.929	-31	-16.26	0.154	54
16000	0.870	-35	-13.44	0.213	37	0.920	-33	-15.46	0.169	48	0.924	-32	-15.82	0.162	49
17000	0.865	-36	-13.36	0.215	35	0.913	-34	-15.36	0.171	45	0.917	-34	-15.76	0.163	46
18000	0.859	-38	-13.44	0.213	32	0.907	-36	-15.50	0.168	41	0.911	-36	-15.92	0.160	42

Typical S-Parameters (cont.)

HPND-4028

Freq. (MHz)	I_F = 1 mA					I_F = 5 mA					I_F = 10 mA				
	S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}		
	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.
1000	0.046	7	-0.38	0.958	-1	0.031	17	-0.24	0.973	-1	0.027	19	-0.20	0.978	-1
2000	0.048	20	-0.40	0.956	-2	0.036	33	-0.26	0.971	-2	0.033	37	-0.22	0.975	-2
3000	0.052	29	-0.40	0.957	-4	0.041	43	-0.26	0.972	-4	0.040	47	-0.22	0.975	-4
4000	0.058	36	-0.40	0.957	-5	0.049	49	-0.26	0.971	-5	0.047	53	-0.22	0.975	-5
5000	0.063	42	-0.40	0.956	-6	0.057	54	-0.26	0.971	-6	0.055	58	-0.22	0.975	-6
6000	0.069	46	-0.40	0.956	-7	0.064	57	-0.26	0.971	-7	0.063	60	-0.24	0.974	-7
7000	0.075	48	-0.40	0.956	-8	0.070	60	-0.26	0.971	-8	0.070	62	-0.22	0.975	-8
8000	0.081	50	-0.40	0.955	-9	0.077	60	-0.28	0.970	-9	0.076	63	-0.24	0.974	-9
9000	0.087	51	-0.40	0.956	-11	0.084	61	-0.28	0.970	-11	0.083	63	-0.24	0.974	-11
10000	0.092	52	-0.40	0.956	-12	0.089	61	-0.28	0.970	-12	0.089	63	-0.24	0.974	-12
11000	0.097	53	-0.40	0.956	-13	0.095	61	-0.26	0.971	-13	0.095	63	-0.22	0.975	-13
12000	0.103	52	-0.40	0.956	-14	0.101	60	-0.26	0.971	-14	0.101	62	-0.22	0.975	-14
13000	0.107	51	-0.40	0.957	-15	0.106	59	-0.26	0.971	-15	0.105	62	-0.22	0.975	-15
14000	0.112	51	-0.42	0.954	-17	0.110	59	-0.30	0.968	-17	0.111	61	-0.24	0.973	-17
15000	0.119	51	-0.42	0.953	-18	0.117	58	-0.28	0.969	-18	0.117	60	-0.26	0.972	-18
16000	0.123	51	-0.44	0.952	-19	0.122	57	-0.28	0.969	-19	0.123	60	-0.26	0.972	-19
17000	0.129	49	-0.44	0.952	-20	0.130	56	-0.30	0.967	-20	0.129	57	-0.26	0.971	-20
18000	0.139	48	-0.46	0.950	-22	0.139	55	-0.32	0.965	-21	0.140	56	-0.28	0.970	-22

HPND-4028

Freq. (MHz)	V_R = 0 V					V_R = 10 V					V_R = 30 V				
	S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}		
	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.
1000	0.997	-4	-27.54	0.042	86	0.999	-3	-33.16	0.022	91	1.000	-2	-33.98	0.020	91
2000	0.988	-7	-21.74	0.082	79	0.997	-6	-27.34	0.043	86	0.998	-5	-28.18	0.039	86
3000	0.974	-11	-18.36	0.121	74	0.994	-8	-23.62	0.066	83	0.996	-7	-24.44	0.060	84
4000	0.958	-14	-16.10	0.157	69	0.991	-10	-21.12	0.088	81	0.992	-10	-21.94	0.080	82
5000	0.940	-17	-14.48	0.189	64	0.986	-13	-19.26	0.109	78	0.987	-13	-20.10	0.099	79
6000	0.921	-21	-13.20	0.219	70	0.979	-16	-17.66	0.131	75	0.982	-15	-18.42	0.120	76
7000	0.898	-24	-12.16	0.247	56	0.972	-19	-16.26	0.054	72	0.976	-18	-17.08	0.140	73
8000	0.879	-26	-11.36	0.271	52	0.965	-21	-15.20	0.174	70	0.970	-21	-15.92	0.160	71
9000	0.857	-29	-10.64	0.294	48	0.954	-24	-14.20	0.195	67	0.960	-23	-14.96	0.179	68
10000	0.836	-32	-10.12	0.312	46	0.942	-27	-13.44	0.213	65	0.950	-26	-14.20	0.195	66
11000	0.816	-35	-9.54	0.334	42	0.931	-30	-12.58	0.235	61	0.937	-29	-13.32	0.216	62
12000	0.795	-37	-9.10	0.351	40	0.917	-33	-11.84	0.256	59	0.926	-32	-12.62	0.234	60
13000	0.778	-40	-8.86	0.361	37	0.904	-36	-11.44	0.268	56	0.913	-34	-12.20	0.246	57
14000	0.761	-42	-8.44	0.379	33	0.892	-38	-10.80	0.289	52	0.903	-37	-11.52	0.266	54
15000	0.744	-44	-8.34	0.383	31	0.876	-41	-10.56	0.297	50	0.888	-39	-11.26	0.274	52
16000	0.733	-46	-8.04	0.397	28	0.867	-43	-10.12	0.312	46	0.881	-42	-10.80	0.289	48
17000	0.720	-48	-7.94	0.401	26	0.855	-45	-9.96	0.318	44	0.869	-44	-10.64	0.294	46
18000	0.709	-50	-8.00	0.399	24	0.846	-47	-9.94	0.319	42	0.861	-46	-10.64	0.294	44

Typical S-Parameters (cont.)

HPND-4038

Freq. (MHz)	I_F = 1 mA					I_F = 5 mA					I_F = 10 mA				
	S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}		
	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.
1000	0.028	15	-0.22	0.976	-1	0.019	28	-0.12	0.987	-1	0.017	35	-0.10	0.989	-1
2000	0.032	34	-0.24	0.974	-2	0.026	50	-0.16	0.984	-2	0.024	56	-0.14	0.986	-2
3000	0.037	47	-0.22	0.975	-3	0.034	61	-0.14	0.985	-3	0.033	66	-0.12	0.988	-4
4000	0.045	55	-0.22	0.975	-5	0.042	67	-0.14	0.985	-5	0.042	70	-0.12	0.987	-5
5000	0.052	61	-0.24	0.974	-6	0.051	72	-0.16	0.984	-6	0.051	75	-0.14	0.986	-6
6000	0.060	65	-0.24	0.974	-7	0.059	74	-0.16	0.984	-7	0.059	77	-0.14	0.986	-7
7000	0.067	67	-0.24	0.974	-8	0.067	76	-0.16	0.984	-8	0.067	78	-0.12	0.987	-8
8000	0.073	69	-0.24	0.974	-9	0.074	76	-0.16	0.983	-9	0.073	78	-0.14	0.986	-9
9000	0.081	70	-0.24	0.973	-10	0.081	77	-0.16	0.984	-10	0.081	78	-0.14	0.986	-10
10000	0.087	71	-0.24	0.974	-11	0.088	77	-0.16	0.982	-11	0.089	79	-0.14	0.986	-11
11000	0.092	71	-0.22	0.975	-12	0.094	77	-0.16	0.984	-12	0.094	79	-0.14	0.986	-12
12000	0.099	70	-0.24	0.974	-14	0.100	76	-0.16	0.984	-14	0.101	77	-0.14	0.986	-14
13000	0.104	70	-0.22	0.975	-15	0.106	75	-0.14	0.985	-15	0.107	76	-0.12	0.987	-15
14000	0.110	69	-0.26	0.972	-16	0.112	74	-0.16	0.982	-16	0.113	75	-0.16	0.984	-16
15000	0.118	67	-0.24	0.973	-17	0.119	72	-0.16	0.983	-17	0.120	73	-0.14	0.985	-17
16000	0.123	66	-0.24	0.973	-18	0.125	71	-0.16	0.982	-18	0.126	72	-0.16	0.984	-18
17000	0.132	64	-0.26	0.972	-19	0.133	68	-0.16	0.982	-19	0.133	69	-0.16	0.984	-19
18000	0.141	62	-0.26	0.972	-20	0.143	66	-0.18	0.980	-20	0.143	67	-0.16	0.983	-20

HPND-4038

Freq. (MHz)	V_R = 0 V					V_R = 10 V					V_R = 30 V				
	S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}			S_{11}/S_{22}		S_{21}/S_{12}		
	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB	Mag.	Ang.
1000	0.993	-5	-23.10	0.070	83	0.998	-3	-28.88	0.036	89	0.999	-3	-29.90	0.032	90
2000	0.976	-10	-17.28	0.137	76	0.995	-7	-22.86	0.072	84	0.996	-6	-23.76	0.065	85
3000	0.953	-15	-14.04	0.199	70	0.990	-10	-19.26	0.109	81	0.992	-9	-20.18	0.098	82
4000	0.923	-19	-11.88	0.255	64	0.982	-13	-16.78	0.145	78	0.986	-12	-17.74	0.130	79
5000	0.890	-23	-10.36	0.304	58	0.973	-16	-14.90	0.180	74	0.977	-15	-15.88	0.161	75
6000	0.857	-27	-9.20	0.347	53	0.962	-20	-13.40	0.214	71	0.968	-19	-14.30	0.193	73
7000	0.822	-31	-8.28	0.386	49	0.947	-23	-12.08	0.249	68	0.956	-22	-12.96	0.225	69
8000	0.790	-34	-7.58	0.418	45	0.933	-27	-11.06	0.280	65	0.945	-25	-11.92	0.254	66
9000	0.757	-38	-7.00	0.447	41	0.915	-30	-10.12	0.312	61	0.928	-29	-10.94	0.284	63
10000	0.727	-41	-6.54	0.471	38	0.897	-34	-9.40	0.339	58	0.912	-32	-10.22	0.309	61
11000	0.697	-44	-6.10	0.496	34	0.877	-37	-8.62	0.371	54	0.892	-35	-9.44	0.338	57
12000	0.668	-46	-5.74	0.517	32	0.854	-41	-8.00	0.399	52	0.874	-38	-8.76	0.365	54
13000	0.643	-49	-5.56	0.528	29	0.834	-44	-7.60	0.417	49	0.854	-42	-8.34	0.383	51
14000	0.620	-51	-5.22	0.549	26	0.813	-47	-7.04	0.445	45	0.839	-45	-7.76	0.410	48
15000	0.599	-53	-5.16	0.553	24	0.793	-50	-6.82	0.457	43	0.818	-48	-7.50	0.422	45
16000	0.584	-55	-4.90	0.569	21	0.778	-53	-6.42	0.478	39	0.805	-50	-7.10	0.442	42
17000	0.570	-57	-4.80	0.576	19	0.762	-55	-6.22	0.489	37	0.790	-53	-6.88	0.453	40
18000	0.556	-59	-4.84	0.574	17	0.747	-58	-6.18	0.491	35	0.776	-55	-6.86	0.454	37

HEWLETT PACKARD

Low Loss Beam Lead PIN Diodes

Technical Data

HPND-4050

Features

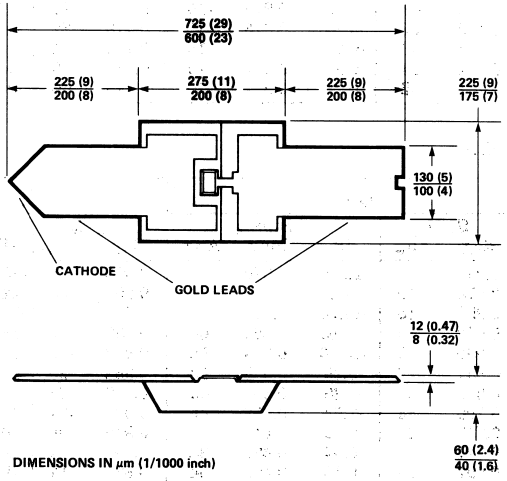
- **Low Series Resistance**
  1.3 Ω Typical
- **Low Capacitance**
  0.07 pF Typical
- **Fast Switching**
  2 ns Typical
- **Rugged Construction**
  4 Grams Minimum Lead Pull

Description

The HPND-4050 is a beam lead PIN diode designed specifically for low capacitance, low series resistance, and rugged construction. The new HP mesa process allows the fabrication of beam lead PINs with a very low RC product. A nitride passivation layer provides immunity from contaminants which would otherwise lead to I_R drift. A polyimide layer provides scratch protection.

Applications

The HPND-4050 beam lead PIN diode is designed for use in stripline or microstrip circuits. Applications include switching, attenuating, phase shifting, and modulating at microwave frequencies. The low capacitance and low series resistance at low current makes this device ideal for applications in the shunt configuration.



Outline 07

Maximum Ratings

Operating Temperature ..... -65°C to +175°C
Storage Temperature ..... -65°C to +200°C
Power Dissipation at T_{CASE} = 25°C ..... 250 mW
(Derate linearly to zero at 175°C.)
Minimum Lead Strength ..... 4 grams pull on either lead
Diode Mounting Temperature ..... 220°C for 10 sec. max.

Bonding and Handling Procedures

See page 4-24.

Electrical Specifications at $T_A = 25°C$

Part Number HPND-	Breakdown Voltage V_{BR} (V)		Series Resistance R_S (Ω)[1]		Capacitance C_T (pF)[1]		Reverse Current I_R (nA)	Forward Voltage V_F (V)	Minority Carrier Lifetime τ (ns)[1]	Reverse Recovery Time t_{rr} (ns)[1]
	Min.	Typ.	Typ.	Max.	Typ.	Max.	Max.	Max.	Typ.	Typ.
4050	30	40	1.3	1.7	0.12	0.15	100	0.98	25	2
Test Conditions	$V_R = V_{BR}$ Measure $I_R \leq 10$ μA		$I_F = 10$ mA f = 100 MHz		$V_R = 10$ V f = 1 MHz		$V_R = 10$ V	$I_F = 20$ mA	$I_F = 10$ mA $I_R = 6$ mA	$I_F = 10$ mA $V_R = 10$ V

Note:
1. Test performed on packaged samples.

Typical Parameters

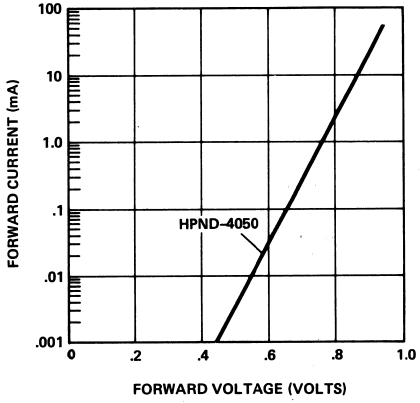


Figure 1. Typical Forward Characteristics.

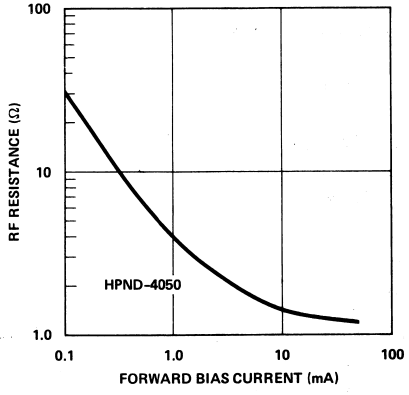


Figure 2. Typical RF Resistance vs. Forward Bias Current.

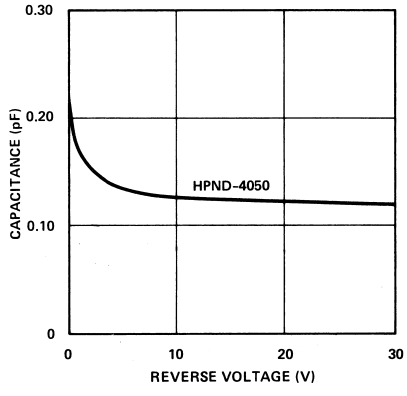


Figure 3. Typical Capacitance vs. Reverse Voltage.

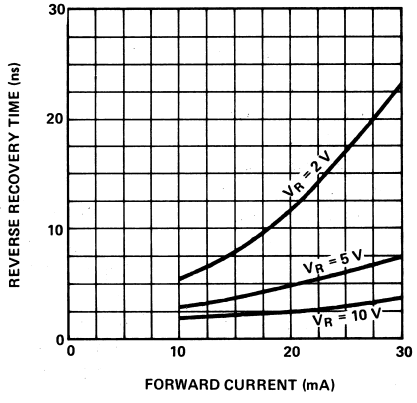


Figure 4. Typical Reverse Recovery Time vs. Forward Current (Shunt Configuration).

HEWLETT PACKARD

Beam Lead PIN Diode

Technical Data

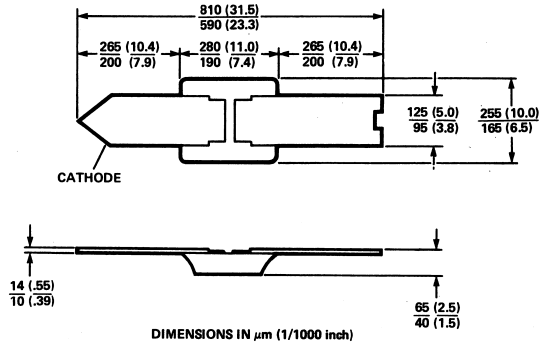
5082-3900

Features

- **High Breakdown Voltage**
  200 V Minimum
- **Low Capacitance**
  0.02 pF Typical
- **Rugged Construction**
  2 grams Minimum Lead Pull
- **Nitride Passivated**

Description

The 5082-3900 planar beam lead PIN diode offers a low capacitance to allow high isolation at RF and microwave frequencies. Nitride passivation and rugged construction insures reliable performance and assembly yields.



Outline 06

Applications

The 5082-3900 beam Lead PIN diode is designed for use in stripline or microstrip circuits using welding or thermocompression bonding techniques. PIN applications include switching, attenuating, phase shifting, limiting and modulating at microwave frequencies.

Bonding and Handling Procedures

See page 4-24

Maximum Ratings

Operating Temperature Range ..... -60°C to +150 °C
Storage Temperature Range ..... -60°C to +150°C
Power Dissipation at T_{CASE} = 25°C ..... 250 mW
(Derate linearly to zero at 150°C)
Minimum Lead Strength ..... 2 grams pull on either lead
Diode Mounting Temperature ..... 220°C for 10 sec. max.

Electrical Specifications at $T_A = 25°C$

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Breakdown Voltage	V_{BR}	150	200	–	V	$I_R = 10\ \mu A$
Series Resistance	R_S	–	6	8	Ω	$I_F = 50$ mA, f = 100 MHz
Capacitance	C_O	–	0.02	0.025	pF	V = 0 V, f = 3 GHz
Minority Carrier Lifetime	τ	–	150	–	ns	$I_F = 50$ mA, $I_R = 250$ mA

Typical Parameters

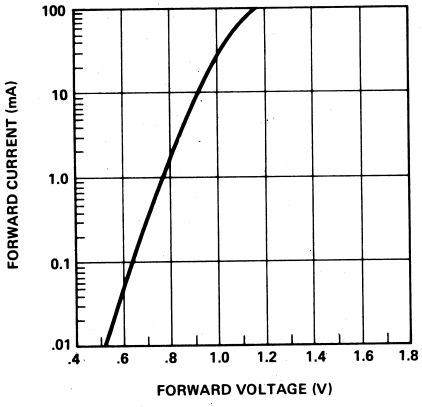


Figure 1. Typical Forward Conduction Characteristics.

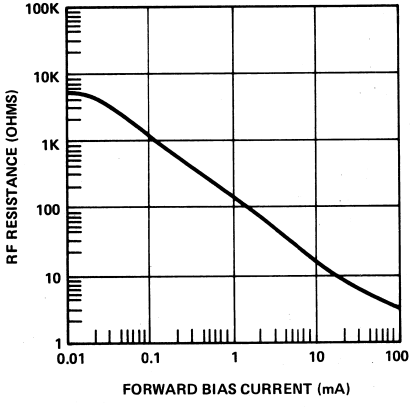


Figure 2. Typical RF Resistance vs. DC Bias Current.

Bonding and Handling Procedures for Beam Lead Diodes

1. Storage

Under normal circumstances, storage of beam lead diodes in HP supplied waffle/gel packs is sufficient. In particularly dusty or chemically hazardous environments, storage in an inert atmosphere desiccator is advised.

2. Handling

In order to avoid damage to beam lead devices, particular care must be exercised during inspection, testing, and assembly. Although the beam lead diode is designed to have exceptional lead strength, its small size and delicate nature requires that special handling techniques be observed so that the devices will not be mechanically or electrically damaged. A vacuum pickup is recommended for picking up beam lead devices, particularly larger ones, e.g., quads. Care must be exercised to assure that the vacuum opening of the needle is sufficiently small to avoid passage of the device through the opening. A #27 tip is recommended for picking up single beam lead devices. A 20X magnification is needed for precise positioning of the tip on the device. Where a vacuum pickup is not used, a sharpened wooden Q-tip dipped in isopropyl alcohol is very commonly used to handle beam lead devices.

3. Cleaning

For organic contamination use a warm (<75°C) rinse of trichloroethane followed by a cold rinse in acetone and methanol. Dry under infrared heat lamp for 5-10 minutes on clean filter paper. Freon degreaser may replace trichloroethane for light organic contamination.

- Ultrasonic cleaning is not recommended.
- Acid solvents should not be used.

4. Bonding

Thermocompression: See Application Note 979 "The Handling and Bonding of Beam Lead Devices Made Easy". This method is good for hard substrates only.

Wobble: This method picks up the device, places it on the substrate and forms a thermocompression bond all in one operation. This is described in MIL-STD-883, Method 2017, and is intended for hard substrates only. Equipment specifically designed for beam lead wobble bonding is available from KULICKE and SOFFA in Horsham, PA.

Resistance Welding or Parallel-GAP Welding: To make welding on soft substrates easier, a low pressure welding head is recommended. Suitable equipment is available from HUGHES, Industrial Products Division in Carlsbad, CA.

Epoxy: With solvent free, low resistivity epoxies (available from ABLESTIK in Gardena, CA, MICON in Lexington, MA, and many others) and improvements in dispensing equipment, the quality of epoxy bonds is sufficient for many applications. Equipment is available from ADVANCED SEMICONDUCTOR MATERIALS AMERICA, INC., Assembly Products Group in Chandler, AZ (Automatic), and WEST BOND in Orange, CA (Manual).

5. Lead Stress

In the process of bonding a beam lead diode, a certain amount of "bugging" occurs. The term *bugging* refers to the chip lifting away from the substrate during the bonding process due to the deformation of the beam by the bonding tool. This effect is beneficial as it provides stress relief for the diode during thermal cycling of the substrate. The coefficient of expansion of some substrate materials, specifically soft substrates, is such that some bugging is essential if the circuit is to be operated over wide temperature extremes.

Thick metal clad ground planes restrict the thermal expansion of the dielectric substrates in the X-Y axis. The expansion of the dielectric will then be mainly in the Z axis, which does not affect the beam lead device. An alternate solution to the problem of dielectric ground plane expansion is to heat the substrate to the maximum required operating temperature during the beam lead attachment. Thus, the substrate is at maximum expansion when the device is bonded. Subsequent cooling of the substrate will cause bugging, similar to bugging in thermocompression bonding or epoxy bonding. Other methods of bugging are preforming the leads during assembly or prestressing the substrate.

HEWLETT PACKARD

Surface Mount PIN Diodes

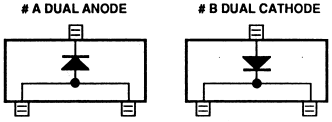
Technical Data

HSMP-38XX and HSMP-48XX Series

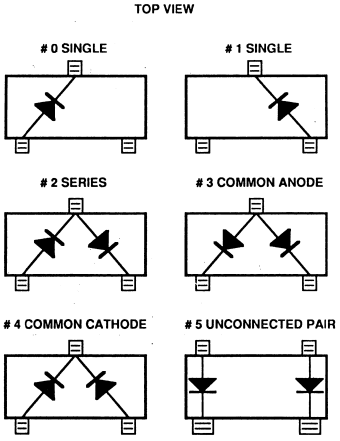
Features

- **Diodes Optimized for:**
  - Low Current Switching
  - Low Distortion Attenuating
  - Ultra-Low Distortion Switching
  - Microwave Frequency Operation
- **Surface Mount SOT-23 Package**
  - Single and Dual Versions
  - Tape and Reel Options Available
- **Low Failure in Time (FIT) Rate***

*For more information see the Surface Mount PIN Reliability Data Sheet.



Package Lead Code Identification



Description/ Applications

The HSMP-3800 and HSMP-3810 series are specifically designed for low distortion attenuator applications. The HSMP-3820 and HSMP-3890 series are optimized for switching applications where low resistance at low current, and low capacitance are required. The HSMP-3880 switching diode is an ultra low distortion device optimized for higher power applications from 50 MHz to 1.5 GHz. The HSMP-48XX series are special products featuring ultra low parasitic inductance in the SOT-23 package, specifically designed for use at frequencies which are much higher than the upper limit for conventional SOT-23 PIN diodes. The HSMP-4810 diode is a low distortion attenuating PIN designed for operation to 3 GHz. The HSMP-4820 diode is ideal for limiting and low inductance switching applications up to 1.5 GHz. The HSMP-4890 is optimized for low current switching applications up to 3 GHz.

Ordering Information

See page 14-14.

Absolute Maximum Ratings** T_A = 25°C

Symbol	Parameter	Value
I_f	Forward Current (1 µs Pulse)	1 Amp
P_t	Total Device Dissipation	250 mW[1]
P_{iv}	Peak Inverse Voltage	Same as V_{BR}
T_j	Junction Temperature	150°C
T_{stg}	Storage Temperature	-65 to 150°C

**Operation in excess of any one of these conditions may result in permanent damage to this device.

Note:
1. CW Power Dissipation at T_{LEAD} = 25°C. Derate to zero at maximum rated temperature.

PIN Attenuator Diodes

Electrical Specifications T_A = 25°C (Each Diode)

Part Number HSMP-	Package Marking Code[1]	Lead Code	Configuration	Nearest Equivalent Axial Lead Part No. 5082-	Minimum Breakdown Voltage V_{BR} (V)	Maximum Series Resistance R_S (Ω)	Maximum Total Capacitance C_T (pF)	Minimum High Resistance R_H (Ω)	Maximum Low Resistance R_L (Ω)
3800 3801 3802 3804	D0 D1 D2 D4	0 1 2 4	Single Single Series Common Cathode	3080	100	2.5	0.35	1000	8
3810 3811 3812 3813 3814	E0 E1 E2 E3 E4	0 1 2 3 4	Single Single Series Common Anode Common Cathode	3081	100	4.0	0.35	1500	10
Test Conditions					$V_R = V_{BR}$ Measure $I_R \leq 10$ μA	I_F = 100 mA f = 100 MHz	V_R = 50 V f = 1 MHz	I_F = 0.01 mA f = 100 MHz	I_F = 20 mA f = 100 MHz

PIN Switching Diodes

Part Number HSMP-	Package Marking Code[1]	Lead Code	Configuration	Nearest Equivalent Axial Lead Part No. 5082-	Minimum Breakdown Voltage V_{BR} (V)	Maximum Series Resistance R_S (Ω)	Maximum Total Capacitance C_T (pF)	Maximum Shunt Mode Harmonic Distortion Hmd (dBc)
3820 3821 3822 3823 3824	F0 F1 F2 F3 F4	0 1 2 3 4	Single Single Series Common Anode Common Cathode	3188	35	0.6*	1.0*	-
3880 3881	S0 S1	0 1	Single Single	-	100	6.5	0.40	-55
3890 3891 3892 3893 3894 3895	G0 G1 G2 G3 G4 G5	0 1 2 3 4 5	Single Single Series Common Anode Common Cathode Unconnected Pair	-	35	2.5	0.30**	-
Test Conditions					$V_R = V_{BR}$ Measure $I_R \leq 10$ μA	I_F = 5 mA f = 100 MHz I_F = 10 mA*	V_R = 50 V f = 1 MHz V_R = 20 V* V_R = 5 V**	2 f_o, Z_o = 50 W f_o = 400 MHz P_{in} = +30 dBm 0 V bias

Note:

1. Package marking code is white. Package marking code is suffix "L" for low profile.

PIN General Purpose Diodes

Part Number HSMP-	Package Marking Code[1]	Lead Code	Configuration	Nearest Equivalent Axial Lead Part No. 5082-	Minimum Breakdown Voltage V_{BR} (V)	Maximum Series Resistance R_S (Ω)	Maximum Total Capacitance C_T (pF)
3830	K0	0	Single	3077	200	1.5	0.3
3831	K1	1	Single				
3832	K2	2	Series				
3833	K3	3	Common Anode				
3834	K4	4	Common Cathode				
Test Conditions					$V_R = V_{BR}$ Measure $I_R \leq 10$ μA	$I_F = 100$ mA f = 100 MHz	$V_R = 50$ V f = 1 MHz

Note:
1. Package marking code is white. Package marking code is suffix "L" for low profile.

High Frequency (Low Inductance, 500 MHz - 3 GHz) PIN Diodes

Part Number HSMP-	Package Marking Code	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Series Resistance R_S (Ω)	Typical Total Capacitance C_T (pF)	Maximum Total Capacitance C_T (pF)	Typical Total Inductance L_T (nH)	Application
4810	EB	B	Dual Cathode	100	4.0	0.35	0.4	1.0	Attenuator
4820	FA	A	Dual Anode	35	0.6*	0.75*	1.0*	1.0*	Limiter
4890	GA	A	Dual Anode	35	2.5*	0.33	0.375	1.0	Switch
				$V_R = V_{BR}$ Measure $I_R \leq 10$ μA	$I_F = 100$ mA $I_F = 10$ mA*	$V_R = 50$ V f = 1 MHz $V_R = 20$ V*	$V_R = 50$ V f = 1 MHz $V_R = 20$ V*	f = 500 MHz - 3 GHz f = 500 MHz - 1.5 GHz	

Note:
1. Package marking code is white. Package marking code is suffix "L" for low profile.

Typical Parameters at $T_A = 25°C$

Part Number HSMP-	Series Resistance R_S (Ω)	Carrier Lifetime T (ns)	Reverse Recovery Time T_{rr} (ns)
380X	55	1800	500
381X/4810	75	1500	300
382X/4820	1.5	70*	7
383X	20	500	80
388X	3.8	2500	550
389X/4890	3.8	200*	–
Test Conditions	$I_F = 1$ mA f = 100 MHz $I_F = 10$ mA*	$I_F = 50$ mA $I_R = 250$ mA $I_F = 10$ mA* $I_R = 6$ mA*	$V_R = 10$ V $I_F = 20$ mA 90% Recovery

Typical Parameters at T_A = 25°C (unless otherwise noted), Single Diode

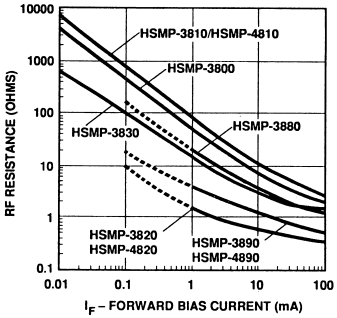


Figure 1. RF Resistance at 25°C vs. Forward Bias Current.

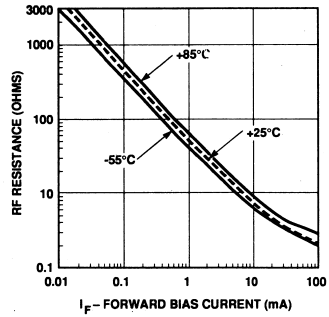


Figure 2. RF Resistance vs. Forward Bias Current for HSMP-3800.

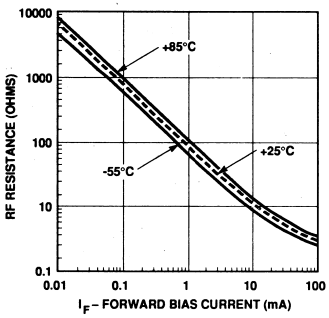


Figure 3. RF Resistance vs. Forward Bias Current for HSMP-3810 and HSMP-4810.

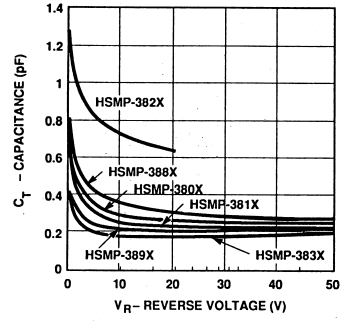


Figure 4. Capacitance vs. Reverse Voltage.

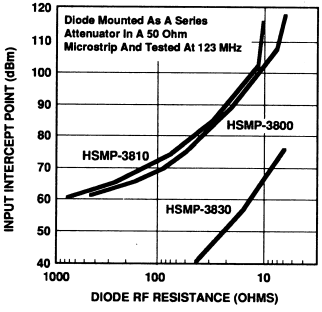


Figure 5. 2nd Harmonic Input Intercept Point vs. Diode RF Resistance for Attenuator Diodes.

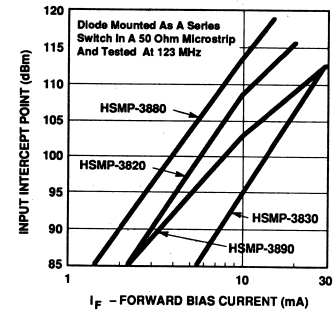


Figure 6. 2nd Harmonic Input Intercept Point vs. Forward Bias Current for Switch Diodes.

Typical Parameters (continued)

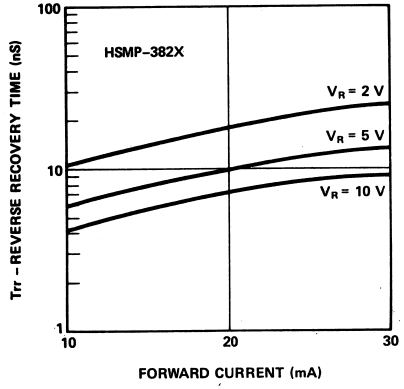


Figure 7. Reverse Recovery Time vs. Forward Current for Various Reverse Voltages. HSMP-3820 Series.

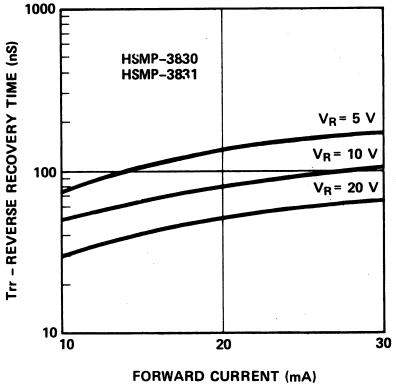


Figure 8. Reverse Recovery Time vs. Forward Current for Various Reverse Voltages. HSMP-3830 Series

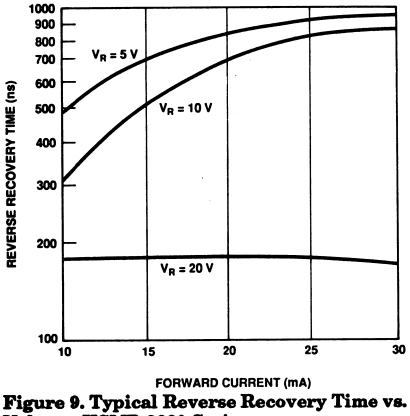


Figure 9. Typical Reverse Recovery Time vs. Reverse Voltage. HSMP-3880 Series.

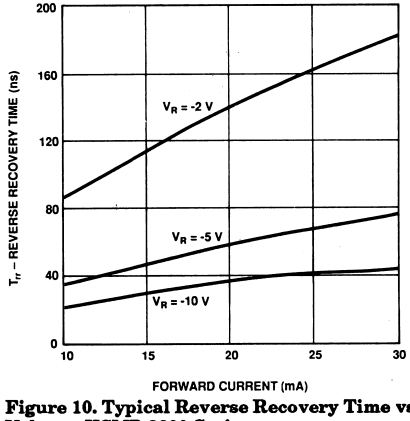


Figure 10. Typical Reverse Recovery Time vs. Reverse Voltage. HSMP-3890 Series.

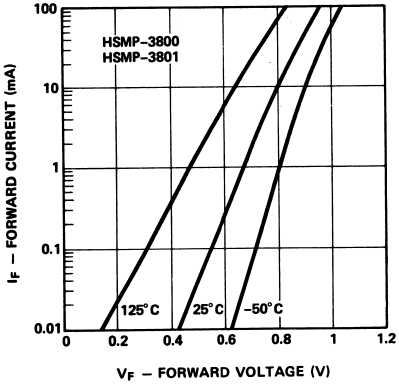


Figure 11. Forward Current vs. Forward Voltage. HSMP-3880 Series.

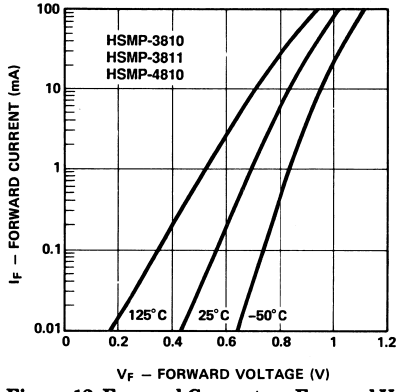


Figure 12. Forward Current vs. Forward Voltage. HSMP-3810 and HSMP-4810 Series.

Typical Parameters (continued)

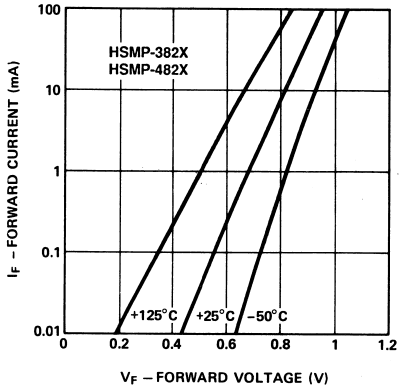


Figure 13. Forward Current vs. Forward Voltage. HSMP-3820 and HSMP-4820 Series.

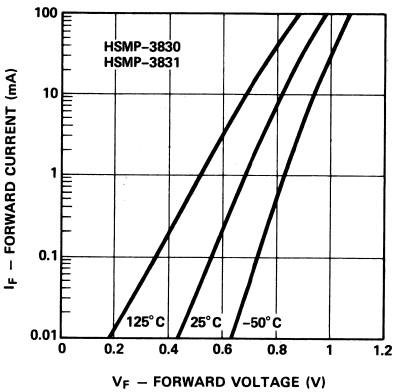


Figure 14. Forward Current vs. Forward Voltage. HSMP-3830 Series.

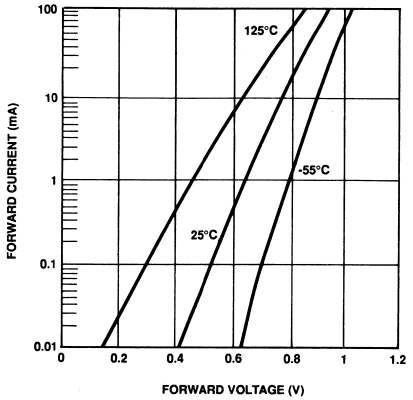


Figure 15. Typical Forward Current vs. Forward Voltage. HSMP-3880 Series.

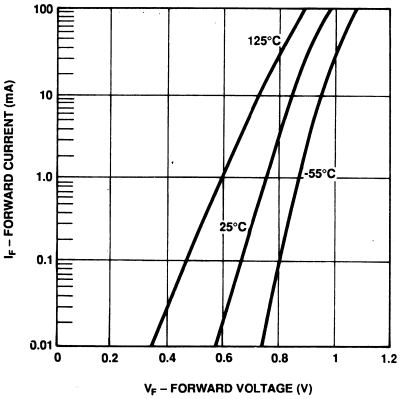
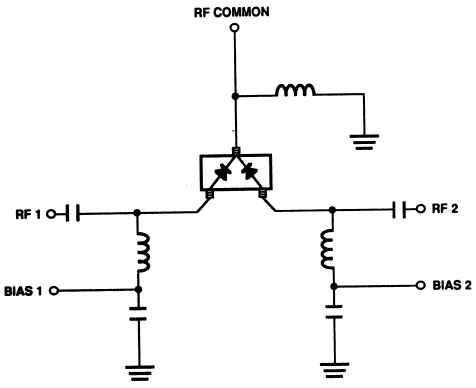
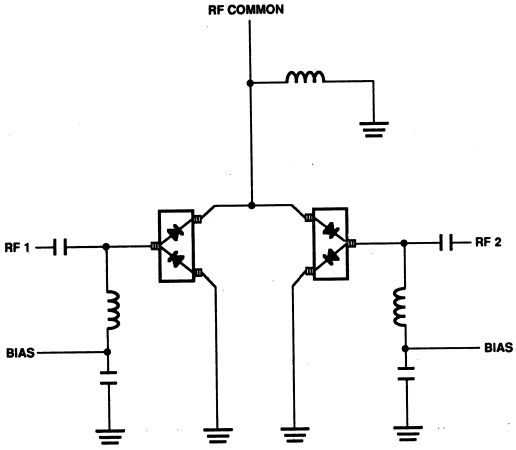


Figure 16. Typical Forward Current vs. Forward Voltage. HSMP-3890 and HSMP-4890 Series.

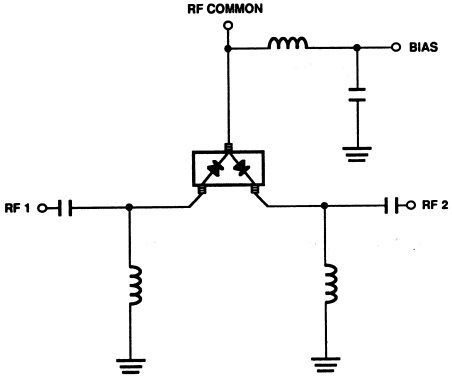
Typical Applications for Multiple Diode Products



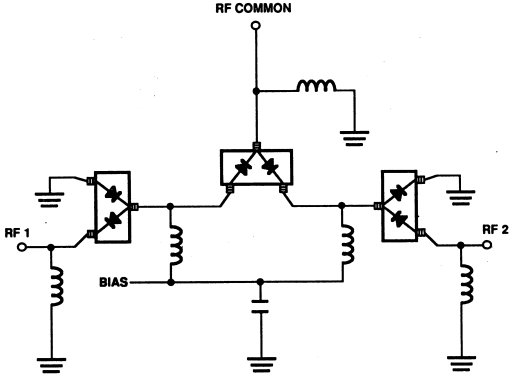
Simple SPDT Switch, Using Only Positive Bias Current.



High Isolation SPDT Switch.

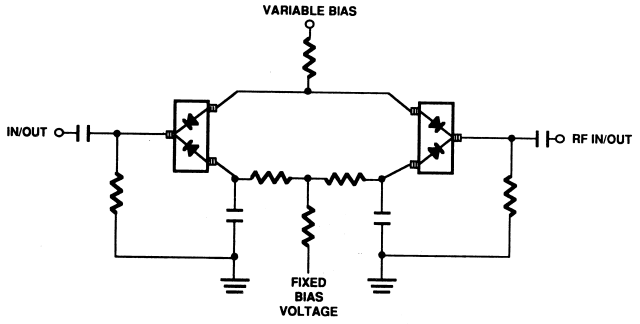


SPDT Switch Using Both Positive and Negative Bias Current.

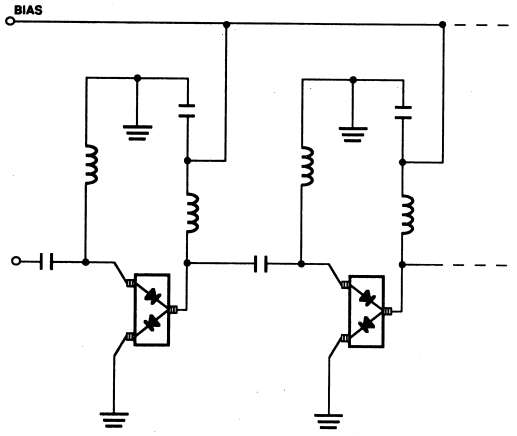


Very High Isolation SPDT Switch.

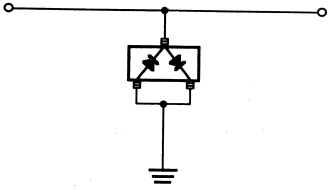
Typical Applications for Multiple Diode Products (cont.)



Four Diode II Attenuator.

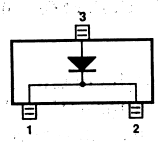


High Isolation SPST Switch (Repeat Cells as Required).

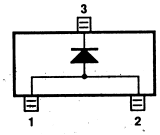


Power Limiter Using HSMP-3822 Diode Pair.

Typical Applications for HSMP-48XX Low Inductance Series

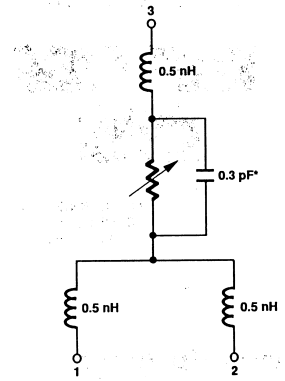


HSMP-4810

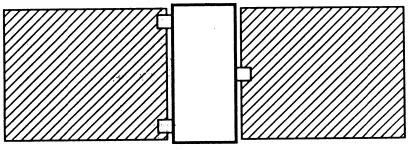


HSMP-4820 & HSMP-4890

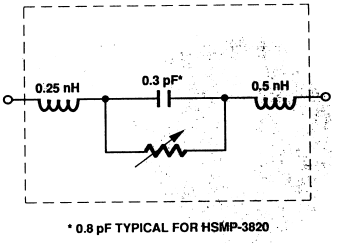
Internal Connections



Equivalent Circuit



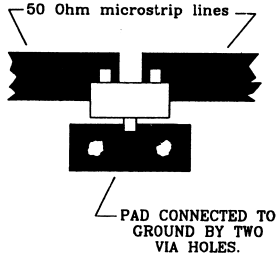
Circuit Layout



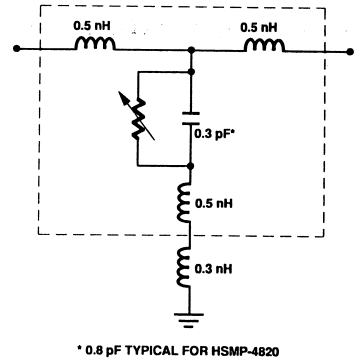
Equivalent Circuit

Microstrip Series Connection for HSMP-48XX Series

In order to take full advantage of the low inductance of the HSMP-48XX series when using them in a series application, both lead 1 and lead 2 should be connected together, as shown above.



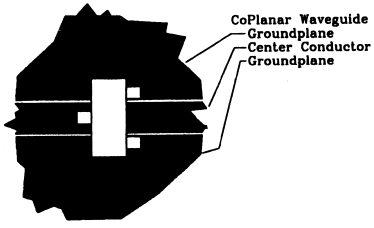
Circuit Layout



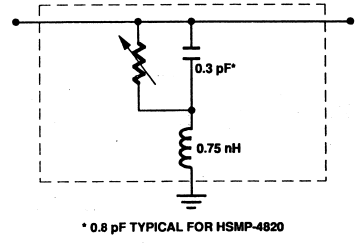
Equivalent Circuit

Microstrip Shunt Connection for HSMP-48XX Series

In the diagram above, the center conductor of the microstrip line is interrupted and leads 1 and 2 of the HSMP-38XX series diode are placed across the resulting gap. This forces the 0.5 nH lead inductance of leads 1 and 2 to appear as part of a low pass filter, reducing the shunt parasitic inductance and increasing the maximum available attenuation. The 0.3 nH of shunt inductance external to the diode is created by the via holes, and is a good estimate for 0.032" thick material.



Circuit Layout

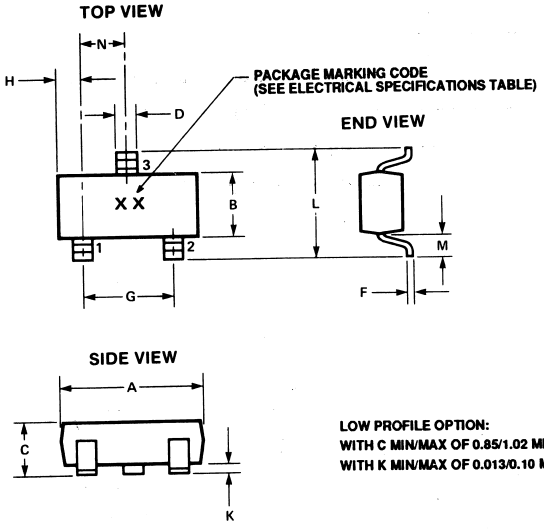


Equivalent Circuit

Co-Planar Waveguide Shunt Connection for HSMP-48XX Series

Co-Planar waveguide, with ground on the top side of the printed circuit board, is shown in the diagram above. Since it eliminates the need for via holes to ground, it offers lower shunt parasitic inductance and higher maximum attenuation when compared to a microstrip circuit.

Package Dimensions



STANDARD PROFILE

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.80	3.06	0.110	0.120
B	1.20	1.40	0.047	0.055
C*	0.85	1.20	0.035	0.047
D	0.37	0.54	0.015	0.021
F	0.086	0.152	0.003	0.006
G	1.78	2.04	0.070	0.080
H	0.45	0.60	0.018	0.024
K*	0.10	0.25	0.004	0.010
L	2.10	2.65	0.083	0.104
M	0.45	0.69	0.018	0.027
N	0.89	1.02	0.035	0.040

LOW PROFILE OPTION:
WITH C MIN/MAX OF 0.85/1.02 MILLIMETERS, 0.033/0.041 INCHES;
WITH K MIN/MAX OF 0.013/0.10 MILLIMETERS, 0.0005/0.004 INCHES

Outline 23 (SOT-23)

Package Characteristics

Lead Material ..... Alloy 42
Lead Finish ..... Tin-Lead
Maximum Soldering Temperature ..... 260°C for 5 seconds
Min. Lead Strength ..... 2 pounds pull
Typical Package Inductance ..... 2 nH
Typical Package Capacitance ..... 0.15 pF (opposite leads)

Ordering Information

Standard Profile

Option T30 = Bulk
Option T31 = Tape and Reel, See Figure 17
Option T32 = Tape and Reel, See Figure 18

Low Profile

Option L30 = Bulk
Option L31 = Tape and Reel, See Figure 17
Option L32 = Tape and Reel, See Figure 18

Conforms to Electronic Industries RS-481, "Taping of Surface Mounted Components for Automated Placement." Standard Quantity is 3,000 Devices/Reel.

Specify Part Number followed by Option Number

Example:

H SMP-X8XX Option X XX

- XX — Bulk or Tape and Reel Option
- X — Profile: Standard = T, or Low = L
- SMP-X8XX — Part Number
- SMP — Surface Mount PIN
- H — HP

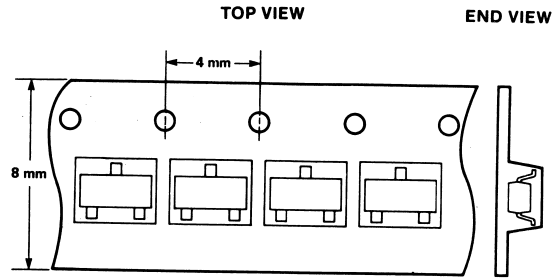
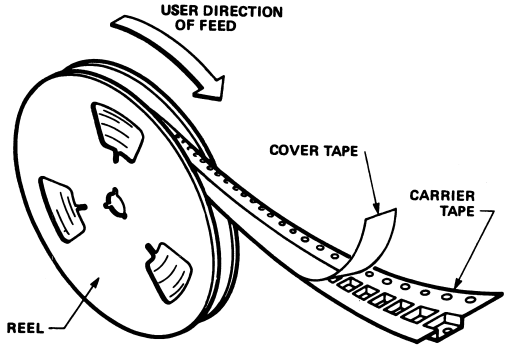


Figure 17. Options T31, L31.



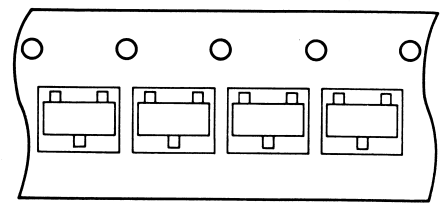


Figure 18. Options T32, L32.

HEWLETT PACKARD

PIN Diodes for RF Switching and Attenuating

Technical Data

1N5719, JAN1N5719/TX
1N5767
5082-3001/02
5082-3039
5082-3042/43
5082-3077
5082-3080/81
5082-3168/88
5082-3379
HPND-4165/66

Features

- **Low Harmonic Distortion**
- **Large Dynamic Range**
- **Low Series Resistance**
- **Low Capacitance**

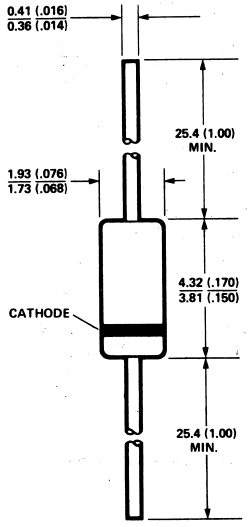
Description/ Applications

These general purpose switching diodes are intended for low power switching applications such as RF duplexers, antenna switching matrices, digital phase shifters, and time multiplex filters. The 5082-3168/3188 are optimized for VHF/UHF bandswitching.

The RF resistance of a PIN diode is a function of the current flowing in the diode. These current controlled resistors are specified for use in control applications such as variable RF attenuators, automatic gain control circuits, RF modulators, electrically tuned filters, analog phase shifters, and RF limiters.

Outline 15 diodes are available on tape and reel. The tape and reel specification is patterned after RS-296-D.

Note: The JAN Series 1N5719 devices are well suited for applications that require the high reliability of a JAN/TX device. The TX devices have solder dipped leads. The JAN1N5719 and JAN1N5719TX undergo testing per MIL-STD-750. More information about these devices can be obtained through your local Hewlett-Packard field sales engineer.



DIMENSIONS IN MILLIMETERS AND (INCHES).

Outline 15

Maximum Ratings

Junction Operating and
Storage Temperature Range ..... -65°C to +150°C
Power Dissipation 25°C ..... 250 mW
(Derate linearly to zero at 150°C)
Peak Inverse Voltage (PIV) ..... same as V_{BR}
Maximum Soldering Temperature ..... 260°C for 5 sec

Mechanical Specifications

The HP Outline 15 package has a glass hermetic seal with dumet leads. The lead finish is 95-5 tin-lead (SnPb) for all PIN diode products except the 5082-3042 and -3043, which have gold plated leads. The leads on the Outline 15 package should be restricted so that the bend starts at least 1/16 inch (1.6 mm) from the glass body. Typical package inductance and capacitance are 2.5 nH and 0.13 pF, respectively. Marking is by digital coding with a cathode band.

General Purpose Diodes
Electrical Specifications at T_A = 25°C

Part Number 5082-	Maximum Total Capacitance C_T (pF)	Minimum Breakdown Voltage V_{BR} (V)	Maximum Residual Series Resistance R_S (Ω)	Effective Carrier Lifetime τ (ns)	Reverse Recovery Time t_{rr} (ns)
General Purpose Switching and Attenuating					
3002	0.25	300	1.0	100 (min.)	100 (typ.)
3001	0.25	200	1.0	100 (min.)	100 (typ.)
3039	0.25	150	1.25	100 (min.)	100 (typ.)
1N5719	0.3**	150	1.25	100 (min.)	100 (typ.)
3077	0.3	200	1.5	100 (min.)	100 (typ)
Fast Switching					
3042	0.4*	70	1.0*	35 (typ.)*	5 (max.)
3043	0.4*	50	1.5*	35 (typ.)*	10 (max.)
Band Switching					
3188	1.0*	35	0.6**	70 (typ.)*	12 (typ.)
3168	2.0*	35	0.5**	70 (typ.)*	12 (typ.)
Test Conditions	V_R = 50 V *V_R = 20 V **V_R = 100 V f = 1 MHz	$V_R = V_{BR}$ Measure $I_R \leq 10$ μA	I_F =100 mA *I_F = 20 mA **I_F = 10 mA f = 100 MHz	I_F = 50 mA I_R = 250 mA *I_F = 10 mA *I_R = 6 mA	I_F = 20 mA V_R = 10 V 90% Recovery

Note:
Typical CW power switching capability for a shunt switch in a 50 Ω system is 2.5 W.

RF Current Controlled Resistor Diodes
Electrical Specifications at T_A = 25°C

Part Number	Effective Carrier Lifetime τ (ns)	Min. Breakdown Voltage V_{BR} (V)	Max. Residual Series Resistance R_S (Ω)	Max. Total Capacitance C_T (pF)	High Resistance Limit, R_H (Ω)		Low Resistance Limit, R_L (Ω)		Max. Difference in Resistance vs. Bias Slope, $\Delta\chi$
					Min.	Max.	Min.	Max.	
HPND-4165	100 (min.)	100	1.5	0.3	1100	1660	16	24	0.04
HPND-4166	100 (min.)	100	1.5	0.3	830	1250	12	18	0.04
5082-3080	1300 (typ.)	100	2.5	0.4	1000			8**	
1N5767*	1300 (typ.)	100	2.5	0.4	1000			8**	
5082-3379	1300 (typ.)	50		0.4				8**	
5082-3081	2500 (typ.)	100	3.5	0.4	1500			8**	
Test Conditions	I_F = 50 mA I_R = 250 mA	$V_R = V_{BR}$, Measure $I_R \leq 10$ µA	I_F = 100 mA f = 100 MHz	V_R = 50 V f = 1 MHz	I_F = 0.01 mA f = 100 MHz		I_F = 1.0 mA I_F = 20 mA** f = 100 MHz		Batch Matched at I_F = 0.01 mA and 1.0 mA f = 100 MHz

*The 1N5767 has the additional specifications: τ = 1.0 µsec minimum
I_R = 1 µA maximum at V_R = 50 V
V_F = 1 V maximum at I_F = 100 mA.

Typical Parameters at T_A = 25°C (unless otherwise noted)

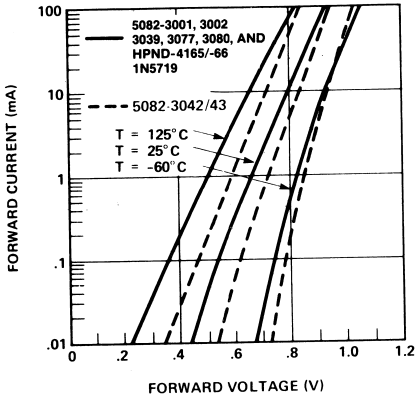


Figure 1. Typical Forward Current vs. Forward Voltage.

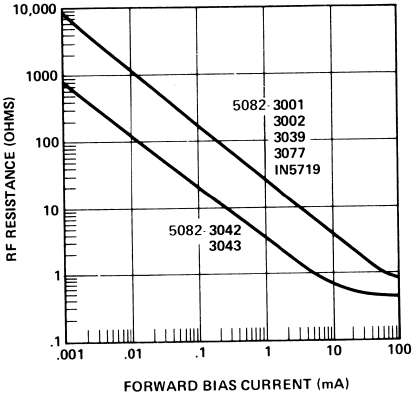


Figure 2. Typical RF Resistance vs. Forward Bias Current.

Typical Parameters at T_A = 25°C (cont.)

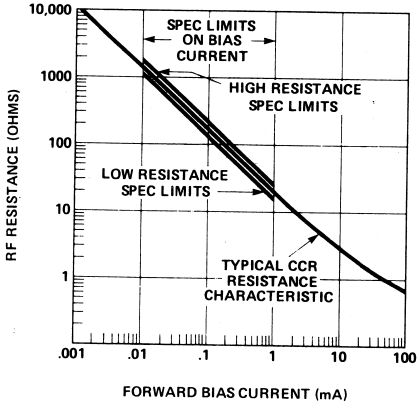


Figure 3. Typical RF Resistance vs. Bias for HPND-4165.

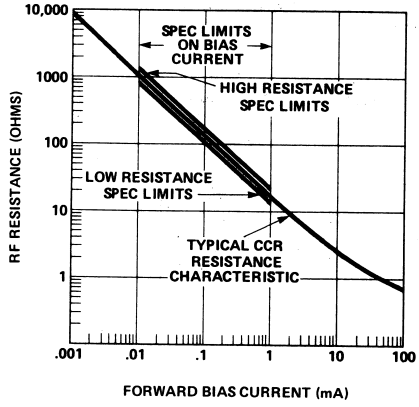


Figure 4. Typical RF Resistance vs. Bias for HPND-4166.

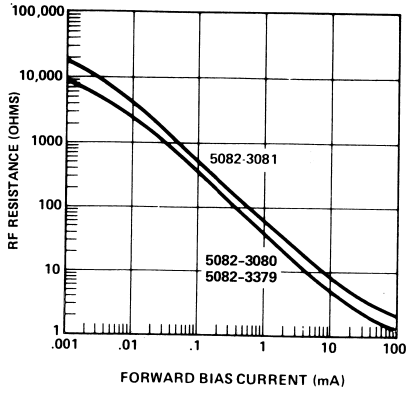


Figure 5. Typical RF Resistance vs. Forward Bias Current.

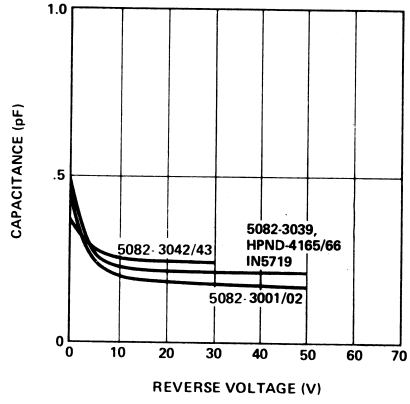


Figure 6. Typical Capacitance vs. Reverse Voltage.

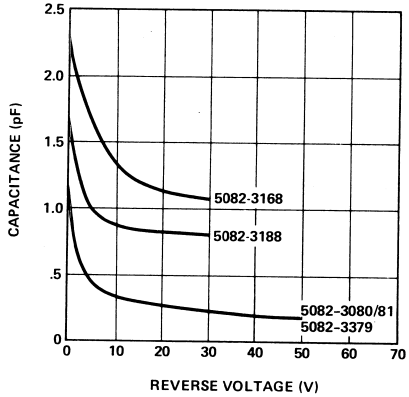


Figure 7. Typical Capacitance vs. Reverse Voltage.

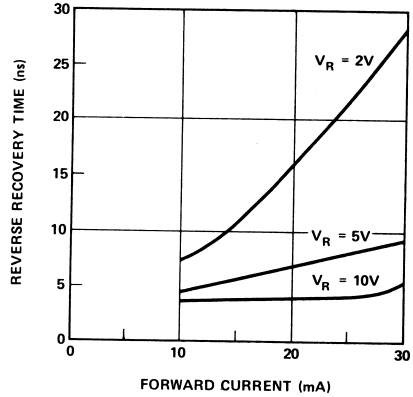


Figure 8. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages, 5082-3042, 3043.

Typical Parameters at $T_A = 25°C$ (cont.)

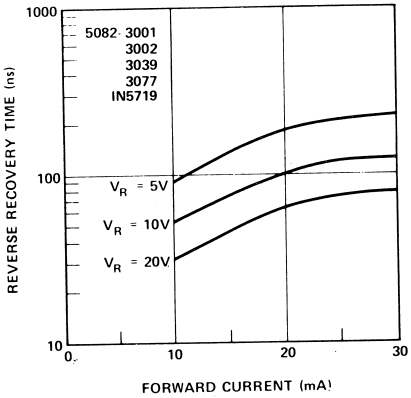


Figure 9. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages.

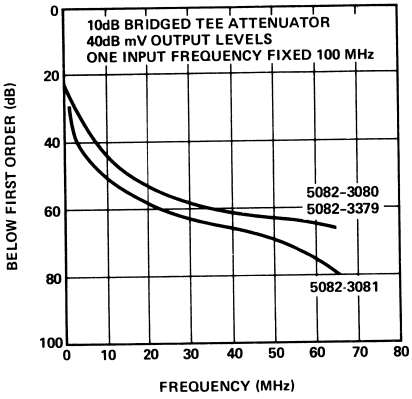


Figure 10. Typical Second Order Intermodulation Distortion.

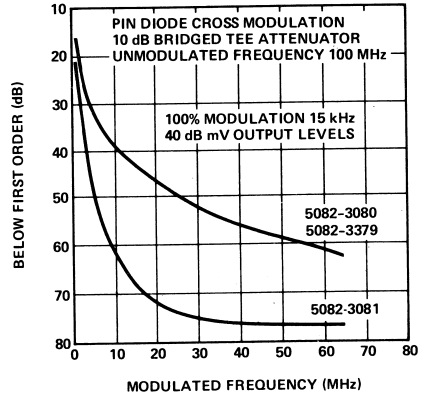


Figure 11. Typical Cross Modulation Distortion.

HEWLETT PACKARD

PIN Diode Limiter

Technical Data

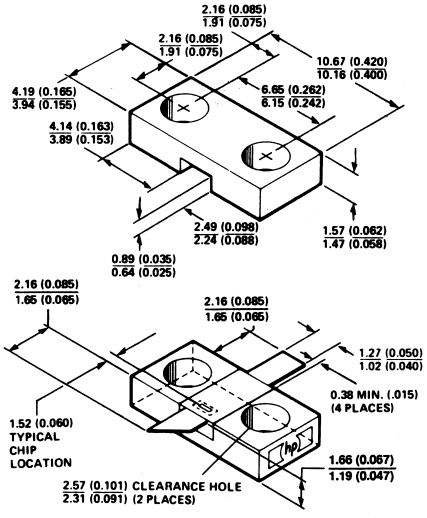
5082-3071

Features

- **High Power Handling Capability**
  50 W Peak Pulse Power
- **Low Intermodulation Products**
  Typical 0.2 W Threshold Assures Wide Dynamic Linear Range
- **Broad Bandwidth**
  500 MHz to 10 GHz
- **Low Insertion Loss**
  Less than 1 dB in X-band
- **Easy to Use**
  Package Compatible with Stripline and Microstrip
- **Negligible Spike Leakage**

Description/ Applications

The HP 5082-3071 passive limiter chip is functionally integrated into a 50 Ω transmission line to provide a broadband, linear, low insertion loss transfer characteristic for small signal levels. At higher signal levels self-rectification reduces the diode resistance to provide limiting as shown in Figure 2. Limiter performance is practically independent of temperature over the rated temperature range.



DIMENSIONS IN MILLIMETERS AND (INCHES)

Outline 61

Maximum Ratings

Junction Operating and Storage Temperature Range ..... -65°C to +125°C
Power Dissipation[1] ..... 1.0 W
Peak Incident Pulse Power[2] ..... 50 W
Peak Inverse Voltage ..... 50 V
Soldering Temperature ..... 230°C for 5 sec

Notes:

1. Device properly mounted in sufficient heat sink at T_A = 25°C, derate linearly to zero at maximum operating temperature.
2. t_p = 1 μs, f = 10 GHz, Du = 0.001, Z_O = 50 Ω, T_A = 25°C.

The 5082-3071 limiter module is designed for applications in telecommunication equipment, ECM receivers, distance measuring equipment, radar receivers, telemetry equipment, and transponders operating anywhere in the frequency range from 500 MHz through 10 GHz. An external dc return is required for self bias operation. This dc return is often present in the existing circuit, i.e. inductively coupled antennas, or it can be provided by a $\lambda/4$ resonant shunt transmission line. Selection of a high characteristic impedance for the shunt transmission line affords broadband operation. Another easy to realize dc return consists of a small diameter wire connected at a right angle to the electric field in a microstrip or stripline circuit. A 10 mA forward current will actuate the PIN diode as a shunt switch providing approximately 20 dB of isolation.

Mechanical Specifications

The cover channel supplied with each diode should be used in balanced stripline circuits in order to provide good electrical continuity from the upper to the lower ground plane through the package base metal. Higher order modes will be excited if this cover is left off or if poor electrical contact is made to the ground plane.

The package transmission channel is filled with epoxy resin which combines a low expansion coefficient with high chemical stability. Outline 61 has a gold plated copper body with gold plated Kovar leads.

Electrical Specifications at $T_A = 25°C$

Part Number 5082-	Package Outline	Heat Sink	Maximum Insertion Loss (dB)	Maximum SWR	Maximum RF Leakage Power (W)	Typical Recovery Time (ns)
3071	61	Cathode	1.2	2.0	1.0	100
Test Conditions			P_{in} = 0 dBm f = 9.4 GHz	P_{in} = 0 dBm f = 9.4 GHz	P_{in} = 50 W 1 µsec f = 9.4 GHz	P_{in} = 50 W 1 µsec

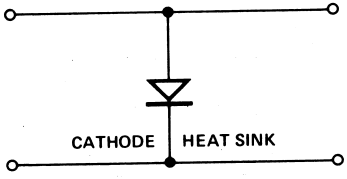


Figure 1. Heat Sink Polarity.

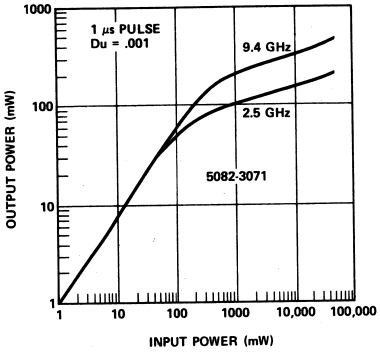


Figure 2. Typical Pulse Limiting Characteristics.

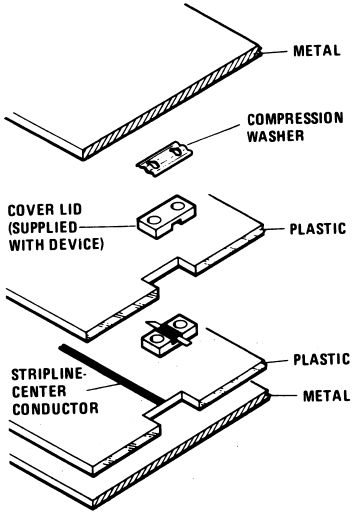


Figure 3. Suggested Stripline Assembly.

HEWLETT PACKARD

Stripline PIN Diode Switches/ Attenuators

5082-3040
5082-3041
5082-3340

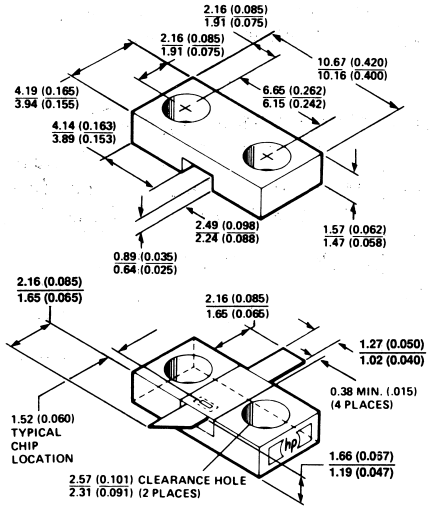
Features

- **Low Cost to Use**
  Designed for Easy Mounting
- **Broadband Operation**
  HF Through X-Band
- **Low Insertion Loss**
  Less than 0.5 dB to 10 GHz (5082-3040, -3340)
- **High Isolation**
  Greater than 20 dB to 10 GHz
- **Fast Switching/Modulation**
  5 ns Typical (5082-3041)
- **Low Drive Current Required**
  Less than 20 mA for 20 dB Isolation (5082-3041)

Description/ Applications

These diodes are designed for applications in microwave and HF-UHF systems using stripline or microstrip transmission line techniques.

Typical circuit functions performed consist of switching, duplexing, multiplexing, leveling, modulating, limiting, or gain control functions as required in TR switches, pulse modulators, phase shifters, and amplitude modulators operating in the frequency range from HF through Ku-Band.



DIMENSIONS IN MILLIMETERS AND (INCHES)

Outline 61

Maximum Ratings

Part No. 5082-	-3040, -3340	-3041
Junction Operating and Storage Temperature Range	-65°C to +125°C	-65°C to +125°C
Power Dissipation[1]	2.5 W	1.0 W
Peak Incident Pulse Power[2]	225 W	50 W
Peak Inverse Voltage	150 V	70 V
Soldering Temperature	230°C for 5 sec	

Notes:

1. Device properly mounted in sufficient heat sink at 25°C, derate linearly to zero at maximum operating temperature.
2. t_p = 1 μs, f = 10 GHz, Du = 0.001, Z_O = 50 Ω, T_A = 25°C.

These diodes provide nearly ideal transmission characteristics from HF through Ku-Band.

The 5082-3340 is a reverse polarity device with characteristics similar to the 5082-3040. The 5082-3041 is recommended for applications requiring fast switching or high frequency modulation of microwave signals, or where the lowest bias current for the maximum attenuation is required.

More information is available in HP AN 922 (Applications of PIN Diodes) and 929 (Fast Switching PIN Diodes).

Mechanical Specifications

The cover channel supplied with each diode should be used in balanced stripline circuits in order to provide good electrical continuity from the upper to the lower ground plane through the package base metal. Higher order modes will be excited if this cover is left off or if poor electrical contact is made to the ground plane.

The package transmission channel is filled with epoxy resin which combines a low expansion coefficient with high chemical stability. Outline 61 has a gold plated copper body with gold plated Kovar leads.

Electrical Specifications at $T_A = 25°C$

Part Number 5082-	Package Outline	Heat Sink	Min. Isolation (dB)	Max. Insertion Loss (dB)	Max. SWR	Max. Reverse Recovery Time t_{rr} (ns)	Typical Carrier Lifetime τ (ns)	Typical CW Power Switching Capability P_A (W)
3040	61	Anode	20	0.5	1.5	–	400	30
3041	61	Cathode	20	1.0	1.5	10	35*	13
3340	61	Cathode	20	0.5	1.5	–	400	30
Test[1] Conditions	–	–	I_F = 100 mA (Except 3041; I_F = 20 mA)	I_F = 0 P_{in} = 1 mW	I_F = 0 P_{in} = 1 mW	I_F = 20 mA V_R = 10 V Recovery to 90%	I_F = 50 mA I_R = 250 mA *I_F = 10 mA *I_R = 6 mA	–

Note:
1. Test Frequencies: 8 GHz 5082-3041; 10 GHz 5082-3040, and -3340.

Typical Parameters

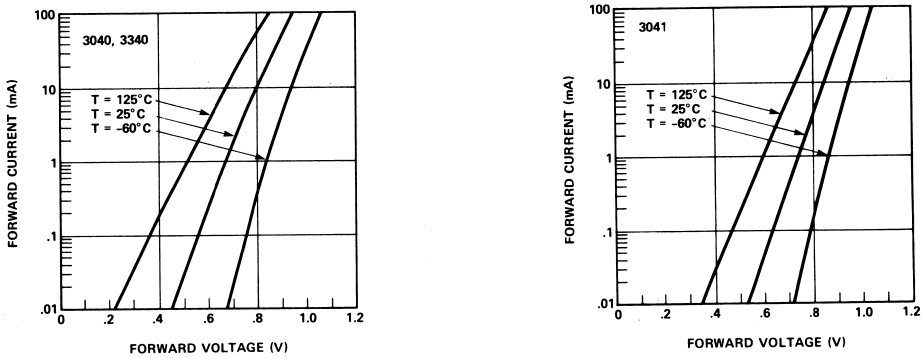


Figure 1. Typical Forward Characteristics.

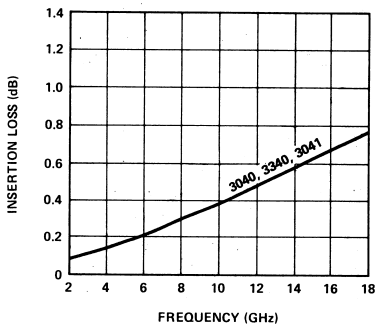


Figure 2. Typical Insertion Loss vs. Frequency.

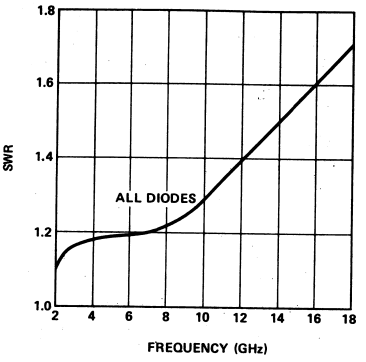


Figure 3. Typical SWR vs. Frequency.

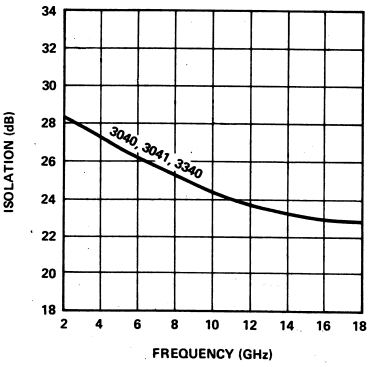


Figure 4. Typical Isolation vs. Frequency.

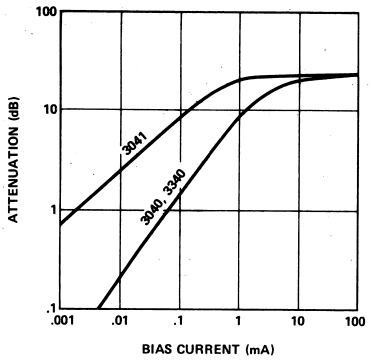
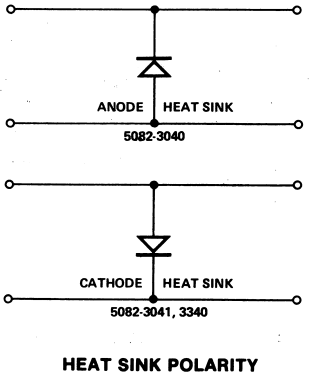


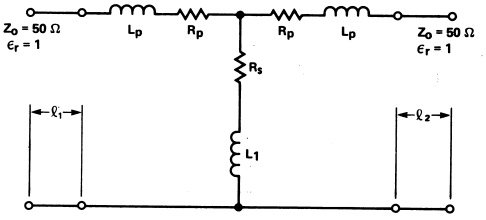
Figure 5. Typical Attenuation above Zero Bias Insertion Loss vs. Bias Current at f = 8 GHz.



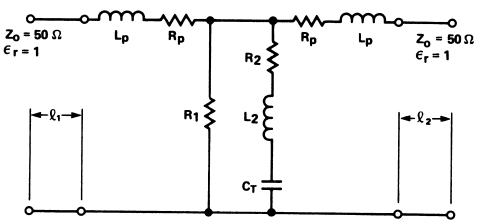
HEAT SINK POLARITY

Equivalent Circuits

Forward Bias (Isolation State)



Zero Bias (Insertion Loss State)



Typical Equivalent Circuit Parameters–Forward Bias

Part Number 5082-	Lp (pH)	Rp (Ω)	Rs (Ω)	L_1 (pH)	1 (mm)	2 (mm)
3040, 3340	200	0.25	1.0	20	2.4	5.0
3041	220	0.25	1.0	20	2.4	5.0

Typical Equivalent Circuit Parameters–Zero Bias

Part Number 5082-	Lp (pH)	Rp (Ω)	R_1 (KΩ)	L_2 (pH)	R_2 K(Ω)	C_T (pF)	1 (mm)	2 (mm)
3040, 3340	200	0.25	∞	0	5.0	0.10	2.4	5.0
3041	220	0.25	∞	0	1.5	0.15	2.4	5.0

Typical Switching Parameters

RF Switching Speed HP 5082-3041

The RF switching speed of the HP 5082-3041 may be considered in terms of the change in RF isolation at 2 GHz. This switching speed is dependent upon the forward bias current, reverse bias drive pulse, and characteristics of the pulse source. The RF switching speed for the shunt-mounted stripline diode in a 50 Ω system is considered for two cases: one driving the diode from the forward bias state to the reverse bias state (isolation to insertion loss), second, driving the diode from the reverse bias state to the forward bias state (insertion loss to isolation).

The total time it takes to switch the shunt diode from the isolation state (forward bias) to the insertion loss state (reverse bias) is shown in Figure 6. These curves are for three forward bias conditions with the diode driven in each case with three different reverse voltage pulses (V_{PR}). The total switching time for each case includes the delay time (pulse initiation to 20 dB isolation) and transition time (20 dB isolation to 0.9 dB isolation). Slightly faster switching times may be realized by spiking the leading edge of the pulse or using a lower impedance pulse driver.

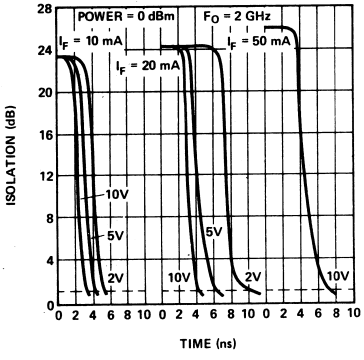


Figure 6. Isolation vs. Time (Turn-on) for HP 5082-3041. Frequency, 2 GHz.

The time it takes to switch the diode from zero or reverse bias to a given isolation is less than the time from isolation to the insertion loss case. For all cases of forward bias generated by the pulse generator (positive pulse), the RF switching time from the insertion loss state to the isolation state was less than 2 nanoseconds. A more detailed treatise on switching speed is published in AN929 "Fast Switching PIN Diodes".

Reverse Recovery Time

Shown below is reverse recovery time, (t_{rr}) vs. forward current, (I_F) for various reverse pulse voltages V_R. The circuit used to measure t_{rr} is shown in Figure 7.

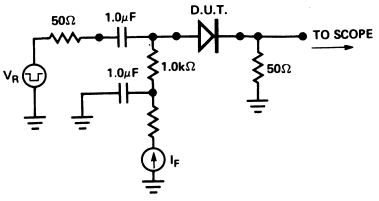


Figure 7. Basic t_{rr} Test Setup.

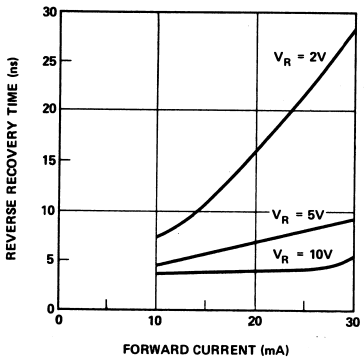


Figure 8. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages, 5082-3041.

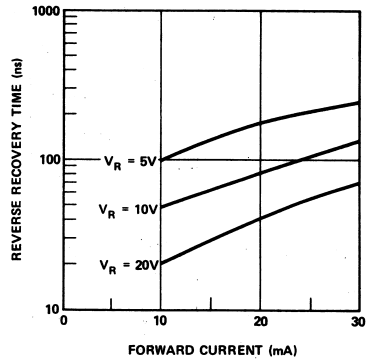


Figure 9. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages, 5082-3340.

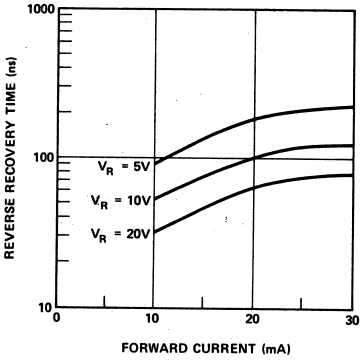


Figure 10. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages, 5082-3040.

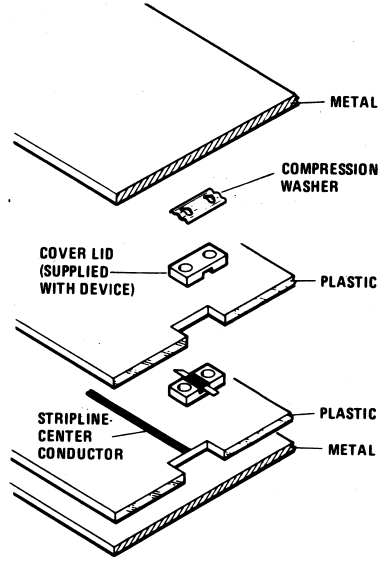


Figure 11. Suggested Stripline Assembly.

HEWLETT PACKARD

PIN Diodes for RF Power Switching/Attenuating

Technical Data

5082-3101
5082-3102
5082-3201
5082-3202
5082-3303
5082-3304

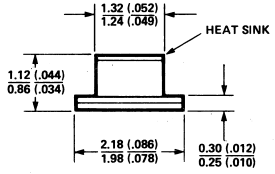
Features

- **High Isolation**
  Greater than 25 dB
- **Low Insertion Loss**
- **High Control Signal Dynamic Range**
  10,000: 1 RF Resistance Change
- **Low Harmonic Distortion**
- **Both Anode and Cathode Heat Sink Models Available**

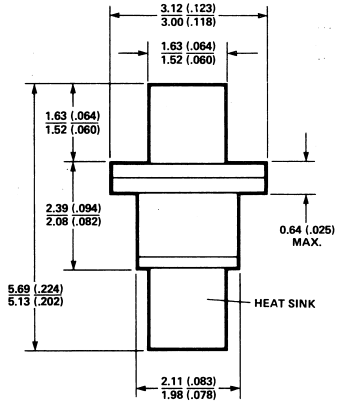
Description/ Applications

HP 5082-3101/02, 5082-3201/02, 5082-3303/04 PIN diodes are silicon devices manufactured using modern processing techniques to provide optimum characteristics for RF switching, signal conditioning and control. These devices are of planar passivated design. Both anode and cathode heat sink models are available.

PIN diodes provide a variable RF resistance with DC bias current. The main advantages of a PIN diode over PN switching diodes are the low forward resistance and the low device capacitance.



Outline 38



Outline 31

Maximum Ratings

Junction Operating and Storage
Temperature Range ..... -65°C to +150°C
DC Power Dissipation at 25°C
(Derate linearly to zero at 150°C)
HP 5082-3101, 3102 ..... 1.0 W
HP 5082-3201, 3202, 3303, 3304 ..... 3.0 W

These HP PIN diodes are intended for use in RF switching, multiplexing, modulating, phase shifting, and attenuating applications from approximately 10 MHz to frequencies well into the microwave region. Due to their low parasitic capacitance and inductance, both HP Package Outline 31 and 38 are well suited for broadband circuits up to 1 GHz and for resonated circuits up to 8 GHz.

These devices are especially useful where the lowest residual series resistance and junction capacitance are required for high on-to-off switching ratios.

Mechanical Specifications

The HP Package Outline 31 has a metal ceramic hermetic seal. The heat sink stud is gold-plated copper. The opposite stud is gold-plated kovar. Typical package inductance is 1.0 nH and typical package capacitance is 0.2 pF.

The HP Package Outline 38 also has a metal ceramic hermetic seal. The heat sink contact is gold plated copper. The opposite contact is gold-plated kovar. Typical package inductance is 0.4 nH and typical package capacitance is 0.2 pF.

The maximum soldering temperature for diodes in either package is 230°C for 5 seconds.

RF Power Switching/Attenuating

Electrical Specifications at T_A = 25°C

Part Number 5082-	Package Outline	Heat Sink	Minimum Breakdown Voltage V_{BR} (V)	Maximum Total Capacitance C_T (pF)	Maximum Residual Series Resistance R_S (Ω)	Minimum Carrier Lifetime τ (ns)	Typical Reverse Recovery Time t_{rr} (ns)	Typical CW Power Handling Capability P_A (W)
3101	38	Anode	200	0.32	1.2	100	100	40
3102	38		300	0.30	1.2	100	100	40
3201	31		200	0.35	1.2	100	100	120
3202	31		300	0.32	1.2	100	100	120
3303	31	Cathode	200	0.40	1.2	100	100	120
3304	31		250	0.32	1.2	100	100	120
Test Conditions			$V_R = V_{BR}$, meas. $I_R \leq 10$ μA	V_R = 50 V, f = 1 MHz	I_F = 100 mA f = 100 MHz	I_F = 50 mA I_R = 250 mA	I_F = 20 mA V_R = 10 V 90% Recovery	Series* Switch in 50 Ω System

*Divide by four for a shunt switch.

Typical Parameters

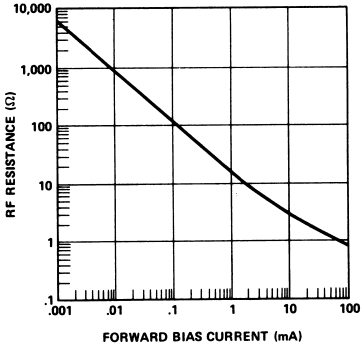


Figure 1. Typical RF Resistance vs. Forward Bias Current.

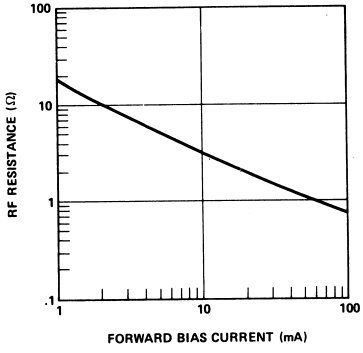


Figure 2. Typical RF Resistance vs. Forward Bias Current.

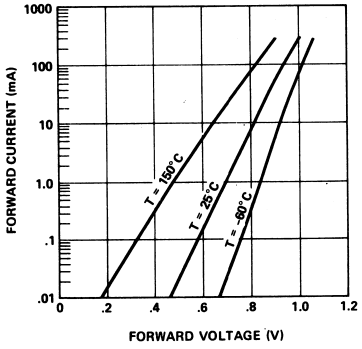


Figure 3. Typical Forward Characteristics.

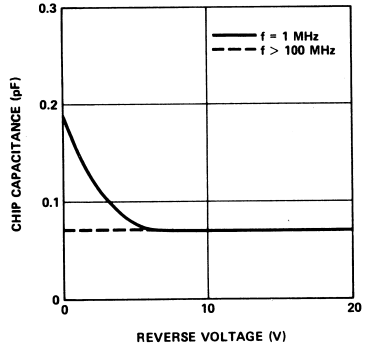
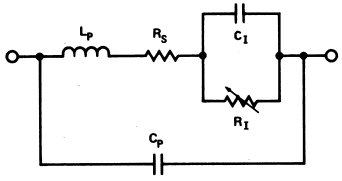


Figure 4. Typical Chip Capacitance vs. Reverse Voltage.



C_P = Package Capacitance
L_P = Package Inductance
R_S = Residual Series Resistance
R_I = I-Layer Resistance
C_I = I-Layer Capacitance

TYPICAL VALUES FOR C_P AND L_P ARE GIVEN UNDER "MECHANICAL SPECIFICATIONS". WITH REVERSE BIAS, $R_I \geq 10^6\ \Omega$. TOTAL CAPACITANCE IS C_T AND IS GIVEN IN "ELECTRICAL SPECIFICATIONS". WITH FORWARD BIAS C_I IS NO LONGER PRESENT. R_I DECREASES WITH INCREASING FORWARD BIAS TO APPROXIMATELY ZERO AT 100 mA.

Figure 5. Device Equivalent Circuit.

HEWLETT PACKARD

Hermetic PIN Diodes for Stripline/Microstrip Switches/ Attenuators

Technical Data

5082-3140
5082-3141
5082-3170

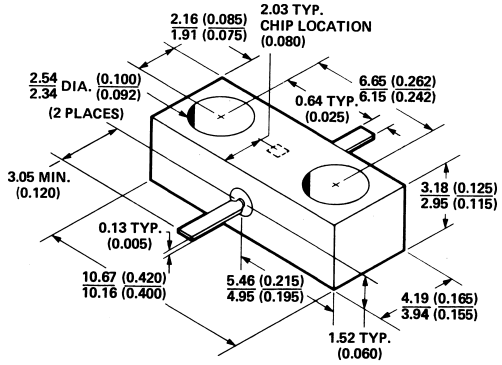
Features

- **Broadband Operation**
  HF through X-Band
- **Low Insertion Loss**
  Less than 0.5 dB to 10 GHz (5082-3140, -3170)
- **High Isolation**
  Greater than 20 dB to 10 GHz (5082-3140, -3170)
- **Fast Switching/Modulation**
  5 ns Typical (5082-3141)
- **Low Drive Current Required**
  Less than 20 mA for 20 dB Isolation (5082-3141)

Description/ Applications

The HP 5082-3140 and -3170 are passivated planar devices and the 5082-3141 is a passivated mesa device. All are in a shunt configuration in hermetic stripline packages which are suitable for Hi-Rel applications. These diodes are optimized for good continuity of characteristic impedance which allows a continuous transition when used in 50 Ω microstrip or stripline circuits.

These diodes are designed for applications in microwave and HF-UHF systems using stripline or microstrip transmission line techniques.



DIMENSIONS IN MILLIMETERS AND (INCHES)

Outline 60

Maximum Ratings

Part No. 5082-	-3140, -3170	-3141
Junction Operating and Storage Temperature Range	-65°C to +150°C	-65°C to +150°C
Power Dissipation[1]	1.75 W	0.75 W
Peak Incident Pulse Power[2]	225 W	50 W
Peak Inverse Voltage	150 V	70 V
Soldering Temperature	230°C for 5 sec.	

Notes:

1. Device properly mounted in sufficient heat sink at 25°C, derate linearly to zero at maximum operating temperature.
2. t_p = 1 μs, f = 10 GHz, Du = 0.001, Z_O = 50 Ω, T_A = 25°C.

Typical circuit functions performed consist of switching, duplexing, multiplexing, leveling, modulating, limiting, or gain control functions as required in TR switches, pulse modulators, phase shifters, and amplitude modulators operating in the frequency range from HF through Ku-Band. These diodes provide nearly ideal transmission characteristics from HF through Ku-Band.

The 5082-3170 is a reverse polarity device with characteristics similar to the 5082-3140.

The 5082-3141 is recommended for applications requiring fast switching or high frequency modulation of microwave signals, or where the lowest bias current for maximum attenuation is required.

More information is available in HP Application Note 922 (Applications of PIN Diodes) and 929 (Fast Switching PIN Diodes).

Mechanical Specifications

Package Outline 60 is hermetically sealed and capable of meeting the stringent requirements of space level high reliability testing. Both the package and lead materials are gold plated Kovar.

Electrical Specifications at $T_A = 25°C$

Part Number 5082-	Package Outline	Heat Sink	Min. Isolation (dB)	Max. Insertion Loss (dB)	Max. SWR	Max. Reverse Recovery Time t_{rr} (ns)	Typical Carrier Lifetime τ (ns)	Typical CW Power Switching Capability P_A (W)
3140	60	Anode	20	0.5	1.5	–	400	30
3141	60	Cathode	20	1.0	1.5	10	35*	13
3170	60	Cathode	20	0.5	1.5	–	400	30
Test[1] Conditions	–	–	I_F = 100 mA (Except 3141; I_F = 20 mA)	I_F = 0 P_{in} = 1 mW	I_F = 0 P_{in} = 1 mW	I_F = 20 mA V_R = 10 V Recovery to 90%	I_F = 50 mA I_R = 250 mA *I_F = 10 mA *I_R = 6 mA	–

Note:
1. Test Frequencies: 8 GHz 5082-3141; 10 GHz 5082-3140, and -3170.

Typical Parameters

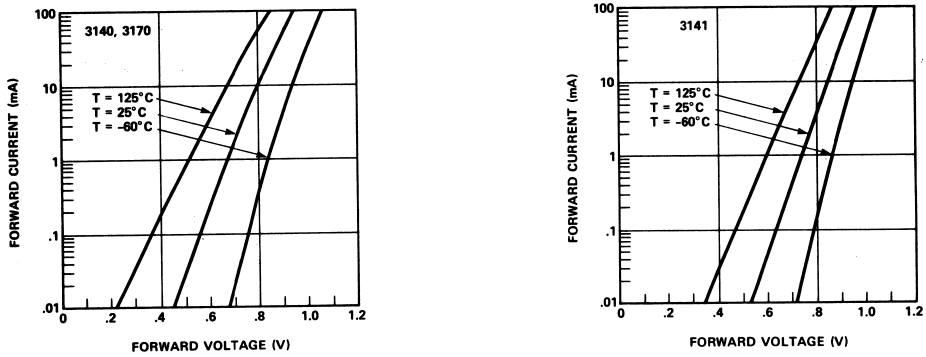


Figure 1. Typical Forward Characteristics.

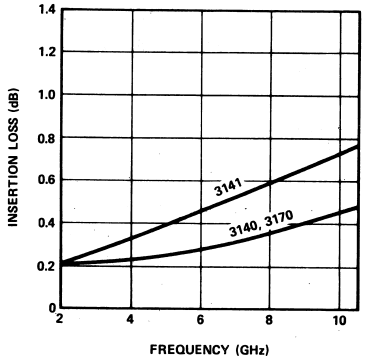


Figure 2. Typical Insertion Loss vs. Frequency.

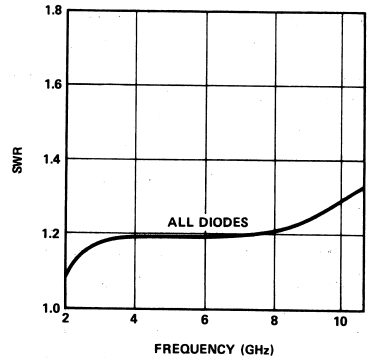


Figure 3. Typical SWR vs. Frequency.

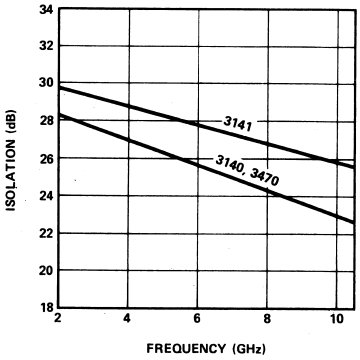


Figure 4. Typical Isolation vs. Frequency.

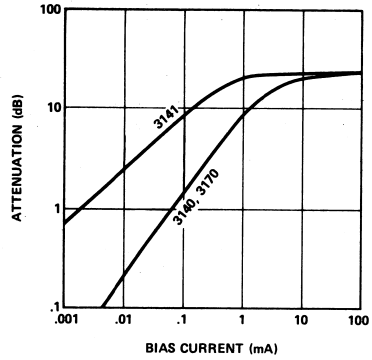
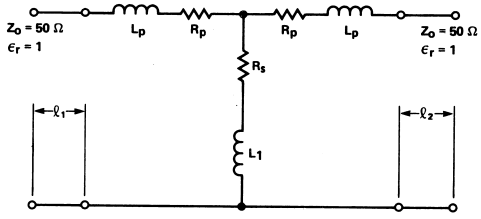


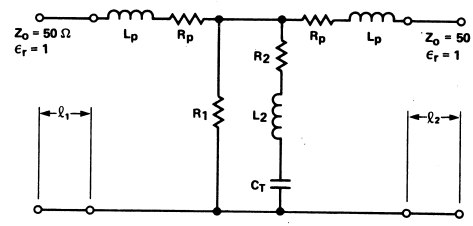
Figure 5. Typical Attenuation Above Zero Bias Insertion Loss vs. Bias Current at f = 8 GHz.

Equivalent Circuits

Forward Bias (Isolation State)



Zero Bias (Insertion Loss State)



Typical Equivalent Circuit Parameters–Forward Bias

Part Number 5082-	Lp (pH)	Rp (Ω)	Rs (Ω)	L_1 (pH)	1 (mm)	2 (mm)
3140, 3170	150	0.0	0.95	30	3.8	3.8
3141	150	0.0	0.8	20	3.8	3.8

Typical Equivalent Circuit Parameters–Zero Bias

Part Number 5082-	Lp (pH)	Rp (Ω)	R_1 (KΩ)	L_2 (pH)	R_2 K(Ω)	C_T (pF)	1 (mm)	2 (mm)
3140, 3170	30	0.0	1.2	16	0.0	0.20	5.3	5.3
3141	200	0.0	∞	0	0.4	0.14	4.4	4.4

Typical Switching Parameters

RF Switching Speed HP 5082-3141

The RF switching speed of the HP 5082-3141 may be considered in terms of the change in RF isolation at 2 GHz. This switching speed is dependent upon the forward bias current, reverse bias drive pulse, and characteristics of the pulse source. The RF switching speed for the shunt-mounted stripline diode in a 50 Ω system is considered for two cases, one driving the diode from the forward bias state to the reverse bias state (isolation to insertion loss), second driving the diode from the reverse bias state to the forward bias state (insertion loss to isolation).

The total time it takes to switch the shunt diode from the isolation state (forward bias) to the insertion loss state (reverse bias) is shown in Figure 6. These curves are for three forward bias conditions with the diode driven in each case with three different reverse voltage pulses (V_{PR}). The total switching time for each case includes the delay time (pulse initiation to 20 dB isolation) and transition time (20 dB isolation to 0.9 dB isolation). Slightly faster switching times may be realized by spiking the leading edge of the pulse or using a lower impedance pulse driver.

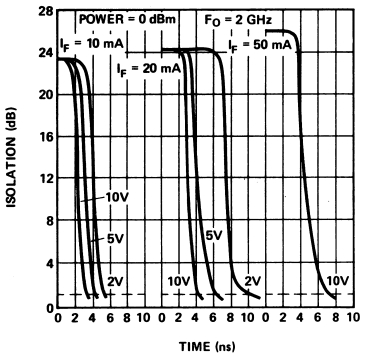


Figure 6. Isolation vs. Time (Turn-on) for HP 5082-3141. Frequency, 2 GHz.

The time it takes to switch the diode from zero or reverse bias to a given isolation is less than the time from isolation to the insertion loss case. For all cases of forward bias generated by the pulse generator (positive pulse), the RF switching time from the insertion loss state to the isolation state was less than 2 nanoseconds. A more detailed treatise on switching speed is published in AN929: "Fast Switching PIN Diodes".

Reverse Recovery Time

Shown below is reverse recovery time, (t_{rr}) vs. forward current, (I_F) for various reverse pulse voltages V_R. The circuit used to measure t_{rr} is shown in Figure 7.

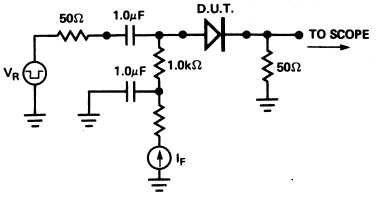


Figure 7. Basic t_{rr} Test Setup.

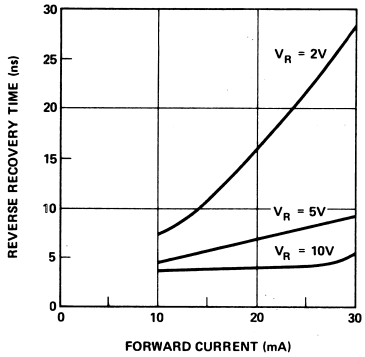


Figure 8. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages, 5082-3141.

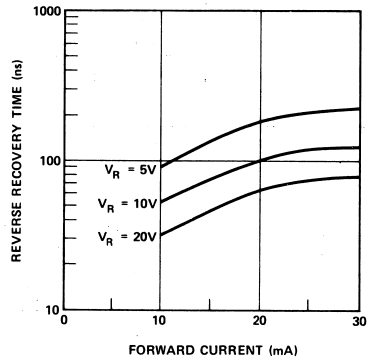


Figure 9. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages, 5082-3140.

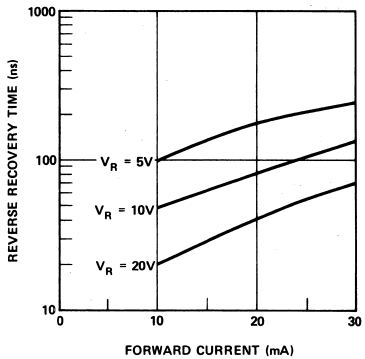


Figure 10. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages, 5082-3170.

HEWLETT PACKARD

PIN Diodes for Fast Switching and Attenuating

Technical Data

5082-3305
5082-3306

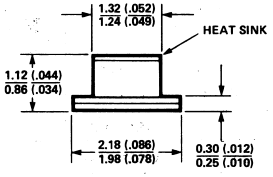
Features

- **Nanosecond Switching Time**
  Typically Less than 5 ns
- **Low Residual Series Resistance**
  Less than 1 Ω
- **Low Drive Current Required**
  Less than 20 mA for 1 Ω R_S
- **High Power Limiting Capability**
  50 W Peak Pulse Power
- **Cathode Heat Sink**

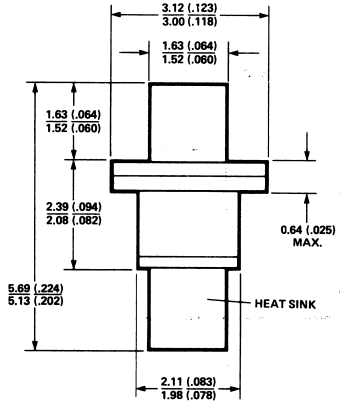
Description/ Applications

The HP 5082-3305 and 5082-3306 are passivated silicon PIN diodes of mesa construction. Precisely controlled processing provides an exceptional combination of fast RF switching and low residual series resistance.

These HP PIN diodes provide unique benefits in the high isolation to insertion loss ratio afforded by the low residual resistance at low bias currents and the ultra-fast recovery realized through lower stored charge. Where low drive power is desired these diodes provide excellent performance at very low bias currents.



Outline 38 (5082-3305)



DIMENSIONS IN MILLIMETERS AND (INCHES).

Outline 31 (5082-3306)

Maximum Ratings

Junction Operating and Storage Temperature Range ..... -65°C to +150°C
DC Power Dissipation at T_{CASE} = 25°C
(Derate linearly to zero at 150°C)
HP 5082-3305 ..... 0.7 W
HP 5082-3306 ..... 1.25 W

The HP 5082-3305 and 5082-3306 ceramic package PIN diodes are intended for controlling and processing microwave signals up to Ku band. Typical applications include single and multi-throw switches, pulse modulators, amplitude modulators, phase shifters, duplexers, diplexers, and TR switches.

Mechanical Specifications

The HP Package Outline 31 has a metal ceramic hermetic seal. The heat sink stud is gold-plated copper. The opposite stud is gold-plated kovar. Typical package inductance is 1.0 nH and typical package capacitance is 0.2 pF.

The HP Package Outline 38 also has a metal ceramic hermetic seal. The heat sink contact is gold plated copper. The opposite contact is gold-plated kovar. Typical package inductance is 0.4 nH and typical package capacitance is 0.2 pF.

The maximum soldering temperature for diodes in either package is 230°C for 5 seconds.

Fast Switching/Attenuating Electrical Specifications at $T_A = 25°C$

Part Number 5082-	Package Outline	Heat Sink	Minimum Breakdown Voltage V_{BR} (V)	Maximum Total Capacitance C_T (pF)	Maximum Series Resistance RS (Ω)	Maximum Reverse Recovery Time t_{rr} (ns)
3305	38	Cathode	70	0.4	1.0	10.0
3306	31	Cathode	70	0.45	1.0	10.0
Test Conditions			$V_R = V_{BR}$, meas. $I_R \leq 10\ \mu A$	f = 1 MHz V_R = 20 V	f = 100 MHz I_F = 20 mA	I_F = 20 mA V_R = 10 V 90% Recovery

Typical Parameters

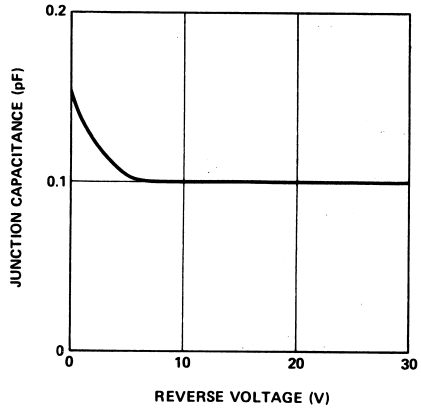


Figure 1. Typical Junction Capacitance vs. Reverse Voltage.

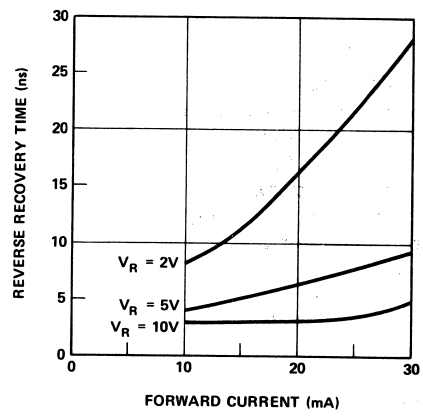


Figure 2. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages.

Typical Parameters (cont.)

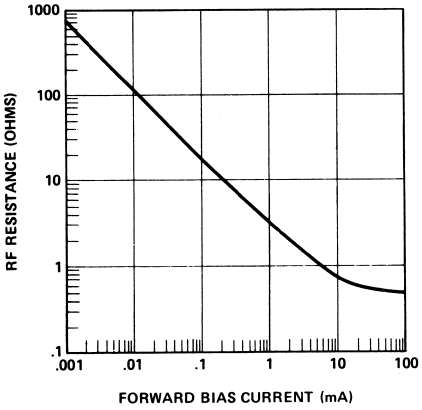


Figure 3. Typical RF Resistance vs. Forward Bias Current.

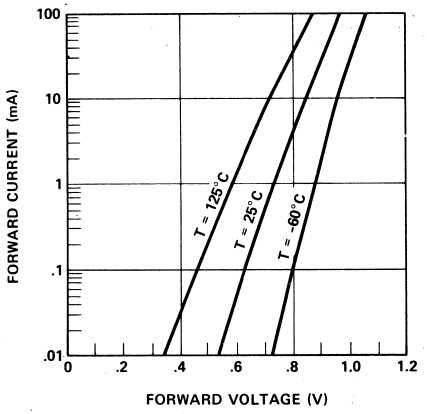


Figure 4. Typical Forward Current vs. Forward Voltage.

HEWLETT PACKARD

Beam Lead PIN Diodes

Reliability Data

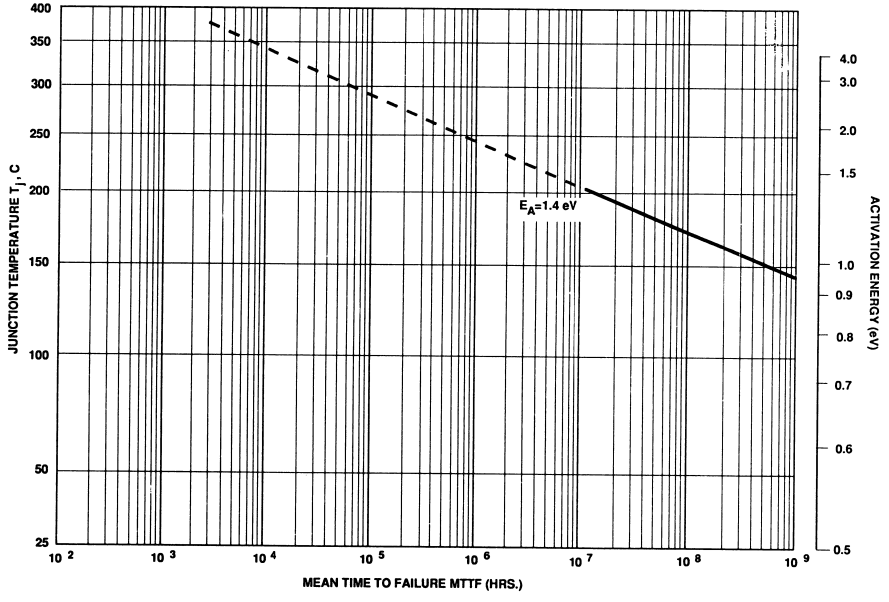
HPND-4005
HPND-4018
HPND-4028
HPND-4038
HPND-4050

Description

For applications requiring component reliability estimation, Hewlett-Packard provides reliability data for all families of devices. Data is initially compiled from reliability tests run prior to market introduction to demonstrate that a product meets design criteria. Additional tests are run periodically. The data on this sheet represents the latest review of accumulated test results.

Applications

This information represents the capabilities of the generic device. Failure rates and MTTF values presented here are achievable with normal MIL-S-19500 TX level screening. Reliability can only be guaranteed by testing specified lots of devices, under specified conditions, with specified LTPD levels.



Mean Time to Failure vs. Junction Temperature

Burn-In and Storage

Test	Test Conditions	LTPD/ 1000 Hours
High Temperature Life	1,000 hrs. min. storage time @ 200°C	3
Steady State Operating Life	1,000 hrs. min. operating time @ I_F = 30 mA, T_A = 150°C	3

Environmental

Test	MIL-STD-750 Reference	Test Conditions	LTPD
Temperature Cycling	1051	-65/+200°C, 100 cycles, 10 min. dwell, 5 min. transfer	7
Thermal Shock	1056	0/100°C, 100 cycles, 10 min. dwell, 10 sec. transfer	7
Moisture Resistance	1021	98% RH, -10°C/+65°C, 10 days	7
Constant Acceleration	2006	20 KGs, 1 min. each axis	7
Mechanical Shock	2016	5 blows each axis at X, Y, Z, 1500 Gs, 0.5 msec pulse	7
Vibration Variable Frequency	2056	20 Gs min., 100 to 2000 Hz, 4 minute cycles each axis X, Y, Z	7
Salt Atmosphere	1041	Salt Fog at 35°C for 24 hrs.	10

HEWLETT PACKARD

Surface Mount PIN Diodes

Reliability Data

HPND-000X Series
5082-0012
HSMP-3800 Series
HSMP-3810 Series
HSMP-3820 Series
HSMP-3830 Series

The following cumulative test results have been obtained from testing performed at Hewlett-Packard Communications Components Division in accordance with the latest revision of MIL-STD-750. Data was gathered from the product qualification, reliability monitor, and engineering evaluation. For the purpose of this reliability data sheet, a failure is any part which fails to meet the electrical and/or mechanical specification listed in this catalog.

1. Life Test

A. Demonstrated Performance

Test	Test Conditions	Units Tested	Total Device Hrs.	Total Failed	Failure Rate 1%/1K Hrs.
High Temp. Rev. Bias (HTRB)	V_R = 80% V_{BR}, T_A = 150°C	342	347,920	0	0
Operating Life (O.L.)	T_A = 25°C, P_{FM} = 250 mW V_R = 80% V_{BR}, 60 Hz	342	264,325	0	0
High Temp. Storage (HTS)	T_A = 150°C	505	511,390	0	0

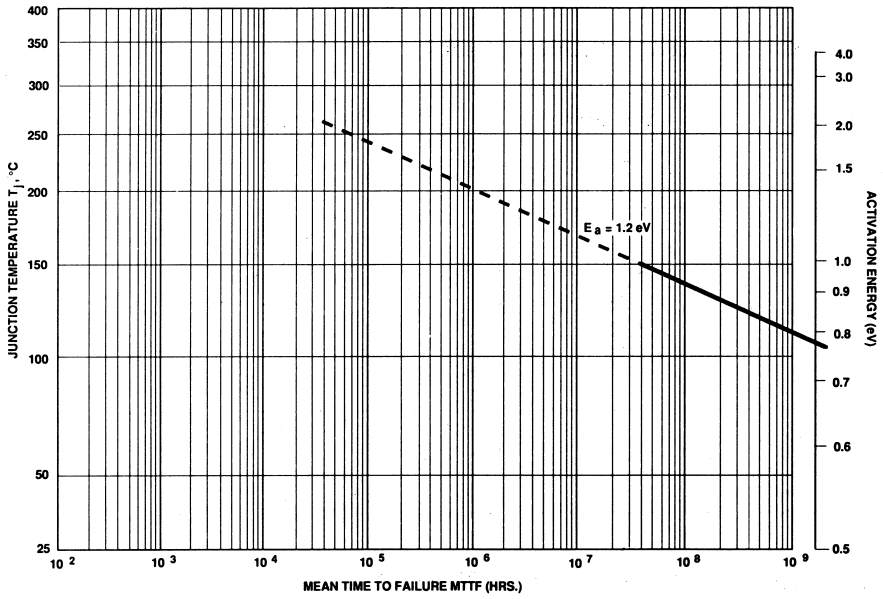
B. Failure Rate Prediction

The failure rate will depend on the junction temperature of the device. The estimated life at different temperatures is calculated, using the Arrhenius plot with activation energy of 1.2 eV, and listed in the following table.

Junction Temp. T_J** (°C)	Point[1]		90% Confidence Level[2]	
	MTTF* (Hours)	FIT[3]	MTTF (Hours)	FIT[3]
150°C	3.5×10^7	28.0	1.5×10^7	66.7
130°C	2.0×10^8	5.0	8.7×10^7	11.5
110°C	1.5×10^9	0.67	6.5×10^8	1.5
90°C	1.0×10^{10}	0.10	4.3×10^9	0.23
75°C	1.0×10^{11}	0.01	4.3×10^{10}	0.023
50°C	2.0×10^{12}	0.0005	8.7×10^{11}	0.0011

*MTTF data collected in Hermetic Package.
**T_J was calculated using a θ_{JA} of 500°C/W.

Notes:
1. The point MTTF is simply the total device hours divided by the number of failures.
2. The MTTF and failure rate represent the performance level for which there is a 90% probability of the device doing better than the stated value. The confidence level is based on the statistics of failure distribution. The assumed distribution is exponential. This particular distribution is commonly used in describing useful life failures.
3. FIT is defined as Failure in Time, or specifically, failures per billion hours. The relationship between MTTF and FIT is as follows: FIT = 10^9/(MTTF).



C. Example of Failure Rate Calculation

At 50°C with a device operating 8 hours a day, 5 days a week, the percent utilization is:

% Utilization = (8 hrs/day x 5 days/wk) ÷ 168 hrs/wk ≡ 25%

Then the point failure rate per year is:

$(5 \times 10^{-13}/\text{hr}) \times (25\%) \times (8760\ \text{hrs/yr}) = 1.1 \times 10^{-7}\%$ per year

Likewise, the 90% confidence level failure rate per year is:

$(1.1 \times 10^{-12}/\text{hr}) \times (25\%) \times (8760\ \text{hrs/yr}) = 2.4 \times 10^{-7}\%$ per year

2. Environmental and Mechanical Tests

Test	MIL-STD-750 Reference	Test Conditions	Units Tested	Total Failed
Solderability	2026	235°C, 5 seconds	350	0
Solder Heat	2031	260°C, 10 seconds	302	0
Resistance to Solvent	1022	4 Solvent Groups	62	0
Autoclave	HP GSS 12-109	121°C, 15 PSIG, 96 hrs.	780	0
Moisture Resistance	HP GSS 12-107, Method B	85°C/85% RH, biased, 1000 hrs.	336	0
Thermal Shock	1056	-65/150°C, 5 min dwell, 200 cycles	336	0
Temperature Cycle	1051	-65/150°C, 10 min dwell, 200 cycles	336	0
Lead Integrity		2.0 pounds minimum	140	0

3. Flammability Test (MIL-STD-202, Method 111):

Meets Needle Flame Test per UL Category D
(Flaming Time <3 sec.) under material classification 94V0.

4. DOD-HDBK-1686A ESD Classification:

HPND-0003, HSMP-3820	Class I
HPND-0001, HSMP-3800	Class I
HPND-0002, HSMP-3810	Class I
5082-0012, HSMP-3830	Class I

HEWLETT PACKARD

PIN Diodes

Reliability Data

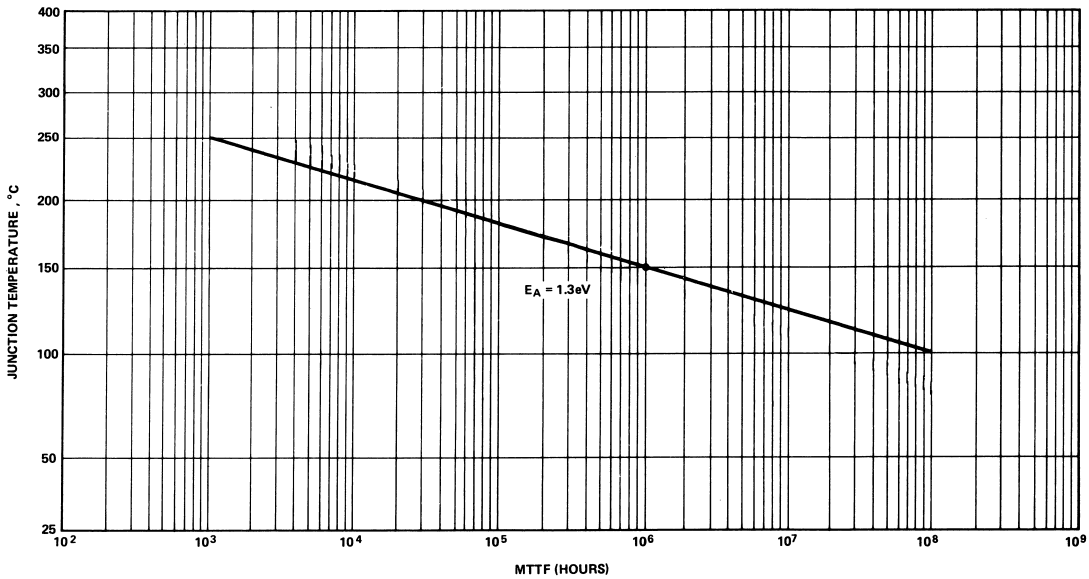
1N5719
5082-3001
5082-3002
5082-3039
5082-3077
HPND-4165
HPND-4166

Description

For applications requiring component reliability estimation, Hewlett-Packard provides reliability data for all families of devices. Data is initially compiled from reliability tests run prior to market introduction to demonstrate that a product meets design criteria. Additional tests are run periodically. The data on this sheet represents the latest review of accumulated test results.

Applications

This information represents the capabilities of the generic device. Failure rates and MTTF values presented here are achievable with normal MIL-S-19500 TX level screening. Reliability can only be guaranteed by testing specified lots of devices, under specified conditions, with specified LTPD levels.



Mean Time to Failure vs. Junction Temperature

Burn-In and Storage

Test	Test Conditions	LTPD/ 1000 Hours
High Temperature Life	1,000 hrs. min. storage time @ 150°C	3
Steady State Operating Life	1,000 hrs. min. operating time @ P_{FM} = 250 mW, $V_{RM} \approx$ 150 V, f = 60 Hz, T_A = 25°C	3

Environmental

Test	MIL-STD-750 Reference	Tests Conditions	LTPD
Solderability	2026	Sn 95, Pb 5, solder at 260°C	10
Temperature Cycling	1051	100 cycles from -65°C to +150°C, 0.5 hrs. at extremes, 5 min. transfer	7
Thermal Shock	1056	100 cycles from 0°C to +100°C, 3 sec. transfer	7
Moisture Resistance	1021	10 days, 90-98% RH, -10 to +65°C, non operating	7
Shock	2016	5 blows each X_1, Y_1, Y_2, 1500 G. 0.5 msec pulse	7
Vibration Variable Frequency	2056	4, 4 minute cycles each X, Y, Z at 20 G min. 100 to 2000 Hz	7
Constant Acceleration	2006	1 minute each X_1, Y_1, Y_2, at 20,000 G	7
Terminal Strength	2036	Miniature glass package, -3, 90° arcs, 2 leads, 8 oz., lead restriction	10
Hermeticity	1014	Fine and gross	2

HEWLETT PACKARD

PIN Diodes

Reliability Data

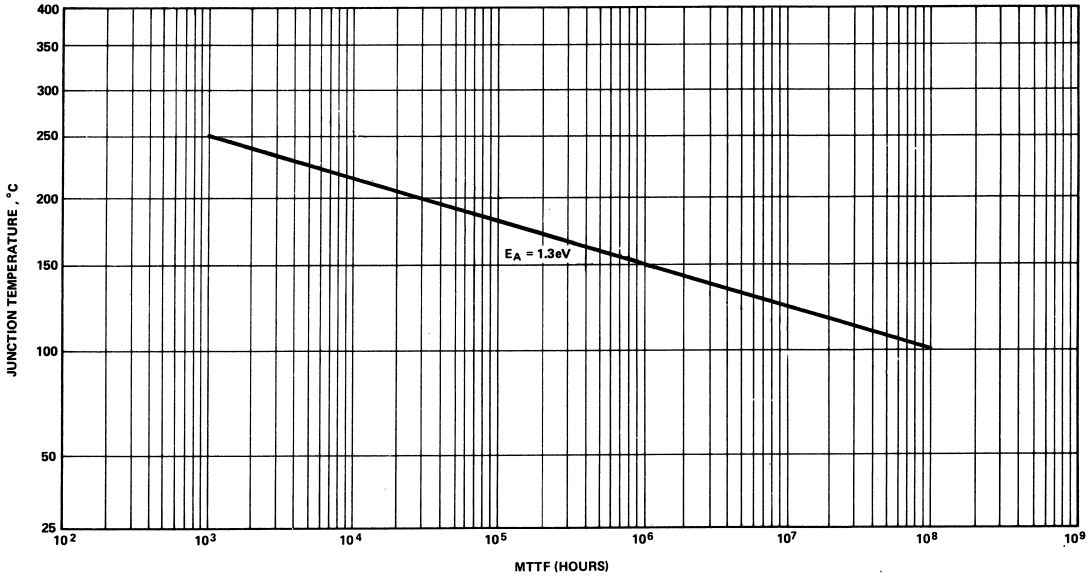
1N5767
5082-3080
5082-3168
5082-3188

Description

For applications requiring component reliability estimation, Hewlett-Packard provides reliability data for all families of devices. Data is initially compiled from reliability tests run prior to market introduction to demonstrate that a product meets design criteria. Additional tests are run periodically. The data on this sheet represents the latest review of accumulated test results.

Applications

This information represents the capabilities of the generic device. Failure rates and MTTF values presented here are achievable with normal MIL-S-19500 TX level screening. Reliability can only be guaranteed by testing specified lots of devices, under specified conditions, with specified LTPD levels.



Mean Time to Failure vs. Junction Temperature

Burn-In and Storage

Test	Test Conditions	LTPD/ 1000 Hours
High Temperature Life	1,000 hrs. min. storage time @ 150°C	3
Steady State Operating Life	1,000 hrs. min. operating time @ P_{FM} = 250 mW, V_{RM} = 20 V, f = 60 Hz, T_A = 25°C	3

Environmental

Test	MIL-STD-750	Tests Conditions	LTPD
Solderability	2026	Sn 95, Pb 5, solder at 260°C	10
Temperature Cycling	1051	100 cycles from -65°C to +150°C, 0.5 hrs. at extremes, 5 min. transfer.	7
Thermal Shock	1056	5 cycles from 0°C to +100°C, 3 sec. transfer	7
Moisture Resistance	1021	10 days, 90-98% RH, -10 to +65°C, non operating	7
Shock	2026	5 blows each X_1, Y_1, Y_2, 1500 G. 0.5 msec pulse	7
Vibration Fatigue	2046	32 ± 8 hrs., each X, Y, Z, 96 hr. total, 60 Hz, 20 G min.	7
Vibration Variable Frequency	2056	4, 4 minute cycles each X, Y, Z at 20 G min. 100 to 2000 Hz	7
Constant Acceleration	2006	1 minute each X_1, Y_1, Y_2, at 20,000 G	7
Terminal Strength	2036	Miniature glass package, -3, 90° arcs, 2 leads, 8 oz., lead restriction	7
Salt Atmosphere	1041	35° fog for 24 hours	7

Step Recovery Diodes



Characteristics of Step Recovery Diodes

The Step Recovery diode is most graphically described as a charge-controlled switch. That is, a forward bias stores charge, a reverse bias depletes this stored charge, and when fully depleted the SRD ceases to conduct current. The action of turning off, or ceasing current conduction, takes place so fast that the diode can be used to produce an impulse. If this is done cyclically, a train of impulses is produced. A periodic series of impulses in the time domain converts to a series of frequencies (all multiples of the basic exciting frequency) in the frequency domain. If these impulses are used to excite a resonant circuit, much of the total power in the spectrum can be concentrated into a single frequency. Thus input power at one frequency can be converted to output power at a higher frequency.

Two specifications that limit the total power output in any given multiplier mode are maximum junction temperature and thermal resistance. Within this limit, the output for a given input is determined by the efficiency of conversion. Efficiency depends heavily on the design of the multiplier, so Hewlett-Packard does not specify it.

The above specifications are related as follows:

1. Maximum Power Dissipation, P_D (power dissipated by the diode)

$$P_D = \frac{200°C - T_A}{\Theta_{JC}}$$

where T_A = ambient temperature, °C, and
Θ_{JC} = thermal resistance, °C/W

2. Efficiency,

$$\eta = P_O/(P_O + P_D) \cdot 100\%$$

where P_O = output power
P_D = power dissipation

The reverse voltage breakdown limit, V_{BR}, limits the pulse height and can limit the input power before the thermal limit is reached.

The low frequency limit of the exciting signal is set by minority carrier lifetime, τ, and the ability to form an effective impulse at the higher frequencies is determined by the transition time, t_t. Under forward current flow, I_F, charge is built up in the SRD. Once reverse biased, reverse current will flow for a short period of time. This is called the delay time, t_d, as in the PIN diode. When all of the carriers have been removed, the current drops abruptly to zero. The time required for the reverse current to go from 0.8 I_R to 0.2 I_R is called transition time. Typical transition times range from 400 psec. down to 60 psec. for Step Recovery diodes.

The delay time t_d is related to minority carrier life time τ by

$$\frac{t_d}{\tau} = \ln\left(1 + \frac{I_F}{I_R}\right).$$

Lifetime is measured by setting $I_F = 1.7\ I_R$ so that $t_D = \tau$.

Minority carrier lifetime sets the lower input frequency limit because as the frequency gets lower and lower, more and more of the charge is dissipated by recombination during a cycle which reduces the energy in the impulse. The input frequency should be larger than the inverse of τ to minimize this loss of energy.

The highest output frequency for reasonable efficiency as a multiplier is limited by the width of the impulse spike which is determined by the transition time. Efficiency declines when the output frequency exceeds the inverse of the transition time.

Applications of Step Recovery Diodes

As brought out in the previous section, the Step Recovery diode can be made to produce very sharp and narrow pulses. These contain harmonics of the exciting frequency.

A circuit which exploits the Step Recovery diode's production of a multitude of frequency components is called a Comb Generator. Comb generators are used in measurement equipment such as Spectrum Analyzers to produce locking signals.

Another type of circuit picks out a single harmonic and optimizes the power output around that harmonic. This circuit is called a Multiplier. The end result of a multiplier is output power at some multiple (2f, 3f, etc.) of the input frequency. The efficiency of the conversion is high enough to make this a very practical scheme for multiplying up from a readily available low frequency oscillator to get a higher frequency signal. Multipliers are used as local oscillators, low power transmitters, or transmitter drivers in radar, telemetry, telecommunications and instrumentation.

Silicon Step Recovery Diodes

Part Number	C_j Typ. (pF)	V_{BR} Min. (V)	Lifetime, τ Typ. (ns)	Transition Time t_t, Typ. (ps)	Package	Page
5082-0032	4.00	65	150	250	chip	5-4
5082-0113	4.50	35	80	250	11	5-6
5082-0114	3.50	35	80	250	11	5-6
5082-0180*	4.00	50	100	225	11	5-6
5082-0112	1.40	35	50	175	11	5-6
5082-0132	1.35	35	50	175	31	5-9
5082-0015	1.20	35	60	150	chip	5-4
5082-0830	0.80	25	10	100	31	5-9
5082-0253	0.50	25	10	100	31	5-9
5082-0151	0.50	15	10	100	11	5-6
5082-0153	0.35	25	10	95	11	5-6
5082-0833	1.00	25	10	90	11	5-6
5082-0320*	0.80	25	25	75	41	5-9
5082-0835	0.40	15	10	75	31	5-9
5082-0840	0.40	15	10	75	11	5-6
5082-0885	0.40	15	10	75	56	5-9
5082-0018	0.50	25	20	70	chip	5-4
5082-0020	0.70	25	20	60	chip	5-4
5082-0335	0.40	25	15	60	31	5-9
5082-0008	0.38	15	10	60	chip	5-4

*Standard Hi-Rel version available.
For reliability data see page 5-13.

HEWLETT PACKARD

Step Recovery Diode Chips

Technical Data

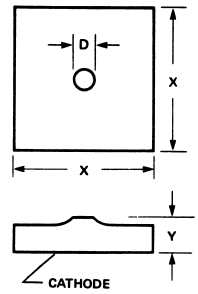
5082-0008
5082-0015
5082-0017
5082-0018
5082-0020
5082-0032

Features

- **Optimized for Both Low and High Order Multiplier Designs from UHF through Ku Band**
- **Passivated Chip for Maximum Stability and Reliability**
- **Gold Top Contact for Long Shelf Life and Bondability**

Description

These diodes are manufactured using modern epitaxial growth techniques. The diodes are passivated with a thermal oxide for maximum stability. The result is a family of devices offering highly repeatable, efficient and reliable performance. Both the anode and cathode contact metallizations are gold allowing long shelf life and repeatable bondability. These diodes are designed to meet the general requirements of MIL-S-19500.



Outline 01B

Dimension	5082-							
	0020	0008	0015	0017	0018	0021	0032	0090
D	0.13 (5)	0.06 (2.5)	0.15 (6)	0.39 (15.5)	0.05 (2)	0.22 (8.5)	0.32 (12.5)	0.15 (6)
X	0.38 (15)	0.38 (15)	0.38 (15)	0.64 (25)	0.38 (15)	0.51 (20)	0.51 (20)	0.38 (15)
Y	0.11 (4.5)	0.11 (4.5)	0.11 (4.5)	0.11 (4.5)	0.11 (4.5)	0.11 (4.5)	0.11 (4.5)	0.11 (4.5)

DIMENSIONS IN MILLIMETERS (1/1000 inch)

Applications

These Step Recovery Diodes are intended for medium and low power multipliers. Typical applications are in hybrid local oscillators, especially where low phase noise is required, in terrestrial communications, satellite communications, TVRO, mobile communications and test equipment. Input frequencies extend down to 10 MHz with output frequencies through 40 GHz.

Maximum Ratings

Junction Operating and Storage Temperature Range ..... -60°C to +200°C
Maximum Die Attach Temperature ..... +310°C for 1 minute

Electrical Specifications at T_A = 25°C

Part Number 5082-	Minimum Breakdown Voltage V_{BR} (V)[1]	Typical Chip Capacitance C_j (pF)[2]	Typical Lifetime τ (ns)[3]	Typical Transition Time		Nearest Equivalent Packaged Part No. 5082-
				Transition Time t_t (ps)	Charge Level (pc)	
0008	15	0.38	20	60	100	0835
0018	25	0.5	20	70	200	0253
0020	25	0.8	20	60	300	0830
0015	35	1.2	60	150	1000	0132
0032	50	4.0	150	250	1500	0241
0017	75	4.0	300	300	2400	0300

Notes:
1. Minimum Breakdown Voltage test condition is I_R = 10 μA.
2. Capacitance sample test condition is V_R = 10 V and f = 1 MHz.
3. Lifetime sample test condition is I_F = 10 mA and I_R = 6 mA.

HEWLETT PACKARD

Glass Packaged Step Recovery Diodes

Technical Data

5082-0112/13/14
5082-0151
5082-0153
5082-0180
5082-0833
5082-0840

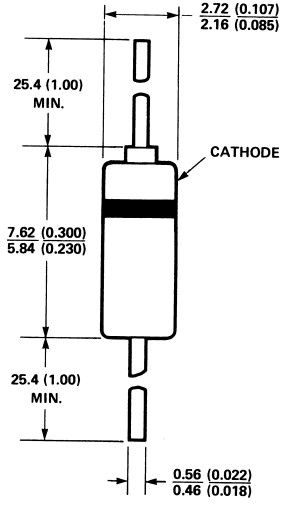
Features

- **Optimized for Both Low and High Order Multiplier Designs from UHF through Ku Band**
- **Passivated Chip for Maximum Stability and Reliability**
- **Available in a Variety of Packages**

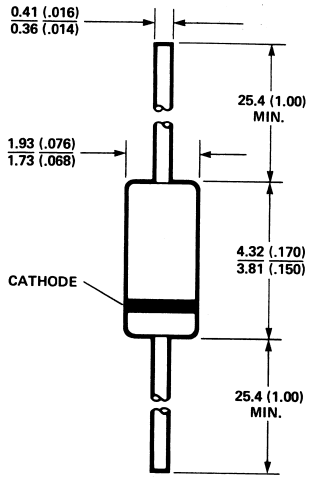
Description/ Applications

These diodes are manufactured using modern epitaxial growth techniques. The diodes are passivated with a thermal oxide for maximum stability. The result is a family of devices offering highly repeatable, efficient and reliable performance which are designed to meet the general requirements of MIL-S-19500.

These diodes are intended for medium and low power multipliers. Typical applications are in local oscillators, especially where low phase noise is required, in terrestrial communications, satellite communications, TVRO, mobile communications and test equipment. Input frequencies extend down to 10 MHz with output frequencies reaching 26 GHz.



Outline 11



Outline 15

Mechanical Specifications

The HP Outline 15 package has a glass hermetic seal with plated Dumet leads which should be restricted so that the bend starts at least 1/16 inch (1.6 mm) from the glass body. With this restriction, it will meet MIL-STD-750, Method 2036, Conditions A and E (4 lb. [1.8 kg] tension for 30 minutes). The maximum soldering temperature is 230°C for five seconds. Marking is by digital coding with a cathode band. Outline 15 package capacitance and inductance are typically 0.18 pF and 1.8 nH respectively.

The HP Outline 11 package has a glass hermetic seal with plated Dumet leads. The package will meet MIL-STD-750, Method 2036, Condition A (2 lbs. tension for 15 sec.) and E. The maximum soldering temperature is 230°C for five seconds. Outline 11 package capacitance and inductance are typically 0.15 pF and 4 nH, respectively.

Maximum Ratings

Junction Operating and Storage Temperature Range ..... -65°C to 200°C

DC Power Dissipation at T_{CASE} = 25°C ..... $\frac{200°C - T_{CASE}}{\theta_{jc}}$

Soldering Temperature ..... 230°C for 5 sec.

Electrical Specifications at T_A = 25°C

Part Number 5082-	Max. Junction Capacitance C_j (pF)	Min. Breakdown Voltage V_{BR} (V)	Min. Cutoff Frequency f_C (GHz)	Transition Time[1]		Min. Lifetime τ (nsec)	Package Outline
				Max. t_t (psec)	Charge Level (pc)		
0840	0.60*	15	300	75	100	10	15
0151	0.65	15	–	100	200	10	15
0153	0.40	25	–	95	200	10	15
0833	1.6*	25	175	90	300	10	15
0112	1.55	35	–	175	1000	50	11
0114	3.85	35	–	225	1500	80	11
0113	4.85	35	–	250	1500	80	11
0180	4.45	50	–	225	1500	100	11
Test Conditions	f = 1 MHz V_R = 10 V *V_R = 6 V	I_R = 10 μA	$f_C = \frac{1}{2\pi R_S C_j}$			I_F = 10 mA I_R = 6 mA	

Notes:

1. The transition times shown for the package 15 devices are limited by the package inductance to a minimum of 100 ps. The lower transition times shown for the -0833, -0840, -0151, and -0153 are based on the performance of the chip.
2. Typical θ_{JC} for Outline 15 is 600°C/W and for Outline 11 is 300°C/W.

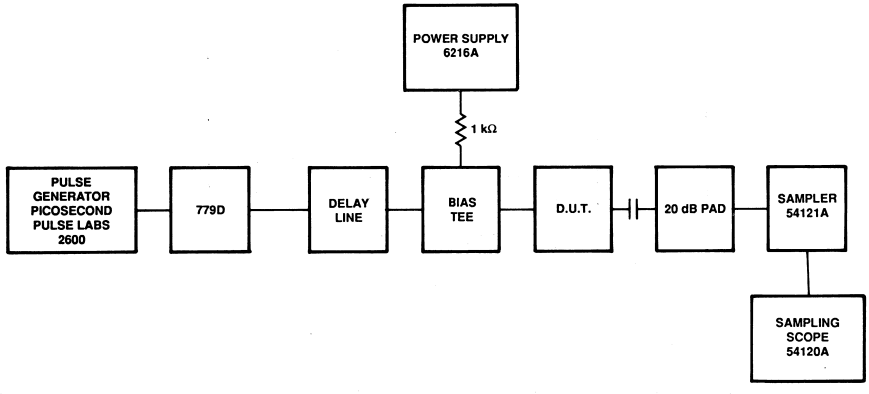


Figure 1. Test circuit for transition time. The pulse generator circuit is adjusted for a 0.5 A pulse when testing 5082-0151 and -0840. A pulse of 1.0 A is used for all other diodes. The bias current is adjusted for the specified stored charge level. The transition time is read between the 20% and the 80% points on the oscilloscope.

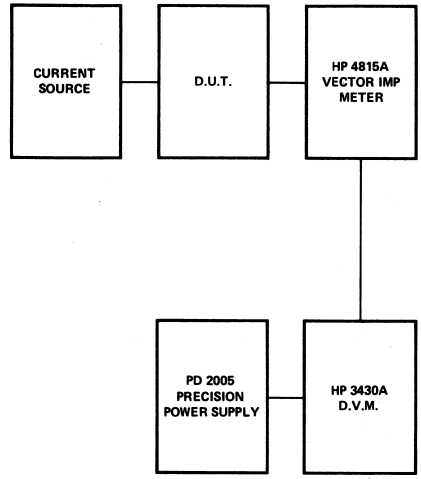


Figure 2. Test set-up for measurement of series resistance. The D.U.T. is forward biased (I_F) and the real part of the diode impedance is measured at 100 MHz. The D.V.M. is set up to read the real part on the Vector voltmeter. The precision power supply is used to offset the test circuit resistance. R_s is measured at I_F = 100 mA.

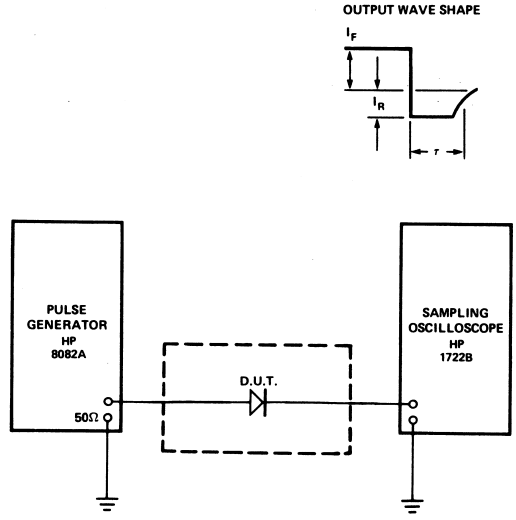


Figure 3. The circuit for measurement of the effective minority carrier lifetime. The value of the reverse current (I_R) is approximately 6 mA and the forward current (I_F) is 10 mA. The lifetime (τ) is measured across the 50% points of the observed wave shape. The input pulse is provided by a pulse generator having a rise time of less than one nanosecond. The output pulse is amplified and observed on a sampling oscilloscope.

HEWLETT PACKARD

Ceramic Packaged Step Recovery Diodes

Technical Data

5082-0132
5082-0253
5082-0300
5082-0320
5082-0335
5082-0800
5082-0830
5082-0835
5082-0885

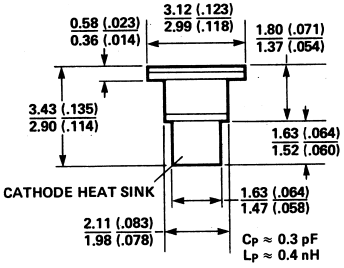
Features

- **UHF Through Ku Band Diodes**
  For Low Order and High Order Multipliers
- **RF Tested**
  For Guaranteed Performance (5082-0300 Series)
- **Hermetic Package**
  For Industrial/Military Environments

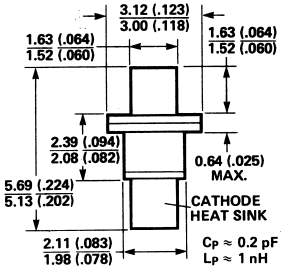
Description/ Applications

HP Step Recovery Diodes are constructed using modern epitaxial techniques. Oxide passivation insures maximum stability and reliability. Devices are available in many package styles.

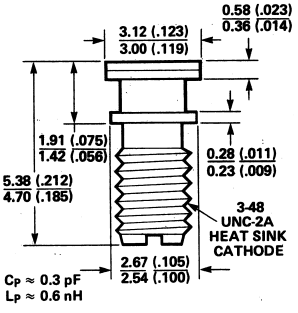
These devices are intended for use as low and high order harmonic generators requiring the ultimate in performance and reliability. They excel as doublers as well as high order multipliers, because the fast transition time design allows full usage of the forward stored charge effect in improving nonlinearity and efficiency for frequency multiplication. These step recovery diodes have the basic design capability to meet the general reliability requirements of MIL-S-19500, in addition to the special reliability requirements of man-rated space systems.



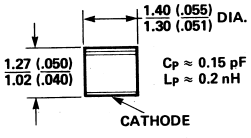
Outline 41



Outline 31



Outline 40



Outline 56

DIMENSIONS IN MILLIMETERS AND (INCHES)

Mechanical Specifications

Hewlett-Packard's Step Recovery Diodes are available in a variety of packages. The metal ceramic packages are hermetically sealed. The anode studs and flanges are gold-plated Kovar. The cathode studs are gold-plated copper. The maximum soldering temperature for metal-ceramic packages is 230°C for five seconds.

Maximum Ratings

Junction Operating and Storage Temperature Range ..... -65°C to 200°C

DC Power Dissipation at T_{CASE} = 25°C ..... $\frac{200°C - T_{CASE}}{\theta_{jc}}$

Soldering Temperature ..... 230°C for 5 sec.

Electrical Specifications at T_A = 25°C

Part Number 5082-	Junction Capacitance C_J (pF)		Min. Breakdown Voltage V_{BR} (V)	Min. Cutoff Frequency f_C (GHz)	Package Outline	Transition Time		Min. Lifetime τ (nsec)	Typical Thermal Resistance θ_{jc} (°C/W)	Typical Output Power P_O (W)
	Min.	Max.				Max. t_t (psec)	Charge Level (pc)			
0835	0.1	0.5	15	350	31	75	100	10	60	0.3
0885	0.1	0.5	15	350	56	75	100	10	60	0.3
0253	–	0.6*	25	–	31	100	200	10	75	–
0830	0.35	1.2	25	200	31	100	300	10	45	1.0
0132	–	1.5*	35	–	31	175	1000	50	40	–
0800	3.5	5.0	75	100	40	400	1500	200	15	10
Test Conditions	f = 1 MHz V_R = 6 V *V_R = 10 V		I_R = 10 μA	$f_C = \frac{1}{2\pi R_S C_j}$				I_F = 10 mA I_R = 6 mA		As a doubler

RF Tested Diodes at T_A = 25°C

Electrical Specifications

Part Number 5082-	Output Frequency, f_O (GHz)	N Order	Min. Output Power, P_O[1] (W)	Junction Capacitance at -10V, 1 MHz, C_j (pF)		Breakdown Voltage at I_R = 10 μA V_{BR} (V)		Max. Thermal Resistance, θ_{jc} (°C/W)	Package Outline	Typical Transition Time		Typical Lifetime τ (ns)
				Min.	Max.	Min.	Max.			t_t (ps)	Charge Level (pc)	
0300	2	X 10	2.0	3.2	4.7	75	100	14	40	300	2400	200
0320	10	X 5	0.23	0.35	1.0	25	40	60	41	60	300	25
0335	16	X 8	0.03	0.25	0.5	20	30	75	31	60	100	15

Note:

1. Guaranteed multiplier tested results. Input power is:
   5082-0300 15 W 5082-0320 2 W
   5082-0335 0.65 W

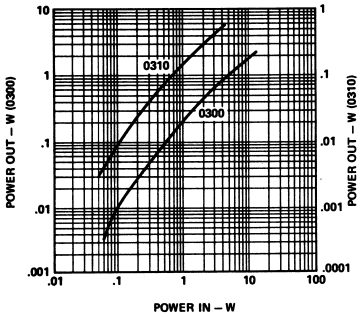


Figure 1. Typical Output Power vs. Input Power at T_A = 25°C. The 5082-0300 is measured in a X 10 multiplier with P_{IN} at 0.2 GHz and P_O at 2.0 GHz.

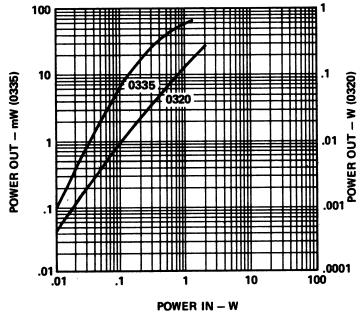


Figure 2. Typical Output Power vs. Input Power at T_A = 25°C. The 5082-0335 is measured in a X 8 multiplier with P_{IN} at 0.2 GHz and P_O at 16 GHz. The 5082-0320 is measured in a X 5 multiplier with P_{IN} at 2.0 GHz and P_O at 10 GHz.

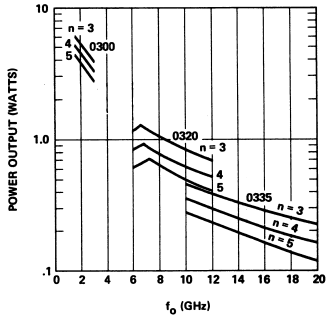


Figure 3. Predicted power output curves for 03XX step recovery diodes in X 3, X 4, and X 5 multiplier applications. These results were obtained using computer optimization programs.

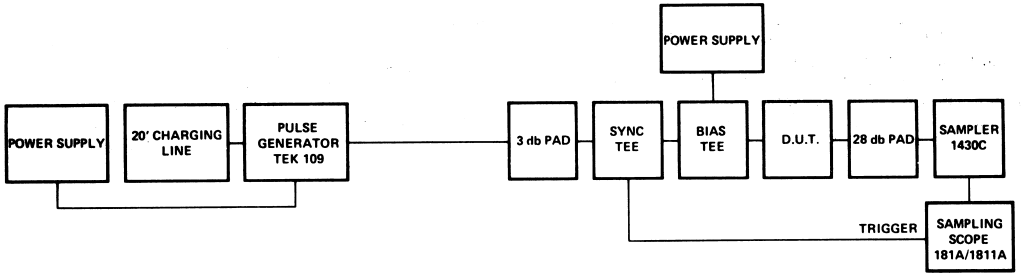


Figure 4. Test circuit for transition time. The pulse generator circuit is adjusted for a 0.5 A pulse when testing 5082-0253, -0335, -0835, and -0885. A pulse of 1.0 A is used for all other diodes. The bias current is adjusted for the specified stored charge level. The transition time is read between the 20% and the 80% points on the oscilloscope.

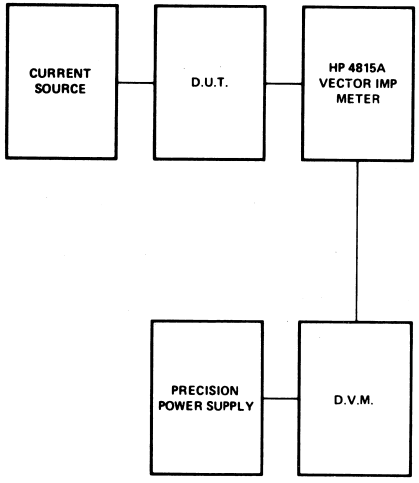


Figure 5. Test setup for measurement of series resistance. The D.U.T. is forward biased (I_F) and the real part of the diode impedance is measured at 100 MHz. The D.V.M. is set up to read the real part on the Vector Voltmeter. The precision power supply is used to offset the test circuit resistance. R_s is measured at I_F = 100 mA, except -0800 where I_F = 500 mA and -0885 where I_F = 300 mA.

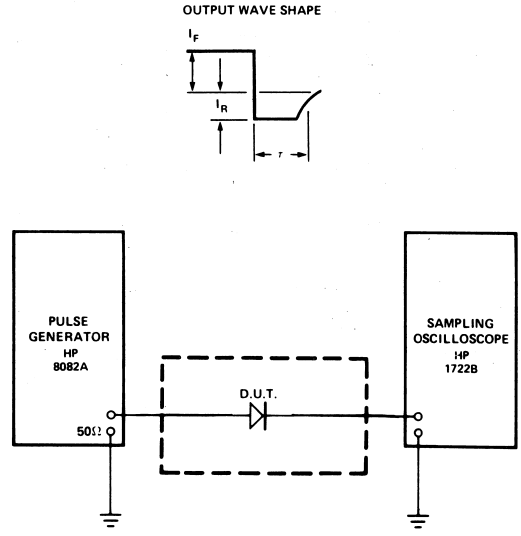


Figure 6. The circuit for measurement of the effective minority carrier lifetime. The value of the reverse current (I_R) is approximately 6 mA and the forward current (I_F) is 10 mA. The lifetime (τ) is measured across the 50% points of the observed wave shape. The input pulse is provided by a pulse generator having a rise time of less than one nanosecond. The output pulse is observed on a sampling oscilloscope.

Step Recovery Diodes

Reliability Data

Description

For applications requiring component reliability estimation, Hewlett-Packard provides reliability data for all families of devices. Data is initially compiled from reliability tests run prior to market introduction to demonstrate that a product meets design criteria. Additional tests are run periodically. The data on this sheet represents the latest review of accumulated test results.

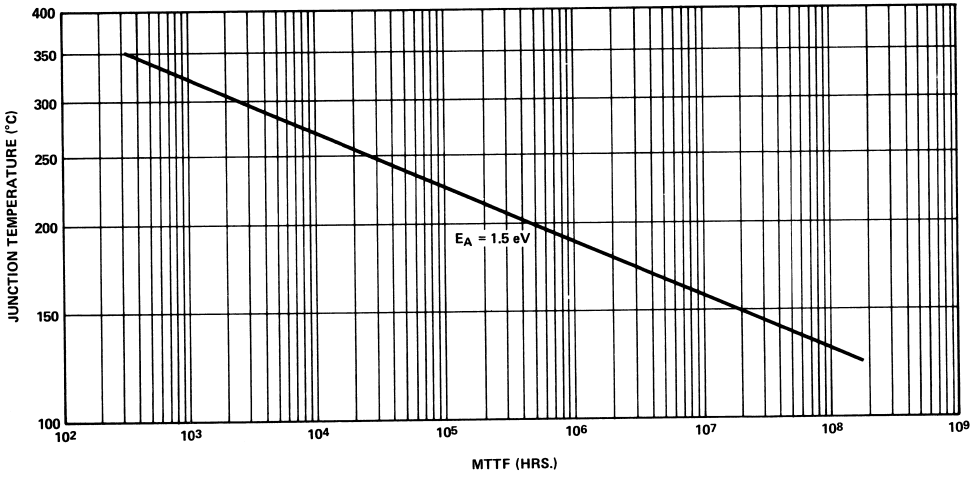
Applications

This information represents the capabilities of the generic device. Failure rates and MTTF values presented here are achievable with normal MIL-S-19500 TX level screening. Reliability can only be guaranteed by testing specified lots of devices, under specified conditions, with specified LTPD levels.

Burn-In and Storage

Preconditioning and screening tests are recommended for devices terminating in high reliability equipments. The following results were obtained with preconditioning and screening.

Test	Test Conditions	LTPD/ 1000 Hours
High Temperature Life	1,000 hrs. min. storage time at 150°C	3
Steady State Operating Life	1,000 hrs. min. operating time, P_{FM} = 175 mW V_{RM} = 12 V, f = 60 Hz, T_A = 25°C	3



Mean Time to Failure vs. Junction Temperature

Environmental

The following cumulative test results have been obtained from reliability testing performed at HP Components Division, in accordance with the latest revisions of Military Semiconductor Specifications MIL-STD-19500, MIL-STD-202 and MIL-STD-750.

Test	MIL-STD-750 Reference	Test Conditions	LTPD
Temperature Cycling	1051	100 cycles from -65°C to +150°C, 0.5 hours at extremes, 5 min. transfer	7
Thermal Shock	1056	100 cycles from 0°C to +100°C, 3 sec. transfer	7
Moisture Resistance	1021	10 days, 90-98% RH, -10 to +65°C, non-operating	7
Shock	2016	5 blows each X_1, Y_1, Y_2, 1500 G. 0.5 msec pulse	7
Vibration Variable Frequency	2056	4, 4 minute cycles each, X, Y, Z, at 20 G min. 100 to 2000 Hz	7
Constant Acceleration	2006	1 minute each X_1, Y_1, Y_2, at 20,000 G	7
Terminal Strength	2036	Pkg. 31 – 2 lbs. for 3 sec, 120° apart	10
Salt Atmosphere	1041	35° fog for 24 hours	10

Silicon Bipolar Transistors



RF and Microwave Silicon Bipolar Transistors

The silicon bipolar transistor is a semiconductor device, with amplification due to current gain. The advantages silicon bipolar transistors have over other transistor types include mature technology (both in the understanding of the device physics and the device design), low cost, and proven reliability. Therefore, silicon bipolar transistors offer designers a familiar, reliable, cost effective solution to many of their design needs.

Hewlett-Packard manufactures bipolar junction transistors using the Self Aligned Transistor (SAT) process. This state-of-the-art silicon process yields an f_T of 10 GHz and an f_{MAX} of 25 GHz. Other process features include ion-implantation, the use of gold metalization, and nitride surface passivation. Transistors manufactured with this proprietary process have excellent performance, repeatability, and reliability.

The performance capabilities of an interdigitated microwave bipolar junction transistor are strongly related to two design parameters. The pitch, or emitter-to-emitter center line spacing, controls the "high performance" aspects of the transistor. Finer pitches result in more gain and lower noise figure at higher frequencies. Devices with coarser pitches are typically easier to manufacture, but are limited to lower frequency applications. The number of emitter fingers controls the current handling ability of the device and is a measure of output power capability. Devices with larger numbers of fingers are suitable for power applications such as transmit stages; devices with small numbers of fingers operate at lower biases and are often the best choice for battery operated applications.

Product Families

Hewlett Packard uses a numbering scheme based on the pitch and number of emitter fingers. Discrete bipolar transistors have part numbers starting with the alpha characters "AT". In general, the first numerical digit of the part number is the emitter to emitter pitch, to the nearest micron. The second and third digits represent the number of emitter fingers. The final two digits represent package style, with the code "00" being reserved for chip form. Devices are manufactured with pitches from 2 to 10 microns (a 10 micron pitch device is designated by a first digit of "0").

10 micron pitch

Two geometries are manufactured with a 10 micron pitch: the AT-005 and the AT-016. Features of these devices include large bond pads for auto-bonding, which, with the large pitch of these devices, make them excellent choices for the most cost sensitive, lower frequency applications that do not require the ultimate in performance. The AT-005 is a "typical" small signal device for general applications, while the AT-016 is a higher power device (150 mW) for driver applications.

6 micron pitch

The AT-601, AT-602, and AT-605 geometries are small devices ideal for many battery powered applications. They function well at voltages as low as 2 V, and can be biased at currents as low as 0.4 mA. The AT-640 is a power device capable of producing 0.5 W typical at 4 GHz.

4 micron pitch

The 4 micron devices are the "backbone" of Hewlett-Packard's bipolar transistor line. The AT-414 is a general purpose part with excellent noise, gain, and power capabilities, and is the starting place for most designs. The AT-420 supplies the same high performance, but with improved output power capability.

2 micron pitch

The AT-214 geometry is a specialty device designed for high frequency oscillator applications. Specially processed for reduced parasitics with an enhanced f_{MAX} of 40 GHz, these devices are capable of producing fundamental oscillations at frequencies as high as 20 GHz.

Silicon Bipolar Transistors

Low Noise Transistors (Typical Specifications at +25°C Case Temperature)

Part Number	Test Freq. (GHz)	NF_o (dB)	P_{1dB} (dBm)	$\|S_{21E}\|^2$ @ 1.0 GHz (dB)	Max. Usable Freq.[a] (GHz)	f_{max}[b] (GHz)	Package	Page
AT-41400	2.0	1.6	+19.0	18.0	4.5	16.0	chip	6-35
AT-60100	2.0	1.9	+4.0	12.5	3.0	15.0	chip	6-84
AT-60200	2.0	1.9	+6.5	15.5	3.5	15.0	chip	6-92
AT-60500	2.0	1.8	+16.0	17.5	4.0	15.0	chip	6-95
AT-41410	2.0	1.6	+19.0	18.0	4.5	15.0	100 mil stripline	6-38
AT-41470	2.0	1.6	+19.0	18.0	4.5	16.0	70 mil stripline	6-47
AT-60510	2.0	1.8	+16.0	17.5	4.0	14.0	100 mil stripline	6-98
AT-60570	2.0	1.8	+16.0	17.5	4.0	15.0	70 mil stripline	6-104
AT-41435	2.0	1.7	+19.0	17.5	4.2	14.0	micro-X ceramic SM	6-44
AT-41472	0.5	1.3	+20.5	11.5	1.0	8.0	TO-72	6-50
AT-60535	2.0	1.8	+16.0	17.0	4.0	13.0	micro-X ceramic SM	6-101
AT-41485	1.0	1.4	+18.5	17.5	4.0	13.0	85 mil plastic	6-52
AT-60585	1.0	1.4	+15.0	17.0	4.0	12.0	85 mil plastic	6-107
AT-41411	1.0	1.4	+17.0	16.5	3.5	11.0	SOT-143 SM plastic	6-41
AT-41486	1.0	1.4	+18.0	17.5	4.0	12.0	85 mil SM plastic	6-55
AT-41511	1.0	1.4	+18.0	16.5	4.0	–	SOT-143 SM plastic	6-58
AT-41586	1.0	1.4	+18.0	17.0	4.0	–	85 mil SM plastic	6-58
AT-60111	1.0	1.4	+4.0	11.5	1.9	10.0	SOT-143 SM plastic	6-87
AT-60211	1.0	1.5	+7.5	14.0	2.1	10.0	SOT-143 SM plastic	6-87
AT-60586	1.0	1.4	+15.0	17.0	4.0	12.0	85 mil SM plastic	6-110

General Purpose and Medium Power (Typical Specifications at +25°C Case Temperature)

Part Number	Test Freq. (GHz)	NF_o (dB)	P_{1dB} (dBm)	$\|S_{21E}\|^2$ @ 1.0 GHz (dB)	Max. Usable Freq.[a] (GHz)	f_{max}[b] (GHz)	Package	Page
AT-00500	2.0	2.5	+16.0	15.5	3.0	9.0	chip	6-9
AT-01600	2.0	3.0	+22.0	13.0	2.3	9.0	chip	6-22
AT-42000	2.0	1.9	+21.0	17.0	3.8	15.0	chip	6-66
AT-00510	2.0	2.5	+16.0	15.0	3.0	8.0	100 mil stripline	6-12
AT-00570	2.0	2.5	+16.0	15.5	3.0	9.0	70 mil stripline	6-18
AT-01610	2.0	3.0	+22.0	12.5	2.3	8.0	100 mil stripline	6-25
AT-01670	2.0	3.0	+22.0	13.0	2.3	9.0	70 mil stripline	6-29
AT-42010	2.0	1.9	+21.0	17.0	3.8	14.0	100 mil stripline	6-69
AT-42070	2.0	1.9	+21.0	17.5	3.8	15.0	70 mil stripline	6-75
AT-00535	2.0	2.5	+16.0	15.0	3.0	8.0	micro-X ceramic SM	6-16
AT-00572	0.5	1.9	+19.0	10.0	1.0	4.0	TO-72	6-20
AT-01635	2.0	3.0	+22.0	12.0	2.2	8.0	micro-X ceramic SM	6-27
AT-01672	0.5	2.0	+24.0	9.0	1.0	3.0	TO-72	6-31
AT-42035	2.0	1.9	+21.0	17.0	3.8	14.0	micro-X ceramic SM	6-72
AT-42085	1.0	1.4	+20.5	17.0	3.5	12.0	85 mil plastic	6-78
AT-00511	1.0	1.8	+11.0	12.5	2.7	5.0	SOT-143 SM plastic	6-14
AT-42086	1.0	1.4	+20.5	17.0	3.5	11.0	85 mil SM plastic	6-81

Notes:
[a] Frequency at which $|S_{21E}|^2$ gain equals 6 dB.
[b] Frequency at which unilateral gain equals unity or 0 dB.

Silicon Bipolar Transistors (cont.)

Linear Power (Typical Specifications at +25°C Case Temperature)

Part Number	Test Freq. (GHz)	P_{1dB} (dBm)	G_{1dB} (dB)	$\|S_{21E}\|^2$ @ 1.0 GHz (dB)	Max. Usable Freq.[a] (GHz)	f_{max}[b] (GHz)	Package	Page
AT-64020	2.0	28.0	+10.0	12.5	2.0	8.0	200 mil BeO disk	6-113
AT-64023	4.0	27.0	+9.5	12.0	2.2	8.0	230 mil flange BeO	6-115

Class C Power (Typical Specifications at +25°C Case Temperature)

Part Number	Test Frequency (MHz)	Power Out (Watts)	G_P (dB)	Tuned η_c (%)	Supply Voltage (V)	Package	Page
ASP-0910	900	10	10	55	25	6 lead power flange	6-5
ASP-0955	900	58	9.2	55	25	6 lead power flange	6-7

Oscillator Devices (Typical Specifications at +25°C Case Temperature)

Part Number	Max. Recommended Operating Freq.[c] (GHz)	Power @ 4.0 GHz (dBm)	Output MAG @ 4.0 GHz (dB)	$\|S_{21E}\|^2$ @ 4.0 GHz (dB)	f_{max}[b] (GHz)	Package	Page
AT-21400	20	+13	16.5	9.5	40	chip	6-33
AT-41400	10	+19	11.0	6.5	25	chip	6-35
AT-42000	10	+21	11.0	5.5	25	chip	6-66
AT-60500	8	+15	11.0	6.5	18	chip	6-95

Notes:
[a] Frequency at which $|S_{21E}|^2$ gain equals 6 dB.
[b] Frequency at which unilateral gain equals unity or 0 dB.
[c] For fundamental oscillation.

HEWLETT PACKARD

ASP-0910
10 Watt, 900 MHz
Silicon Power Transistor

Features

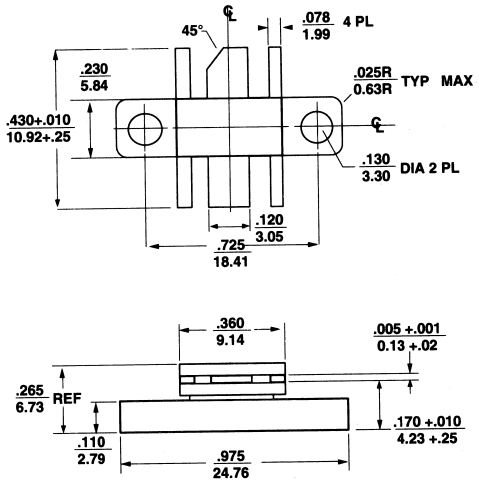
- **Power Out: 10 Watts**
- **Common Base Class C Power Transistor**
- **Frequency: 800-960 MHz**
- **Voltage: 25 V**
- **Efficiency: 50% Min.**
- **Load Mismatch Tolerance: 10:1**

Description

The ASP-0910 is a large signal, Class C common base, NPN silicon bipolar power transistor, housed in a BeO flange package for excellent thermal transfer. This device is designed for use as a 10 W driver or output amplifier for base station applications in cellular telephone systems operating in the 800 to 960 MHz frequency range.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of these devices. Emitter ballasting ensures a rugged device capable of withstanding severe load mismatches.

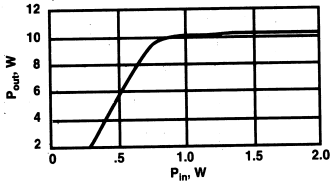
Power Flange



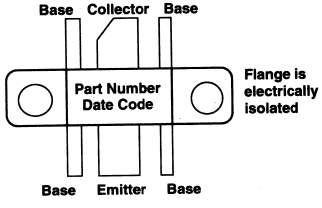
Dimensions are $\frac{\text{in}}{\text{mm}}$

Tolerances: in .xxx = ±.005 mm .xx = ±.13

Power Output vs. Power Input
V_{CE} = 25 V, f = 900 MHz
(Broadband performance in demo circuit)



Marking and Lead Configuration



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
P_{out}	Output Power[1]	V_{CE} = 25 V, Pin = 1 W, f = 900 MHz	Watts	9	10	
G_P	Power Gain[1]	V_{CE} = 25 V, Pin = 1 W, f = 900 MHz	dB	9.5	10	
η_C	Collector Efficiency[1]	V_{CE} = 25 V, Pin = 1 W, f = 900 MHz	%	50	55	
	Load Mismatch Tolerance	V_{CE} = 25 V, rated P_{out}, f = 900 MHz	-	10:1		
BV_{CEO}	Collector-Emitter Voltage	V_{EB} = open, I_C = 50 mA	V	24	28	
BV_{CES}	Collector-Emitter Voltage	V_{EB} = 0 V, I_C = 100 mA	V	50	55	
BV_{EBO}	Emitter-Base Voltage	V_{CB} = open, I_E = 15 mA	V	3.5	4.5	
h_{FE}	Forward Current Transfer Ratio	V_{CE} = 5 V, I_C = 1 A	-	20	60	120
I_{CES}	Collector Leakage Current	V_{CE} = 26 V	mA		1	5
C_{OB}	Collector-Base Capacitance	f = 1 MHz, V_{CB} = 25 V, I_E = 0 mA	pF		10	

Notes: 1. Tuned narrow band test.

ASP-0910
10 Watt, 900 MHz Class C Power Transistor

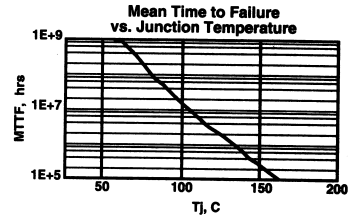
Absolute Maximum Ratings

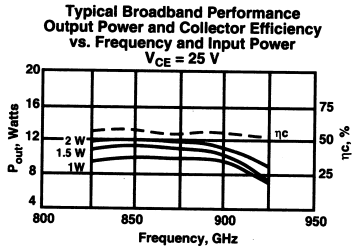
Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	4.0 V
Collector-Emitter Voltage	V_{CES}	50 V
Collector Current	I_C	2.0 A
Power Dissipation[2, 3]	P_T	25 W
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	-65 to 150°C

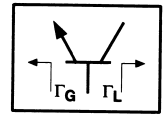
Thermal Resistance[2]: θ_{jc} = 6.3°C/W

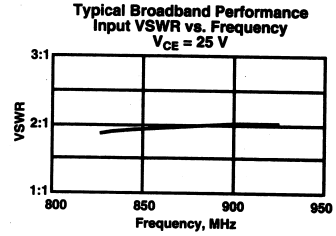
Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{case} = 25°C
3. Derate at .16 W/°C for T_{case} > 45°C

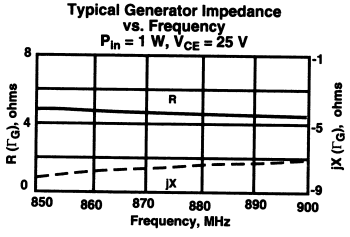
Typical Performance, T_A = 25°C
(Unless otherwise noted.)



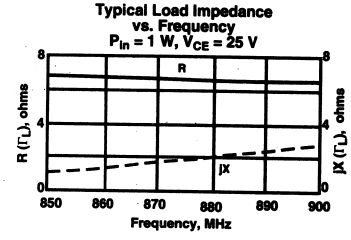




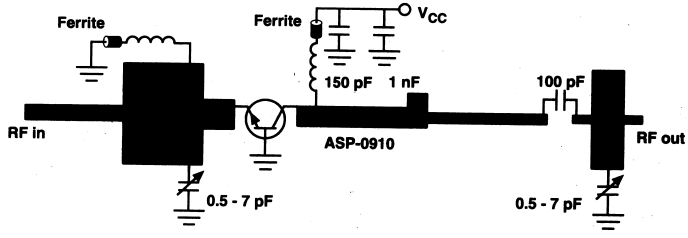




Freq.	Γ_G		Γ_L	
MHz	R	jX	R	jX
850	4.9	-8.1	6.9	1.1
860	4.8	-7.9	6.9	1.4
870	4.7	-7.7	6.9	1.7
880	4.6	-7.5	6.8	2.0
890	4.6	-7.3	6.8	2.4
900	4.5	-7.1	6.7	2.7



Test Circuit Layout and Schematic
850-900 MHz



Inductors are 3T 0.1" dia. 30 mil wire

(not to scale)

HEWLETT PACKARD

ASP-0955
55 Watt, 900 MHz
Silicon Power Transistor

Features

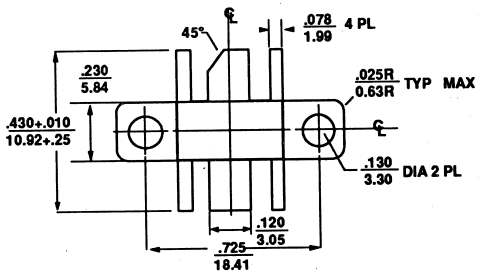
- **Power Out: 55 Watts**
- **Common Base Class C Power Transistor**
- **Frequency: 800-960 MHz**
- **Voltage: 25 V**
- **Efficiency: 50% Min.**
- **Load Mismatch Tolerance: 4.3:1**

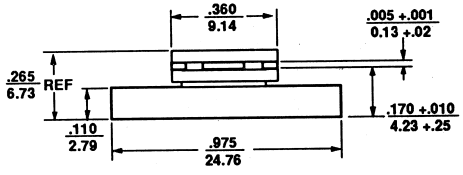
Description

The ASP-0955 is a large signal, Class C common base, NPN silicon bipolar power transistor, housed in a BeO flange package for excellent thermal transfer. This device is designed for use as a 55 W driver or output amplifier for base station applications in cellular telephone systems operating in the 830 to 960 MHz frequency range.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of these devices. Emitter ballasting ensures a rugged device capable of withstanding severe load mismatches.

Power Flange

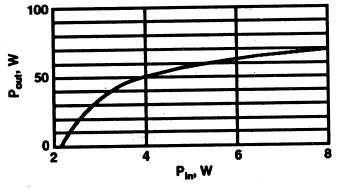




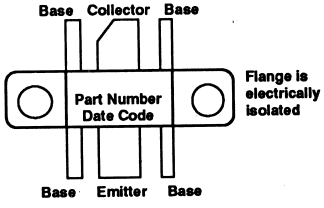
Dimensions are $\frac{\text{in}}{\text{mm}}$

Tolerances: in .xxx = ±.005 mm .xx = ±.13

Power Output vs. Power Input
V_{CE} = 25 V, f = 900 MHz
(Broadband performance in demo circuit)



Marking and Lead Configuration



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
P_{out}	Output Power[1]	V_{CE} = 25 V, Pin = 7 W, f = 900 MHz	Watts	55	58	
G_P	Power Gain[1]	V_{CE} = 25 V, Pin = 7 W, f = 900 MHz	dB	8.9	9.2	
η_C	Collector Efficiency[1]	V_{CE} = 25 V, Pin = 7 W, f = 900 MHz	%	50	55	
	Load Mismatch Tolerance	V_{CE} = 25 V, rated P_{out}, f = 900 MHz	-	4.3:1		
BV_{CEO}	Collector-Emitter Voltage	V_{EB} = open, I_C = 50 mA	V	24	28	
BV_{CES}	Collector-Emitter Voltage	V_{EB} = 0 V, I_C = 100 mA	V	50	55	
BV_{EBO}	Emitter-Base Voltage	V_{CB} = open, I_E = 15 mA	V	3.5	4.5	
h_{FE}	Forward Current Transfer Ratio	V_{CE} = 5 V, I_C = 3 A	-	20	60	120
I_{CES}	Collector Leakage Current	V_{CE} = 26 V	mA		1	15
C_{OB}	Collector-Base Capacitance	f = 1 MHz, V_{CB} = 25 V, I_E = 0 mA	pF		62	

Notes: 1. Tuned narrow band test.

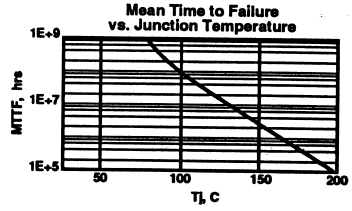
Absolute Maximum Ratings

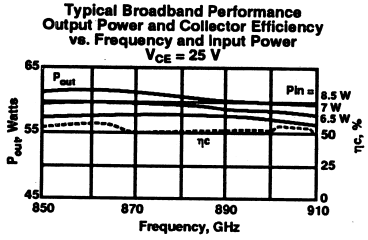
Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	4.0 V
Collector-Emitter Voltage	V_{CES}	50 V
Collector Current	I_C	8.0 A
Power Dissipation[2, 3]	P_T	115 W
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	-65 to 150°C

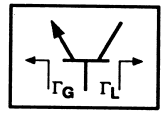
Thermal Resistance[2]: θ_{jc} = 1.2°C/W

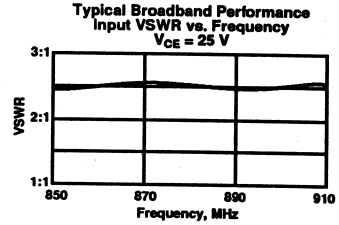
Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{case} = 25°C
3. Derate at .83 W/°C for T_{case} > 62°C

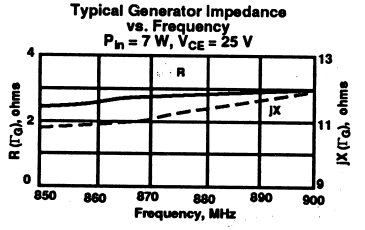
Typical Performance, T_A = 25°C
(Unless otherwise noted.)



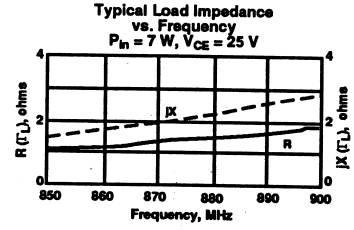




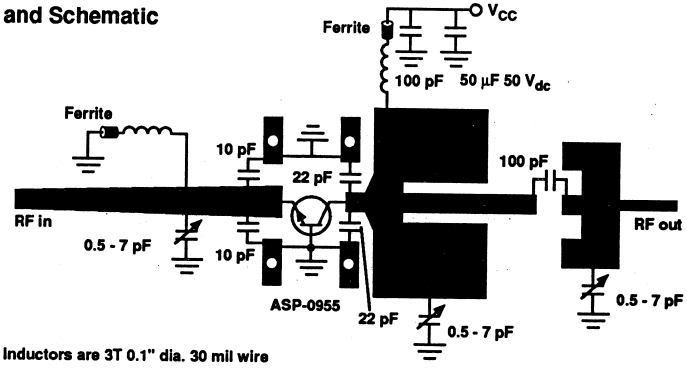




Freq.	Γ_G		Γ_L	
MHz	R	jX	R	jX
850	2.5	10.8	1.3	1.6
860	2.6	11.0	1.4	1.8
870	2.8	11.2	1.5	2.0
880	2.9	11.5	1.6	2.3
890	3.0	11.7	1.8	2.6
900	3.1	12.0	2.0	2.9



Test Circuit Layout and Schematic
850-900 MHz



(not to scale)

HEWLETT PACKARD

AT-00500
Up to 4 GHz General Purpose Silicon Bipolar Transistor Chip

Features

- **16.0 dBm typical $P_{1\,dB}$ at 2.0 GHz**
- **11.5 dB typical $G_{1\,dB}$ at 2.0 GHz**
- **2.5 dB typical NF_O at 2.0 GHz**
- **High Gain-Bandwidth Product: 9.0 GHz typical f_T**

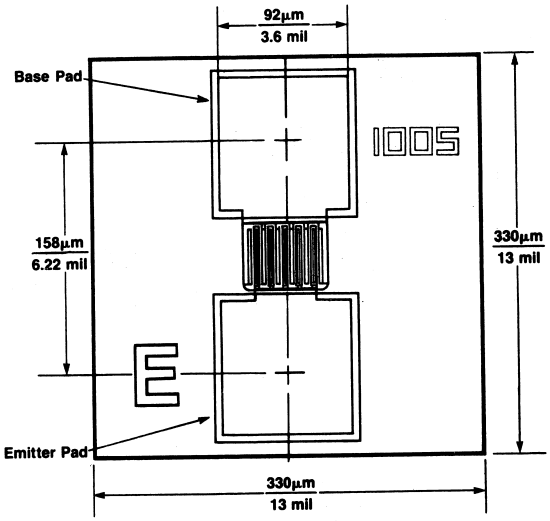
Description

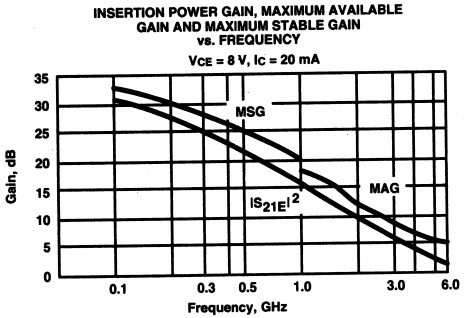
The AT-00500 is a high performance NPN silicon bipolar transistor chip designed for use in wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

The die are nitride-passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire. See also "Chip Use" in the APPLICATIONS section.

Chip Outline





Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 20 mA	f = 1.0 GHz f = 2.0 GHz	dB		15.5 9.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 20 mA	f = 2.0 GHz	dB		16.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 20 mA	f = 2.0 GHz	dB		11.5	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 5 mA	f = 2.0 GHz	dB		2.5	
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 5 mA	f = 2.0 GHz	dB		10.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 20 mA		GHz		9.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8V, I_C = 20 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		µA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		µA			1.0
C_{CB}	Collector Base Capacitance[2]: V_{CB} = 8 V, f = 1 MHz		pF		0.45	

Notes: 1. RF performance is determined by packaging and testing 10 devices per wafer.
2. For this test, the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	50 mA
Power Dissipation[2,3]	P_T	500 mW
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 75°C/W

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 13.3 mW/°C for T_C > 163°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

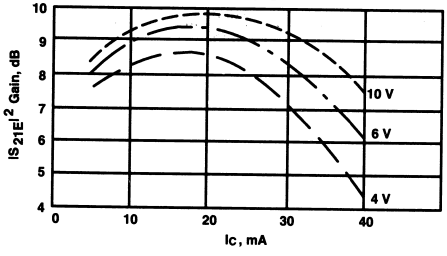
Part Number Ordering Information

Part Number	Devices Per Tray
AT-00500-GP2	10
AT-00500-GP4	100
AT-00500-GP6	up to 300

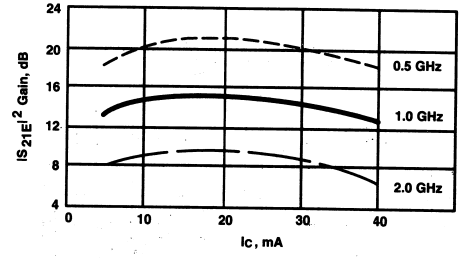
Typical Performance, T_A = 25°C

(unless otherwise noted)

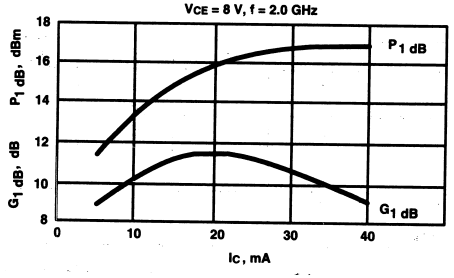
INSERTION POWER GAIN
vs. COLLECTOR CURRENT AND COLLECTOR VOLTAGE
f = 2.0 GHz



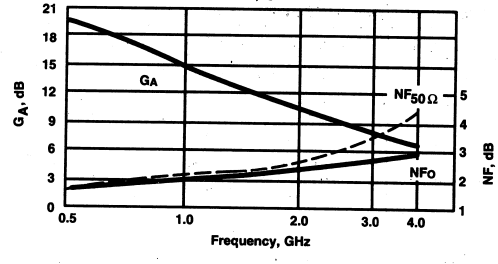
INSERTION POWER GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



OUTPUT POWER AND 1 dB COMPRESSED GAIN
vs. COLLECTOR CURRENT
V_{CE} = 8 V, f = 2.0 GHz



NOISE FIGURE AND ASSOCIATED GAIN
vs.FREQUENCY
V_{CE} = 8 V, I_C = 5 mA



Typical Scattering Parameters: Common Emitter, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 5$ mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.87	–29	23.2	14.43	161	–32.4	.024	76	.96	–14
0.5	.66	–103	18.2	8.17	116	–23.2	.069	45	.61	–42
1.0	.57	–142	13.6	4.78	94	–21.4	.085	40	.44	–47
1.5	.54	–162	10.2	3.24	81	–20.4	.096	44	.39	–50
2.0	.54	–176	8.0	2.51	72	–19.4	.107	49	.38	–53
2.5	.54	178	6.1	2.02	64	–18.6	.118	52	.38	–55
3.0	.56	171	4.8	1.73	55	–17.5	.134	53	.39	–59
3.5	.56	163	3.6	1.52	51	–16.5	.149	58	.40	–63
4.0	.58	158	2.5	1.33	44	–15.9	.160	59	.43	–66
4.5	.59	153	1.6	1.20	39	–15.1	.176	60	.46	–71
5.0	.59	149	0.6	1.07	33	–14.2	.194	61	.48	–76
5.5	.60	144	–0.1	0.99	29	–13.8	.204	62	.50	–83
6.0	.62	141	–1.1	0.88	23	–13.4	.215	63	.54	–88

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 20$ mA

0.1	.64	–66	30.4	33.05	145	–35.4	.017	65	.82	–29
0.5	.56	–149	21.1	11.31	99	–28.4	.038	52	.34	–53
1.0	.55	–172	15.5	5.96	86	–24.9	.057	61	.25	–52
1.5	.55	178	11.9	3.95	77	–22.3	.077	66	.24	–54
2.0	.56	169	9.6	3.03	70	–20.3	.097	68	.25	–56
2.5	.55	165	7.6	2.41	64	–18.8	.115	69	.26	–59
3.0	.57	160	6.3	2.06	57	–17.3	.136	69	.27	–63
3.5	.57	155	5.1	1.81	53	–16.2	.155	70	.28	–67
4.0	.59	150	3.9	1.57	47	–15.4	.170	69	.32	–70
4.5	.60	146	3.1	1.42	43	–14.3	.192	69	.35	–75
5.0	.60	144	2.1	1.27	38	–13.7	.207	62	.37	–79
5.5	.62	139	1.4	1.18	33	–13.1	.221	68	.39	–85
6.0	.62	136	0.4	1.05	29	–12.5	.237	68	.43	–90

A model for this device is available in the DEVICE MODELS section.

AT-00510
Up to 4 GHz General Purpose Silicon Bipolar Transistor

Features

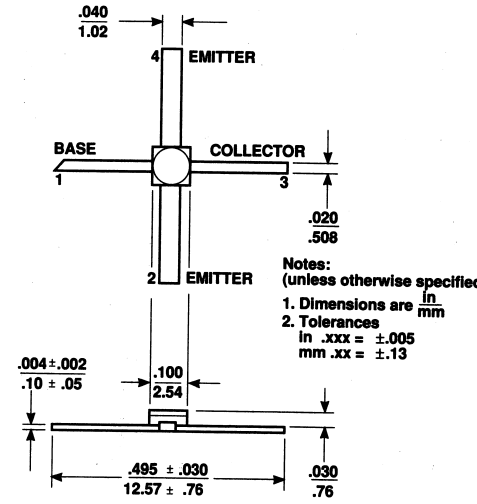
- **16.0 dBm typical $P_{1\,dB}$ at 2.0 GHz**
- **10.5 dB typical $G_{1\,dB}$ at 2.0 GHz**
- **2.5 dB typical NF_O at 2.0 GHz**
- **High Gain-Bandwidth Product: 8.0 GHz typical f_T**
- **Hermetic Gold-ceramic Microstrip Package**

Description

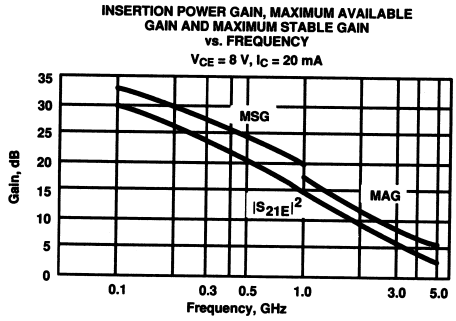
The AT-00510 is a high performance NPN silicon bipolar transistor housed in a hermetic, high reliability package. This device is designed for use in wide band amplifier and oscillator applications operating over VHF, UHF and mcirowave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

100 mil Package



Outline 10A



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 20 mA	f = 1.0 GHz f = 2.0 GHz	dB	13.0	15.0 9.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 20 mA	f = 2.0 GHz	dBm		16.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 20 mA	f = 2.0 GHz	dB		10.5	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 5 mA	f = 2.0 GHz	dB		2.5	
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 5 mA	f = 2.0 GHz	dB		10.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 20 mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 20 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		µA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		µA			1.0
C_{CB}	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		0.5	

Note: 1. For this test, the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	50 mA
Power Dissipation[2,3]	P_T	500 mW
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	–65°C to 200°C

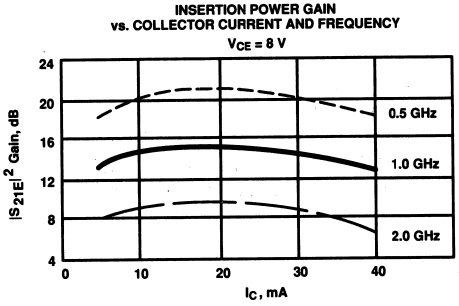
Thermal Resistance[2,4]: θ_{jc} = 150°C/W

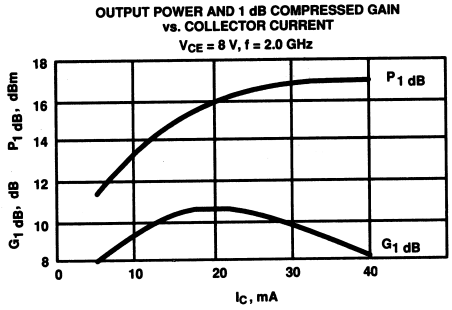
Notes:

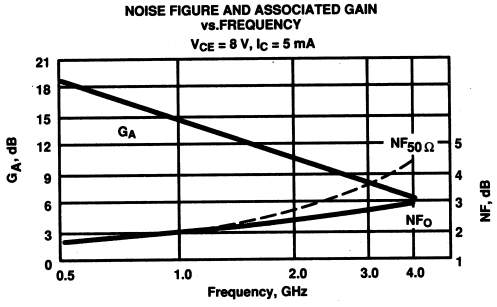
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 6.7 mW/°C for T_C > 125°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)







Typical Scattering Parameters: Common Emitter, Z_O = 50 Ω

T_A = 25°C, V_{CE} = 8 V, I_C = 5 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	.75	–31	23.3	14.61	160	–31.7	.026	81	.95	–16
0.5	.60	–112	18.3	8.22	111	–23.0	.071	42	.58	–51
1.0	.54	–152	13.4	4.65	85	–21.4	.085	33	.41	–63
1.5	.52	–173	10.2	3.24	69	–20.1	.099	33	.36	–70
2.0	.52	171	7.9	2.49	55	–19.2	.109	33	.35	–77
2.5	.53	163	6.3	2.07	47	–17.8	.128	35	.33	–81
3.0	.55	153	4.9	1.75	36	–17.1	.139	36	.34	–90
3.5	.55	143	3.8	1.54	24	–16.1	.157	32	.36	–101
4.0	.55	134	2.7	1.37	13	–15.4	.170	30	.38	–111
4.5	.55	123	1.9	1.24	3	–14.4	.190	25	.40	–121
5.0	.55	111	1.1	1.14	8	–13.7	.206	20	.42	–131

T_A = 25°C, V_{CE} = 8 V, I_C = 20 mA

0.1	.47	–71	29.7	30.66	145	–34.4	.019	63	.83	–30
0.5	.52	–156	20.8	10.90	97	–27.7	.041	51	.34	–66
1.0	.53	–179	15.1	5.68	78	–24.7	.058	52	.24	–72
1.5	.52	167	11.8	3.87	65	–21.4	.085	55	.22	–76
2.0	.53	156	9.4	2.94	53	–19.6	.105	51	.22	–84
2.5	.54	151	7.7	2.42	46	–17.8	.128	51	.22	–88
3.0	.56	143	6.2	2.04	37	–16.7	.146	50	.23	–98
3.5	.56	135	5.0	1.78	26	–15.6	.165	44	.25	–107
4.0	.55	126	4.0	1.59	16	–14.6	.186	39	.27	–117
4.5	.55	117	3.2	1.44	6	–13.7	.206	32	.30	–126
5.0	.56	105	2.4	1.32	–4	–13.0	.223	26	.31	–135

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

AT-00511
Surface Mount General Purpose Silicon Bipolar Transistor

Features

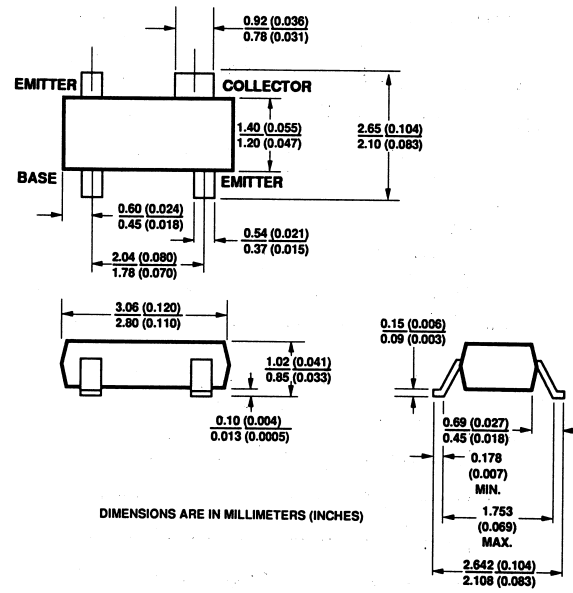
- 11 dB Typical P_{1dB} at 2.0 GHz
- 11.5 dB Typical G_{1dB} at 2.0 GHz
- 1.8 dB typical NF_O at 1.0 GHz
- High Gain-Bandwidth Product: 7.0 GHz Typical f_T
- Low Cost Surface Mount Plastic Package
- Tape-and-Reel Package Option Available[1]

Description

The AT-00511 is a low cost NPN silicon bipolar transistor housed in the surface mount plastic SOT-143 package. This device is designed for use in low noise, wideband amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

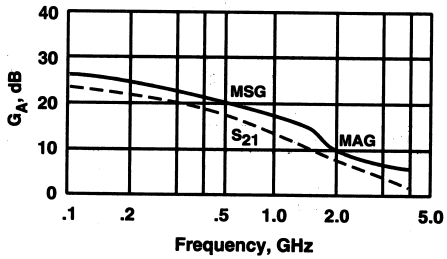
Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

SOT-143 Plastic Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency
V_{CE} = 8V, I_C= 5 mA



Typical Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

FREQ GHz	NF_O dB	Γ OPT MAG	Γ OPT ANG	R_N/Z_O -
0.1	1.3	.50	4	0.45
0.5	1.4	.46	19	0.44
1.0	1.8	.37	38	0.42
2.0	2.7	.22	87	0.37
4.0	4.4	.20	-154	0.42

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 5 mA	f = 1.0 GHz	dB	11.0	12.5	
		f = 2.0 GHz			7.2	
P_{1dB}	Power Output @ 1 dB Compression: V_{CE} = 8 V, I_C = 15 mA	f = 2.0 GHz	dBm		11.0	
G_{1dB}	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 15 mA	f = 2.0 GHz	dB		11.5	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 5 mA	f = 1.0 GHz	dB		1.8	
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 10 mA	f = 1.0 GHz	dB		11.0	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 15 mA		GHz		7.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 20 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		µA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		µA			1.0

Notes: 1. Refer to PACKAGING Section of Data Book, "Tape-and-Reel Packaging for Semiconductor Devices."

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	I_{CEO}	12 V
Collector Current	I_C	50 mA
Power Dissipation [2,3]	P_T	230 mW
Junction Temperature	T_J	150°C
Storage Temperature	T_{STG}	-65°C to 150°C

Thermal Resistance [2,4]: θ_{jc}=530°C/W

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{case} = 25°C
3. Derate at 1.9 mW/ °C for T_C>28°C
4. See MEASUREMENTS section of DATA BOOK for more information

Part Number Order Information

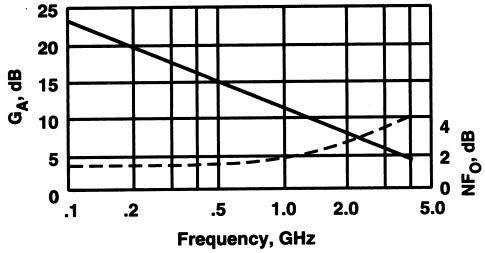
Part Number	Devices Per Reel	Reel Size
AT-00511-TR1	3000	7"
AT-00511-TR2	10000	13"

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

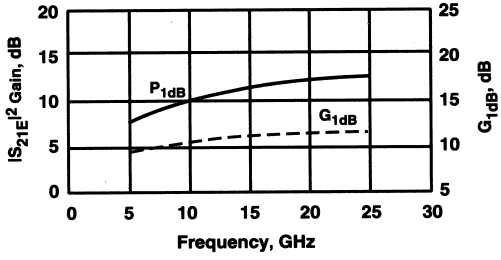
Typical Performance, T_A = 25°C

(Unless otherwise noted)

Noise Figure and Associated Gain vs. Frequency
V_{CE} = 8V, I_C= 5 mA



Output Power and 1dB Compressed Gain vs. Collector Current
V_{CE} = 8V, f = 2 GHz



Typical Scattering Parameters: Common Source, Z_o = 50 Ω

T_A = 25°C, V_{CE} = 8 V, I_C = 5 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.88	-28	22.76	13.73	159	-31.42	.027	79	.95	-15
0.5	.59	-100	17.52	7.52	110	-23.12	.070	43	.60	-43
1.0	.45	-138	12.54	4.23	85	-20.73	.092	41	.47	-52
1.5	.40	-162	9.45	2.97	69	-19.12	.111	42	.45	-57
2.0	.38	178	7.25	2.30	56	-17.70	.130	41	.44	-62
2.5	.39	163	5.60	1.91	47	-16.69	.146	44	.44	-65
3.0	.41	147	4.19	1.62	36	-15.75	.163	44	.43	-73
3.5	.46	136	2.88	1.39	25	-14.81	.182	39	.43	-83
4.0	.49	127	1.73	1.22	15	-13.95	.201	37	.44	-94

Typical Scattering Parameters: Common Source, Z_o = 50 Ω

T_A = 25°C, V_{CE}= 8 V, I_C = 15 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.71	-51	28.12	25.48	147	-33.11	.022	70	.85	-25
0.5	.49	-136	19.56	9.51	99	-26.28	.049	50	.41	-50
1.0	.43	-166	14.00	5.01	80	-22.83	.072	52	.34	-54
1.5	.41	176	10.72	3.43	67	-20.61	.093	53	.34	-58
2.0	.41	160	8.41	2.63	55	-18.27	.122	54	.35	-64
2.5	.42	149	6.68	2.16	48	-16.70	.146	53	.35	-68
3.0	.45	137	5.21	1.82	38	-15.56	.167	52	.34	-76
3.5	.48	127	3.94	1.57	28	-14.45	.189	49	.35	-89
4.0	.51	119	2.75	1.37	20	-13.45	.213	45	.36	-99

HEWLETT PACKARD

AT-00535
Up to 4 GHz General Purpose Silicon Bipolar Transistor

Features

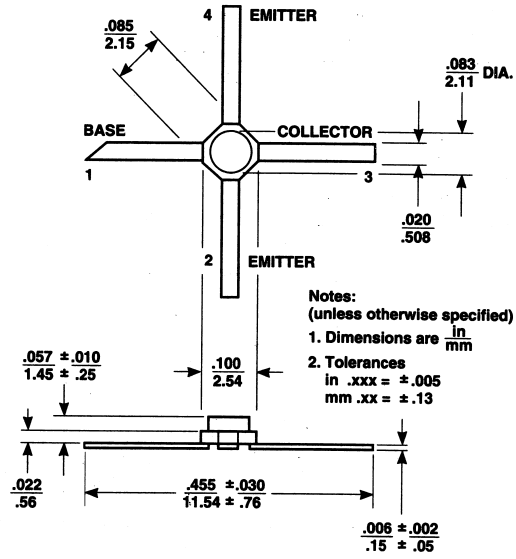
- **16.0 dBm typical $P_{1\,dB}$ at 2.0 GHz**
- **10.5 dB typical $G_{1\,dB}$ at 2.0 GHz**
- **2.5 dB typical NF_O at 2.0 GHz**
- **High Gain-Bandwidth Product: 8.0 GHz typical f_T**
- **Cost Effective Ceramic Microstrip Package**

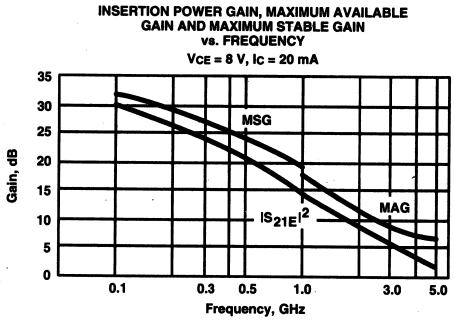
Description

The AT-00535 is a high performance NPN silicon bipolar transistor housed in a cost effective, microstrip package. This device is designed for use in wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

35 micro-X Package





Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 20 mA	f = 1.0 GHz f = 2.0 GHz	dB	13.0	15.0 9.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 20 mA	f = 2.0 GHz	dBm		16.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 20 mA	f = 2.0 GHz	dB		10.5	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 5 mA	f = 2.0 GHz	dB		2.5	
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 5 mA	f = 2.0 GHz	dB		10.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 20 mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 20 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		µA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		µA			1.0
C_{CB}	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		0.5	

Note: 1. For this test, the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	50 mA
Power Dissipation[2,3]	P_T	500 mW
Junction Temperature	T_j	200°C
Storage Temperature[4]	T_{STG}	–65°C to 200°C

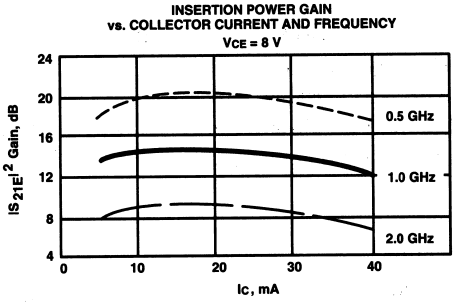
Thermal Resistance[2,5]: θ_{jc} = 180°C/W

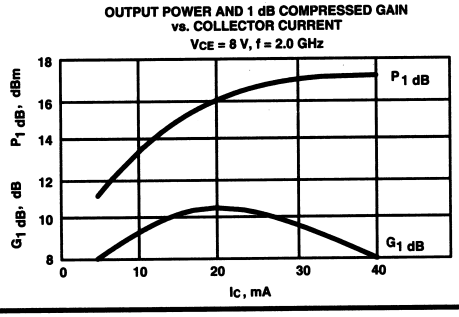
Notes:

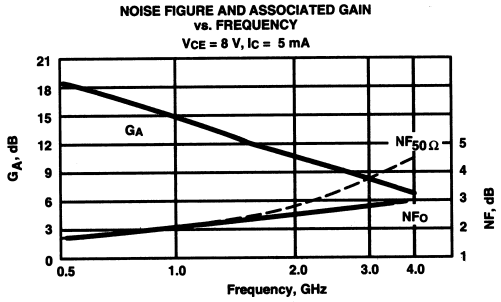
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 5.6 mW/°C for T_{CASE} > 110°C.
4. Storage above 150°C may tarnish the leads of this package making it difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safely stored up to 200°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)







Typical Scattering Parameters: Common Emitter, Z_O = 50 Ω

T_A = 25°C, V_{CE} = 8 V, I_C = 5 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	.82	–29	23.4	14.90	159	–33.1	.022	69	.95	–16
0.5	.58	–106	18.3	8.20	110	–23.4	.068	44	.58	–47
1.0	.49	–149	13.4	4.67	83	–20.9	.090	37	.41	–57
1.5	.48	–175	10.3	3.28	66	–19.6	.105	39	.35	–64
2.0	.49	167	8.1	2.53	52	–18.1	.125	37	.32	–74
2.5	.50	156	6.4	2.10	43	–17.0	.141	41	.31	–82
3.0	.53	144	5.0	1.78	31	–15.9	.160	39	.30	–97
3.5	.54	134	3.9	1.56	19	–15.0	.178	36	.34	–110
4.0	.54	124	2.8	1.38	8	–13.9	.202	34	.37	–120
4.5	.55	112	2.0	1.25	–3	–12.8	.229	29	.39	–129
5.0	.56	98	1.2	1.15	–15	–11.9	.253	23	.40	–139

T_A = 25°C, V_{CE} = 8 V, I_C = 20 mA

0.1	.56	–63	29.6	30.24	143	–34.4	.019	62	.81	–28
0.5	.47	–150	20.3	10.37	96	–27.3	.043	54	.36	–52
1.0	.47	–178	14.7	5.43	76	–23.4	.068	56	.27	–54
1.5	.48	165	11.4	3.71	62	–20.4	.095	57	.24	–61
2.0	.50	152	9.1	2.84	49	–18.3	.121	53	.23	–72
2.5	.51	145	7.3	2.33	41	–16.7	.146	53	.21	–82
3.0	.54	135	5.9	1.96	31	–15.5	.167	50	.23	–98
3.5	.56	126	4.7	1.72	20	–14.2	.194	44	.26	–113
4.0	.56	116	3.7	1.53	9	–13.2	.219	40	.29	–123
4.5	.55	106	2.8	1.38	–2	–12.2	.244	32	.32	–131
5.0	.57	93	2.1	1.27	–13	–11.3	.273	25	.33	–141

A model for this device is available in the DEVICE MODELS section.

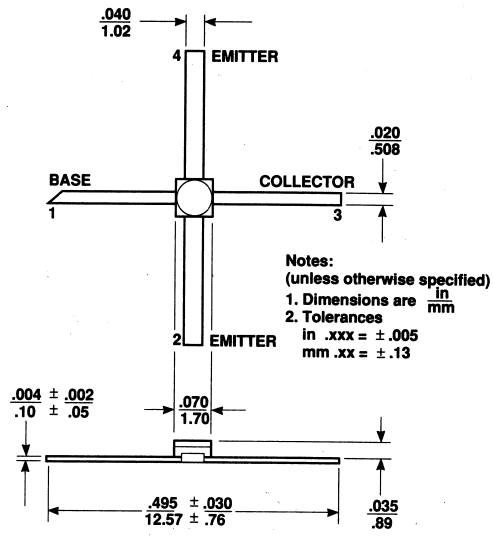
HEWLETT PACKARD

AT-00570
Up to 4 GHz General Purpose Silicon Bipolar Transistor

Features

- **16.0 dBm typical $P_{1\,dB}$ at 2.0 GHz**
- **11.5 dB typical $G_{1\,dB}$ at 2.0 GHz**
- **2.5 dB typical NF_O at 2.0 GHz**
- **High Gain-Bandwidth Product: 8.0 GHz typical f_T**
- **Hermetic Gold-ceramic Microstrip Package**

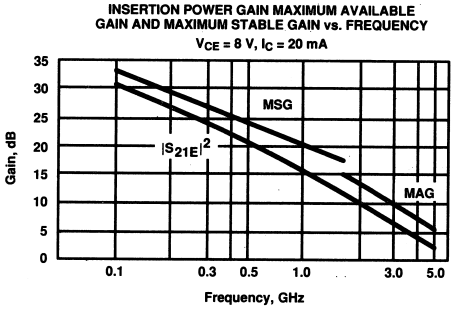
70 mil Package



Description

The AT-00570 is a high performance NPN silicon bipolar transistor housed in a hermetic, high reliability package. This device is designed for use in wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 20 mA	f = 1.0 GHz f = 2.0 GHz	dB	14.0	15.5 9.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 20 mA	f = 2.0 GHz	dBm		16.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 20 mA	f = 2.0 GHz	dB		11.5	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 5 mA	f = 2.0 GHz	dB		2.5	
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 5 mA	f = 2.0 GHz	dB		10.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 20 mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 20 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		μA			1.0
C_{CB}	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		0.5	

Note: 1. For this test, the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	50 mA
Power Dissipation[2,3]	P_T	500 mW
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	–65°C to 200°C

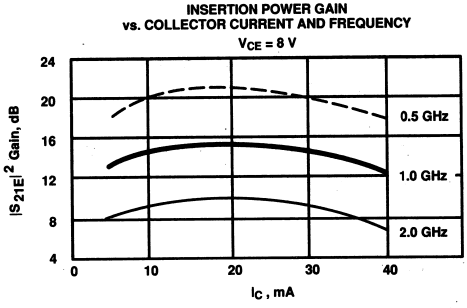
Thermal Resistance[2,4]: θ_{jc} = 155°C/W

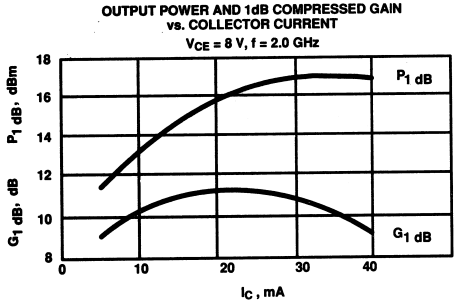
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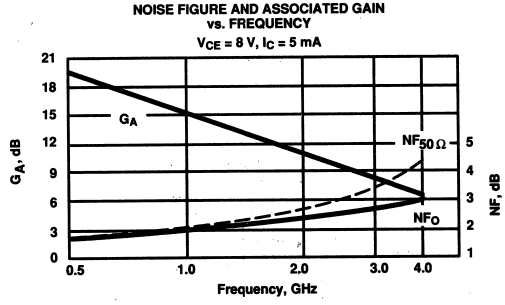
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 6.5 mW/°C for T_C > 123°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)







Typical Scattering Parameters: Common Emitter, Z_O = 50 Ω

T_A = 25°C, V_{CE} = 8 V, I_C = 5 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	.82	–29	23.4	14.78	160	–33.1	.022	83	.95	–15
0.5	.64	–106	18.5	8.41	113	–23.5	.067	40	.59	–49
1.0	.57	–144	13.6	4.79	88	–21.2	.087	33	.42	–60
1.5	.55	–164	10.5	3.35	73	–20.4	.096	33	.38	–66
2.0	.54	–178	8.2	2.57	60	–19.5	.106	32	.36	–74
2.5	.54	175	6.6	2.13	53	–18.4	.120	35	.36	–78
3.0	.54	167	5.0	1.79	43	–17.7	.130	36	.37	–87
3.5	.54	159	3.8	1.56	32	–17.2	.138	33	.40	–97
4.0	.53	153	2.8	1.38	22	–16.3	.153	31	.44	–104
4.5	.52	145	1.9	1.24	13	–15.6	.166	28	.47	–110
5.0	.50	135	1.1	1.13	4	–14.9	.180	24	.49	–117

T_A = 25°C, V_{CE} = 8 V, I_C = 20 mA

0.1	.57	–68	30.2	32.27	145	–37.1	.014	64	.82	–30
0.5	.56	–151	21.0	11.22	98	–28.4	.038	47	.34	–62
1.0	.55	–173	15.3	5.84	80	–24.7	.058	53	.26	–68
1.5	.55	175	12.0	3.96	68	–22.6	.074	55	.25	–71
2.0	.54	165	9.6	3.00	57	–20.9	.090	52	.26	–78
2.5	.55	161	7.8	2.45	52	–19.0	.112	54	.27	–81
3.0	.55	156	6.3	2.06	43	–18.2	.123	51	.29	–90
3.5	.55	149	5.0	1.78	34	–17.0	.141	48	.33	–98
4.0	.54	144	3.9	1.57	25	–16.0	.159	43	.36	–103
4.5	.52	137	3.1	1.42	16	–15.1	.176	39	.40	–108
5.0	.50	128	2.3	1.30	8	–14.3	.192	35	.41	–112

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

AT-00572
Up to 1 GHz General Purpose Silicon Bipolar Transistor

Features

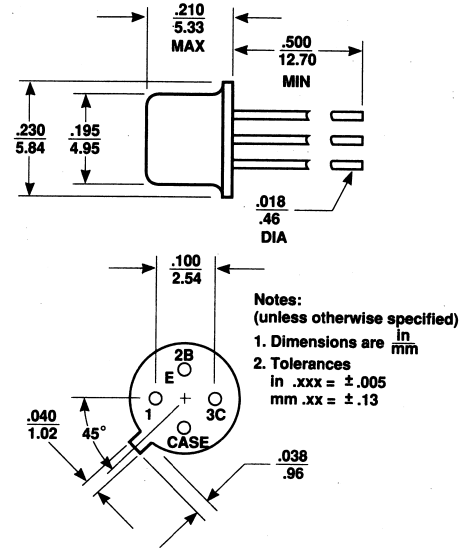
- **19.0 dBm typical $P_{1\,dB}$ at 1.0 GHz**
- **6.0 dB typical $G_{1\,dB}$ at 1.0 GHz**
- **2.3 dB typical NF_O at 1.0 GHz**
- **High Gain-Bandwidth Product: 6.5 GHz typical f_T**
- **Hermetic, Metal Package**

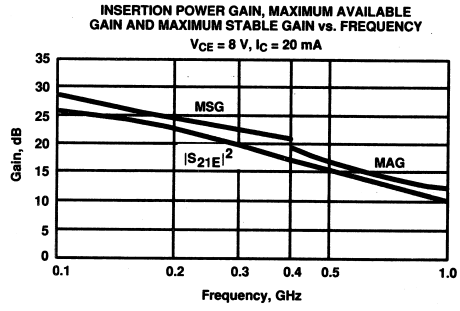
Description

The AT-00572 is a high performance NPN silicon bipolar transistor housed in a hermetic high reliability metal package. This device is designed for use in wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

TO-72 Package





Electrical Specifications, $T_A = 25°C$

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 20 mA	f = 0.5 GHz f = 1.0 GHz	dB	14.0	15.5 10.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 20 mA	f = 1.0 GHz	dBm		19.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 20 mA	f = 1.0 GHz	dB		6.0	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 5 mA	f = 0.5 GHz f = 1.0 GHz	dB		1.9 2.3	
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 5 mA	f = 0.5 GHz f = 1.0 GHz	dB		12.0 8.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 20 mA		GHz		6.5	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 20 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		μA			1.0
C_{CB}	Collector Base Capacitance[1]: V_{CE} = 8 V, f = 1 MHz		pF		0.65	

Note: 1. For this test, the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	50 mA
Power Dissipation[2,3]	P_T	500 mW
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	–65°C to 200°C

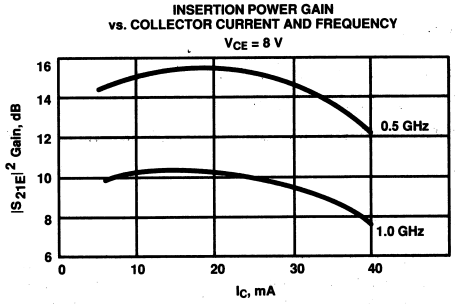
Thermal Resistance[2,4]: θ_{jc} = 235°C/W

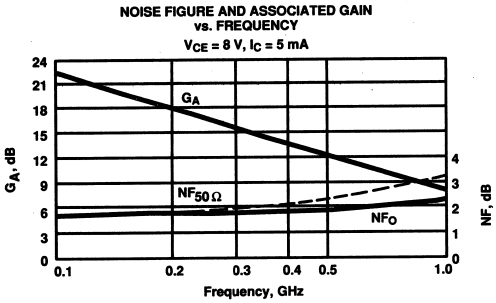
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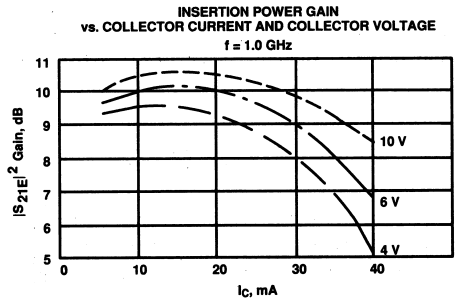
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 4.3 mW/°C for T_C > 83°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)







Typical Scattering Parameters: Common Emitter, Z_O = 50 Ω

T_A = 25°C, V_{CE} = 8 V, I_C = 5 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	.82	–22	19.1	8.99	150	–31.4	.027	75	.87	–19
0.2	.65	–40	18.7	8.57	129	–27.1	.044	72	.72	–27
0.3	.51	–54	17.6	7.55	116	–24.3	.061	69	.64	–30
0.4	.40	–61	16.0	6.29	103	–22.6	.074	66	.57	–30
0.5	.31	–65	14.6	5.34	94	–21.3	.086	65	.51	–31
0.6	.25	–70	13.5	4.73	91	–19.7	.103	67	.48	–35
0.7	.21	–73	12.4	4.17	84	–18.6	.118	65	.45	–39
0.8	.17	–76	11.6	3.81	79	–17.6	.131	64	.44	–43
0.9	.16	–81	10.5	3.37	76	–16.8	.145	65	.46	–47
1.0	.14	–83	10.0	3.14	72	–16.0	.158	64	.46	–48

T_A = 25°C, V_{CE} = 8 V, I_C = 20 mA

0.1	.51	–39	25.7	19.28	131	–32.8	.023	77	.74	–21
0.2	.33	–51	22.3	12.96	110	–28.2	.039	77	.60	–24
0.3	.24	–58	19.6	9.50	100	–25.2	.055	77	.53	–26
0.4	.19	–58	17.3	7.28	91	–23.2	.069	74	.49	–24
0.5	.16	–57	15.4	5.91	85	–21.6	.084	72	.46	–25
0.6	.13	–57	14.1	5.09	83	–19.8	.102	73	.44	–29
0.7	.11	–56	13.0	4.44	78	–18.5	.119	70	.42	–33
0.8	.09	–59	12.1	4.02	74	–17.5	.134	69	.41	–37
0.9	.08	–64	10.9	3.52	72	–16.5	.149	70	.43	–42
1.0	.08	–64	10.3	3.29	68	–15.8	.163	68	.44	–44

HEWLETT PACKARD

AT-01600
Up to 4 GHz General Purpose Silicon Bipolar Transistor Chip

Features

- **22.0 dBm typical $P_{1\,dB}$ at 2.0 GHz**
- **10.5 dB typical $G_{1\,dB}$ at 2.0 GHz**
- **High Gain-Bandwidth Product: 8.0 GHz typical f_T**

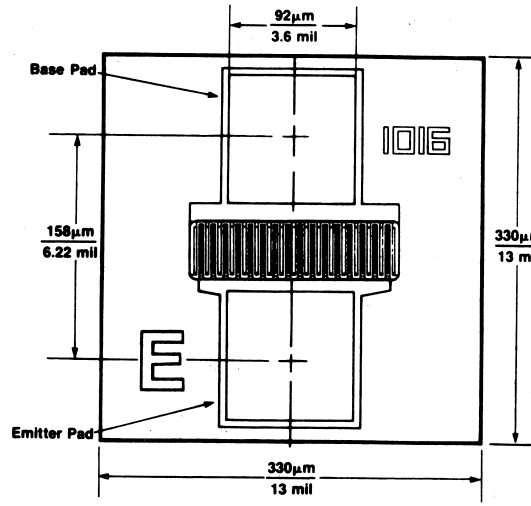
Description

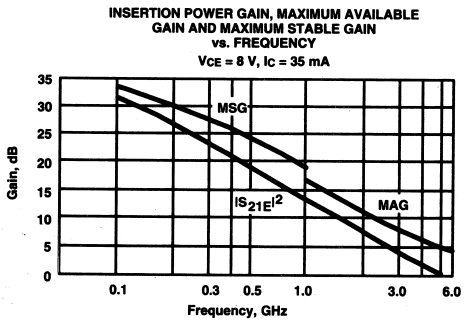
The AT-01600 is a high performance NPN silicon bipolar transistor chip designed for use in medium power, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

The die are nitride-passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire. See also "Chip Use" in the APPLICATIONS section.

Chip Outline





Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 35 mA	f = 1.0 GHz f = 2.0 GHz	dB		13.0 7.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 60 mA	f = 2.0 GHz	dBm		22.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 60 mA	f = 2.0 GHz	dB		10.5	
NFO	Optimum Noise Figure: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz	dB		3.0	
G_A	Gain @ NFO: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz	dB		10.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 35 mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 35 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		µA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		µA			2.0
C_{CB}	Collector Base Capacitance[2]: V_{CB} = 8 V, f = 1 MHz		pF		0.75	

Notes: 1. RF performance is determined by packaging and testing 10 devices per wafer.
2. For this test, the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	150 mA
Power Dissipation[2,3]	P_T	1000 mW
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 40°/W

Notes:

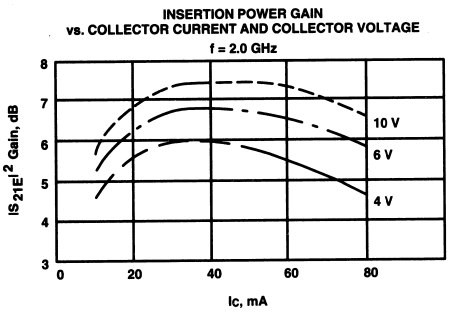
1. Operation of this device above any one of these parameters may cause permanent damage.
2. $T_{MOUNTING\ SURFACE}$ = 25°C.
3. Derate at 25 mW/°C for $T_{MOUNTING\ SURFACE}$ > 160°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

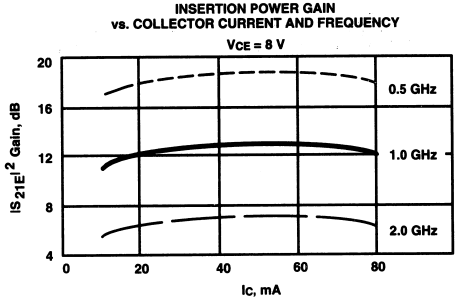
Part Number Ordering Information

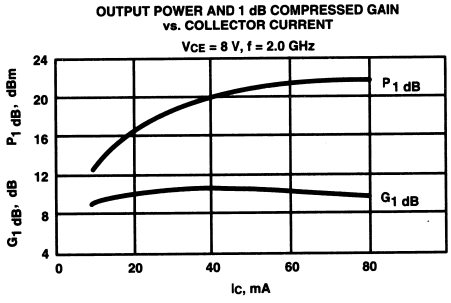
Part Number	Devices Per Tray
AT-01600-GP2	10
AT-01600-GP4	100
AT-01600-GP6	up to 300

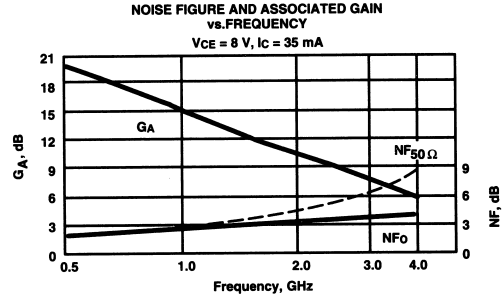
Typical Performance, T_A = 25°C

(unless otherwise noted)









Typical Scattering Parameters: Common Emitter, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 35$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.67	−124	31.1	35.75	123	−34.0	.020	47	.55	−71
0.5	.72	−172	18.7	8.64	90	−29.1	.035	53	.24	−128
1.0	.72	175	13.0	4.45	81	−24.9	.057	65	.22	−141
1.5	.72	169	9.4	2.94	73	−21.9	.080	69	.22	−143
2.0	.73	163	7.2	2.29	66	−19.7	.103	71	.22	−141
2.5	.72	160	5.4	1.86	60	−18.1	.124	72	.24	−139
3.0	.74	155	4.0	1.58	53	−16.6	.148	70	.25	−136
3.5	.73	150	2.9	1.40	49	−15.4	.170	71	.27	−135
4.0	.75	145	1.7	1.22	43	−14.0	.187	69	.29	−135
4.5	.75	141	0.8	1.10	39	−13.6	.210	69	.32	−133
5.0	.75	139	−0.2	0.98	35	−13.0	.225	67	.35	−132
5.5	.76	134	−0.7	0.92	29	−12.3	.242	67	.38	−133
6.0	.76	130	−1.7	0.82	26	−11.7	.261	66	.42	−134

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 60$ mA

0.1	.65	−146	31.6	38.06	119	−37.0	.014	48	.50	−77
0.5	.74	−178	19.0	8.94	90	−30.8	.029	65	.22	−134
1.0	.75	173	13.0	4.44	80	−25.7	.052	72	.21	−142
1.5	.75	168	9.5	2.99	73	−22.5	.075	76	.22	−142
2.0	.74	163	7.0	2.24	66	−20.4	.096	75	.23	−139
2.5	.75	157	5.4	1.86	62	−18.3	.121	76	.25	−137
3.0	.76	154	3.9	1.56	55	−16.8	.144	75	.27	−134
3.5	.75	150	2.7	1.36	50	−15.8	.162	75	.29	−133
4.0	.75	146	1.7	1.21	48	−14.8	.183	76	.32	−129
4.5	.76	143	0.5	1.06	42	−14.0	.200	74	.34	−130
5.0	.77	139	−0.2	0.98	39	−13.1	.221	74	.36	−127
5.5	.76	137	−1.0	0.89	35	−12.3	.243	73	.39	−127
6.0	.75	132	−1.6	0.83	31	−11.6	.262	71	.42	−126

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

AT-01610
Up to 4 GHz General Purpose Silicon Bipolar Transistor

Features

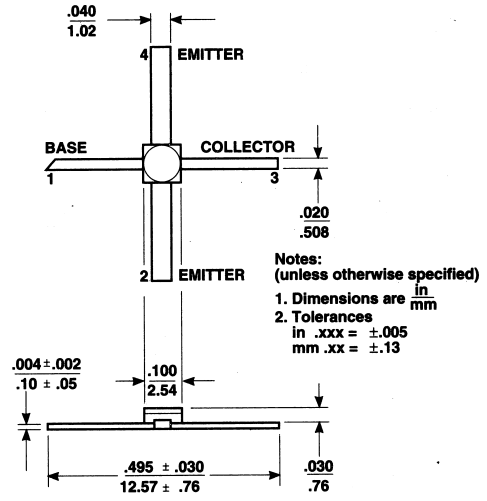
- **22.0 dBm typical $P_{1\,dB}$ at 2.0 GHz**
- **9.5 dB typical $G_{1\,dB}$ at 2.0 GHz**
- **High Gain-Bandwidth Product: 7.0 GHz typical f_T**
- **Hermetic Gold-ceramic Microstrip Package**

Description

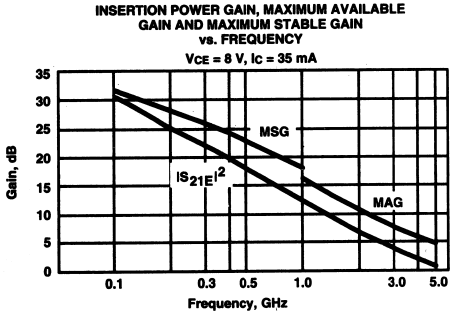
The AT-01610 is a high performance NPN silicon bipolar transistor housed in a hermetic, high reliability package. This device is designed for use in medium power, wide band amplifier applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

100 mil Package



Outline 10A



Electrical Specifications, $T_A = 25°C$

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 35 mA	f = 1.0 GHz f = 2.0 GHz	dB	11.0	12.5 6.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 60 mA	f = 2.0 GHz	dBm		22.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 60 mA	f = 2.0 GHz	dB		9.5	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz	dB		3.0	
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz	dB		10.0	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 35 mA		GHz		7.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 35 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		μA			2.0
C_{CB}	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		0.8	

Note: 1. For this test, the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	150 mA
Power Dissipation[2,3]	P_T	1000 mW
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	–65°C to 200°C

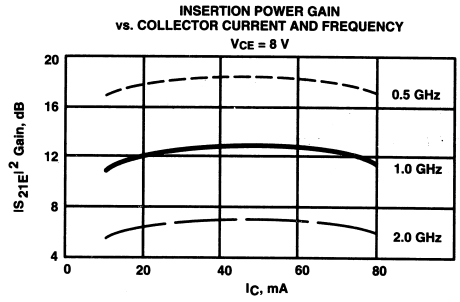
Thermal Resistance[2,4]: θ_{jc} = 115°C/W

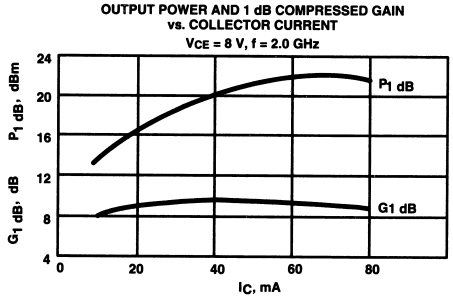
Notes:

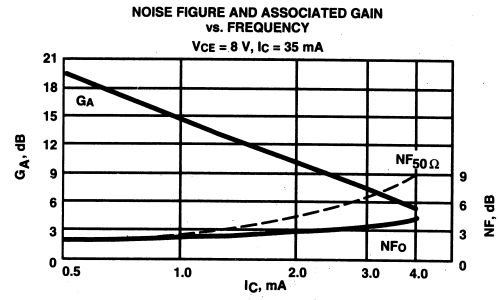
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 8.7 mW/°C for T_C > 85°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)







Typical Scattering Parameters: Common Emitter, Z_O = 50 Ω

T_A = 25°C, V_{CE} = 8 V, I_C = 35 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	.69	–125	30.9	35.08	119	–33.6	.021	44	.53	–80
0.5	.72	–175	18.3	8.22	86	–28.4	.038	45	.28	–146
1.0	.71	171	12.4	4.17	72	–24.6	.059	50	.26	–162
1.5	.71	160	9.1	2.85	60	–21.8	.081	56	.24	–169
2.0	.72	151	6.7	2.16	49	–19.4	.107	50	.24	–174
2.5	.72	147	5.1	1.80	42	–17.8	.129	51	.25	–175
3.0	.73	140	3.8	1.55	32	–16.7	.147	47	.25	179
3.5	.73	132	2.8	1.37	22	–15.5	.168	41	.27	176
4.0	.72	124	1.8	1.23	11	–14.6	.187	36	.28	173
4.5	.72	114	0.9	1.11	1	–13.5	.211	30	.29	169
5.0	.73	103	0.1	1.01	–9	–12.9	.226	23	.30	163

T_A = 25°C, V_{CE} = 8 V, I_C = 60 mA

0.1	.69	–138	31.5	37.69	114	–34.4	.019	42	.46	–92
0.5	.72	–178	18.4	8.34	85	–30.4	.030	60	.28	–154
1.0	.72	169	12.6	4.25	71	–24.6	.059	59	.25	–167
1.5	.72	159	9.3	2.91	60	–21.8	.081	59	.25	–173
2.0	.72	150	6.9	2.22	49	–19.3	.109	52	.24	–177
2.5	.72	146	5.2	1.83	42	–17.5	.133	54	.25	–179
3.0	.73	139	3.8	1.55	33	–16.6	.148	49	.26	176
3.5	.73	132	2.7	1.37	22	–15.4	.169	44	.27	174
4.0	.73	123	1.7	1.21	12	–14.4	.191	37	.29	171
4.5	.73	114	0.8	1.10	2	–13.5	.212	30	.30	166
5.0	.73	103	0.0	1.00	–8	–12.8	.228	24	.31	160

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

AT-01635
Up to 4 GHz General Purpose Silicon Bipolar Transistor

Features

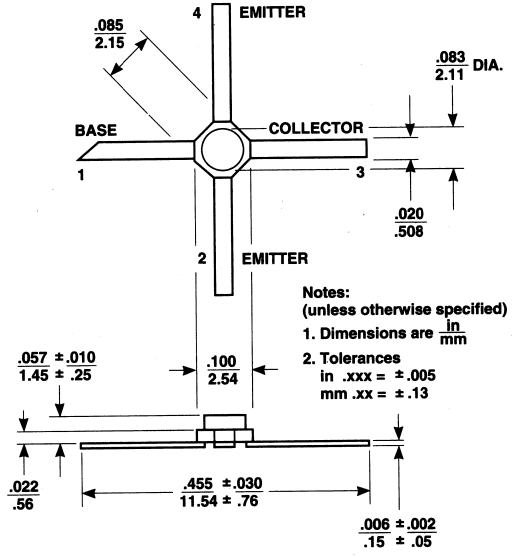
- **22.0 dBm typical $P_{1\,dB}$ at 2.0 GHz**
- **9.5 dB typical $G_{1\,dB}$ at 2.0 GHz**
- **High Gain-Bandwidth Product: 7.0 GHz typical f_T**
- **Cost Effective Ceramic Microstrip Package**

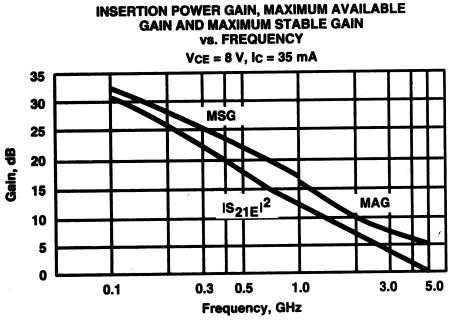
Description

The AT-01635 is a high performance NPN silicon bipolar transistor housed in a cost effective, microstrip package. This device is designed for use in medium power, wide band amplifier applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

35 micro-X Package





Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\lvert S_{21E}\rvert^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 35 mA	f = 1.0 GHz f = 2.0 GHz	dB	11.0	12.0 6.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 60 mA	f = 2.0 GHz	dBm		22.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 60 mA	f = 2.0 GHz	dB		9.5	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz	dB		3.0	
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz	dB		10.0	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 35 mA		GHz		7.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 35 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		µA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		µA			2.0
C_{CB}	Collector Base Capacitance[1]: V_{CE} = 8 V, f = 1 MHz		pF		0.8	

Note: 1. For this test, the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	150 mA
Power Dissipation[2,3]	P_T	1000 mW
Junction Temperature	T_j	200°C
Storage Temperature[4]	T_{STG}	−65°C to 200°C

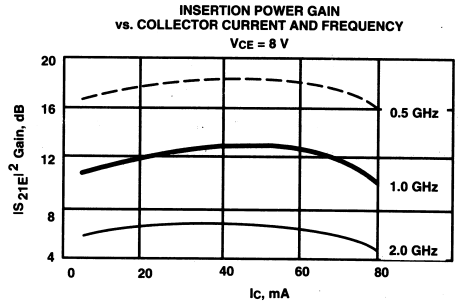
Thermal Resistance[2,5]: θ_{jc} = 145°C/W

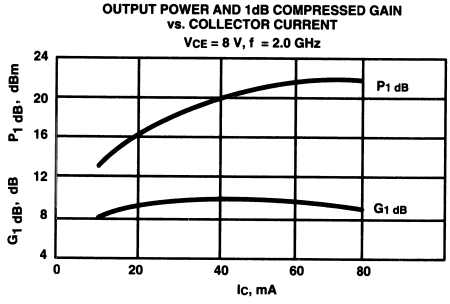
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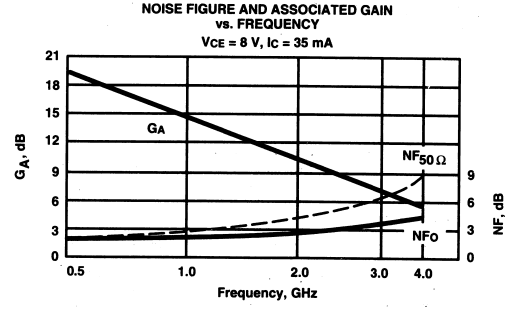
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 6.9 mW/°C for T_C > 55°C.
4. Storage above 150°C may tarnish the leads of this package making it difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safely stored up to 200°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)







Typical Scattering Parameters: Common Emitter, Z_O = 50 Ω

T_A = 25°C, V_{CE} = 8 V, I_C = 35 mA

Freq. GHz	S11 Mag	S11 Ang	S21 dB	S21 Mag	S21 Ang	S12 dB	S12 Mag	S12 Ang	S22 Mag	S22 Ang
0.1	.61	−119	30.6	33.90	119	−32.4	.024	52	.50	−69
0.5	.62	−173	18.0	7.97	85	−26.0	.050	53	.20	−130
1.0	.63	169	12.3	4.10	68	−21.4	.085	52	.18	−152
1.5	.65	157	9.0	2.80	55	−19.0	.112	48	.18	−167
2.0	.67	146	6.6	2.14	42	−17.1	.139	43	.20	−178
2.5	.69	140	4.9	1.75	34	−15.7	.164	41	.23	176
3.0	.71	132	3.4	1.47	23	−14.9	.180	36	.25	172
3.5	.71	123	2.2	1.29	12	−13.9	.202	31	.28	169
4.0	.71	115	1.2	1.15	2	−12.9	.226	25	.29	168
4.5	.70	104	0.4	1.05	−8	−12.2	.246	19	.30	165
5.0	.71	93	−0.3	0.97	−19	−11.4	.270	12	.30	158

T_A = 25°C, V_{CE} = 8 V, I_C = 60 mA

0.1	.60	−132	31.0	35.53	114	−35.4	.017	51	.42	−78
0.5	.64	−176	18.1	8.00	84	−27.0	.045	55	.20	−137
1.0	.66	167	12.3	4.11	68	−22.2	.077	55	.18	−160
1.5	.67	155	9.0	2.80	54	−19.7	.104	51	.19	−172
2.0	.68	144	6.5	2.12	41	−17.5	.133	46	.21	176
2.5	.70	138	4.8	1.73	34	−16.1	.157	45	.23	174
3.0	.71	130	3.3	1.46	23	−15.0	.178	40	.26	170
3.5	.72	122	2.1	1.27	13	−13.9	.203	33	.29	168
4.0	.71	114	1.1	1.13	2	−13.1	.221	28	.30	166
4.5	.71	104	0.4	1.04	−8	−12.1	.249	21	.30	163
5.0	.71	92	−0.3	0.95	−19	−11.4	.269	14	.31	156

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

AT-01670
Up to 4 GHz General Purpose Silicon Bipolar Transistor

Features

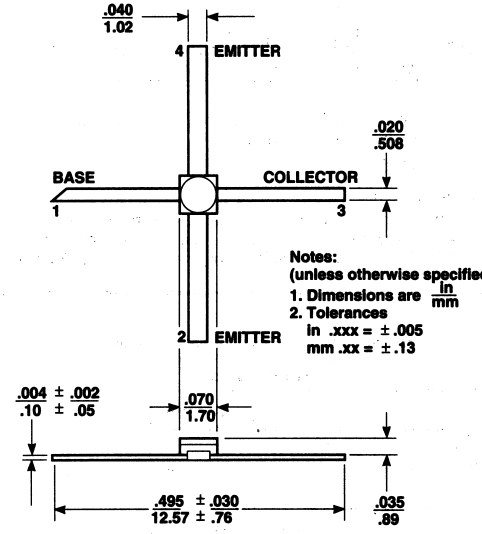
- **22.0 dBm typical $P_{1\,dB}$ at 2.0 GHz**
- **10.5 dB typical $G_{1\,dB}$ at 2.0 GHz**
- **High Gain-Bandwidth Product: 7.0 GHz typical f_T**
- **Hermetic Gold-ceramic Microstrip Package**

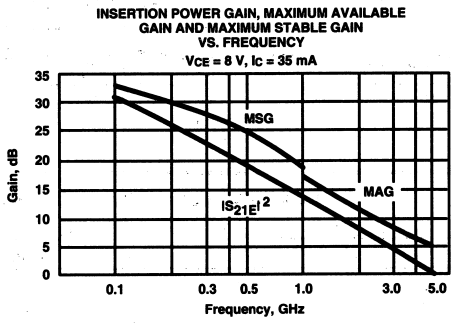
Description

The AT-01670 is a high performance NPN silicon bipolar transistor housed in a hermetic, high reliability package. This device is designed for use in medium power, wide band amplifier applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

70 mil Package





Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 35 mA	f = 1.0 GHz f = 2.0 GHz	dB	12.0	13.0 7.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 60 mA	f = 2.0 GHz	dBm		22.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 60 mA	f = 2.0 GHz	dB		10.5	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz	dB		3.0	
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz	dB		10.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 35 mA		GHz		7.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 35 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		μA			2.0
C_{CB}	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		0.8	

Note: 1. For this test, the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	150 mA
Power Dissipation[2,3]	P_T	1000 mW
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	–65°C to 200°C

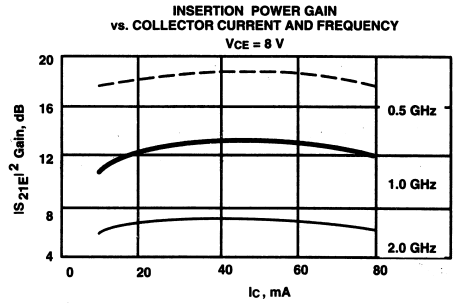
Thermal Resistance[2,4]: θ_{jc} = 120°C/W

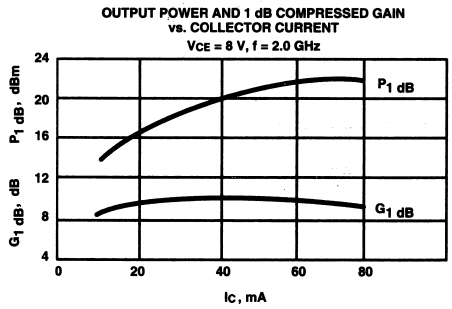
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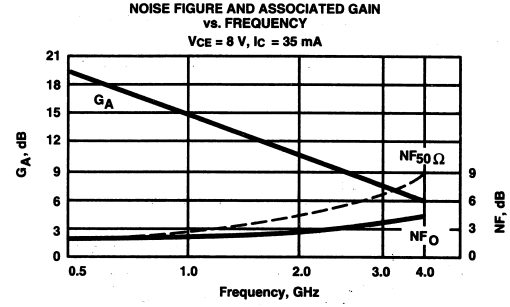
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 8.3 mW/°C for T_C > 80°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)







Typical Scattering Parameters: Common Emitter, Z_O = 50 Ω

T_A = 25°C, V_{CE} = 8 V, I_C = 35 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	.68	–129	31.1	36.01	122	–35.4	.017	47	.56	–71
0.5	.77	–173	18.7	8.63	88	–30.4	.030	42	.25	–133
1.0	.76	175	12.9	4.41	75	–26.8	.046	55	.22	–148
1.5	.76	167	9.6	3.02	64	–24.2	.062	54	.22	–153
2.0	.76	160	7.2	2.30	54	–22.0	.079	55	.22	–154
2.5	.76	157	5.5	1.88	49	–20.2	.098	58	.23	–156
3.0	.77	152	4.0	1.59	40	–19.1	.111	55	.25	–157
3.5	.77	147	2.9	1.39	31	–17.9	.128	50	.27	–159
4.0	.75	141	1.9	1.24	22	–16.8	.144	49	.29	–160
4.5	.74	135	1.1	1.13	13	–15.6	.166	44	.31	–162
5.0	.73	126	0.4	1.04	4	–14.8	.182	39	.32	–165

T_A = 25°C, V_{CE} = 8 V, I_C = 60 mA

0.1	.70	–143	31.6	38.01	116	–35.4	.017	40	.48	–81
0.5	.77	–177	18.7	8.56	87	–31.4	.027	49	.24	–141
1.0	.77	173	12.8	4.36	74	–27.2	.043	59	.22	–152
1.5	.77	166	9.5	2.98	64	–23.8	.064	58	.22	–155
2.0	.77	159	7.1	2.27	53	–21.8	.082	59	.22	–157
2.5	.76	156	5.4	1.85	48	–20.2	.097	61	.23	–158
3.0	.77	152	3.9	1.56	39	–19.2	.110	57	.25	–159
3.5	.77	146	2.7	1.37	31	–17.7	.131	54	.27	–160
4.0	.76	141	1.7	1.22	21	–16.6	.148	51	.29	–161
4.5	.75	134	0.9	1.11	13	–15.4	.169	45	.31	–162
5.0	.73	126	0.2	1.02	3	–14.6	.186	41	.31	–166

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

AT-01672
Up to 1 GHz General Purpose Silicon Bipolar Transistor

Features

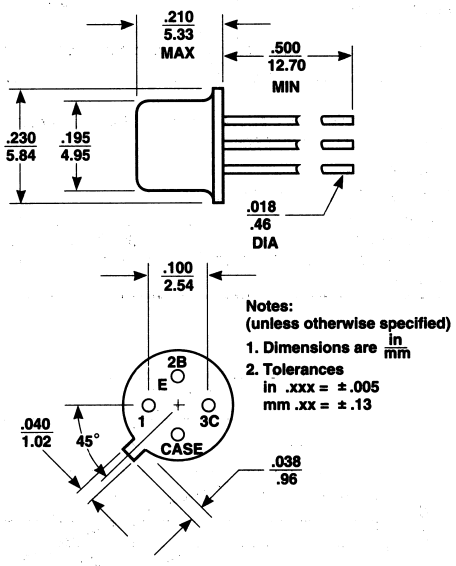
- **24.0 dBm typical $P_{1\,dB}$ at 1.0 GHz**
- **5.5 dB typical $G_{1\,dB}$ at 1.0 GHz**
- **High Gain-Bandwidth Product: 5.5 GHz typical f_T**
- **Hermetic, Metal Package**

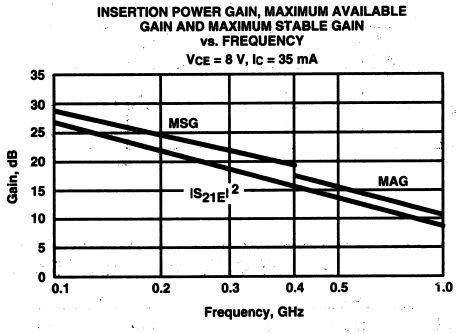
Description

The AT-01672 is a high performance NPN silicon bipolar transistor housed in a hermetic high reliability metal package. This device is designed for use in medium power amplifier applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

TO-72 Package





Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 35 mA	f = 0.5 GHz f = 1.0 GHz	dB	13.0	14.5 9.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 60 mA	f = 1.0 GHz	dBm		24.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 60 mA	f = 1.0 GHz	dB		5.5	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 35 mA	f = 0.5 GHz f = 1.0 GHz	dB		2.0 3.0	
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 35 mA	f = 0.5 GHz f = 1.0 GHz	dB		10.5 6.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 10 mA		GHz		5.5	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 35 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		μA			2.0
C_{CB}	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		1.0	

Note: 1. For this test, the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	150 mA
Power Dissipation[2,3]	P_T	1000 mW
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	–65° to 200°C

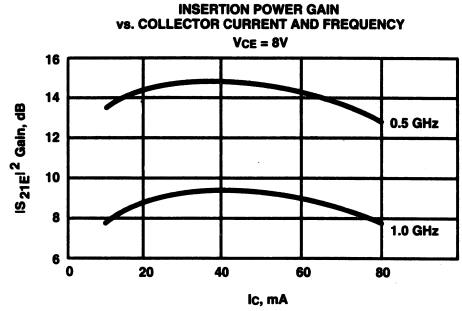
Thermal Resistance[2,4]: θ_{jc} = 190°C/W

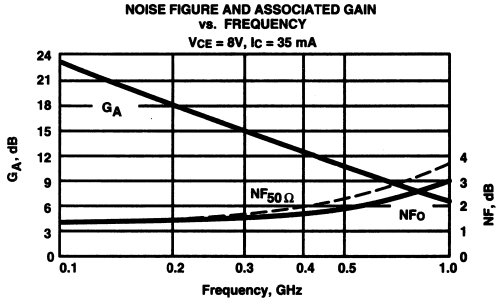
Notes:

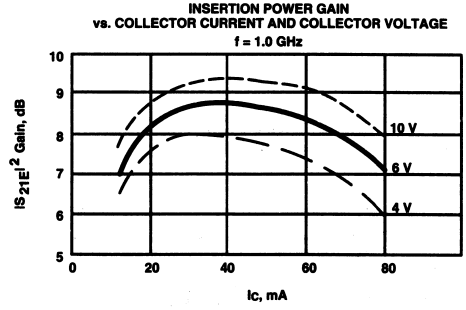
1. Operation of this device above any one of these parameters may use permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 5.3 mW/°C for T_C > 10°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)







Typical Scattering Parameters: Common Emitter, Z_O = 50 Ω

T_A = 25°C, V_{CE} = 8 V, I_C = 35 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.33	–81	26.7	21.73	114	–30.2	.031	72	.51	–36
0.2	.22	–112	21.8	12.28	98	–26.0	.050	75	.36	–36
0.3	.19	–134	18.7	8.61	92	–22.8	.072	74	.30	–37
0.4	.18	–148	16.4	6.58	83	–21.0	.090	72	.26	–34
0.5	.17	–159	14.6	5.35	79	–19.1	.111	70	.22	–33
0.6	.17	–171	13.1	4.51	77	–17.5	.133	71	.21	–38
0.7	.17	178	12.0	3.97	72	–16.2	.154	68	.19	–45
0.8	.18	171	11.1	3.61	68	–15.3	.172	66	.18	–53
0.9	.18	169	9.9	3.12	65	–14.3	.192	66	.20	–58
1.0	.19	164	9.2	2.89	61	–13.5	.212	63	.22	–60

T_A = 25°C, V_{CE} = 8 V, I_C = 60 mA

0.1	.30	–92	26.7	21.60	110	–30.4	.030	73	.47	–35
0.2	.22	–125	21.5	11.92	96	–26.2	.049	76	.33	–35
0.3	.21	–145	18.4	8.29	90	–23.0	.070	75	.28	–34
0.4	.20	–159	16.1	6.35	82	–21.0	.089	72	.26	–31
0.5	.19	–169	14.2	5.16	77	–19.3	.109	70	.23	–31
0.6	.20	–178	12.8	4.34	76	–17.7	.131	72	.21	–37
0.7	.20	173	11.6	3.81	71	–16.4	.152	68	.19	–43
0.8	.21	167	10.8	3.47	67	–15.4	.170	66	.19	–51
0.9	.21	165	9.5	2.99	64	–14.5	.189	67	.21	–58
1.0	.22	160	8.9	2.78	60	–13.6	.208	64	.23	–60

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

AT-21400
20 GHz NPN Silicon Bipolar Oscillator Transistor

Features

- **Fundamental Oscillation to > 20 GHz**
- **Low Phase Noise Compared to GaAs FETs**
- **High S21 Gain: 9.5 dB Typical at 4 GHz**
- **High MAG: 16.5 dB Typical at 4 GHz**

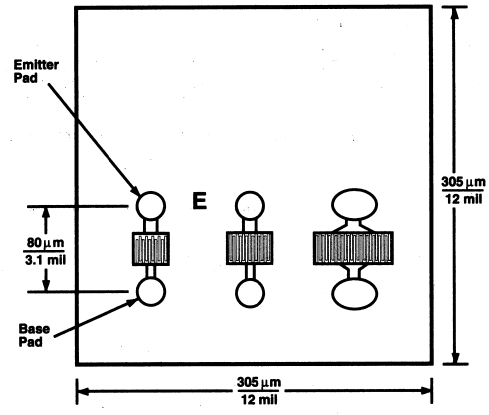
Description

The AT-21400 is a very high performance NPN silicon bipolar transistor chip designed for use in low-phase noise narrow and wideband oscillator applications at fundamental frequencies to greater than 20 GHz.

The AT-21400 oscillator transistor is fabricated using HP's 10 GHz, f_T, 40 GHz f_{MAX} TurboSAT silicon bipolar process which uses nitride self-alignment, thick planar-field oxide, subhalf-micrometer lithography, ion implantation, gold metallization and nitride scratch protection to achieve excellent performance, uniformity and reliability.

The recommended mounting procedure is gold-silicon eutectic die attach at 400 °C. Assembly can be performed with either wedge or ball bonding using 0.5 or 0.7 mil gold wire. See also "Chip Use" in the APPLICATIONS section.

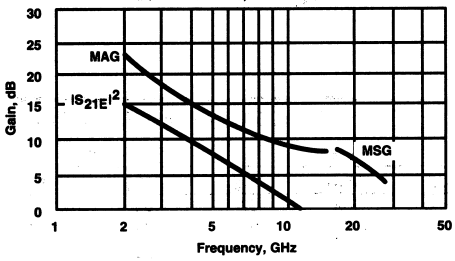
Chip Outline[1]



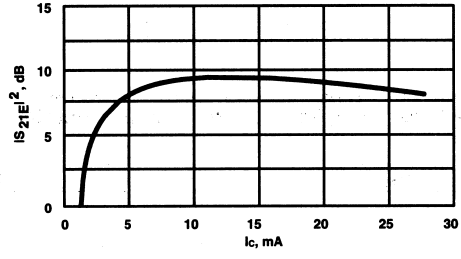
Typical Dimensions are in µm / mil

Bond Pad Diameters are 20 µm / 0.8 mil

MAXIMUM STABLE GAIN, MAXIMUM AVAILABLE GAIN and INSERTION POWER GAIN vs. FREQUENCY
V_{CE} = 8 V, I_C = 14 mA



INSERTION POWER GAIN vs. COLLECTOR CURRENT
f = 4 GHz, V_{CE} = 8 V



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions [1,2,3]		Units	Min.	Typ.	Max.
MAG	Maximum Available Gain: V_{CE} = 8 V, I_C = 14 mA	f = 4 GHz	dB		16.5	
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 14 mA	f = 4 GHz	dB		9.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 14 mA	f = 2 GHz	GHz		10	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 14 mA			30	100	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		µA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		µA			5.0
C_{CB}	Collector Base Capacitance: V_{CB} = 8 V	f = 1 MHz	pF		.08	

Notes:
1. This chip contains 3 active transistors. The performance specified applies only to the device whose base and emitter pads are indicated on the chip outline. Performance and functionality of the other 2 transistors is not guaranteed.
2. RF performance of the chip is determined by testing 10 devices per wafer assembled in a common-emitter configuration on a standard chip carrier.
3. The normal operating collector current range for this transistor is 10 to 15 mA.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	10 V
Collector Current	I_C	28 mA
Power Dissipation[2]	P_T	250 mW
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	–65°C to 200°C

Thermal Resistance; junction to substrate[3]: θ_{js} = 170°C/W

Notes:

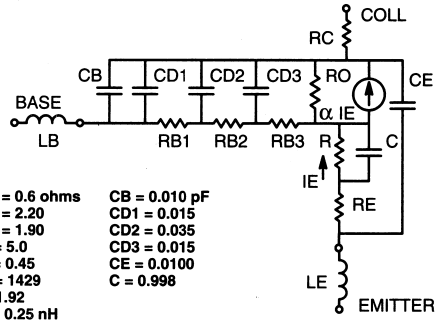
1. Permanent damage may occur if any of these limits are exceeded.
2. Derate at 5.9 m W/°C for $T_{MOUNTING\ SURFACE}$ > 158°C.
3. $T_{MOUNTING\ SURFACE}$ = 25°C.

Part Number Ordering Information

Part Number	Devices Per Tray
AT–21400–GP1	5
AT–21400–GP4	100
AT–21400–GP6	up to 300

LINEAR EQUIVALENT CIRCUIT[4]

V_{CE} = 8 V, I_C = 14 mA

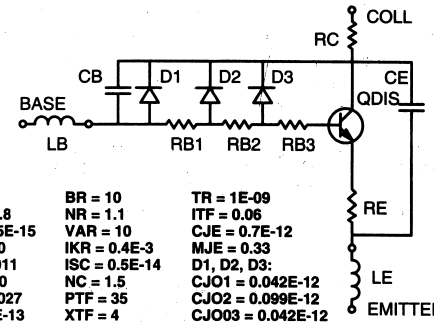


RB1 = 0.6 ohms
RB2 = 2.20
RB3 = 1.90
RC = 5.0
RE = 0.45
RO = 1429
R = 1.92
LB = 0.25 nH
LE = 0.10

CB = 0.010 pF
CD1 = 0.015
CD2 = 0.035
CD3 = 0.015
CE = 0.0100
C = 0.998

TOUCHSTONE™ CCCS: M=.99, A=0
R1=R, R2=1E8, F=22.7, T=7.4

SPICE EQUIVALENT CIRCUIT[4]



QDIS:
XTB = 1.8
IS = 0.65E-15
BF = 100
NF = 1.011
VAF = 20
IKF = 0.027
ISE = 3E-13
NE = 2.0

BR = 10
NR = 1.1
VAR = 10
IKR = 0.4E-3
ISC = 0.5E-14
NC = 1.5
PTF = 35
XTF = 4
TF = 12E-12

TR = 1E-09
ITF = 0.06
CJE = 0.7E-12
MJE = 0.33
D1, D2, D3:
CJO1 = 0.042E-12
CJO2 = 0.099E-12
CJO03 = 0.042E-12
IS = 0, VJ = 0.73

Modeled Scattering Parameters, Common Emitter [5]

T_A = 25°C, V_{CE} = 8 V, I_C = 14 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
2	.67	–168	15.8	6.19	90	–34.0	.02	52	.65	–9
3	.67	–180	12.4	4.17	81	–32.0	.025	59	.65	–10
4	.67	172	10.0	3.15	74	–30.5	.03	64	.65	–11
5	.68	165	8.1	2.53	68	–28.0	.04	68	.65	–12
6	.68	160	6.5	2.12	62	–28.0	.04	70	.65	–14
7	.69	154	5.2	1.82	56	–26.0	.05	72	.65	–16
8	.70	149	4.1	1.60	51	–24.4	.06	73	.65	–18
9	.70	144	3.1	1.43	46	–24.4	.06	74	.65	–20
10	.71	140	2.2	1.29	41	–23.1	.07	74	.65	–22
11	.72	135	1.4	1.18	36	–21.9	.08	74	.65	–24
12	.73	131	0.7	1.08	31	–21.9	.08	75	.66	–26
13	.74	127	0	1.00	27	–20.9	.09	75	.66	–28
14	.75	123	–0.6	0.93	23	–20.0	.10	75	.66	–30
15	.76	120	–1.3	0.86	18	–19.2	.11	74	.67	–32
16	.77	116	–1.9	0.80	14	–19.2	.11	74	.67	–34
18	.79	109	–3.1	0.70	7	–17.7	.13	74	.68	–39
20	.80	103	–4.2	0.62	–1	–17.1	.14	73	.69	–44
22	.82	97	–5.4	0.54	–7	–15.9	.16	72	.70	–48
24	.84	92	–6.6	0.47	–14	–14.9	.18	71	.71	–53
26	.85	87	–8.0	0.40	–20	–14.0	.20	70	.72	–58

Notes: 4. These equivalent circuits are provided only as 1st-order design aids. Their accuracy for critical designs at very high frequencies has not been validated.
5. S-Parameters are from linear equivalent circuit. Below 10 GHz, they have been fit to measurements of die on a standard carrier with 1 bond wire to the base and 4 bond wires to the emitter.

HEWLETT PACKARD

AT-41400
Up to 6 GHz Low Noise Silicon Bipolar Transistor Chip

Features

- **Low Noise Figure: 1.6 dB typical at 2.0 GHz**
  3.0 dB typical at 4.0 GHz
- **High Associated Gain: 14.5 dB typical at 2.0 GHz**
  10.5 dB typical at 4.0 GHz
- **High Gain-Bandwidth Product: 9.0 GHz typical f_T**

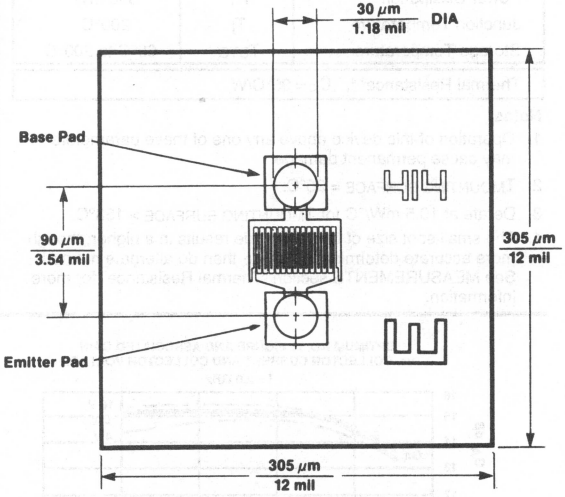
Description

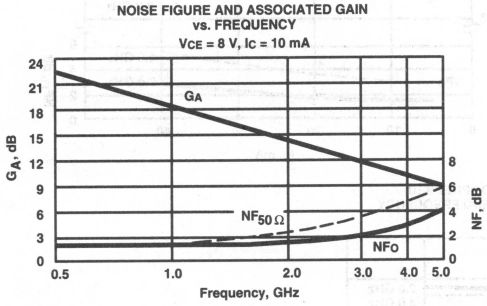
The AT-41400 is a high performance NPN silicon bipolar transistor chip designed for use low noise, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

The die are nitride-passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implanation, self-alignment techniques, and gold metallization in the fabrication of these devices.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire. See also "Chip Use" in the APPLICATIONS section.

Chip Outline





Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
0.1	1.2	.12	3	0.17
0.5	1.2	.10	15	0.17
1.0	1.3	.06	27	0.16
2.0	1.6	.24	163	0.16
4.0	3.0	.52	–153	0.18

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 10 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		1.3 1.6 3.0	
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 10 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		18.5 14.5 10.5	
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 25 mA	f = 2.0 GHz f = 4.0 GHz	dB		12.0 6.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 25 mA	f = 2.0 GHz f = 4.0 GHz	dBm		19.0 18.5	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 25 mA	f = 2.0 GHz f = 4.0 GHz	dB		15.0 10.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 25 mA		GHz		9.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 10 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		μA			1.0
C_{CB}	Collector Base Capacitance[2]: V_{CB} = 8 V, f = 1 MHz		pF		0.17	

Notes: 1. RF performance is determined by packaging and testing 10 devices per wafer.
2. For this test, the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	60 mA
Power Dissipation[2,3]	P_T	500 mW
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	−65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 95°C/W

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. $T_{MOUNTING\ SURFACE}$ = 25°C.
3. Derate at 10.5 mW/°C for $T_{MOUNTING\ SURFACE}$ > 153°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

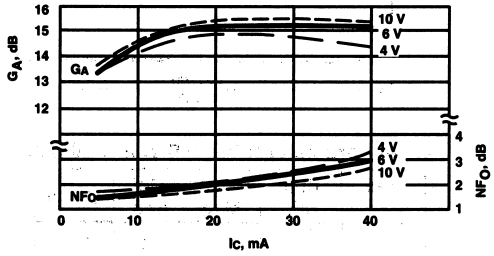
Part Number Ordering Information

Part Number	Devices Per Tray
AT-41400-GP2	10
AT-41400-GP4	100
AT-41400-GP6	up to 300

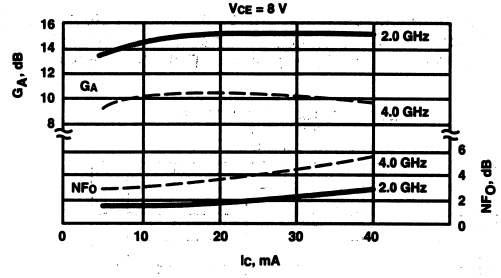
Typical Performance, T_A = 25°C

(unless otherwise noted)

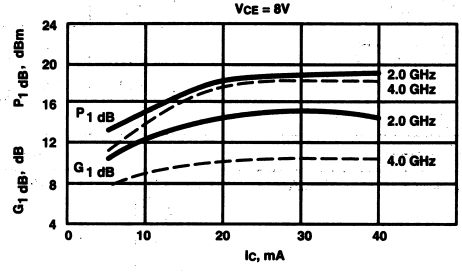
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN vs. COLLECTOR CURRENT AND COLLECTOR VOLTAGE
f = 2.0 GHz



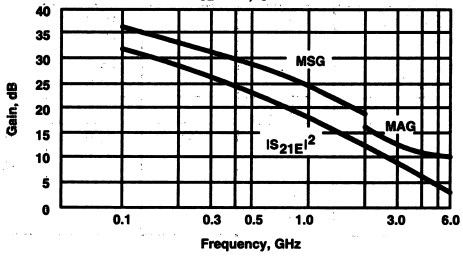
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN vs. COLLECTOR CURRENT AND FREQUENCY
VCE = 8 V



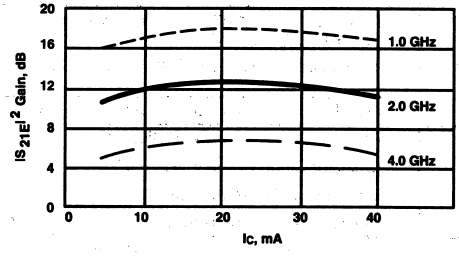
OUTPUT POWER AND 1 dB COMPRESSED GAIN vs. COLLECTOR CURRENT AND FREQUENCY
VCE = 8V



INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
VCE = 8 V, IC = 25 mA



INSERTION POWER GAIN vs. COLLECTOR CURRENT AND FREQUENCY
VCE = 8 V



Typical Scattering Parameters: Common Emitter, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 10$ mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.73	–39	28.3	25.84	159	–39.2	.011	75	.94	–12
0.5	.60	–121	22.2	12.91	113	–30.2	.031	48	.61	–28
1.0	.57	–156	17.2	7.27	94	–28.0	.040	51	.50	–25
1.5	.56	–172	13.7	4.84	84	–26.4	.048	59	.47	–25
2.0	.57	176	11.4	3.71	77	–24.9	.057	66	.46	–24
2.5	.57	170	9.5	2.97	71	–23.6	.066	69	.46	–26
3.0	.60	164	8.0	2.52	64	–22.3	.077	72	.45	–28
3.5	.60	157	6.8	2.18	61	–20.9	.090	77	.47	–29
4.0	.61	152	5.5	1.89	55	–20.1	.099	79	.47	–30
4.5	.63	147	4.7	1.72	51	–18.7	.116	81	.47	–36
5.0	.63	144	3.7	1.53	46	–17.8	.129	80	.48	–40
5.5	.65	139	3.1	1.42	42	–17.0	.141	82	.49	–44
6.0	.66	136	2.1	1.28	38	–16.1	.156	83	.50	–47

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 25$ mA

0.1	.56	–60	31.8	39.07	152	–40.9	.009	69	.87	–18
0.5	.54	–145	23.5	15.00	104	–32.8	.023	56	.49	–28
1.0	.54	–170	18.1	8.03	90	–29.6	.033	65	.42	–23
1.5	.55	179	14.5	5.30	82	–26.9	.045	72	.41	–22
2.0	.56	170	12.1	4.04	76	–24.7	.058	75	.41	–23
2.5	.56	165	10.2	3.24	72	–23.1	.070	78	.40	–23
3.0	.58	159	8.8	2.75	65	–21.6	.083	79	.40	–25
3.5	.59	154	7.5	2.37	62	–20.4	.096	82	.41	–26
4.0	.60	149	6.3	2.06	57	–19.3	.108	83	.42	–28
4.5	.61	145	5.4	1.87	53	–18.1	.124	84	.42	–33
5.0	.62	142	4.5	1.67	49	–17.3	.136	83	.43	–36
5.5	.64	137	3.8	1.54	44	–16.5	.150	85	.42	–40
6.0	.65	134	2.9	1.40	41	–15.7	.165	84	.44	–45

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

AT-41410
Up to 6 GHz Low Noise Silicon Bipolar Transistor

Features

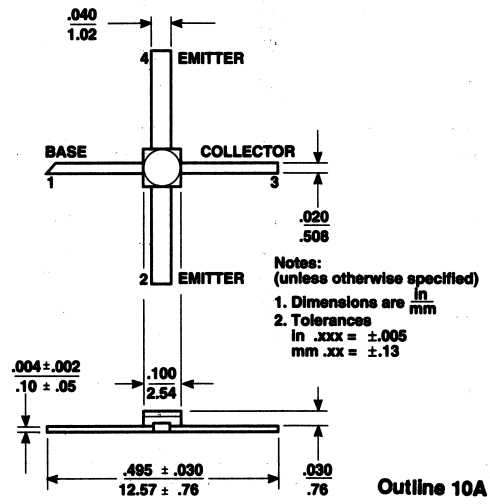
- **Low Noise Figure: 1.6 dB typical at 2.0 GHz**
  3.0 dB typical at 4.0 GHz
- **High Associated Gain: 14.0 dB typical at 2.0 GHz**
  10.0 dB typical at 4.0 GHz
- **High Gain-Bandwidth Product: 8.0 GHz typical f_T**
- **Hermetic, Gold-ceramic Microstrip Package**

Description

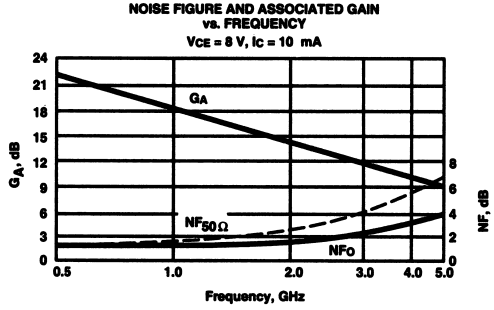
The AT-41410 is a high performance NPN silicon bipolar transistor housed in a hermetic, high reliability package. This device is designed for use in low noise, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

100 mil Package



Outline 10A



Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
0.1	1.2	.12	4	0.17
0.5	1.2	.10	23	0.17
1.0	1.3	.06	49	0.16
2.0	1.6	.26	172	0.16
4.0	3.0	.46	−133	0.26

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 10 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		1.3 1.6 3.0	1.9
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 10 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB	13.0	18.5 14.0 10.0	
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 25 mA	f = 2.0 GHz f = 4.0 GHz	dB		12.0 6.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression:	f = 2.0 GHz	dBm		19.0	
	V_{CE} = 8 V, I_C = 25 mA	f = 4.0 GHz			18.5	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 25 mA	f = 2.0 GHz f = 4.0 GHz	dB		14.0 9.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 25 mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 10 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		μA			1.0
C_{CB}	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		0.2	

Note: 1. For this test, the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	60 mA
Power Dissipation[2,3]	P_T	500 mW
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	–65°to 200°C

Thermal Resistance[2,4]: θ_{jc} = 170°C/W

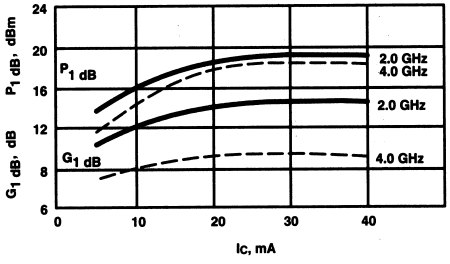
Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 5.9 mW/°C for T_C > 115°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

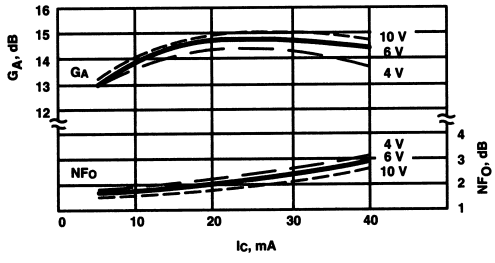
Typical Performance, T_A = 25°C

(unless otherwise noted)

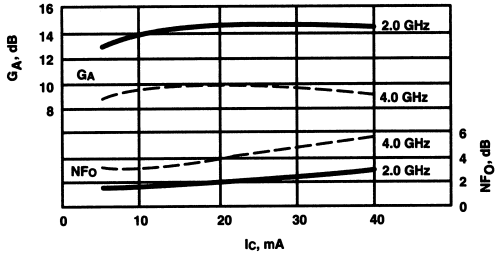
OUTPUT POWER AND 1 dB COMPRESSED GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



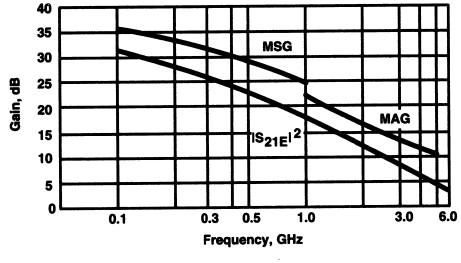
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN
vs. COLLECTOR CURRENT AND COLLECTOR VOLTAGE
f = 2.0 GHz



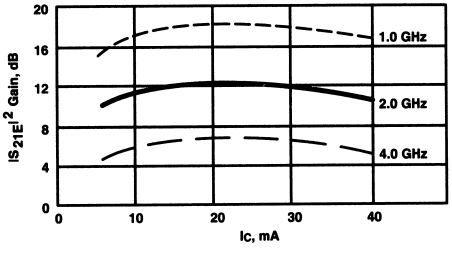
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



INSERTION POWER GAIN, MAXIMUM AVAILABLE
GAIN AND MAXIMUM STABLE GAIN
vs. FREQUENCY
V_{CE} = 8 V, I_C = 25 mA



INSERTION POWER GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



Typical Scattering Parameters: Common Emitter, $Z_O = 50\ \Omega$ **$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 10$ mA**

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.61	–40	27.7	24.38	159	–40.0	.010	75	.94	–13
0.5	.60	–127	22.2	12.83	110	–30.4	.030	40	.62	–33
1.0	.60	–163	17.1	7.12	86	–28.2	.039	35	.50	–38
1.5	.60	179	13.8	4.89	71	–27.5	.042	45	.46	–42
2.0	.61	165	11.4	3.72	59	–26.0	.050	42	.45	–48
2.5	.61	157	9.7	3.04	52	–24.7	.058	46	.44	–52
3.0	.62	149	8.2	2.56	42	–23.9	.064	50	.44	–58
3.5	.63	140	7.0	2.23	31	–22.3	.077	48	.46	–68
4.0	.62	130	5.9	1.96	20	–21.3	.086	44	.48	–78
4.5	.61	120	4.9	1.76	10	–20.4	.095	41	.50	–85
5.0	.61	106	4.0	1.59	–1	–18.9	.113	38	.52	–91
5.5	.62	94	3.2	1.45	–11	–18.3	.121	33	.52	–97
6.0	.66	82	2.4	1.31	–22	–17.5	.133	30	.51	–105
										$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 25$ mA
0.1	.45	–69	31.4	37.17	150	–39.2	.011	64	.87	–18
0.5	.58	–153	23.3	14.63	101	–33.6	.021	43	.49	–33
1.0	.59	–178	17.7	7.68	81	–30.4	.030	53	.43	–35
1.5	.60	169	14.3	5.21	68	–28.2	.039	58	.41	–40
2.0	.60	157	11.9	3.94	56	–25.8	.051	55	.41	–45
2.5	.61	151	10.1	3.20	50	–24.4	.060	55	.40	–49
3.0	.62	144	8.6	2.70	40	–23.1	.070	58	.40	–56
3.5	.63	135	7.4	2.35	30	–21.9	.080	54	.42	–66
4.0	.62	126	6.3	2.07	19	–20.5	.094	53	.44	–76
4.5	.61	116	5.3	1.85	9	–19.3	.108	45	.46	–84
5.0	.61	103	4.5	1.67	–2	–18.5	.119	41	.49	–90
5.5	.63	91	3.6	1.52	–12	–17.6	.131	34	.49	–96
6.0	.67	80	2.8	1.37	–22	–16.8	.144	29	.47	–104

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

AT-41411
Surface Mount Low Noise Silicon Bipolar Transistor

Features

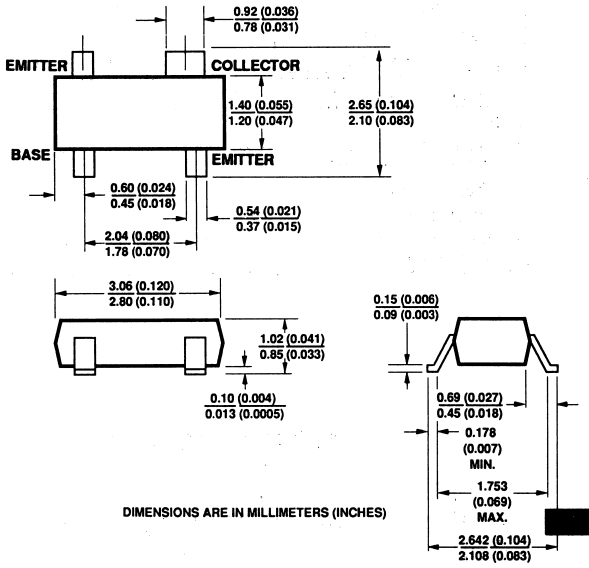
- **Low Noise Figure: 1.4 dB typical at 1.0 GHz**
  1.8 dB typical at 2.0 GHz
- **High Associated Gain: 18.0 dB typical at 1.0 GHz**
  13.0 dB typical at 2.0 GHz
- **High Gain-Bandwidth Product: 7.0 GHz typical f_T**
- **Low Cost Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Description

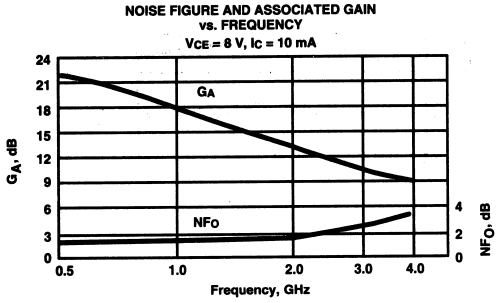
The AT-41411 is a low cost NPN silicon bipolar transistor housed in the surface mount plastic SOT-143 package. This device is designed for use in low noise, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

SOT-143 Plastic



DIMENSIONS ARE IN MILLIMETERS (INCHES)



Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq. GHz	NFO dB	Gamma Opt Mag	Gamma Opt Ang	RN/50
0.1	1.3	.12	4	0.17
0.5	1.3	.10	23	0.17
1.0	1.4	.07	57	0.16
2.0	1.8	.09	–158	0.16
4.0	3.5	.31	–87	0.38

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NFO	Optimum Noise Figure: VCE = 8 V, IC = 10 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		1.4 1.8 3.5	
GA	Gain @ NFO: VCE = 8 V, IC = 10 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		18.0 13.0 9.0	
$\|S_{21E}\|^2$	Insertion Power Gain: VCE = 8 V, IC = 20 mA	f = 1.0 GHz f = 2.0 GHz	dB	14.5	16.5 11.0	
P1 dB	Power Output @ 1 dB Gain Compression: VCE = 8 V, IC = 20 mA	f = 2.0 GHz	dBm		17.0	
G1 dB	1 dB Compressed Gain: VCE = 8 V, IC = 20 mA	f = 2.0 GHz	dB		13.0	
f_T	Gain Bandwidth Product: VCE = 8 V, IC = 20 mA		GHz		7.0	
hFE	Forward Current Transfer Ratio: VCE = 8 V, IC = 10 mA			30	150	300
ICBO	Collector Cutoff Current: VCB = 8 V		mA			0.2
IEBO	Emitter Cutoff Current: VEB = 1 V		mA			1.0

Note: 1. Refer to PACKAGING Section of Data Book, "Tape-and-Reel Packaging for Semiconductor Devices."

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	50 mA
Power Dissipation[2,3]	P_T	225 mW
Junction Temperature	T_j	150°C
Storage Temperature	T_{STG}	–65°C to 150°C

Thermal Resistance[2,4]: θ_{jc} = 550° C/W

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 1.8 mW/°C for T_C >26°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information

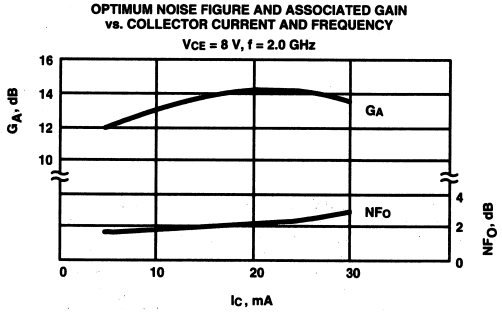
Part Number Ordering Information

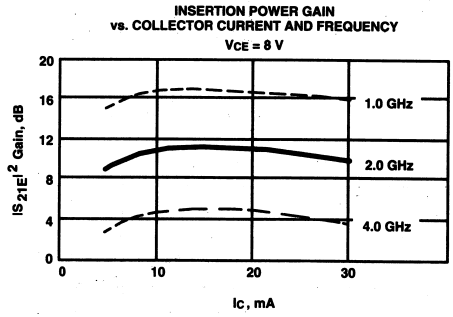
Part Number	Devices Per Reel	Reel Size
AT-41411-TR1	3000	7"
AT-41411-TR2	10000	13"

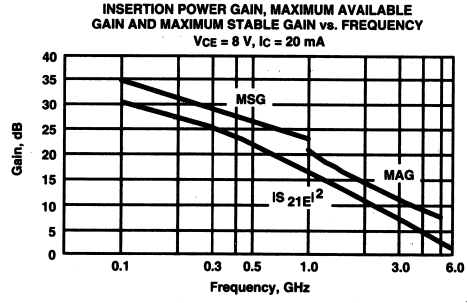
For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

Typical Performance, T_A = 25°C

(unless otherwise noted)







Typical Scattering Parameters: Common Emitter, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 10$ mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.85	–30	27.3	23.20	158	–37.7	.013	64	.93	–11
0.5	.58	–112	21.7	12.18	109	–29.1	.035	44	.62	–30
1.0	.49	–156	16.5	6.70	85	–27.2	.044	43	.50	–33
1.5	.49	178	13.2	4.58	71	–25.0	.056	47	.46	–36
2.0	.50	160	10.8	3.45	59	–23.4	.068	47	.45	–41
2.5	.53	153	9.0	2.82	53	–22.5	.075	56	.43	–43
3.0	.55	142	7.5	2.37	43	–21.0	.089	54	.43	–53
3.5	.56	133	6.1	2.02	33	–19.8	.102	52	.44	–63
4.0	.56	121	4.9	1.76	23	–18.8	.115	49	.46	–73

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 20$ mA

0.1	.65	–46	30.4	33.07	150	–40.0	.010	59	.89	–15
0.5	.46	–137	22.4	13.21	100	–32.0	.025	56	.57	–26
1.0	.43	–175	16.7	6.85	80	–28.4	.038	58	.52	–29
1.5	.44	163	13.3	4.63	67	–26.4	.048	61	.51	–32
2.0	.47	148	10.8	3.47	56	–24.2	.062	61	.50	–37
2.5	.50	140	9.0	2.82	50	–22.9	.071	60	.47	–39
3.0	.53	132	7.5	2.36	40	–20.7	.092	61	.46	–48
3.5	.55	122	6.1	2.02	30	–19.6	.105	57	.45	–60
4.0	.56	112	4.8	1.74	19	–18.3	.122	53	.45	–73

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

AT-41435
Up to 6 GHz Low Noise Silicon Bipolar Transistor

Features

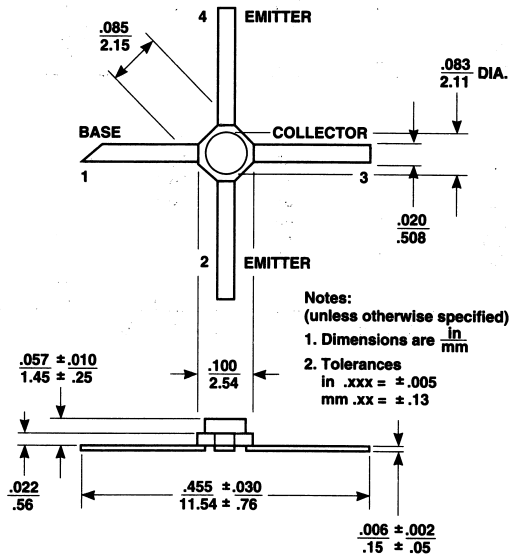
- **Low Noise Figure: 1.7 dB typical at 2.0 GHz**
  3.0 dB typical at 4.0 GHz
- **High Associated Gain: 14.0 dB typical at 2.0 GHz**
  10.0 dB typical at 4.0 GHz
- **High Gain-Bandwidth Product: 8.0 GHz typical f_T**
- **Cost Effective Ceramic Microstrip Package**

Description

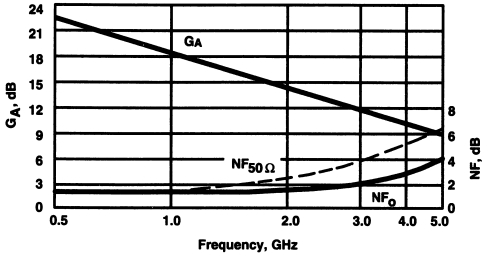
The AT-41435 is a high performance NPN silicon bipolar transistor housed in a cost effective, microstrip package. This device is designed for use in low noise, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

35 micro-X Package



NOISE FIGURE AND ASSOCIATED GAIN vs. FREQUENCY
V_{CE} = 8 V, I_C = 10 mA



Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
0.1	1.2	.12	3	0.17
0.5	1.2	.10	14	0.17
1.0	1.3	.05	28	0.17
2.0	1.7	.30	−154	0.16
4.0	3.0	.54	−118	0.35

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 10 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		1.3 1.7 3.0	2.0
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 10 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB	13.0	18.5 14.0 10.0	
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 25 mA	f = 2.0 GHz f = 4.0 GHz	dB		11.5 6.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 25 mA	f = 2.0 GHz f = 4.0 GHz	dBm		19.0 18.5	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 25 mA	f = 2.0 GHz f = 4.0 GHz	dB		14.0 9.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 25 mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 10 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		μA			1.0
C_{CB}	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		0.2	

Note: 1. For this test the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	60 mA
Power Dissipation[2,3]	P_T	500 mW
Junction Temperature	T_j	200°C
Storage Temperature[4]	T_{STG}	–65°C to 200°C

Thermal Resistance[2,5]: $\theta_{jc} = 200°/W$

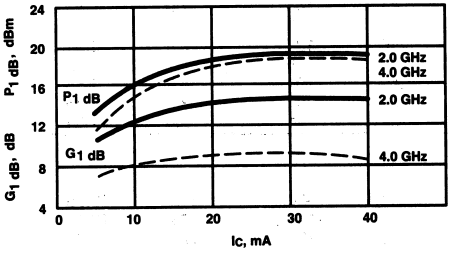
Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. $T_{CASE} = 25°C$.
3. Derate at 5 mW/°C for $T_C > 100°C$.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safely stored up to 200°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

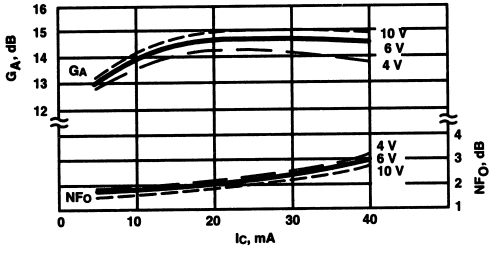
Typical Performance, $T_A = 25°C$

(unless otherwise noted)

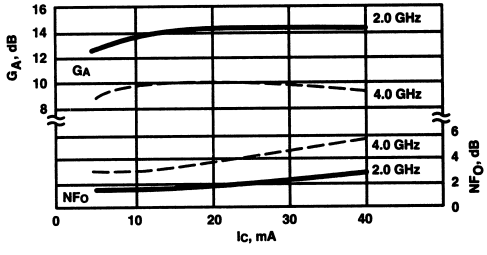
OUTPUT POWER AND 1 dB COMPRESSED GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
$V_{CE} = 8$ V



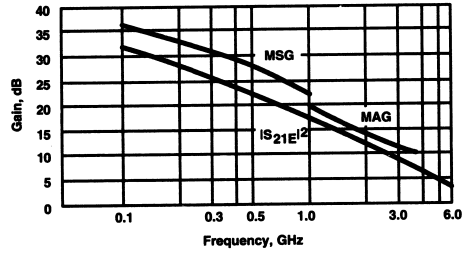
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN
vs. COLLECTOR CURRENT AND COLLECTOR VOLTAGE
f = 2.0 GHz



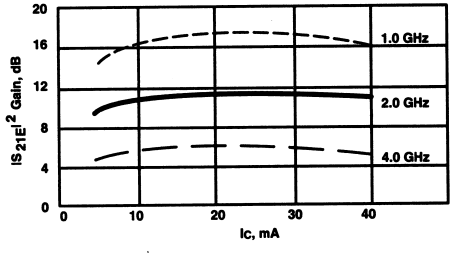
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
$V_{CE} = 8$ V



INSERTION POWER GAIN, MAXIMUM AVAILABLE
GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
$V_{CE} = 8$ V, $I_C = 25$ mA



INSERTION POWER GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
$V_{CE} = 8$ V



Typical Scattering Parameters: Common Emitter, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 10$ mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.80	–32	28.0	24.99	157	–39.2	.011	82	.93	–12
0.5	.50	–110	21.8	12.30	108	–29.6	.033	52	.61	–28
1.0	.40	–152	16.6	6.73	85	–26.2	.049	56	.51	–30
1.5	.38	–176	13.3	4.63	71	–24.0	.063	59	.48	–32
2.0	.39	166	11.0	3.54	60	–21.9	.080	58	.46	–37
2.5	.41	156	9.3	2.91	53	–20.4	.095	61	.44	–40
3.0	.44	145	7.9	2.47	43	–18.8	.115	61	.43	–48
3.5	.46	137	6.7	2.15	33	–17.5	.133	58	.43	–58
4.0	.46	127	5.6	1.91	23	–16.0	.153	53	.45	–68
4.5	.47	116	4.7	1.72	13	–15.0	.178	50	.46	–75
5.0	.49	104	4.0	1.58	3	–13.9	.201	47	.48	–82
5.5	.52	91	3.3	1.45	–7	–13.0	.224	40	.47	–89
6.0	.59	81	2.5	1.34	–17	–12.1	.247	36	.43	–101

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 25$ mA

0.1	.63	–50	31.8	39.08	146	–40.0	.010	83	.84	–18
0.5	.39	–137	22.9	13.97	99	–31.4	.027	60	.50	–26
1.0	.36	–171	17.2	7.28	80	–27.1	.044	67	.45	–26
1.5	.36	171	13.9	4.94	68	–23.5	.067	66	.43	–30
2.0	.38	156	11.5	3.76	58	–21.6	.083	63	.41	–34
2.5	.40	149	9.8	3.08	52	–19.6	.105	63	.39	–38
3.0	.43	140	8.3	2.61	43	–18.3	.122	64	.38	–47
3.5	.45	132	7.2	2.28	33	–16.8	.144	59	.39	–57
4.0	.46	122	6.1	2.02	23	–15.6	.165	55	.40	–67
4.5	.46	112	5.2	1.82	14	–14.6	.185	50	.42	–75
5.0	.47	101	4.4	1.66	4	–13.7	.207	45	.43	–81
5.5	.51	89	3.7	1.54	–5	–12.6	.233	39	.42	–89
6.0	.58	79	3.0	1.41	–15	–11.8	.257	33	.37	–101

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

AT-41470
Up to 6 GHz Low Noise Silicon Bipolar Transistor

Features

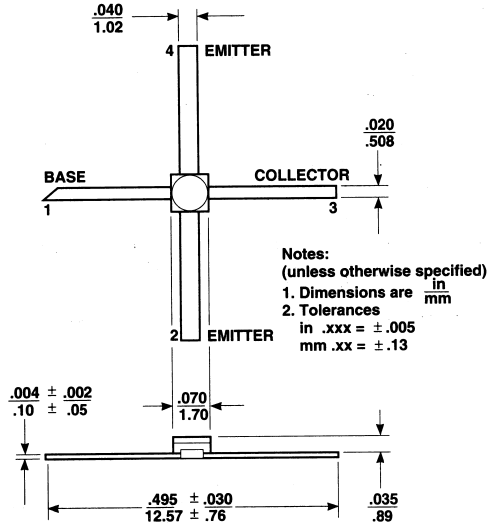
- **Low Noise Figure: 1.6 dB typical at 2.0 GHz**
  3.0 dB typical at 4.0 GHz
- **High Associated Gain: 14.5 dB typical at 2.0 GHz**
  10.5 dB typical at 4.0 GHz
- **High Gain-Bandwidth Product: 8.0 GHz typical f_T**
- **Hermetic, Gold-ceramic Microstrip Package**

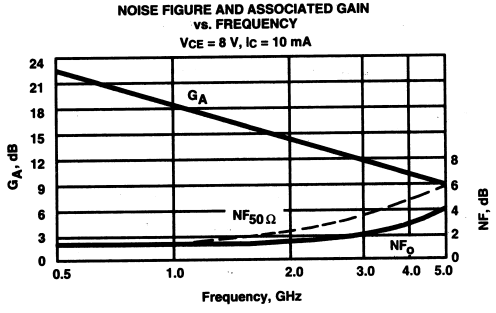
Description

The AT-41470 is a high performance NPN silicon bipolar transistor housed in a hermetic, high reliability package. This device is designed for use in low noise, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

70 mil Package





Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
0.1	1.2	.12	5	0.17
0.5	1.2	.11	17	0.17
1.0	1.3	.06	35	0.17
2.0	1.6	.21	160	0.16
4.0	3.0	.45	–150	0.20

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 10 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		1.3 1.6 3.0	1.9
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 10 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB	13.0	18.5 14.5 10.5	
$\|S21E\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 25 mA	f = 2.0 GHz f = 4.0 GHz	dB		12.0 6.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 25 mA	f = 2.0 GHz f = 4.0 GHz	dBm		19.0 18.5	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 25 mA	f = 2.0 GHz f = 4.0 GHz	dB		15.0 10.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 25 mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 10 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		µA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		µA			1.0
C_{CB}	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		0.2	

Note: 1. For this test, the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	60 mA
Power Dissipation[2,3]	P_T	500 mW
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 175°C/W

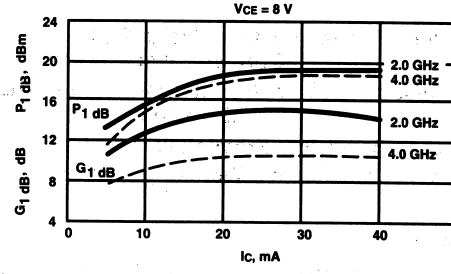
Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 5.7 mW/°C for T_C > 113°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

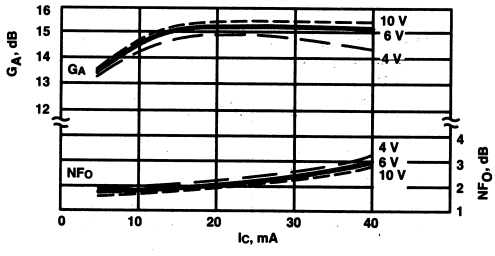
Typical Performance, T_A = 25°C

(unless otherwise noted)

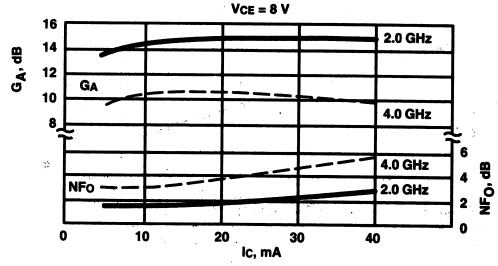
OUTPUT POWER AND 1 dB COMPRESSED GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



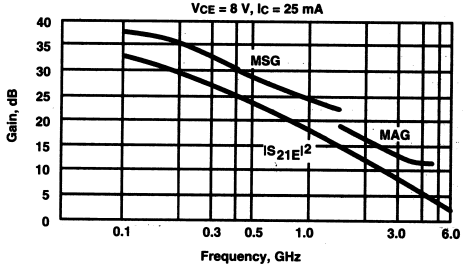
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN
vs. COLLECTOR CURRENT AND COLLECTOR VOLTAGE
f = 2.0 GHz



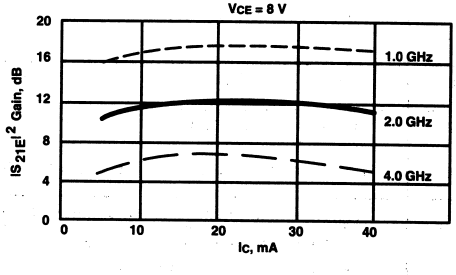
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



INSERTION POWER GAIN, MAXIMUM AVAILABLE
GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{CE} = 8 V, I_C = 25 mA



INSERTION POWER GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



Typical Scattering Parameters: Common Emitter, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 10$ mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.79	–37	28.4	26.27	157	–39.2	.011	57	.94	–13
0.5	.65	–120	22.3	13.05	110	–30.8	.029	40	.62	–30
1.0	.61	–155	17.1	7.17	88	–28.9	.036	41	.52	–32
1.5	.60	–172	13.9	4.93	76	–27.5	.042	46	.50	–36
2.0	.60	176	11.5	3.75	65	–26.4	.048	46	.50	–40
2.5	.61	169	9.7	3.06	59	–26.0	.050	58	.48	–41
3.0	.62	161	8.3	2.59	51	–24.7	.058	61	.49	–48
3.5	.61	154	7.0	2.24	42	–23.2	.069	63	.51	–56
4.0	.60	146	5.9	1.97	32	–21.4	.085	62	.52	–63
4.5	.60	137	4.9	1.77	24	–20.1	.099	59	.55	–69
5.0	.60	127	4.1	1.61	15	–19.5	.106	59	.57	–75
5.5	.61	115	3.4	1.47	6	–18.3	.121	56	.58	–80
6.0	.64	104	2.6	1.34	–4	–17.4	.135	53	.57	–87

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 25$ mA

0.1	.64	–62	32.5	42.11	147	–40.9	.009	75	.85	–19
0.5	.61	–146	23.7	15.31	100	–34.4	.019	47	.50	–30
1.0	.61	–170	18.1	8.00	83	–30.2	.031	53	.44	–31
1.5	.60	177	14.7	5.42	72	–29.1	.035	62	.44	–34
2.0	.61	167	12.3	4.10	62	–27.1	.044	60	.44	–39
2.5	.61	163	10.4	3.32	58	–25.7	.052	67	.43	–39
3.0	.62	156	9.0	2.81	50	–23.6	.066	67	.44	–46
3.5	.62	150	7.7	2.44	41	–22.6	.074	67	.46	–55
4.0	.62	142	6.6	2.13	32	–21.7	.082	63	.48	–62
4.5	.61	134	5.6	1.91	24	–20.1	.099	62	.50	–68
5.0	.60	123	4.8	1.73	15	–18.9	.113	59	.52	–73
5.5	.61	112	4.0	1.59	6	–18.1	.124	54	.54	–78
6.0	.64	102	3.2	1.45	–3	–17.3	.136	50	.53	–85

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

AT-41472
Up to 1 GHz Low Noise Silicon Bipolar Transistor

Features

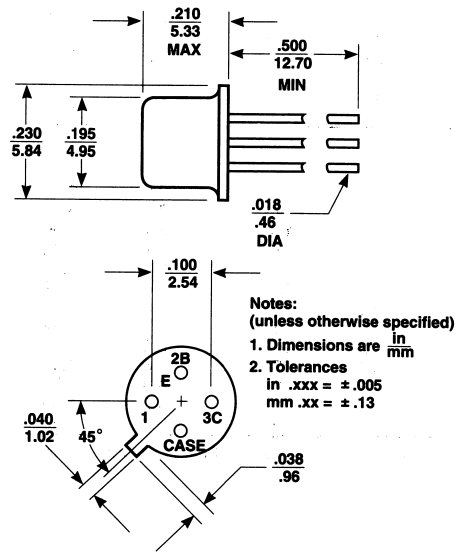
- **Low Noise Figure: 1.3 dB typical at 0.5 GHz**
  2.0 dB typical at 1.0 GHz
- **High Associated Gain: 14.0 dB typical at 0.5 GHz**
  10.0 dB typical at 1.0 GHz
- **High Gain-Bandwidth Product: 6.5 GHz typical f_T**
- **Hermetic, Metal Package**

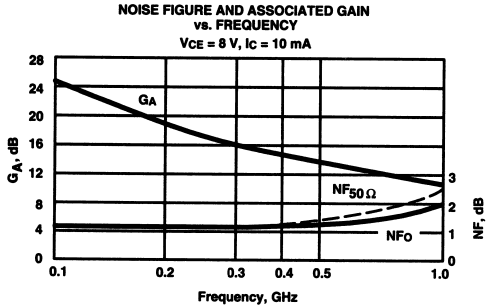
Description

The AT-41472 is a high performance NPN silicon bipolar transistor housed in a hermetic, high reliability metal package. This device is designed for use in low noise, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

TO-72 Package





Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 10 mA	f = 0.5 GHz f = 1.0 GHz	dB		1.3 2.0	1.6
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 10 mA	f = 0.5 GHz f = 1.0 GHz	dB		14.0 10.0	
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 25 mA	f = 0.5 GHz f = 1.0 GHz	dB		16.5 11.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 25 mA	f = 1.0 GHz	dBm		20.5	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 25 mA	f = 1.0 GHz	dB		7.0	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 25 mA		GHz		6.5	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 10 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		μA			1.0
C_{CB}	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		0.35	

Note: 1. For this test, the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	60 mA
Power Dissipation[2,3]	P_T	500 mW
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	–65°C to 200°C

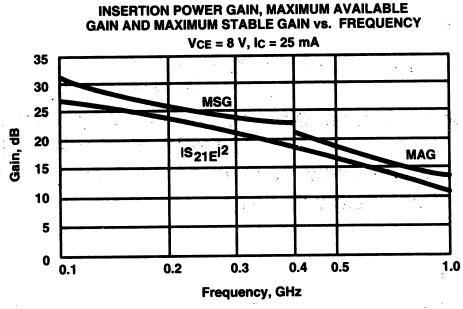
Thermal Resistance[2,4]: θ_{jc} = 260°C/W

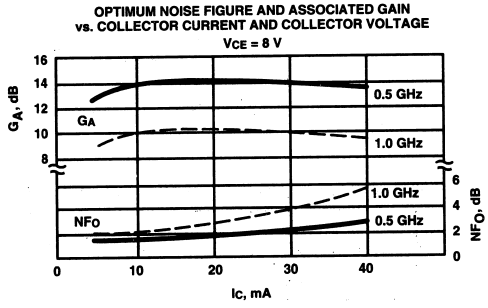
Notes:

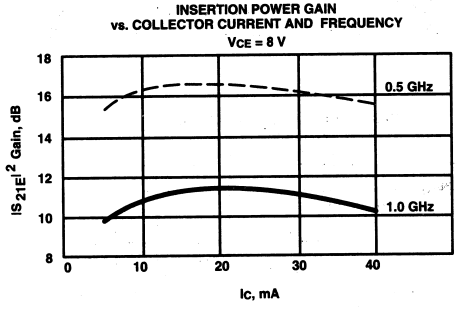
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 3.8 mW/°C for T_C > 70°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)







Typical Scattering Parameters: Common Emitter, Z_O = 50 Ω

T_A = 25°C, V_{CE} = 8 V, I_C = 10 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	.67	–24	25.1	18.00	144	–35.6	.017	71	.89	–12
0.2	.51	–37	22.3	12.98	122	–30.5	.030	71	.78	–17
0.3	.41	–42	19.9	9.84	110	–28.5	.038	72	.71	–18
0.4	.34	–45	17.9	7.87	101	–26.4	.048	71	.67	–20
0.5	.29	–48	16.4	6.60	94	–24.5	.060	71	.65	–21
0.6	.25	–49	15.0	5.64	87	–22.9	.072	71	.62	–24
0.7	.22	–47	13.8	4.92	82	–21.7	.082	69	.61	–28
0.8	.21	–45	12.7	4.32	76	–21.1	.088	67	.61	–31
0.9	.20	–45	11.6	3.81	70	–20.1	.099	64	.61	–35
1.0	.19	–45	10.8	3.46	67	–19.8	.103	64	.62	–38

T_A = 25°C, V_{CE} = 8 V, I_C = 25 mA

0.1	.58	–30	26.9	22.02	131	–35.4	.017	78	.78	–15
0.2	.40	–38	23.4	14.70	111	–30.8	.029	80	.68	–17
0.3	.32	–41	20.7	10.79	101	–27.5	.042	79	.64	–18
0.4	.27	–37	18.4	8.26	92	–25.7	.052	76	.61	–17
0.5	.24	–37	16.5	6.71	86	–23.9	.064	73	.57	–18
0.6	.22	–38	15.3	5.82	85	–22.0	.079	74	.56	–22
0.7	.20	–36	14.2	5.15	79	–20.8	.091	72	.54	–26
0.8	.19	–35	13.2	4.56	76	–19.8	.102	71	.53	–30
0.9	.19	–38	12.1	4.01	74	–18.8	.115	72	.56	–33
1.0	.18	–37	11.4	3.71	69	–18.2	.123	69	.56	–34

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

AT-41485
Up to 6 GHz Low Noise Silicon Bipolar Transistor

Features

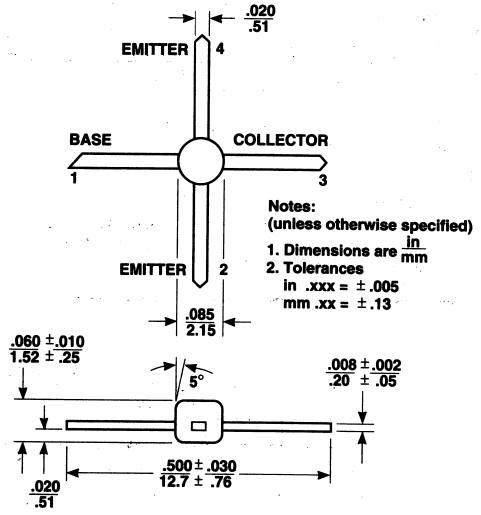
- **Low Noise Figure: 1.4 dB typical at 1.0 GHz**
  1.7 dB typical at 2.0 GHz
- **High Associated Gain: 18.5 dB typical at 1.0 GHz**
  13.5 dB typical at 2.0 GHz
- **High Gain-Bandwidth Product: 8.0 GHz typical f_T**
- **Low Cost Plastic Package**

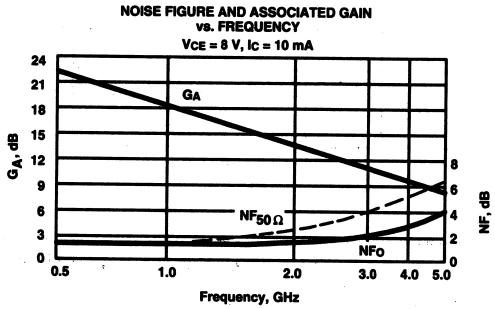
Description

The AT-41485 is a high performance NPN silicon bipolar transistor housed in a low cost plastic package. This device is designed for use in low noise, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

85 Plastic Package





Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq. GHz	NFO dB	Gamma Opt Mag	Gamma Opt Ang	RN/50
0.1	1.3	.12	5	0.17
0.5	1.3	.10	25	0.17
1.0	1.4	.06	50	0.16
2.0	1.7	.25	172	0.16
4.0	3.0	.48	–131	0.24

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NFO	Optimum Noise Figure: VCE = 8 V, IC = 10 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		1.4 1.7 3.0	1.8
GA	Gain @ NFO: VCE = 8 V, IC = 10 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB	17.5	18.5 13.5 9.5	
$\|S21E\|^2$	Insertion Power Gain: VCE = 8 V, IC = 25 mA	f = 1.0 GHz f = 2.0 GHz	dB		17.5 11.5	
P1 dB	Power Output @ 1 dB Gain Compression: VCE = 8 V, IC = 25 mA	f = 2.0 GHz	dBm		18.5	
G1 dB	1 dB Compressed Gain: VCE = 8 V, IC = 25 mA	f = 2.0 GHz	dB		14.0	
fT	Gain Bandwidth Product: VCE = 8 V, IC = 25 mA		GHz		8.0	
hFE	Forward Current Transfer Ratio: VCE = 8 V, IC = 10 mA			30	150	300
ICBO	Collector Cutoff Current: VCB = 8 V		µA			0.2
IEBO	Emitter Cutoff Current: VEB = 1 V		µA			1.0
CCB	Collector Base Capacitance[1]: VCB = 8 V, f = 1 MHz		pF		0.25	

Note: 1. For this test the emitter is grounded.

Absolute Maximum Ratings

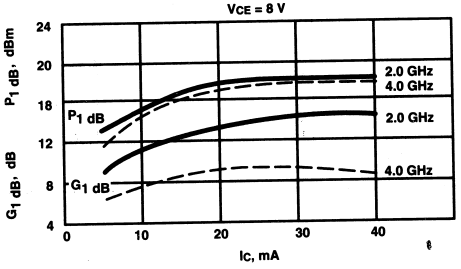
Parameter	Symbol	Absolute Maximum
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	60 mA
Power Dissipation[2,3]	P_T	500 mW
Junction Temperature	T_j	150°C
Storage Temperature	T_{STG}	–65°C to 150°C

Thermal Resistance[2,4]: θ_{jc} = 155°C/W

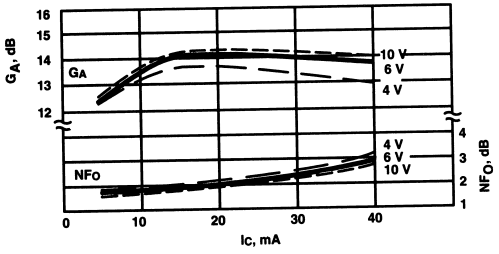
Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 6.5 mW/°C for T_C > 73°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Typical Performance, T_A = 25°C
(unless otherwise noted)

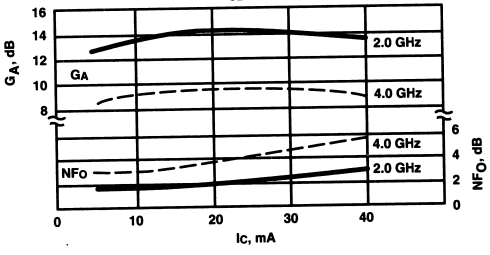
OUTPUT POWER AND 1 dB COMPRESSED GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



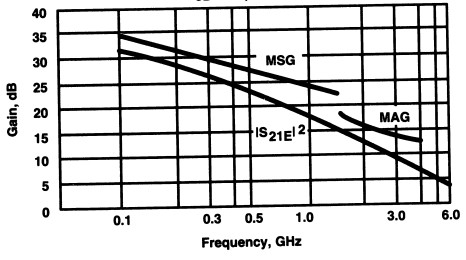
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN
vs. COLLECTOR CURRENT AND COLLECTOR VOLTAGE
f = 2.0 GHz



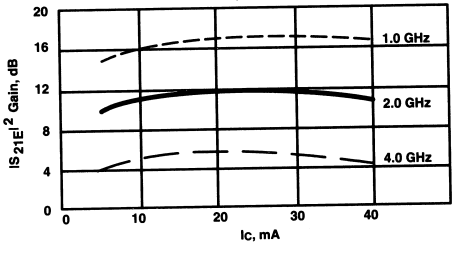
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



INSERTION POWER GAIN, MAXIMUM AVAILABLE
GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{CE} = 8 V, I_C = 25 mA



INSERTION POWER GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



Typical Scattering Parameters: Common Emitter, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 10$ mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.74	–40	28.2	25.80	156	–35.6	.017	81	.93	–14
0.5	.61	–126	21.9	12.46	108	–29.2	.035	44	.57	–31
1.0	.57	–161	16.6	6.80	87	–27.9	.040	38	.46	–33
1.5	.57	–180	13.4	4.67	75	–25.7	.052	47	.43	–34
2.0	.58	166	11.0	3.55	64	–24.5	.060	54	.41	–38
2.5	.59	160	9.3	2.92	59	–23.3	.068	58	.40	–39
3.0	.61	150	7.7	2.42	50	–21.9	.080	63	.39	–46
3.5	.62	142	6.4	2.09	41	–20.8	.091	61	.41	–54
4.0	.62	134	5.3	1.84	32	–19.5	.106	59	.42	–62
4.5	.62	125	4.3	1.65	24	–18.4	.120	57	.43	–67
5.0	.63	115	3.5	1.50	15	–17.2	.138	54	.44	–73
5.5	.65	103	2.7	1.37	6	–16.1	.157	49	.43	–78
6.0	.69	92	1.8	1.24	–4	–15.3	.172	46	.40	–86

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 25$ mA

0.1	.55	-68	32.0	40.01	146	–40.9	.009	57	.85	–19
0.5	.58	–153	23.1	14.20	99	–32.7	.023	52	.47	–29
1.0	.58	–177	17.4	7.39	82	–29.8	.032	63	.41	–28
1.5	.58	169	14.0	5.01	71	–27.3	.043	60	.39	–30
2.0	.60	158	11.6	3.78	61	–24.6	.059	64	.38	–36
2.5	.60	153	9.8	3.09	58	–23.7	.065	71	.36	–39
3.0	.63	147	8.1	2.55	48	–21.7	.082	68	.35	–47
3.5	.64	140	6.9	2.21	39	–20.7	.092	67	.37	–56
4.0	.64	133	5.8	1.94	31	–19.4	.107	65	.39	–64
4.5	.64	125	4.8	1.74	23	–18.1	.125	63	.40	–71
5.0	.64	115	4.0	1.58	14	–17.1	.140	56	.41	–78
5.5	.66	105	3.2	1.45	5	–15.9	.160	50	.40	–82
6.0	.70	94	2.4	1.32	–5	–15.1	.175	47	.37	–91

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

AT-41486
Up to 6 GHz Low Noise Silicon Bipolar Transistor

Features

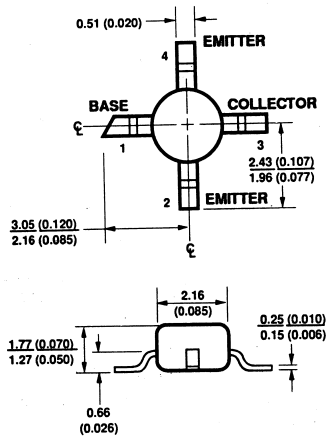
- **Low Noise Figure: 1.4 dB typical at 1.0 GHz**
  1.7 dB typical at 2.0 GHz
- **High Associated Gain: 18.0 dB typical at 1.0 GHz**
  13.0 dB typical at 2.0 GHz
- **High Gain-Bandwidth Product: 8.0 GHz typical f_T**
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Description

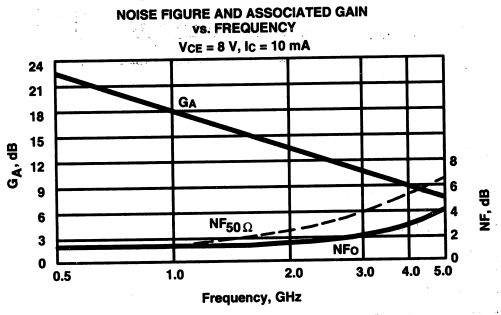
The AT-41486 is a high performance NPN silicon bipolar transistor housed in a low cost, surface mount plastic package. This device is designed for use in low noise, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

86 Plastic Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)



Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq. GHz	NFO dB	Gamma Opt Mag	Gamma Opt Ang	RN/50
0.1	1.3	.12	3	0.17
0.5	1.3	.10	16	0.17
1.0	1.4	.04	43	0.16
2.0	1.7	.12	–145	0.16
4.0	3.0	.44	–99	0.40

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NFO	Optimum Noise Figure: VCE = 8 V, IC = 10 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		1.4 1.7 3.0	1.8
GA	Gain @ NFO: VCE = 8 V, IC = 10 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB	17.0	18.0 13.0 9.0	
$\|S_{21E}\|^2$	Insertion Power Gain: VCE = 8 V, IC = 25 mA	f = 1.0 GHz f = 2.0 GHz	dB		17.5 11.5	
P1 dB	Power Output @ 1 dB Gain Compression: VCE = 8 V, IC = 25 mA	f = 2.0 GHz	dBm		18.0	
G1 dB	1 dB Compressed Gain: VCE = 8 V, IC = 25 mA	f = 2.0 GHz	dB		13.5	
f_T	Gain Bandwidth Product: VCE = 8 V, IC = 25 mA		GHz		8.0	
hFE	Forward Current Transfer Ratio: VCE = 8 V, IC = 10 mA			30	150	300
ICBO	Collector Cutoff Current: VCB = 8 V		µA			0.2
IEBO	Emitter Cutoff Current: VEB = 1 V		µA			1.0
CCB	Collector Base Capacitance[2]: VCB = 8 V, f = 1 MHz		pF		0.25	

Notes: 1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices."
2. For this test, the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	60 mA
Power Dissipation[2,3]	P_T	500 mW
Junction Temperature	T_j	150°C
Storage Temperature	T_{STG}	–65°C to 150°C

Thermal Resistance[2,4]: θ_{jc} = 165°C/W

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 6 mW/°C for T_C > 68°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Part Number Ordering Information

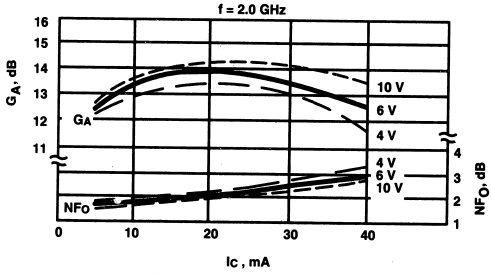
Part Number	Devices Per Reel	Reel Size
AT-41486-TR1	1000	7"
AT-41486-TR2	4000	13"

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

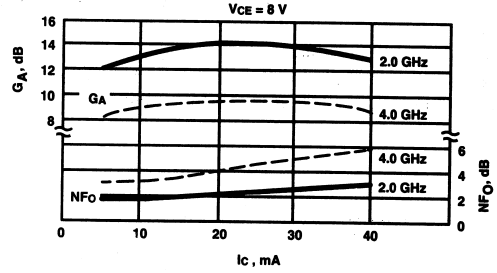
Typical Performance, T_A = 25°C

(unless otherwise noted)

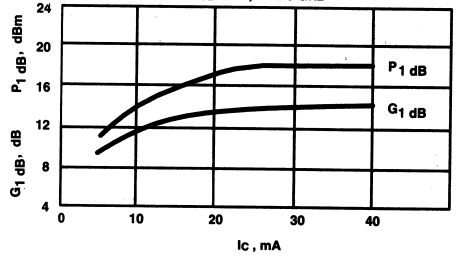
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN vs. COLLECTOR CURRENT AND COLLECTOR VOLTAGE
f = 2.0 GHz



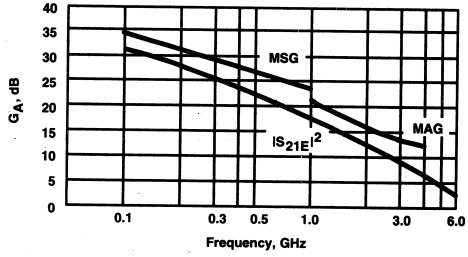
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN vs. COLLECTOR CURRENT AND FREQUENCY
VCE = 8 V



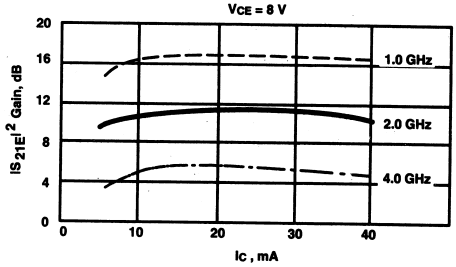
OUTPUT POWER AND 1 dB COMPRESSED GAIN vs. COLLECTOR CURRENT
VCE = 8 V, f = 2.0 GHz



INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
VCE = 8 V, IC = 25 mA



INSERTION POWER GAIN vs. COLLECTOR CURRENT AND FREQUENCY
VCE = 8 V



Typical Scattering Parameters: Common Emitter, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 10$ mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.74	–38	28.1	25.46	157	–39.6	.011	68	.94	–12
0.5	.59	–127	22.0	12.63	107	–30.2	.031	47	.60	–29
1.0	.56	–168	16.8	6.92	84	–27.7	.041	46	.49	–29
1.5	.57	169	13.5	4.72	69	–26.2	.049	49	.45	–32
2.0	.62	152	11.1	3.61	56	–24.8	.058	43	.42	–39
2.5	.63	142	9.3	2.91	47	–23.4	.068	52	.40	–42
3.0	.64	130	7.6	2.41	37	–22.2	.078	52	.39	–50
3.5	.68	122	6.3	2.06	26	–20.6	.093	51	.37	–60
4.0	.71	113	5.1	1.80	16	–19.5	.106	48	.35	–70
4.5	.74	105	4.0	1.59	7	–18.0	.125	48	.35	–84
5.0	.77	99	3.1	1.42	–4	–17.2	.139	43	.35	–98
5.5	.79	93	2.0	1.27	–13	–16.3	.153	38	.35	–114
6.0	.81	87	1.1	1.13	–22	–15.4	.170	34	.35	–131

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 25$ mA

0.1	.50	–75	32.0	40.01	142	–41.3	.009	54	.85	–17
0.5	.55	–158	23.2	14.38	97	–34.1	.020	48	.51	–24
1.0	.57	177	17.5	7.50	78	–29.9	.032	61	.46	–24
1.5	.57	161	14.1	5.07	65	–27.3	.043	62	.44	–28
2.0	.59	148	11.5	3.75	53	–24.8	.058	59	.43	–35
2.5	.61	139	9.6	3.02	45	–22.9	.072	58	.40	–41
3.0	.65	128	8.0	2.52	34	–21.6	.083	57	.38	–49
3.5	.70	121	6.7	2.17	24	–20.1	.099	56	.36	–59
4.0	.74	113	5.7	1.92	14	–18.8	.115	52	.34	–72
4.5	.78	107	4.7	1.72	3	–17.6	.132	47	.32	–87
5.0	.78	102	3.7	1.53	–8	–16.6	.149	42	.31	–106
5.5	.78	96	2.7	1.36	–19	–15.4	.169	36	.31	–125
6.0	.76	91	1.6	1.21	–29	–14.5	.188	31	.33	–144

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

Low Cost General Purpose Transistors

Technical Data

AT-41511
AT-41586

Features

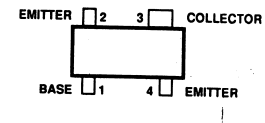
- **Low Noise Figure**
  1.4 dB Typical at 1 GHz
  1.7 dB Typical at 2 GHz
- **High Associated Gain**
  17.0 dB Typical at 1 GHz
  12.5 dB Typical at 2 GHz
- **Low Cost Surface Mount Packages**
- **Tape and Reel Option Available**

Description

The AT-41511 and AT-41586 are low cost NPN silicon bipolar transistors housed in surface mount plastic packages. These devices are designed for use in low noise, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

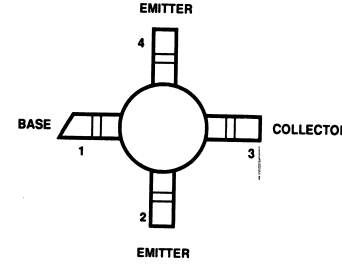
Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

AT-41511



Outline 143

AT-41586



Outline 86

Electrical Specifications, T_A = 25°C

V_{CE} = 8 V

Symbol	Parameters and Test Conditions		Unit	AT-41511			AT-41586		
				Min.	Typ.	Max.	Min.	Typ.	Max.
NF_o	Optimum Noise Figure: I_C = 10 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		1.4 1.8 3.5			1.4 1.7 3.0	
G_A	Gain @ NF_0: I_C = 10 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		17.0 12.5 6.5			17.0 12.5 8.0	
$\|S_{21E}\|^2$	Insertion Power Gain: I_C = 25 mA	f = 1.0 GHz f = 2.0 GHz	dB		16.5 10.5			17.0 11.0	
P_{1dB}	Power Output @ 1 dB Gain Compression: I_C = 25 mA	f = 2.0 GHz	dBm		18.0			18.0	
G_{1dB}	1 dB Compressed Gain: I_C = 25 mA	f = 2.0 GHz	dB		11.5			13.0	
f_T	Gain Bandwidth Product: I_C = 25 mA		GHz		8.0			8.0	
h_{FE}	Forward Current Transfer Ratio: I_C = 10 mA			30	150	300	30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		mA			0.2			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		mA			1.0			1.0

Note:
1. For more information on outlines 143 and 86, refer to "Tape and Reel Packaging for Surface Mount Devices."

Absolute Maximum Ratings[1]

Symbol	Parameter	Units	AT-41511	AT-41586
V_{EBO}	Emitter-Base Voltage	V	1.5	1.5
V_{CBO}	Collector-Base Voltage	V	20	20
V_{CEO}	Collector-Emitter Voltage	V	12	12
I_C	Collector Current	mA	50	60
P_T	Power Dissipation[2]	mW	225	500
T_j	Junction Temperature	°C	150	150
T_{STG}	Storage Temperature	°C	-65 to 150	-65 to 150
--	Thermal Resistance[3]	°C/W	Θ_{ja} = 550	Θ_{jc} = 165

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. See MEASUREMENTS section, "Thermal Resistance", for more information.

Typical Parameters

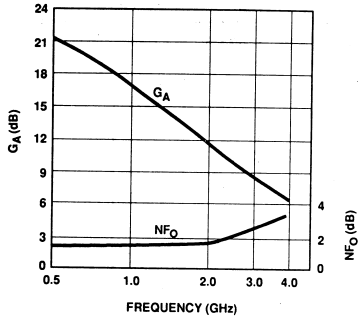


Figure 1. AT-41511 and AT-41586 Noise Figure and Associated Gain vs. Frequency at V_{CE} = 8 V, I_C = 10 mA.

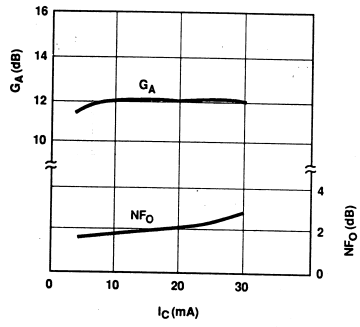


Figure 2. AT-41511 and AT-41586 Optimum Noise Figure and Associated Gain vs. Collector Current at V_{CE} = 8 V, f = 2.0 GHz.

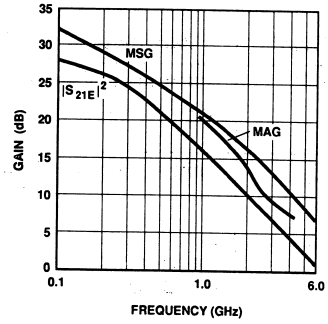


Figure 3. AT-41511 Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency at V_{CE} = 8 V, I_C = 25 mA.

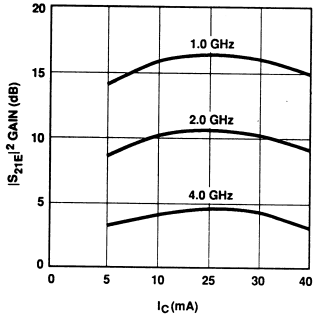


Figure 4. AT-41511 Insertion Power Gain vs. Collector Current and Frequency at 25°C, V_{CE} = 8 V.

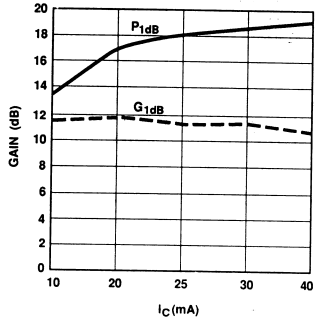


Figure 5. AT-41511 P_{1dB} and G_{1dB} vs. Collector Current, at f = 2.0 GHz.

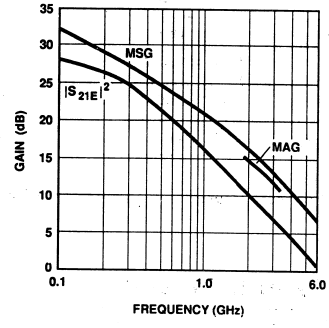


Figure 6. AT-41586 Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency at V_{CE} = 8 V, I_C = 10 mA.

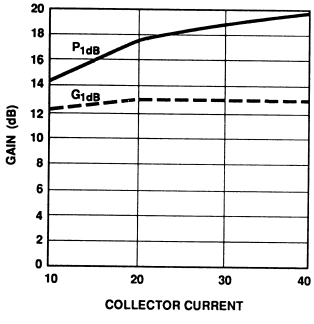


Figure 7. AT-41586 P_{1dB} and G_{1dB} vs. Collector Current, at f = 2.0 GHz.

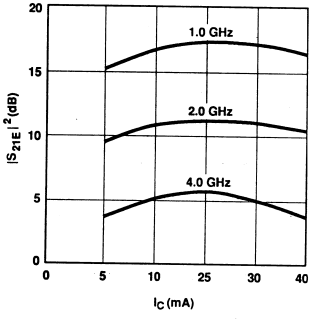


Figure 8. AT-41586 Insertion Power Gain vs. Collector Current and Frequency at 25°C, V_{CE} = 8 V.

Typical Scattering Parameters at $T_A = 25°C$

AT-41511
$V_{CE} = 8$ V, $I_C = 10$ mA, $Z_o = 50\ \Omega$

Frequency (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
0.100	0.81	-37	27.9	24.9	155	-36.4	0.015	71	0.91	-15
0.200	0.73	-67	26.4	20.9	136	-31.7	0.026	59	0.78	-26
0.300	0.65	-91	24.7	17.1	122	-29.8	0.032	50	0.67	-32
0.400	0.60	-108	22.9	14.0	113	-28.8	0.036	46	0.58	-35
0.500	0.57	-121	21.4	11.7	106	-28.1	0.039	44	0.52	-37
0.600	0.54	-132	20.0	10.0	100	-27.5	0.042	43	0.48	-38
0.700	0.52	-139	18.8	8.7	96	-27.1	0.044	43	0.45	-39
0.800	0.51	-146	17.3	7.7	92	-26.7	0.046	43	0.44	-40
0.900	0.50	-151	16.8	6.9	89	-26.1	0.049	43	0.43	-41
1.000	0.46	-155	16.0	6.3	86	-25.8	0.051	44	0.42	-41
1.500	0.49	-170	12.7	4.3	74	-23.8	0.064	47	0.44	-44
2.000	0.46	173	10.4	3.3	63	-22.0	0.079	49	0.45	-47
2.500	0.42	154	8.0	2.5	53	-20.6	0.093	49	0.43	-53
3.000	0.39	139	6.8	2.2	48	-19.2	0.109	48	0.41	-49
3.500	0.45	124	5.6	1.9	37	-17.8	0.128	47	0.41	-52
4.000	0.51	118	4.1	1.6	30	-16.7	0.146	45	0.37	-60
4.500	0.62	113	3.5	1.5	22	-15.5	0.167	42	0.36	-74
5.000	0.66	110	2.3	1.3	14	-14.7	0.182	39	0.35	-90
5.500	0.67	111	1.6	1.2	8	-13.8	0.203	35	0.35	-104
6.000	0.65	110	0.8	1.1	4	-12.8	0.228	31	0.42	-115

AT-41511
$V_{CE} = 8$ V, $I_C = 25$ mA, $Z_o = 50\ \Omega$

Frequency (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
0.100	0.67	-58	31.4	37.2	144	-37.7	0.013	64	0.81	-22
0.200	0.58	-97	28.5	26.7	123	-33.9	0.020	53	0.63	-31
0.300	0.53	-120	26.0	19.9	111	-32.3	0.024	49	0.52	-34
0.400	0.51	-145	23.9	15.6	103	-24.7	0.028	49	0.46	-35
0.500	0.49	-153	22.1	12.7	98	-30.4	0.030	50	0.42	-35
0.600	0.48	-159	20.6	10.7	94	-29.3	0.034	52	0.39	-35
0.700	0.48	-163	19.4	9.3	90	-28.6	0.037	53	0.38	-35
0.800	0.47	-167	18.3	8.2	87	-27.9	0.040	55	0.37	-36
0.900	0.47	-170	17.3	7.3	85	-27.1	0.044	56	0.36	-37
1.000	0.47	-171	16.4	6.6	82	-26.5	0.047	57	0.37	-38
1.500	0.44	177	13.8	4.9	71	-23.7	0.065	59	0.40	-42
2.000	0.41	163	10.6	3.4	61	-21.6	0.083	58	0.42	-45
2.500	0.39	145	8.6	2.7	51	-20.0	0.100	57	0.42	-48
3.000	0.45	132	7.2	2.3	46	-18.4	0.119	55	0.40	-47
3.500	0.51	120	6.0	2.0	36	-17.1	0.139	51	0.38	-54
4.000	0.55	114	4.6	1.7	28	-16.1	0.156	49	0.34	-65
4.500	0.61	110	3.5	1.5	21	-15.0	0.176	45	0.34	-78
5.000	0.66	108	2.3	1.3	13	-14.4	0.190	42	0.32	-93
5.500	0.67	108	1.6	1.2	7	-13.4	0.212	38	0.32	-106
6.000	0.64	107	0.8	1.1	2	-12.5	0.237	33	0.40	-116

Typical Scattering Parameters at $T_A = 25°C$

AT-41586

$V_{CE} = 8$ V, $I_C = 10$ mA, $Z_o = 50\ \Omega$

Frequency (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
0.100	0.78	-39	28.4	26.3	154	-36.4	0.015	71	0.91	-16
0.200	0.71	-71	26.9	22.1	134	-31.7	0.026	59	0.79	-27
0.300	0.65	-95	25.2	18.1	122	-29.8	0.032	50	0.67	-34
0.400	0.61	-113	23.5	15.0	119	-28.8	0.036	44	0.58	-38
0.500	0.59	-127	22.0	12.6	114	-28.1	0.039	43	0.52	-40
0.600	0.57	-137	20.7	10.8	100	-27.5	0.042	43	0.47	-40
0.700	0.56	-146	19.6	9.5	95	-27.1	0.044	43	0.44	-41
0.800	0.56	-154	18.5	8.4	91	-26.5	0.047	43	0.42	-41
0.900	0.55	-160	17.6	7.6	86	-26.1	0.049	44	0.40	-42
1.000	0.55	-166	16.8	6.9	83	-25.8	0.051	47	0.38	-42
1.500	0.55	173	13.4	4.7	70	-23.8	0.064	49	0.34	-45
2.000	0.57	157	10.9	3.5	57	-22.0	0.079	49	0.32	-52
2.500	0.59	144	9.2	2.9	44	-20.6	0.093	48	0.31	-61
3.000	0.62	133	7.6	2.4	34	-19.3	0.108	47	0.30	-71
3.500	0.64	123	6.0	2.0	25	-18.1	0.124	45	0.30	-83
4.000	0.67	114	5.1	1.8	16	-17.0	0.141	42	0.31	-95
4.500	0.70	106	4.1	1.6	5	-15.9	0.159	39	0.32	-108
5.000	0.73	99	2.9	1.4	-3	-15.0	0.176	35	0.32	-121
5.500	0.76	93	1.6	1.2	-8	-14.2	0.193	31	0.34	-135
6.000	0.78	88	0.8	1.1	-18	-13.5	0.209	31	0.36	-150

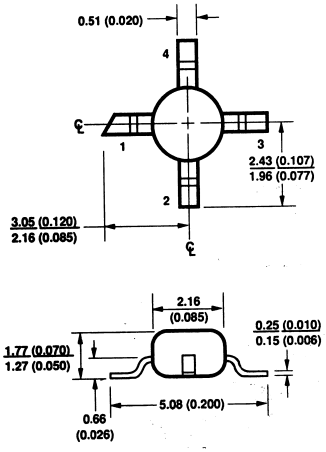
AT-41586

$V_{CE} = 8$ V, $I_C = 25$ mA, $Z_o = 50\ \Omega$

Frequency (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
0.100	0.64	-61	31.9	39.4	154	-37.0	0.014	64	0.82	-24
0.200	0.59	-101	29.2	28.7	169	-33.1	0.022	53	0.64	-35
0.300	0.56	-125	26.6	21.4	124	-31.7	0.026	49	0.53	-38
0.400	0.55	-140	24.6	17.0	111	-30.4	0.030	49	0.47	-39
0.500	0.54	-151	22.9	14.0	104	-29.6	0.033	50	0.43	-38
0.600	0.54	-159	21.4	11.7	97	-28.8	0.036	52	0.40	-38
0.700	0.54	-166	20.1	10.1	91	-28.1	0.039	53	0.40	-37
0.800	0.54	-171	19.0	8.9	86	-27.5	0.042	55	0.38	-37
0.900	0.54	-176	18.0	7.9	81	-26.9	0.045	56	0.37	-37
1.000	0.55	177	17.1	7.2	77	-26.3	0.048	57	0.36	-37
1.500	0.57	164	13.6	4.8	64	-23.8	0.064	59	0.34	-42
2.000	0.57	152	11.1	3.6	55	-21.9	0.080	57	0.32	-49
2.500	0.60	141	9.2	2.9	44	-20.0	0.100	55	0.31	-58
3.000	0.62	132	7.6	2.4	34	-18.4	0.120	52	0.31	-68
3.500	0.64	124	6.4	2.1	24	-17.0	0.140	49	0.31	-80
4.000	0.67	116	5.6	1.9	18	-14.8	0.180	45	0.32	-94
4.500	0.70	109	4.1	1.6	9	-15.9	0.160	45	0.30	-109
5.000	0.73	102	3.5	1.5	1	-15.3	0.170	42	0.30	-123
5.500	0.77	96	2.3	1.3	-7	-14.4	0.190	38	0.32	-138
6.000	0.76	90	1.6	1.2	-14	-13.9	0.200	33	0.35	-152

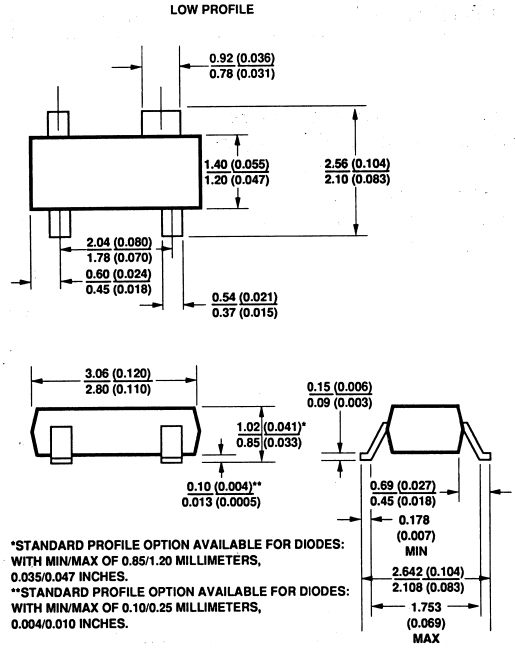
Package Dimensions

Outline 86



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Outline 143 (SOT-143)



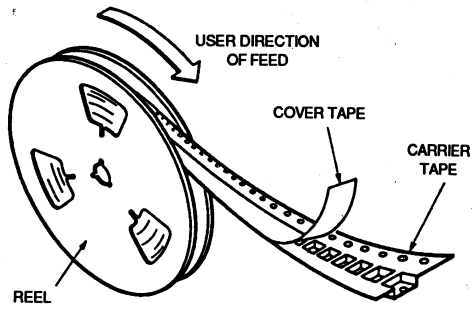
*STANDARD PROFILE OPTION AVAILABLE FOR DIODES: WITH MIN/MAX OF 0.85/1.20 MILLIMETERS, 0.035/0.047 INCHES.
**STANDARD PROFILE OPTION AVAILABLE FOR DIODES: WITH MIN/MAX OF 0.10/0.25 MILLIMETERS, 0.004/0.010 INCHES.

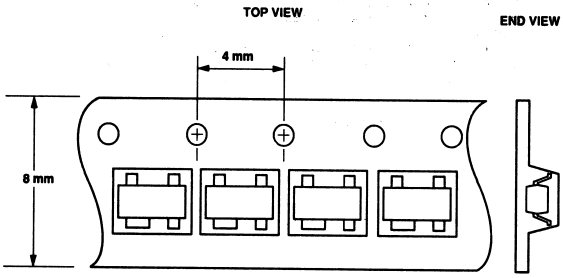
DIMENSIONS ARE IN MILLIMETERS (INCHES)

Part Number Ordering Information

Part Number	Devices per Reel	Reel Size
AT-41511-TR1	3000	7"
AT-41511-TR2	10000	13"

Conforms to Electronic Industries Standard RS-481, "Taping of Surface Mounted Components for Automated Placement." Standard Quantity is 3,000 Devices/Reel.

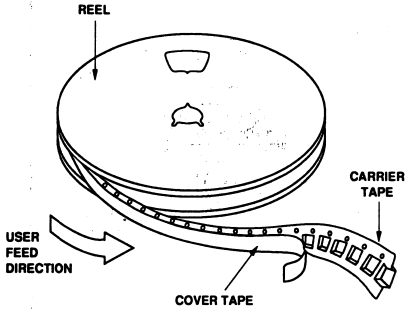


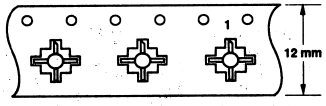


For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

Ordering Information For AT-41586 Only

Part Number	Devices Per Reel	Reel Size
AT-41586-TR1	1000	7"
AT-41586-TR2	4000	13"





NOTE: 1. INDICATES PIN 1 ORIENTATION.

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

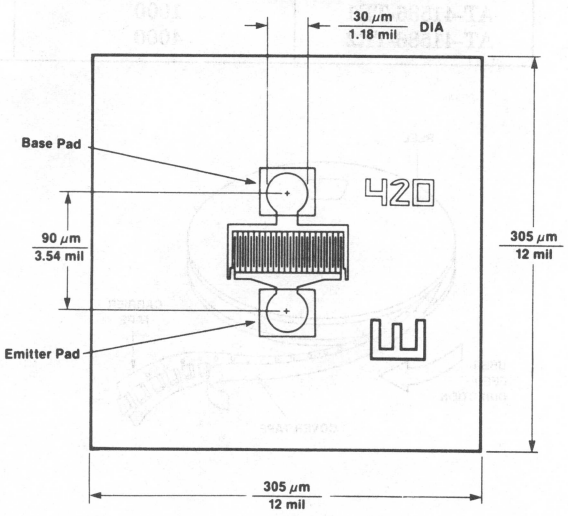
HEWLETT PACKARD

AT-42000
Up to 6 GHz Medium Power Silicon Bipolar Transistor Chip

Features

- **High Output Power:**
  21.0 dBm typical $P_{1\,dB}$ at 2.0 GHz
  20.5 dBm typical $P_{1\,dB}$ at 4.0 GHz
- **High Gain at 1 dB Compression:**
  15.0 dB typical $G_{1\,dB}$ at 2.0 GHz
  10.0 dB typical $G_{1\,dB}$ at 4.0 GHz
- **Low Noise Figure:**
  1.9 dB typical NF_O at 2.0 GHz
- **High Gain-Bandwidth Product:**
  9.0 GHz typical f_T

Chip Outline



Description

The AT-42000 is a high performance NPN silicon bipolar transistor chip designed for use in medium power, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

The die are nitride-passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self alignment techniques, and gold metallization in the fabrication of these devices.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire. See also "Chip Use" in the APPLICATIONS section.

Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
0.1	1.0	.04	13	0.13
0.5	1.1	.05	69	0.13
1.0	1.5	.09	127	0.12
2.0	1.9	.23	171	0.11
4.0	3.0	.47	–154	0.14

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f = 4.0 GHz	dB		11.5 5.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f = 4.0 GHz	dBm		21.0 20.5	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f = 4.0 GHz	dB		15.0 10.0	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz f = 4.0 GHz	dB		1.9 3.0	
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz f = 4.0 GHz	dB		14.0 10.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 35 mA		GHz		9.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 35 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		μA			2.0
C_{CB}	Collector Base Capacitance[2]: V_{CB} = 8 V, f = 1 MHz		pF		0.23	

Notes: 1. RF performance is determined by packaging and testing 10 devices per wafer.
2. For this test the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	80 mA
Power Dissipation[2,3]	P_T	600 mW
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 70°C/W

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. $T_{MOUNTING\ SURFACE}$ = 25°C.
3. Derate at 14.3 mW/°C for $T_{MOUNTING\ SURFACE}$ > 158°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

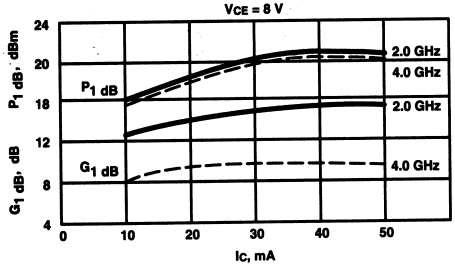
Part Number Ordering Information

Part Number	Devices Per Tray
AT-42000-GP2	10
AT-42000-GP4	100
AT-42000-GP6	up to 300

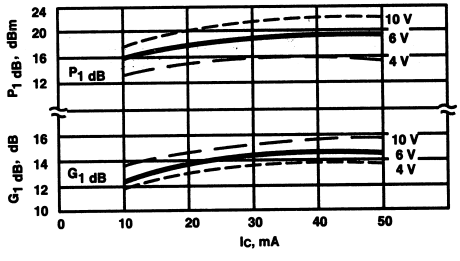
Typical Performance, T_A = 25°C

(unless otherwise noted)

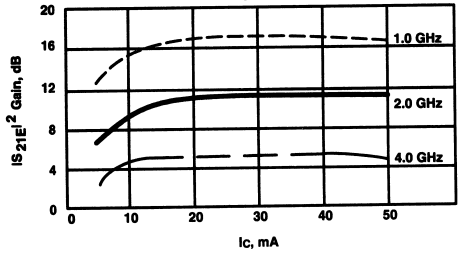
OUTPUT POWER AND 1 dB COMPRESSED GAIN vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



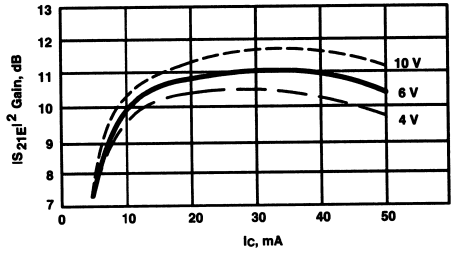
OUTPUT POWER AND 1 dB COMPRESSED GAIN vs. COLLECTOR CURRENT AND VOLTAGE
f = 2.0 GHz



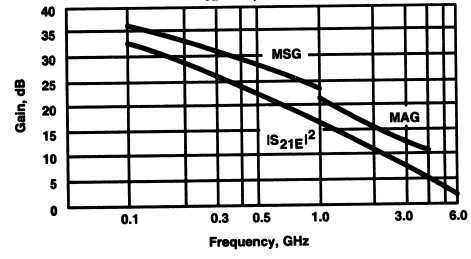
INSERTION POWER GAIN vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8V



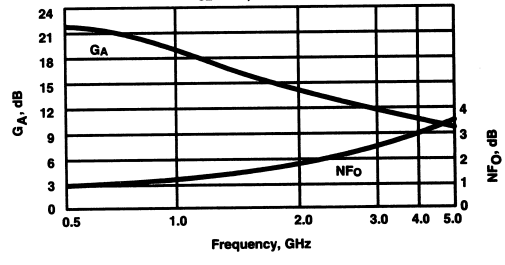
INSERTION POWER GAIN vs. COLLECTOR CURRENT AND VOLTAGE
f = 2.0 GHz



INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{CE} = 8 V, I_C = 35 mA



NOISE FIGURE AND ASSOCIATED GAIN vs. FREQUENCY
V_{CE} = 8 V, I_C = 10 mA



Typical Scattering Parameters: Common Emitter, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 10$ mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.70	–50	28.0	25.19	155	–37.7	.013	71	.92	–14
0.5	.67	–136	20.9	11.04	108	–30.5	.030	43	.57	–27
1.0	.66	–166	15.7	6.08	90	–28.9	.036	47	.50	–24
1.5	.66	–173	12.1	4.02	86	–28.2	.039	52	.48	–23
2.0	.66	179	9.8	3.09	82	–27.5	.042	57	.47	–23
2.5	.67	170	7.8	2.46	74	–26.0	.050	66	.47	–23
3.0	.67	165	6.3	2.08	68	–24.7	.058	72	.47	–26
3.5	.70	157	5.1	1.80	61	–23.4	.068	77	.47	–28
4.0	.70	151	3.9	1.56	57	–21.8	.081	82	.48	–30
4.5	.71	145	2.9	1.40	51	–20.7	.092	86	.50	–34
5.0	.73	138	1.9	1.24	41	–19.3	.109	87	.51	–38
5.5	.74	132	1.2	1.15	36	–17.2	.138	88	.51	–50
6.0	.76	129	0.2	1.02	32	–16.3	.154	87	.53	–56

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 35$ mA

0.1	.49	–96	33.0	44.61	143	–40.9	.009	65	.79	–24
0.5	.62	–163	22.8	13.87	98	–34.4	.019	58	.42	–26
1.0	.63	179	17.2	7.25	86	–30.5	.030	70	.38	–22
1.5	.63	171	13.5	4.74	78	–27.7	.041	76	.38	–23
2.0	.65	163	11.2	3.62	72	–25.4	.054	79	.38	–25
2.5	.65	159	9.3	2.90	67	–23.6	.066	82	.38	–27
3.0	.68	154	7.8	2.44	60	–22.1	.079	82	.38	–29
3.5	.67	148	6.5	2.12	57	–20.6	.093	84	.39	–32
4.0	.69	144	5.3	1.83	51	–19.7	.104	86	.40	–34
4.5	.70	139	4.4	1.65	47	–18.3	.121	86	.41	–40
5.0	.70	137	3.3	1.46	43	–17.5	.133	85	.42	–44
5.5	.72	131	2.7	1.36	38	–16.5	.149	86	.41	–48
6.0	.74	128	1.7	1.22	34	–15.7	.164	85	.44	–55

A model for this device is available in the DEVICE MODELS section.

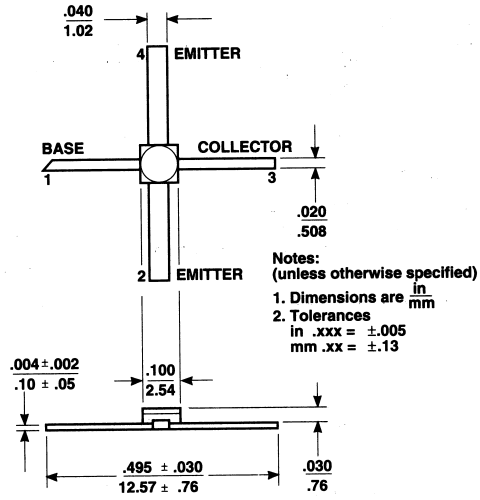
HEWLETT PACKARD

AT-42010
Up to 6 GHz Medium Power Silicon Bipolar Transistor

Features

- **High Output Power:**
  12.0 dBm typical $P_{1\,dB}$ at 2.0 GHz
  20.5 dBm typical $P_{1\,dB}$ at 4.0 GHz
- **High Gain at 1 dB Compression:**
  14.0 dB typical $G_{1\,dB}$ at 2.0 GHz
  9.5 dB typical $G_{1\,dB}$ at 4.0 GHz
- **Low Noise Figure:**
  1.9 dB typical NF_O at 2.0 GHz
- **High Gain-Bandwidth Product:**
  8.0 GHz typical f_T
- **Hermetic Gold-ceramic Microstrip Package**

100 mil Package



Outline 10A

Description

The AT-42010 is a high performance NPN silicon bipolar transistor housed in a hermetic, high reliability package. This device is designed for use in medium power, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
0.1	1.0	.04	15	0.13
0.5	1.1	.05	76	0.12
1.0	1.5	.10	132	0.12
2.0	1.9	.23	–177	0.11
4.0	3.0	.45	–125	0.26

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f = 4.0 GHz	dB	10.5	11.5 5.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f = 4.0 GHz	dBm		21.0 20.5	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f = 4.0 GHz	dB		14.0 9.5	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz f = 4.0 GHz	dB		1.9 3.0	
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz f = 4.0 GHz	dB		13.5 10.0	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 35 mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 35 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		µA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		µA			2.0
C_{CB}	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		0.28	

Note: 1. For this test the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	80 mA
Power Dissipation[2,3]	P_T	600 mW
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 150°C/W

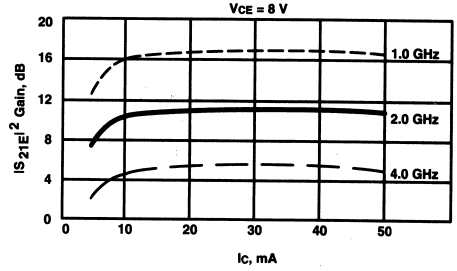
Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 6.7 mW/°C for T_C > 110°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

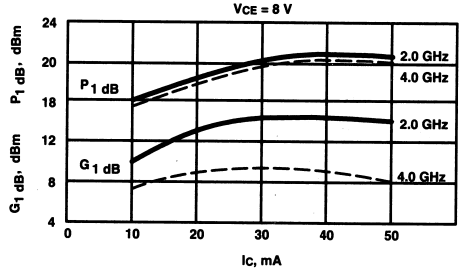
Typical Performance, T_A = 25°C

(unless otherwise noted)

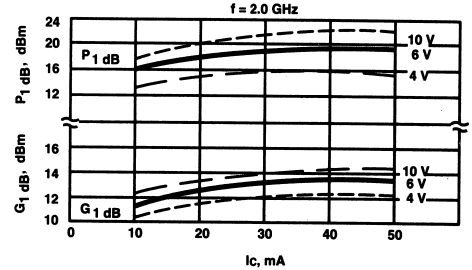
INSERTION POWER GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



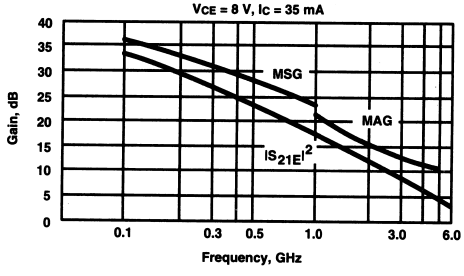
OUTPUT POWER AND 1 dB COMPRESSED GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



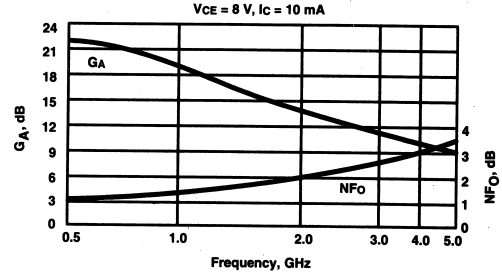
OUTPUT POWER AND 1 dB COMPRESSED GAIN
vs. COLLECTOR CURRENT AND VOLTAGE
f = 2.0 GHz



INSERTION POWER GAIN, MAXIMUM AVAILABLE
GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{CE} = 8 V, I_C = 35 mA



NOISE FIGURE AND ASSOCIATED GAIN
vs. FREQUENCY
V_{CE} = 8 V, I_C = 10 mA



Typical Scattering Parameters: Common Emitter, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 10$ mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.74	–47	28.5	26.65	153	–36.4	.015	72	.91	–18
0.5	.65	–136	21.4	11.71	103	–29.4	.034	38	.51	–39
1.0	.63	–168	15.9	6.24	82	–27.2	.044	36	.40	–42
1.5	.63	174	12.6	4.26	69	–26.0	.050	42	.38	–45
2.0	.63	161	10.1	3.23	57	–24.6	.059	43	.38	–49
2.5	.64	154	8.4	2.64	51	–23.0	.070	52	.38	–51
3.0	.65	145	6.9	2.22	41	–22.0	.080	54	.37	–56
3.5	.66	136	5.8	1.94	31	–21.0	.090	51	.38	–65
4.0	.66	126	4.7	1.72	21	–19.7	.104	50	.39	–74
4.5	.66	115	3.8	1.55	11	–18.0	.126	45	.40	–82
5.0	.66	103	3.0	1.41	1	–17.3	.136	41	.40	–89
5.5	.68	90	2.1	1.28	–9	–16.1	.156	36	.40	–98
6.0	.72	81	1.3	1.16	–19	–15.4	.170	31	.37	–110

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 35$ mA

0.1	.54	–90	33.3	45.97	138	–39.2	.011	54	.76	–29
0.5	.62	–163	22.8	13.83	94	–33.2	.022	52	.34	–40
1.0	62	177	17.0	7.10	78	–28.8	.036	59	.30	–40
1.5	.62	166	13.6	4.82	67	–26.2	.049	61	.29	–42
2.0	.62	155	11.3	3.65	56	–23.8	.065	57	.29	–47
2.5	.63	150	9.5	2.99	51	–21.8	.081	62	.29	–50
3.0	.64	142	8.0	2.52	42	–21.0	.090	63	.30	–57
3.5	.65	133	6.8	2.19	32	–19.7	.103	59	.30	–67
4.0	.65	124	5.7	1.93	22	–18.4	120	54	.31	–76
4.5	.65	113	4.7	1.72	13	–17.2	.138	49	.33	–85
5.0	.66	102	3.9	1.56	3	–16.6	.148	45	.34	–92
5.5	.69	91	3.0	1.41	–6	–15.6	.166	39	.33	–100
6.0	.73	83	2.1	1.27	–16	–14.9	.180	32	.30	–110

A model for this device is available in the DEVICE MODELS section.

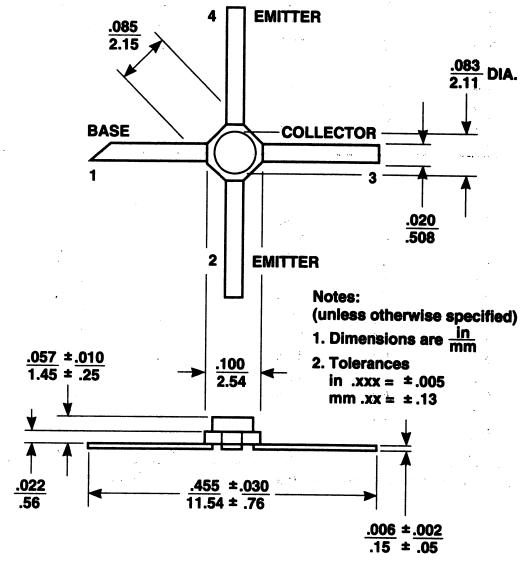
HEWLETT PACKARD

AT-42035
Up to 6 GHz Medium Power Silicon Bipolar Transistor

Features

- **High Output Power:**
  21.0 dBm typical $P_{1\,dB}$ at 2.0 GHz
  20.5 dBm typical $P_{1\,dB}$ at 4.0 GHz
- **High Gain at 1 dB Compression:**
  14.0 dB typical $G_{1\,dB}$ at 2.0 GHz
  9.5 dB typical $G_{1\,dB}$ at 4.0 GHz
- **Low Noise Figure:**
  1.9 dB typical NF_O at 2.0 GHz
- **High Gain-Bandwidth Product:**
  8.0 GHz typical f_T
- **Cost Effective Ceramic Microstrip Package**

35 micro-X Package



Description

The AT-42035 is a high performance NPN silicon bipolar transistor housed in a cost effective, microstrip package. This device is designed for use in medium power, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
0.1	1.0	.04	10	0.13
0.5	1.1	.04	66	0.12
1.0	1.3	.07	150	0.12
2.0	2.0	.20	–178	0.12
4.0	3.0	.51	–110	0.36

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f = 4.0 GHz	dB	10.5	11.0 5.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f = 4.0 GHz	dBm		21.0 20.5	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f = 4.0 GHz	dB		14.0 9.5	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz f = 4.0 GHz	dB		1.9 3.0	
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz f = 4.0 GHz	dB		13.5 10.0	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 35 mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 35 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		µA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		µA			2.0
C_{CB}	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		0.28	

Note: 1. For this test the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	80 mA
Power Dissipation[2,3]	P_T	600 mW
Junction Temperature	T_j	200°C
Storage Temperature[4]	T_{STG}	–65°C to 200°C

Thermal Resistance[2,5]: θ_{jc} = 175°C/W

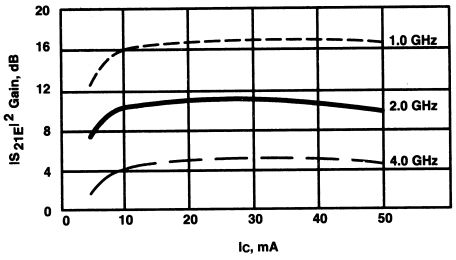
Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 5.7 mW/°C for T_C > 95°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safely stored up to 200°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

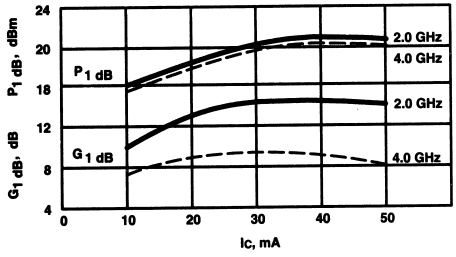
Typical Performance, T_A = 25°C

(unless otherwise noted)

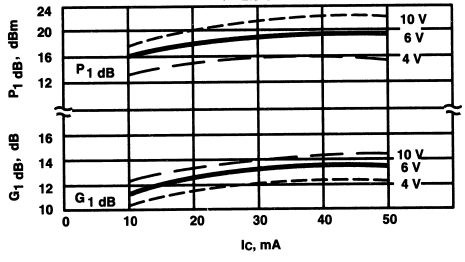
INSERTION POWER GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



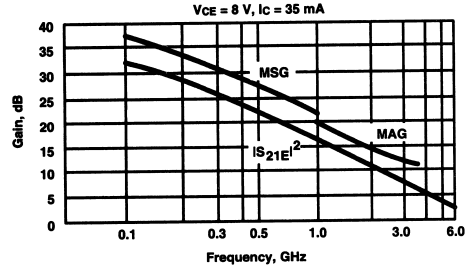
OUTPUT POWER AND 1 dB COMPRESSED GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



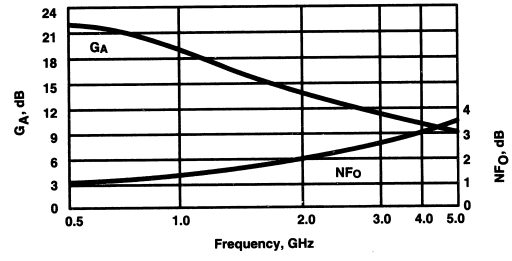
OUTPUT POWER AND 1 dB COMPRESSED GAIN
vs. COLLECTOR CURRENT AND VOLTAGE
f = 2.0 GHz



INSERTION POWER GAIN, MAXIMUM AVAILABLE
GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{CE} = 8 V, I_C = 35 mA



NOISE FIGURE AND ASSOCIATED GAIN
vs. FREQUENCY
V_{CE} = 8 V, I_C = 10 mA



Typical Scattering Parameters: Common Emitter, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 10$ mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.72	–46	28.3	26.09	152	–37.0	.014	73	.92	–14
0.5	.59	–137	20.9	11.13	102	–31.0	.028	44	.58	–27
1.0	.56	–171	15.4	5.91	80	–28.2	.039	47	.51	–29
1.5	.56	169	12.1	4.03	67	–26.6	.047	52	.50	–33
2.0	.58	155	9.7	3.06	55	–24.2	.062	55	.48	–38
2.5	.59	147	8.0	2.50	48	–22.6	.074	61	.47	–42
3.0	.61	137	6.5	2.10	38	–20.8	.092	65	.46	–51
3.5	.63	128	5.2	1.82	27	–19.6	.105	62	.47	–63
4.0	.63	117	4.0	1.60	17	–18.0	.126	57	.49	–72
4.5	.63	106	3.1	1.43	7	–16.5	.149	53	.51	–80
5.0	.64	93	2.3	1.30	–3	–15.4	.169	48	.52	–87
5.5	.67	79	1.5	1.19	–13	–14.3	.193	41	.51	–94
6.0	.72	70	0.6	1.07	–23	–13.4	.215	35	.46	–105

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 35$ mA

0.1	.50	–88	33.2	45.64	135	–42.0	.008	68	.77	–22
0.5	.52	–164	22.4	13.24	92	–32.8	.023	57	.45	–25
1.0	.53	174	16.6	6.75	76	–28.2	.039	63	.42	–26
1.5	.53	160	13.1	4.55	64	–25.6	.053	66	.41	–30
2.0	.55	148	10.8	3.45	53	–23.2	.069	65	.41	–36
2.5	.57	142	9.0	2.81	47	–21.6	.084	67	.39	–40
3.0	.59	134	7.5	2.37	37	–20.0	.101	64	.38	–49
3.5	.60	125	6.3	2.06	27	–18.4	.120	61	.39	–61
4.0	.60	116	5.2	1.81	17	–17.0	.141	57	.41	–71
4.5	.60	104	4.2	1.62	7	–16.0	.158	50	.43	–78
5.0	.61	92	3.4	1.47	–2	–14.9	.179	45	.44	–84
5.5	.64	79	2.6	1.35	–13	–14.1	.198	37	.43	–91
6.0	.69	70	1.7	1.21	–23	–13.2	.219	30	.38	–102

A model for this device is available in the DEVICE MODELS section.

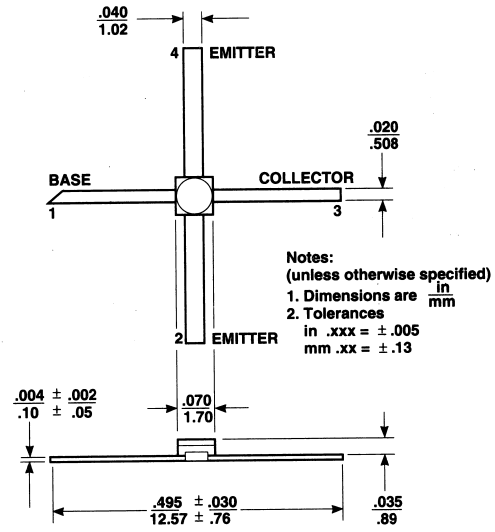
HEWLETT PACKARD

AT-42070
Up to 6 GHz Medium Power Silicon Bipolar Transistor

Features

- **High Output Power:**
  21.0 dBm typical $P_{1\,dB}$ at 2.0 GHz
  20.5 dBm typical $P_{1\,dB}$ at 4.0 GHz
- **High Gain at 1 dB Compression:**
  15.0 dB typical $G_{1\,dB}$ at 2.0 GHz
  10.0 dB typical $G_{1\,dB}$ at 4.0 GHz
- **Low Noise Figure:**
  1.9 dB typical NF_O at 2.0 GHz
- **High Gain-Bandwidth Product:**
  8.0 GHz typical f_T
- **Hermetic Gold-ceramic Microstrip Package**

70 mil Package



Description

The AT-42070 is a high performance NPN silicon bipolar transistor housed in a hermetic high reliability package. This device is designed for use in medium power, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
0.1	1.0	.05	15	0.13
0.5	1.1	.06	75	0.13
1.0	1.5	.10	126	0.12
2.0	1.9	.23	172	0.11
4.0	3.0	.45	–145	0.17

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f = 4.0 GHz	dB	10.5	11.5 5.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f = 4.0 GHz	dBm		21.0 20.5	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f = 4.0 GHz	dB		15.0 10.0	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz f = 4.0 GHz	dB		1.9 3.0	
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz f = 4.0 GHz	dB		14.0 10.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 35 mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 35 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		µA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		µA			2.0
C_{CB}	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		0.28	

Note: 1. For this test the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	80 mA
Power Dissipation[2,3]	P_T	600 mW
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 150°C/W

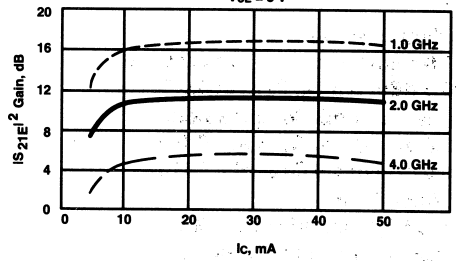
Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 6.7 mW/°C for T_C > 110°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

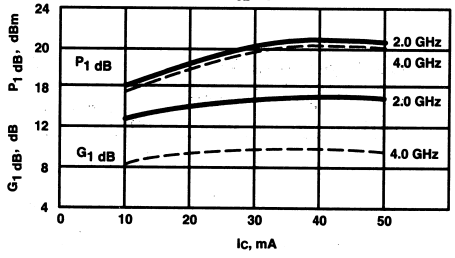
Typical Performance, T_A = 25°C

(unless otherwise noted)

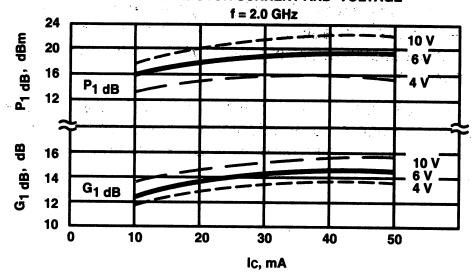
INSERTION POWER GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



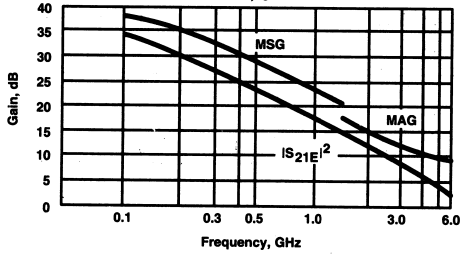
OUTPUT POWER AND 1 dB COMPRESSED GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



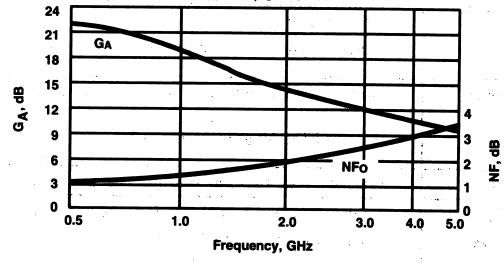
OUTPUT POWER AND 1 dB COMPRESSED GAIN
vs. COLLECTOR CURRENT AND VOLTAGE
f = 2.0 GHz



INSERTION POWER GAIN, MAXIMUM AVAILABLE
GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{CE} = 8 V, I_C = 35 mA



NOISE FIGURE AND ASSOCIATED GAIN
vs. FREQUENCY
V_{CE} = 8 V, I_C = 10 mA



Typical Scattering Parameters: Common Emitter, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 10$ mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.70	–49	28.5	26.56	154	–36.0	.016	77	.91	–18
0.5	.69	–137	21.5	11.85	105	–29.6	.033	34	.50	–41
1.0	.69	–165	16.0	6.34	85	–27.2	.044	29	.40	–44
1.5	.68	–179	12.7	4.33	72	–27.4	.043	37	.38	–48
2.0	.69	169	10.3	3.26	62	–25.6	.052	42	.37	–54
2.5	.69	164	8.5	2.64	56	–25.4	.054	46	.37	–55
3.0	.70	157	6.9	2.22	48	–23.8	.065	52	.39	–63
3.5	.70	151	5.6	1.91	39	–22.4	.076	51	.41	–71
4.0	.69	144	4.5	1.68	30	–21.4	.085	55	.43	–77
4.5	.68	137	3.5	1.50	22	–20.4	.096	49	.46	–83
5.0	.68	128	2.7	1.37	14	–19.4	.107	50	.48	–87
5.5	.68	117	2.0	1.26	5	–18.3	.121	45	.48	–91
6.0	.70	107	1.2	1.15	–3	–17.6	.132	44	.48	–98

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 35$ mA

0.1	.52	–95	33.4	46.52	139	–40.0	.010	50	.77	–29
0.5	.66	–163	23.1	14.33	95	–34.4	.019	46	.34	–42
1.0	.67	179	17.3	7.36	80	–29.6	.033	51	.28	–41
1.5	.67	169	13.9	4.97	69	–28.0	.040	59	.27	–44
2.0	.68	160	11.4	3.74	60	–27.3	.053	59	.27	–51
2.5	.69	157	9.6	3.04	55	–23.8	.065	65	.28	–53
3.0	.69	151	8.1	2.55	47	–22.8	.072	65	.28	–62
3.5	.69	145	6.8	2.20	39	–21.4	.086	59	.30	–72
4.0	.68	139	5.7	1.93	20	–20.2	.097	60	.33	–80
4.5	.67	132	4.7	1.74	22	–19.3	.109	54	.36	–85
5.0	.67	123	4.0	1.59	13	–18.0	.126	50	.38	–90
5.5	.67	113	3.2	1.46	5	–17.2	.138	46	.39	–94
6.0	.69	103	2.5	1.34	–4	–16.4	.152	40	.38	–102

A model for this device is available in the DEVICE MODELS section.

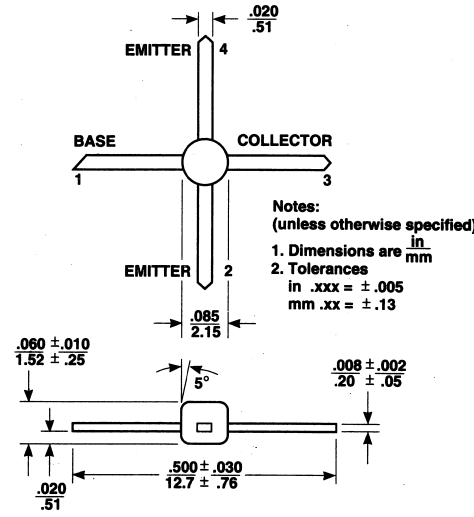
HEWLETT PACKARD

AT-42085
Up to 6 GHz Medium Power Silicon Bipolar Transistor

Features

- **High Output Power:**
  20.5 dBm typical $P_{1\,dB}$ at 2.0 GHz
- **High Gain at 1 dB Compression:**
  14.0 dB typical $G_{1\,dB}$ at 2.0 GHz
- **Low Noise Figure:**
  1.9 dB typical NF_O at 2.0 GHz
- **High Gain-Bandwidth Product:**
  8.0 GHz typical f_T
- **Low Cost Plastic Package**

85 Plastic Package



Description

The AT-42085 is a high performance NPN silicon bipolar transistor housed in a low cost plastic package. This device is designed for use in medium power, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
0.1	1.1	.05	16	0.13
0.5	1.2	.06	77	0.13
1.0	1.3	.10	131	0.12
2.0	2.0	.24	–179	0.11
4.0	3.5	.46	–128	0.25

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 35 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB	16.0	17.0 11.0 5.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f = 4.0 GHz	dBm		20.5 20.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f = 4.0 GHz	dB		14.0 9.5	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz f = 4.0 GHz	dB		1.9 3.5	
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz f = 4.0 GHz	dB		13.5 9.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 35 mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8V, I_C = 35 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		μA			2.0
C_{CB}	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		0.32	

Note: 1. For this test the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	80 mA
Power Dissipation[2,3]	P_T	500 mW
Junction Temperature	T_j	150°C
Storage Temperature	T_{STG}	–65°C to 150°C

Thermal Resistance[2,4]: θ_{jc} = 130°C/W

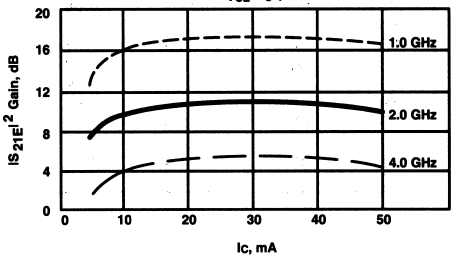
Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 7.7 mW/°C for T_C > 85°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

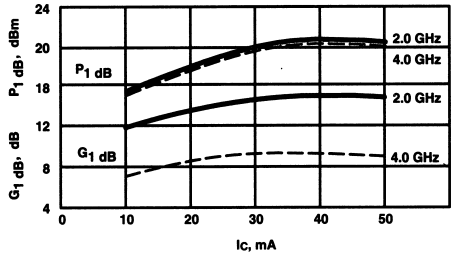
Typical Performance, T_A = 25°C

(unless otherwise noted)

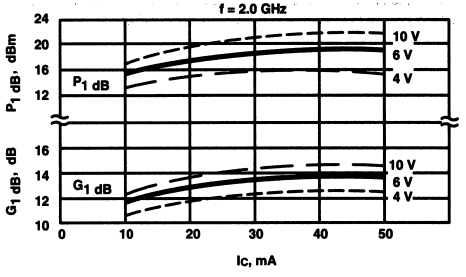
INSERTION POWER GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



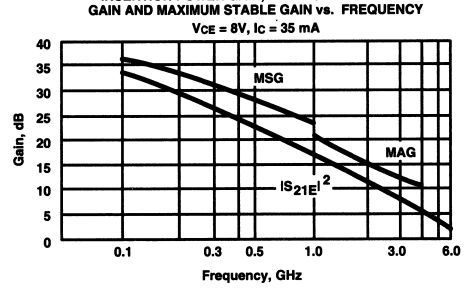
OUTPUT POWER AND 1 dB COMPRESSED GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



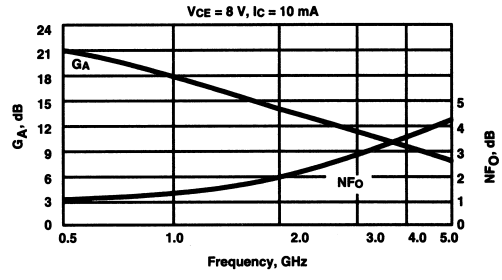
OUTPUT POWER AND 1 dB COMPRESSED GAIN
vs. COLLECTOR CURRENT AND VOLTAGE
f = 2.0 GHz



INSERTION POWER GAIN, MAXIMUM AVAILABLE
GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{CE} = 8V, I_C = 35 mA



NOISE FIGURE AND ASSOCIATED GAIN
vs. FREQUENCY
V_{CE} = 8 V, I_C = 10 mA



Typical Scattering Parameters: Common Emitter, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 10$ mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.72	–50	28.5	26.52	152	–37.0	.014	73	.90	–16
0.5	.66	–139	21.0	11.23	103	–29.2	.035	36	.53	–32
1.0	.65	–168	15.5	5.96	84	–28.6	.037	39	.45	–33
1.5	.65	175	12.2	4.06	71	–27.0	.045	46	.43	–36
2.0	.65	163	9.7	3.06	60	–25.3	.054	51	.42	–41
2.5	.66	157	8.0	2.51	55	–24.0	.063	60	.42	–42
3.0	.68	149	6.3	2.07	46	–22.8	.072	65	.41	–48
3.5	.68	141	5.1	1.79	38	–21.4	.085	64	.43	–55
4.0	.69	133	3.9	1.57	29	–19.7	.104	64	.45	–61
4.5	.69	125	3.0	1.41	21	–18.5	.119	63	.46	–66
5.0	.69	114	2.2	1.28	12	–17.1	.139	58	.47	–71
5.5	.71	103	1.4	1.17	3	–15.9	.161	55	.44	–76
6.0	.75	91	0.6	1.07	–6	–15.1	.177	49	.40	–85

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 35$ mA

0.1	.54	–90	33.1	45.38	137	–40.1	.010	66	.76	–26
0.5	.61	–163	22.6	13.45	95	–32.8	.023	52	.38	–30
1.0	.61	178	16.8	6.90	79	–29.5	.034	61	.34	–28
1.5	.62	167	13.4	4.67	68	–26.4	.048	68	.32	–31
2.0	.63	156	10.9	3.52	59	–23.9	.064	66	.31	–36
2.5	.64	152	9.2	2.89	54	–22.5	.075	68	.31	–40
3.0	.66	146	7.6	2.39	45	–21.2	.088	69	.30	–48
3.5	.67	139	6.3	2.07	37	–19.8	.102	67	.31	–58
4.0	.68	131	5.2	1.81	28	–18.6	.117	65	.33	–67
4.5	.68	123	4.2	1.62	19	–17.2	.138	60	.35	–73
5.0	.68	114	3.4	1.48	10	–16.4	.152	56	.35	–79
5.5	.71	103	2.5	1.34	1	–15.3	.171	50	.34	–85
6.0	.74	93	1.7	1.21	–8	–14.5	.188	46	.31	–96

A model for this device is available in the DEVICE MODELS section.

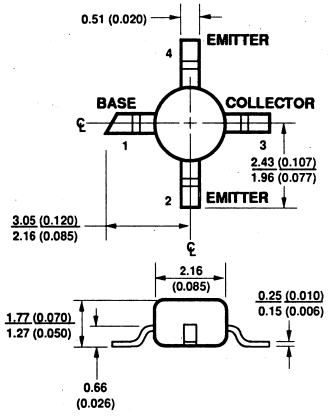
HEWLETT PACKARD

AT-42086
Up to 6 GHz Medium Power Silicon Bipolar Transistor

Features

- **High Output Power:**
  20.5 dBm typical $P_{1\,dB}$ at 2.0 GHz
- **High Gain at 1 dB Compression:**
  13.5 dB typical $G_{1\,dB}$ at 2.0 GHz
- **Low Noise Figure:**
  1.9 dB typical NF_O at 2.0 GHz
- **High Gain-Bandwidth Product:**
  8.0 GHz typical f_T
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

86 Plastic Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Description

The AT-42086 is a high performance NPN silicon bipolar transistor housed in a low cost, surface mount plastic package. This device is designed for use in medium power, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of these devices.

Noise Parameters: V_{CE} = 8 V, I_C = 10 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
0.1	1.0	.04	8	0.13
0.5	1.1	.03	62	0.12
1.0	1.5	.06	168	0.12
2.0	1.9	.25	–146	0.12
4.0	3.5	.58	–100	0.52

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 35 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB	15.0	16.5 10.5 4.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f = 4.0 GHz	dBm		20.5 20.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 35 mA	f = 2.0 GHz f = 4.0 GHz	dB		13.5 9.0	
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz f = 4.0 GHz	dB		1.9 3.5	
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz f = 4.0 GHz	dB		13.0 9.0	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 35 mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 35 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		μA			2.0
C_{CB}	Collector Base Capacitance[2]: V_{CB} = 8 V, f = 1 MHz		pF		0.32	

Notes: 1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices."
2. For this test, the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	80 mA
Power Dissipation[2,3]	P_T	500 mW
Junction Temperature	T_j	150°C
Storage Temperature	T_{STG}	–65°C to 150°C

Thermal Resistance[2,4]: θ_{jc} = 140°C/W

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 7.1 mW/°C for T_C > 80°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Part Number Ordering Information

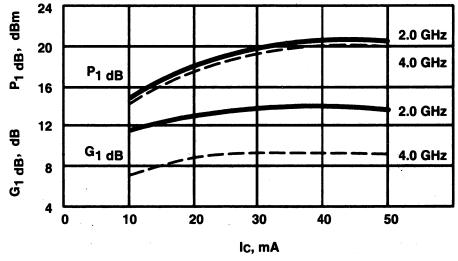
Part Number	Devices Per Reel	Reel Size
AT-42086-TR1	1000	7"
AT-42086-TR2	4000	13"

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

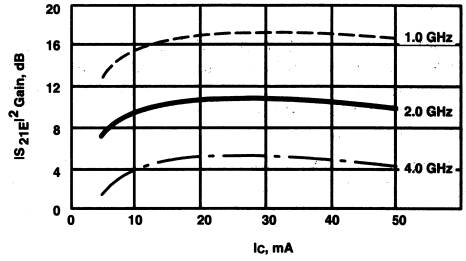
Typical Performance, T_A = 25°C

(unless otherwise noted)

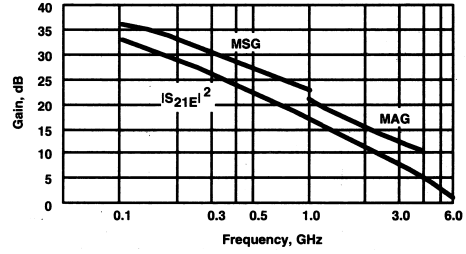
OUTPUT POWER AND 1 dB COMPRESSED GAIN vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



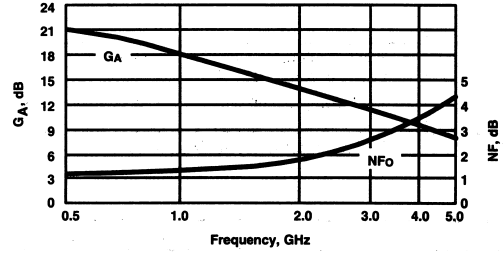
INSERTION POWER GAIN vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{CE} = 8 V, I_C = 35 mA



NOISE FIGURE AND ASSOCIATED GAIN vs. FREQUENCY
V_{CE} = 8 V, I_C = 10 mA



Typical Scattering Parameters: Common Emitter, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 10$ mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.68	–48	28.0	25.12	153	–36.0	.016	65	.91	–15
0.5	.63	–141	20.9	11.07	102	–29.9	.032	42	.54	–30
1.0	.63	–176	15.4	5.87	80	–27.4	.043	43	.43	–30
1.5	.65	164	12.0	3.98	65	–26.0	.050	46	.40	–34
2.0	.66	151	9.5	2.99	53	–23.9	.064	52	.38	–40
2.5	.69	142	7.8	2.44	45	–23.1	.070	53	.36	–46
3.0	.71	132	6.2	2.04	34	–21.6	.084	54	.34	–54
3.5	.73	123	4.8	1.74	24	–19.7	.104	53	.33	–67
4.0	.75	115	3.6	1.51	14	–18.3	.122	51	.30	–80
4.5	.78	108	2.6	1.34	5	–17.2	.138	50	.31	–94
5.0	.80	101	1.6	1.20	–4	–16.0	.159	46	.31	–110
5.5	.82	95	0.6	1.08	–12	–14.8	.182	40	.32	–129
6.0	.85	89	–0.2	0.97	–21	–14.0	.200	35	.34	–148

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 35$ mA

0.1	.48	–94	32.8	43.62	137	–37.7	.013	65	.77	–25
0.5	.57	–168	22.4	13.21	92	–32.6	.023	57	.39	–28
1.0	.59	168	16.5	6.69	75	–28.7	.037	62	.33	–27
1.5	.61	154	13.0	4.48	62	–24.8	.057	64	.31	–31
2.0	.63	143	10.5	3.36	51	–23.0	.071	61	.29	–37
2.5	.68	137	8.7	2.72	43	–21.0	.089	56	.26	–45
3.0	.68	127	7.0	2.25	33	–19.7	.104	58	.25	–53
3.5	.71	118	5.7	1.92	24	–18.4	.121	55	.24	–65
4.0	.73	111	4.5	1.69	14	–17.3	.136	49	.20	–80
4.5	.76	104	3.5	1.49	5	–15.9	.161	46	.21	–95
5.0	.78	98	2.4	1.32	–3	–15.2	.174	43	.21	–115
5.5	.81	91	1.6	1.20	–12	–14.3	.193	36	.22	–136
6.0	.84	85	0.7	1.08	–20	–13.4	.213	31	.25	–156

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

AT-60100
Up to 6 GHz Low Noise Silicon Bipolar Transistor Chip

Features

- **Low Bias Current Operation**
- **Low Noise Figure: 1.9 dB typical at 2.0 GHz**
  3.0 dB typical at 4.0 GHz
- **High Associated Gain: 8.0 dB typical at 2.0 GHz**
  5.0 dB typical at 4.0 GHz
- **High Gain-Bandwidth Product: 9.0 GHz typical f_T**

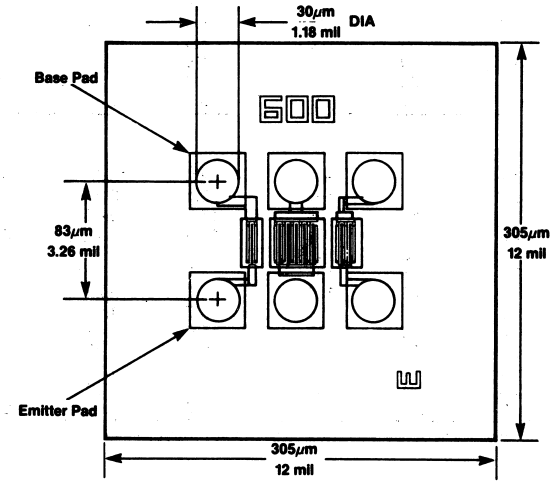
Description

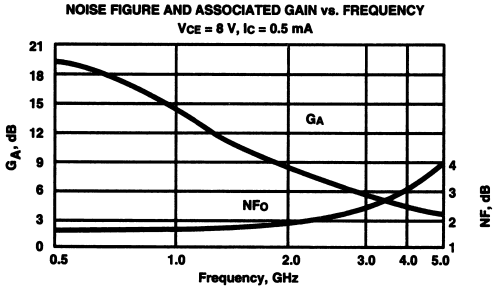
The AT-60100 is a high performance NPN silicon bipolar transistor chip designed for use in low noise, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

The die are nitride-passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self alignment techniques, and gold metallization in the fabrication of these devices.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire. See also "Chip Use" in the APPLICATIONS section.

Chip Outline[1]





Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions[1,2]		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 0.5 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		1.6 1.9 3.0	
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 0.5 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		14.5 8.0 5.0	
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 3 mA	f = 2.0 GHz f = 4.0 GHz	dB		9.0 4.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 3 mA	f = 2.0 GHz	dBm		4.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 3 mA	f = 2.0 GHz	dB		12.0	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 3 mA		GHz		9.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 3 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		μA			1.0
C_{CB}	Collector Base Capacitance[3]: V_{CB} = 8 V, f = 1 MHz		pF		0.07	

Notes: 1. This chip contains 3 active devices. The performance specified applies only to the device whose base and emitter pads are indicated on the chip outline.
2. RF performance is determined by packaging and testing 10 devices per wafer.
3. For this test, the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	8 mA
Power Dissipation[2,3]	P_T	80 mW
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 190°C/W

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. $T_{MOUNTING\ SURFACE}$ = 25°C.
3. Derate at 5.3 mW/°C for $T_{MOUNTING\ SURFACE}$ > 185°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

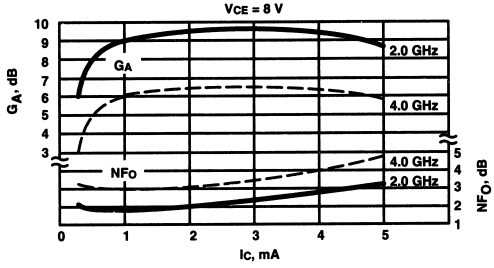
Part Number Ordering Information

Part Number	Devices Per Tray
AT-60100-GP2	10
AT-60100-GP4	100
AT-60100-GP6	up to 300

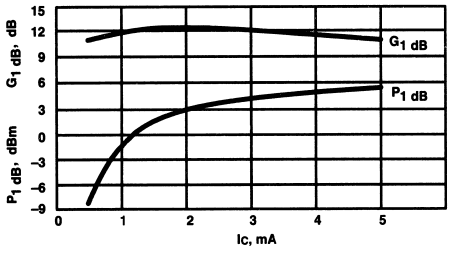
Typical Performance, T_A = 25°C

(unless otherwise noted)

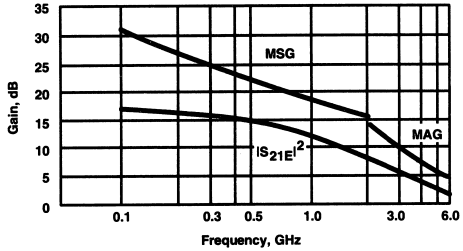
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



OUTPUT POWER AND 1 dB COMPRESSED GAIN
vs. COLLECTOR CURRENT
V_{CE} = 8 V, f = 2.0 GHz



INSERTION POWER GAIN, MAXIMUM AVAILABLE
GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{CE} = 8V, I_C = 3 mA



Typical Scattering Parameters: Common Emitter, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 0.5$ mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.99	2	4.2	1.63	−179	−43.1	.007	88	.99	−7
0.5	.98	−9	3.5	1.49	165	−29.9	.032	86	.99	−5
1.0	.92	−17	1.7	1.22	148	−24.4	.060	78	.99	−6
1.5	.90	−30	1.1	1.14	134	−21.2	.087	70	.96	−9
2.0	.76	−37	1.4	1.18	122	−19.6	.105	67	.92	−13
2.5	.70	−38	0.7	1.08	113	−18.2	.123	66	.91	−15
3.0	.61	−46	0.4	1.05	102	−17.1	.139	63	.88	−17
3.5	.52	−49	−0.5	0.95	94	−16.8	.145	61	.86	−20
4.0	.50	−60	−1.1	0.88	87	−16.4	.151	62	.86	−21
5.0	.50	−45	−2.2	0.78	80	−13.9	.202	62	.85	−26

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 3$ mA

0.1	.98	−2	17.4	7.43	176	−44.4	.006	83	.95	−7
0.5	.83	−26	15.3	5.81	145	−31.0	.028	78	.95	−9
1.0	.63	−44	12.5	4.23	124	−26.4	.048	70	.89	−10
1.5	.47	−57	10.6	3.38	114	−24.3	.061	68	.84	−11
2.0	.35	−61	8.9	2.77	98	−22.6	.074	67	.81	−13
2.5	.29	−61	7.4	2.33	91	−21.0	.089	69	.79	−14
3.0	.21	−68	6.2	2.03	83	−19.9	.101	69	.78	−15
3.5	.18	−68	4.9	1.76	79	−19.1	.111	70	.77	−18
4.0	.14	−80	4.0	1.59	75	−18.3	.122	73	.78	−19
5.0	.10	−63	2.4	1.31	67	−16.5	.150	71	.78	−25

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

Surface Mount, Low Current Silicon Bipolar Transistor

Technical Data

AT-60111
AT-60211

Features

- **Low Current Operation**
  AT-60111: 0.4 mA at 3 V
  AT-60211: 0.8 mA at 3 V
- **Low Noise Figure**
  AT-60111: 1.4 dB at 1 GHz
  AT-60211: 1.5 dB at 1 GHz
- **High Associated Gain**
  AT-60111: 10.5 dB at 1 GHz
  AT-60211: 12.5 dB at 1 GHz
- **Low Cost Surface Mount Plastic Package**
- **Tape and Reel Option Available**

Description

The AT-60111 and AT-60211 are low current, low cost NPN silicon bipolar transistors mounted in the surface mount plastic SOT-143 package. These devices are designed for use in gain stages, low noise amplifiers, or oscillators operating in the VHF, UHF, and microwave frequencies, and are ideally suited for battery powered applications.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

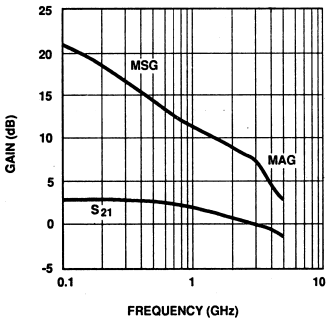


Figure 1. AT-60111 Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency, V_{CE} = 3 V, I_C = 0.4 mA.

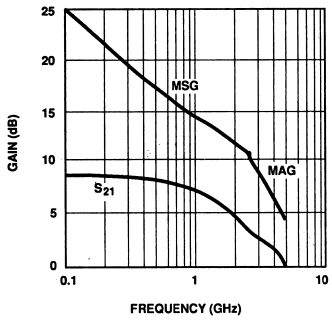
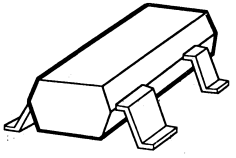
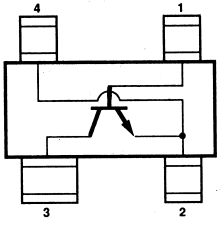


Figure 2. AT-60211 Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency, V_{CE} = 3 V, I_C = 0.8 mA.

Plastic SOT-143 Package



Pin Configuration



Pin Description
1 Base
2 Emitter
3 Collector
4 Emitter

Absolute Maximum Ratings[1] (T_A = 25°C)

Symbol	Parameter	Units	AT-60111	AT-60211
V_{EBO}	Emitter-Base Voltage	V	1.5	1.5
V_{CBO}	Collector-Base Voltage	V	20	20
V_{CEO}	Collector-Emitter Voltage	V	12	12
I_C	Collector Current	mA	8	16
P_T	Power Dissipation	mW	80[3]	160[4]
T_j	Junction Temperature	°C	150	150
T_{stg}	Storage Temperature	°C	-65 to +150	-65 to +150
Θ_{jc}	Thermal Resistance Junction to Case[2]	°C/W	645	610

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. T_j = 150°C.
3. Derate at 1.55 mW/°C for T_{CASE} > 98°C.
4. Derate at 1.64 mW/°C for T_{CASE} > 102°C.

Electrical Specifications, T_A = 25 °C

Symbol	Parameter	Units	AT-60111			AT-60211		
			Min.	Typ.	Max.	Min.	Typ.	Max.
NF_O	Optimum Noise Figure	dB						
	AT-60111: V_{CE} = 3 V, I_C = 0.4 mA f = 1 GHz			1.4				
	AT-60211: V_{CE} = 3 V, I_C = 0.8 mA f = 1 GHz						1.5	
G_A	Gain at NF_O	dB						
	AT-60111: V_{CE} = 3 V, I_C = 0.4 mA f = 1 GHz			10.5				
	AT-60211: V_{CE} = 3 V, I_C = 0.8 mA f = 1 GHz						12.5	
MSG	Maximum Stable Gain	dB						
	AT-60111: V_{CE} = 3 V, I_C = 0.4 mA f = 1 GHz			11.5				
	f = 2 GHz			9.0				
	AT-60211: V_{CE} = 3 V, I_C = 0.8 mA f = 1 GHz						14.5	
	f = 2 GHz						11.5	
S_{21}	Insertion Power Gain	dB						
	AT-60111: V_{CE} = 6 V, I_C = 2.5 mA f = 1 GHz		9.5	11.5				
	f = 2 GHz			7.0				
	AT-60211: V_{CE} = 6 V, I_C = 5.0 mA f = 1 GHz					12.5	14.0	
	f = 2 GHz						9.0	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	dBm						
	AT-60111: V_{CE} = 6 V, I_C = 2.5 mA f = 1 GHz			4.0				
	AT-60211: V_{CE} = 6 V, I_C = 5.0 mA f = 1 GHz						7.5	
$G_{1\,dB}$	1 dB Compressed Gain	dB						
	AT-60111: V_{CE} = 6 V, I_C = 2.5 mA f = 1 GHz			14.0				
	AT-60211: V_{CE} = 6 V, I_C = 5.0 mA f = 1 GHz						18	
f_T	Gain Bandwidth Product	GHz						
	AT-60111: V_{CE} = 6 V, I_C = 2.5 mA			5				
	AT-60211: V_{CE} = 6 V, I_C = 5.0 mA						6	
h_{fe}	Forward Current Transfer Ratio							
	AT-60111: V_{CE} = 6 V, I_C = 2.5 mA		30	150	300			
	AT-60211: V_{CE} = 6 V, I_C = 5.0 mA					30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 6 V	μA			0.2			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V	μA			1.0			1.0

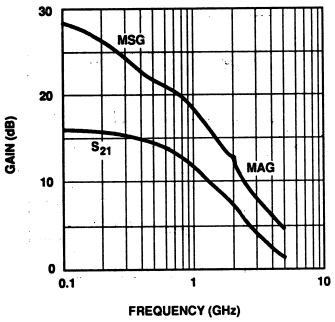


Figure 3. AT-60111 Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency, V_{CE} = 6 V, I_C = 2.5 mA.

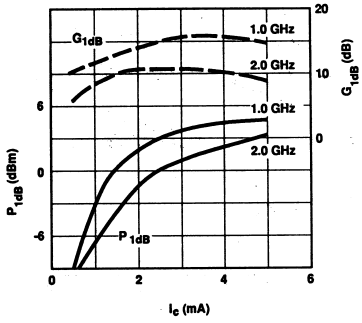


Figure 4. AT-60111 Typical Output Power and 1 dB Compressed Gain vs. Collector Current, V_{CE} = 6 V, f = 1 GHz.

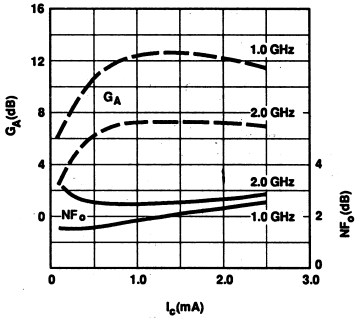


Figure 5. AT-60111 Typical Optimum Noise Figure and Associated Gain vs. Collector Current and Frequency, V_{CE} = 3 V.

AT-60111 Typical S-Parameters (V_{CE} = 3 V, I_C = 0.4 mA)

Freq. (MHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	.99	-3	2.78	1.38	176	-39.4	.011	85	.99	-3
200	.98	-6	2.81	1.38	171	-34.1	.020	90	.99	-5
500	.97	-15	2.64	1.35	159	-26.8	.046	75	.99	-12
1000	.91	-28	1.92	1.25	140	-21.2	.087	64	.96	-22
1500	.85	-38	1.26	1.16	124	-19.1	.111	58	.93	-29
2000	.78	-45	0.92	1.11	111	-17.3	.137	52	.90	-35
2500	.71	-51	0.40	1.05	101	-15.9	.160	48	.88	-38
3000	.62	-59	0.13	1.01	88	-14.7	.183	41	.85	-44
3500	.53	-68	-0.00	1.00	76	-14.3	.192	37	.81	-51
4000	.45	-79	-0.33	0.96	64	-13.6	.209	30	.79	-57
4500	.37	-90	-0.73	0.92	52	-13.3	.217	25	.77	-64
5000	.32	-102	-1.25	0.87	42	-13.1	.221	20	.77	-70

AT-60111 Typical S-Parameters (V_{CE} = 6 V, I_C = 2.5 mA)

Freq. (MHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	.93	-8	16.10	6.39	171	-40.1	.010	80	.99	-4
200	.90	-15	15.83	6.19	162	-36.2	.015	72	.98	-8
500	.79	-33	14.59	5.36	138	-29.2	.035	67	.92	-17
1000	.58	-50	11.71	3.85	111	-25.1	.055	56	.84	-26
1500	.44	-58	9.26	2.90	94	-22.7	.074	57	.80	-32
2000	.34	-60	7.23	2.30	81	-20.9	.090	55	.78	-35
2500	.27	-58	5.71	1.93	73	-20.1	.099	55	.76	-37
3000	.21	-55	4.50	1.68	64	-18.9	.114	54	.75	-40
3500	.15	-52	3.60	1.52	53	-17.7	.131	51	.74	-46
4000	.10	-49	2.64	1.35	45	-16.6	.148	47	.73	-52
4500	.07	-33	1.86	1.24	37	-15.7	.164	45	.72	-59
5000	.06	-11	1.03	1.13	28	-15.0	.178	42	.71	-66

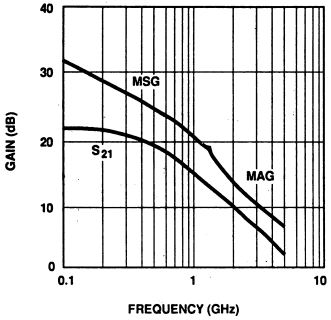


Figure 6. AT-60211 Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency, V_{CE} = 6 V, I_C = 5.0 mA.

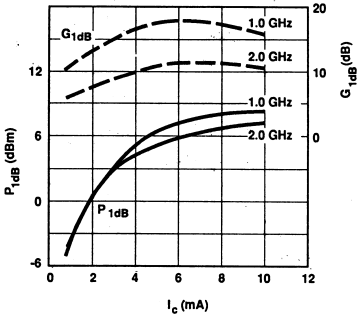


Figure 7. AT-60211 Typical Output Power and 1 dB Compressed Gain vs. Collector Current, V_{CE} = 6 V, f = 1 GHz.

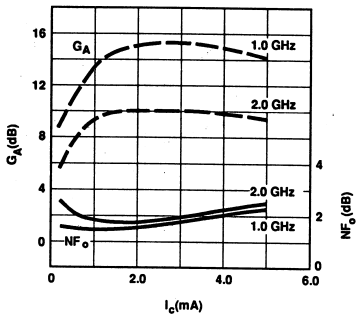


Figure 8. AT-60211 Typical Optimum Noise Figure and Associated Gain vs. Collector Current and Frequency, V_{CE} = 3 V.

AT-60211 Typical S-Parameters (V_{CE}= 3 V, I_C = 0.8 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
(MHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	.98	-5	8.63	2.70	175	-40.9	.009	93	.99	-4
200	.97	-9	8.52	2.67	170	-34.4	.019	87	.99	-7
500	.93	-22	8.21	2.57	154	-26.2	.049	70	.97	-17
1000	.82	-42	7.08	2.26	131	-21.7	.082	57	.91	-30
1500	.73	-59	5.79	1.95	112	-19.4	.107	46	.86	-40
2000	.64	-72	4.67	1.71	98	-19.1	.111	38	.81	-46
2500	.57	-80	3.58	1.51	87	-18.2	.123	37	.79	-50
3000	.50	-88	2.80	1.38	76	-17.8	.129	34	.77	-57
3500	.41	-95	2.29	1.30	65	-17.7	.131	34	.75	-65
4000	.32	-107	1.68	1.21	53	-17.2	.138	31	.74	-75
4500	.24	-128	0.97	1.12	42	-17.0	.141	30	.73	-83
5000	.21	-160	0.18	1.02	32	-16.8	.144	31	.73	-90

AT-60211 Typical S-Parameters (V_{CE}= 6 V, I_C = 5.0 mA)

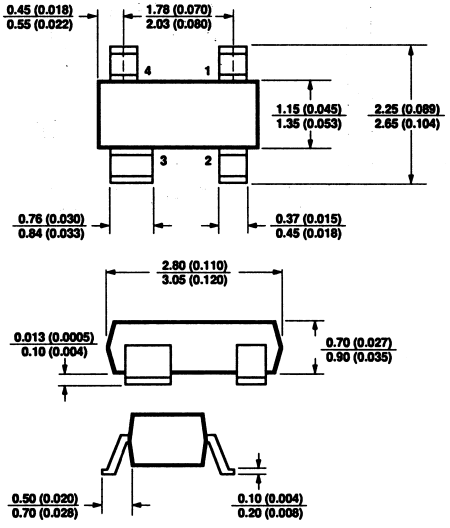
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
(MHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	.87	-14	21.65	12.09	168	-41.9	.008	80	.98	-5
200	.82	-26	21.15	11.41	156	-35.8	.016	80	.95	-10
500	.64	-56	18.96	8.87	128	-29.7	.033	59	.85	-19
1000	.41	-87	15.01	5.63	102	-26.6	.047	54	.76	-25
1500	.28	-105	12.13	4.04	86	-25.1	.056	54	.73	-29
2000	.19	-123	9.91	3.13	75	-23.0	.070	56	.71	-32
2500	.14	-147	8.24	2.58	68	-21.9	.080	60	.71	-33
3000	.12	174	6.84	2.20	59	-20.7	.093	58	.69	-36
3500	.15	145	5.66	1.92	50	-19.7	.104	58	.69	-42
4000	.19	129	4.61	1.70	41	-18.8	.115	56	.68	-49
4500	.23	118	3.58	1.51	33	-17.6	.132	53	.68	-55
5000	.26	109	2.71	1.37	25	-16.9	.142	53	.68	-62

Part Number Ordering Information

Part Number	Devices Per Reel	Reel Size
AT-60111-TR1	3000	7"
AT-60111-TR2	10000	13"
AT-60211-TR1	3000	7"
AT-60211-TR2	10000	13"

Package Dimensions

SOT-143 Plastic Package



DIMENSIONS ARE IN MM (INCHES).

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

HEWLETT PACKARD

AT-60200
Up to 6 GHz Low Noise Silicon Bipolar Transistor Chip

Features

- **Low Bias Current Operation**
- **Low Noise Figure: 1.9 dB typical at 2.0 GHz**
  3.0 dB typical at 4.0 GHz
- **High Associated Gain: 10.0 dB typical at 2.0 GHz**
  6.5 dB typical at 4.0 GHz
- **High Gain-Bandwidth Product: 9.0 GHz typical f_T**

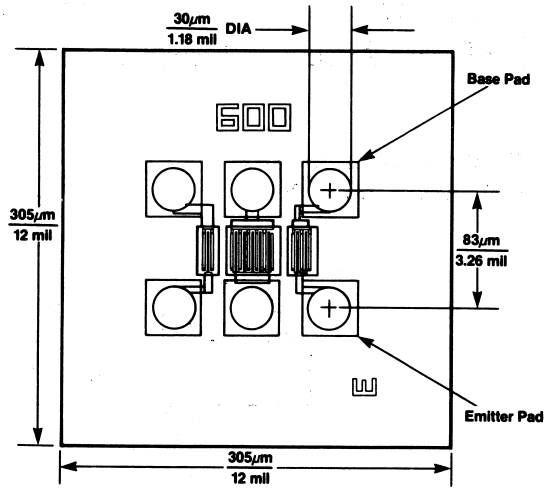
Description

The AT-60200 is a high performance NPN silicon bipolar transistor chip designed for use in low noise, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

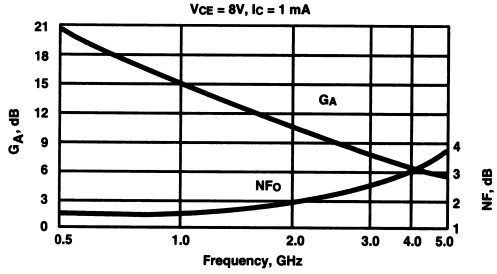
The die are nitride-passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self alignment techniques, and gold metallization in the fabrication of these devices.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire. See also "Chip Use" in the APPLICATIONS section.

Chip Outline[1]



NOISE FIGURE AND ASSOCIATED GAIN vs. FREQUENCY
V_{CE} = 8V, I_C = 1 mA



Electrical Specifications, T_A = 25°C

Symbol	Parameter and Test Conditions[1,2]		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 1 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		1.4 1.9 3.0	
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 1 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		15.0 10.0 6.5	
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 5 mA	f = 2.0 GHz f = 4.0 GHz	dB		11.0 5.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 5 mA	f = 2.0 GHz	dBm		6.5	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 5 mA	f = 2.0 GHz	dB		13.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 5 mA		GHz		9.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 5 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		μA			1.0
C_{CB}	Collector Base Capacitance[3]: V_{CB} = 8 V, f = 1 MHz		pF		0.08	

Notes: 1. This chip contains 3 active devices. The performance specified applies only to the device whose base and emitter pads are indicated on the chip outline.
2. RF performance is determined by packaging and testing 10 devices per wafer.
3. For this test, the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	16 mA
Power Dissipation[2,3]	P_T	160 mW
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 155°C/W

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. $T_{MOUNTING\ SURFACE}$ = 25°C.
3. Derate at 6.5 mW/°C for $T_{MOUNTING\ SURFACE}$ > 175°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Part Number Ordering Information

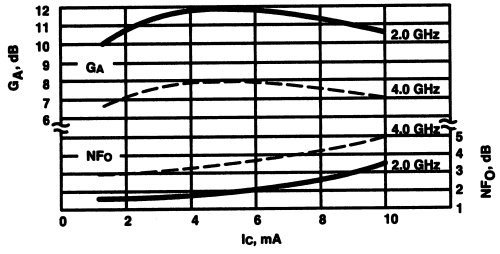
Part Number	Devices Per Tray
AT-60200-GP2	10
AT-60200-GP4	100
AT-60200-GP6	up to 300

Typical Performance, T_A = 25°C

(unless otherwise noted)

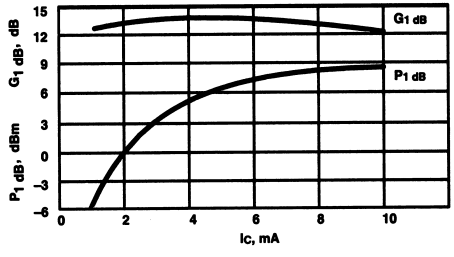
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN vs. COLLECTOR CURRENT AND FREQUENCY

V_{CE} = 8 V



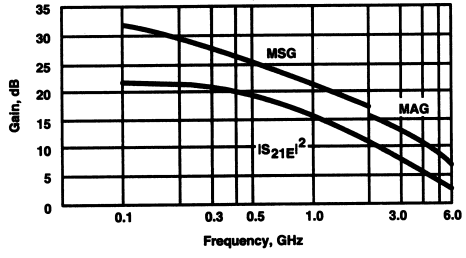
OUTPUT POWER AND 1 dB COMPRESSED GAIN vs. COLLECTOR CURRENT

V_{CE} = 8 V, f = 2.0 GHz



INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY

V_{CE} = 8 V, I_C = 5 mA



Typical Scattering Parameters: Common Emitter, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 1$ mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.97	–8	16.9	7.00	172	–43.1	.007	87	.99	–3
0.5	.85	–32	15.8	6.13	147	–29.9	.032	73	.94	–11
1.0	.66	–57	13.6	4.78	126	–25.2	.055	64	.87	–13
1.5	.52	–74	11.7	3.86	108	–23.4	.068	59	.79	–14
2.0	.41	–89	9.9	3.12	99	–22.2	.078	58	.75	–17
2.5	.34	–101	8.7	2.71	90	–20.8	.091	59	.74	–17
3.0	.29	–114	7.3	2.31	82	–20.0	.100	61	.72	–18
3.5	.25	–126	6.2	2.03	74	–19.3	.108	60	.71	–20
4.0	.23	–137	5.3	1.83	69	–18.4	.120	61	.71	–23
5.0	.20	–163	3.4	1.47	57	–17.5	.133	61	.72	–26

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 5$ mA

0.1	.87	–8	22.0	12.51	169	–50.5	.003	88	.92	–6
0.5	.70	–44	19.0	8.94	138	–31.4	.027	72	.90	–12
1.0	.48	–74	15.7	6.12	113	–27.7	.041	65	.81	–11
1.5	.32	–97	13.1	4.54	100	–26.0	.050	66	.76	–11
2.0	.24	–114	10.9	3.50	90	–24.4	.060	67	.73	–13
2.5	.19	–134	9.3	2.90	83	–23.0	.071	71	.73	–14
3.0	.15	–161	7.7	2.42	76	–21.7	.082	74	.73	–15
3.5	.11	–160	6.4	2.08	74	–20.5	.095	75	.73	–18
4.0	.15	178	5.4	1.87	70	–19.5	.106	80	.73	–18
5.0	.14	168	4.0	1.59	61	–17.4	.135	74	.72	–24

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

AT-60500
Up to 6 GHz Low Noise Silicon Bipolar Transistor Chip

Features

- **Low Bias Current Operation**
- **Low Noise Figure: 1.8 dB typical at 2.0 GHz**
  2.8 dB typical at 4.0 GHz
- **High Associated Gain: 12.5 dB typical at 2.0 GHz**
  8.0 dB typical at 4.0 GHz
- **High Gain-Bandwidth Product: 9.0 GHz typical f_T**

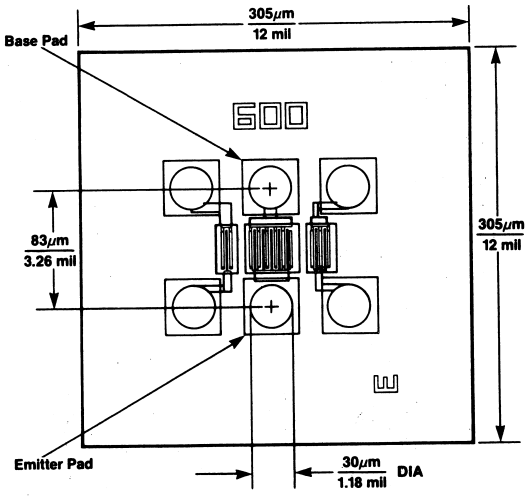
Description

The AT-60500 is a high performance NPN silicon bipolar transistor chip designed for use low noise, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

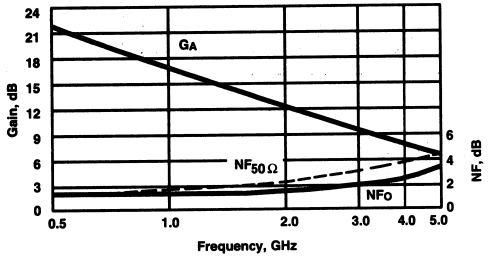
The die are nitride-passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implanation, self-alignment techniques, and gold metallization in the fabrication of these devices.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire. See also "Chip Use" in the APPLICATIONS section.

Chip Outline[1]



NOISE FIGURE AND ASSOCIATED GAIN vs. FREQUENCY
V_{CE} = 8 V, I_C = 2 mA



Noise Parameters: V_{CE} = 8 V, I_C = 2 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
1.0	1.4	.58	44	0.20
2.0	1.8	.48	90	0.24
4.0	2.8	.50	155	0.20

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions[1,2]		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 2 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		1.4 1.8 2.8	
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 2 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		16.5 12.5 8.0	
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz f = 4.0 GHz	dB		12.0 6.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz	dBm		16.0	
	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz	dB		12.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 10 mA		GHz		9.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 10 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		μA			1.0
C_{CB}	Collector Base Capacitance[3]: V_{CB} = 8 V, f = 1 MHz		pF		0.11	

Notes: 1. This chip contains 3 active devices. The performance specified applies only to the device whose base and emitter pads are indicated on the chip outline.
2. RF performance is determined by packaging and testing 10 devices per wafer.
3. For this test, the emitter is grounded.

AT-60500
Low Noise Silicon Bipolar Transistor

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	40 mA
Power Dissipation[2,3]	P_T	400 mW
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 120°C/W

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. $T_{MOUNTING\ SURFACE}$ = 25°C.
3. Derate at 8.3 mW/°C for $T_{MOUNTING\ SURFACE}$ > 152°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

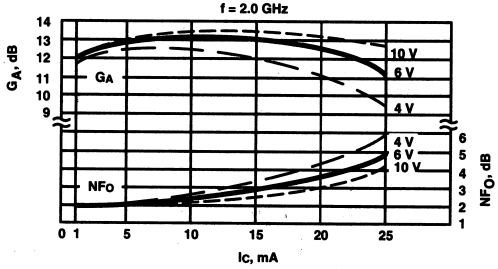
Part Number Ordering Information

Part Number	Devices Per Tray
AT-60500-GP2	10
AT-60600-GP4	100
AT-60500-GP6	up to 300

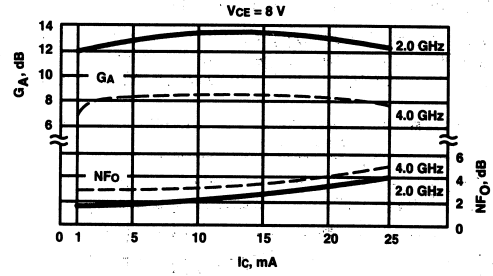
Typical Performance, T_A = 25°C

(unless otherwise noted)

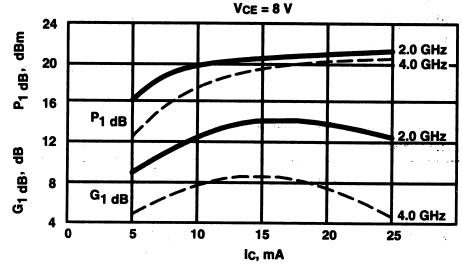
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN vs. COLLECTOR CURRENT AND COLLECTOR VOLTAGE
f = 2.0 GHz



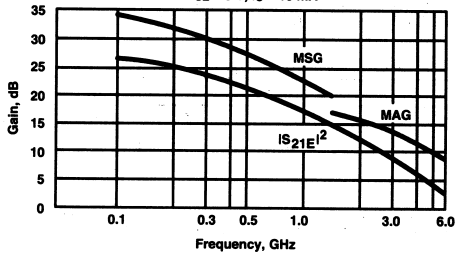
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN vs. COLLECTOR CURRENT AND FREQUENCY
VCE = 8 V



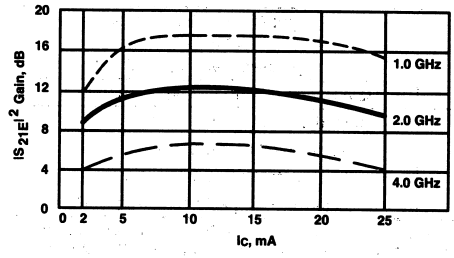
OUTPUT POWER AND 1 dB COMPRESSED GAIN vs. COLLECTOR CURRENT AND FREQUENCY
VCE = 8 V



INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
VCE = 8 V, Ic = 10 mA



INSERTION POWER GAIN vs. COLLECTOR CURRENT AND FREQUENCY
VCE = 8 V



Typical Scattering Parameters: Common Emitter, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 2$ mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.97	–6	16.7	6.86	176	–40.0	.010	85	.92	–7
0.5	.88	–34	14.3	5.17	149	–27.3	.043	71	.95	–13
1.0	.74	–72	12.0	4.00	127	–23.3	.068	55	.84	–16
1.5	.60	–101	10.2	3.22	112	–22.6	.074	48	.76	–19
2.0	.57	–123	9.0	2.83	97	–21.6	.083	43	.71	–22
2.5	.53	–140	7.7	2.43	88	–21.4	.085	45	.69	–23
3.0	.49	–158	6.5	2.11	79	–21.4	.085	50	.67	–24
3.5	.50	–167	5.3	1.85	73	–21.0	.089	51	.66	–26
4.0	.50	–176	4.2	1.63	68	–20.6	.093	56	.66	–28
4.5	.50	174	3.1	1.43	61	–20.5	.095	58	.67	–30
5.0	.50	166	2.3	1.30	56	–20.0	.100	64	.68	–32
5.5	.52	158	1.7	1.22	50	–19.4	.107	67	.67	–36
6.0	.50	148	0.8	1.10	45	–18.9	.114	70	.69	–39

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 10$ mA

0.1	.68	–21	26.9	22.02	166	–40.9	.009	80	.95	–7
0.5	.55	–93	22.5	13.27	123	–31.7	.026	60	.74	–20
1.0	.46	–137	17.8	7.73	101	–28.9	.036	58	.63	–17
1.5	.44	–160	14.7	5.41	90	–27.1	.044	65	.58	–16
2.0	.44	–173	12.2	4.05	82	–25.5	.053	68	.57	–17
2.5	.45	178	10.5	3.36	77	–23.9	.064	72	.57	–18
3.0	.45	169	9.1	2.84	71	–22.5	.075	76	.56	–20
3.5	.46	163	7.8	2.45	66	–21.4	.085	78	.56	–22
4.0	.46	157	6.7	2.16	63	–20.4	.096	81	.57	–24
4.5	.47	150	5.5	1.88	56	–19.5	.106	80	.58	–27
5.0	.47	144	4.7	1.72	53	–18.6	117	83	.59	–28
5.5	.50	140	4.0	1.58	48	–17.8	.129	83	.59	–32
6.0	.49	132	3.1	1.43	43	–17.1	.139	82	.61	–36

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

AT-60510
Up to 6 GHz Low Noise Silicon Bipolar Transistor

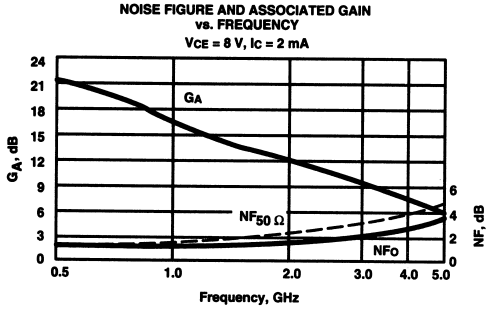
Features

- **Low Bias Current Operation:**
- **Low Noise Figure: 1.8 dB typical at 2.0 GHz**
  2.8 dB typical at 4.0 GHz
- **High Associated Gain: 12.0 dB typical at 2.0 GHz**
  7.5 dB typical at 4.0 GHz
- **High Gain-Bandwidth Product: 8.0 GHz typical f_T**
- **Hermetic Gold-ceramic Microstrip Package**

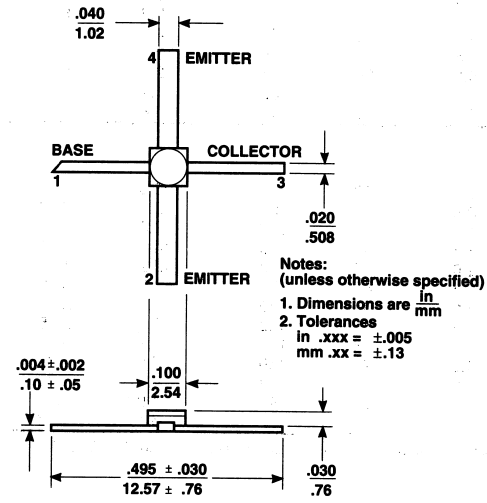
Description

The AT-60510 is a high performance NPN silicon bipolar transistor housed in a hermetic, high reliability package. This device is designed for use in low noise, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.



100 mil Package



Outline 10A

Noise Parameters: V_{CE} = 8 V, I_C = 2 mA

Freq. GHz	NFO dB	Gamma Opt Mag	Gamma Opt Ang	RN/50
1.0	1.4	.50	50	0.32
2.0	1.8	.44	97	0.42
4.0	2.8	.38	–163	0.42

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NFO	Optimum Noise Figure: VCE = 8 V, IC = 2 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		1.4 1.8 2.8	2.1
GA	Gain @ NFO: VCE = 8 V, IC = 2 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB	11.0	16.5 12.0 7.5	
$\|S_{21E}\|^2$	Insertion Power Gain: VCE = 8 V, IC = 10 mA	f = 2.0 GHz f = 4.0 GHz	dB		12.0 6.5	
P1 dB	Power Output @ 1 dB Gain Compression: VCE = 8 V, IC = 10 mA	f = 2.0 GHz	dBm		16.0	
G1 dB	1 dB Compressed Gain: VCE = 8 V, IC = 10 mA	f = 2.0 GHz	dB		11.5	
fT	Gain Bandwidth Product: VCE = 8 V, IC = 10 mA		GHz		8.0	
hFE	Forward Current Transfer Ratio: VCE = 8 V, IC = 10 mA			30	150	300
ICBO	Collector Cutoff Current: VCB = 8 V		µA			0.2
IEBO	Emitter Cutoff Current: VEB = 1 V		µA			1.0
CCB	Collector Base Capacitance[1]: VCB = 8 V, f = 1 MHz		pF		0.15	

Note: 1. For this test the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	40 mA
Power Dissipation[2,3]	P_T	400 mW
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 200°C/W

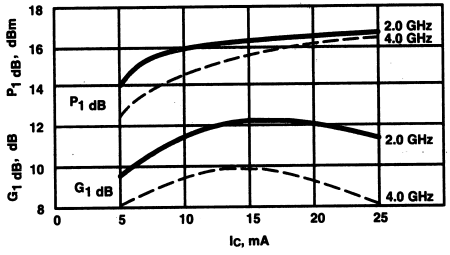
Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 5 mW/°C for T_C > 120°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

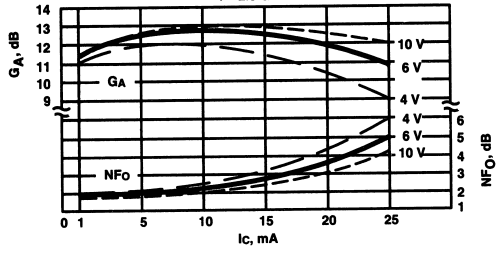
Typical Performance, T_A = 25°C

(unless otherwise noted)

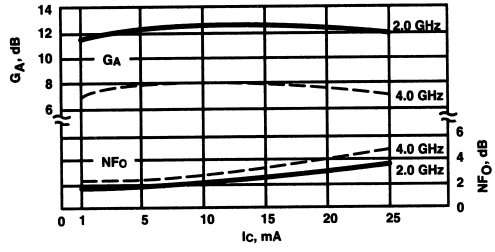
OUTPUT POWER AND 1 dB COMPRESSED GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8V



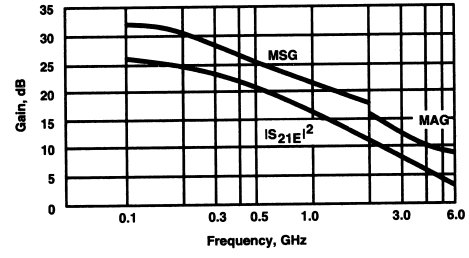
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN
vs. COLLECTOR CURRENT AND COLLECTOR VOLTAGE
f = 2.0 GHz



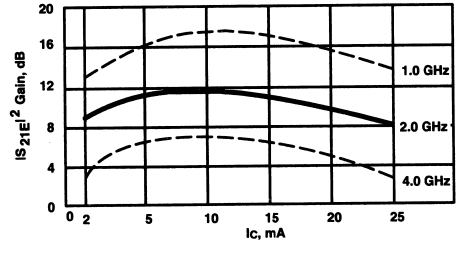
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



INSERTION POWER GAIN, MAXIMUM AVAILABLE
GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{CE} = 8 V, I_C = 10 mA



INSERTION POWER GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



Typical Scattering Parameters: Common Emitter, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 2$ mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.95	–10	15.9	6.25	171	–39.2	.011	91	.99	–4
0.5	.86	–47	14.8	5.46	141	–26.8	.046	61	.92	–19
1.0	.71	–82	12.4	4.16	112	–23.0	.071	43	.83	–31
1.5	.59	–108	10.3	3.26	92	–21.8	.082	33	.76	–38
2.0	.52	–131	8.4	2.63	76	–21.2	.088	26	.72	–44
2.5	.48	–146	7.0	2.25	66	–20.4	.095	27	.70	–45
3.0	.45	–162	5.8	1.94	54	–21.0	.089	24	.68	–50
3.5	.45	–178	4.6	1.71	42	–20.4	.096	21	.69	–56
4.0	.43	167	3.6	1.52	31	–20.0	.100	22	.70	–63
4.5	.42	152	2.8	1.38	20	–19.6	.105	20	.70	–68
5.0	.41	134	2.0	1.26	9	–19.1	.111	18	.70	–73
5.5	.43	116	1.4	1.17	0	–18.5	.119	16	.70	–77
6.0	.48	101	0.7	1.09	–10	–18.2	.123	16	.67	–83

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 10$ mA

0.1	.71	–26	26.6	21.30	162	–39.2	.011	75	.96	–9
0.5	.55	–100	22.1	12.77	116	–30.8	.029	50	.71	–27
1.0	.46	–141	17.3	7.36	90	–27.6	.042	43	.59	–31
1.5	.43	–165	14.1	5.11	76	–25.6	.052	48	.57	–35
2.0	.42	178	11.8	3.91	64	–24.2	.061	45	.55	–40
2.5	.43	168	10.1	3.21	57	–23.4	.068	54	.54	–41
3.0	.43	157	8.7	2.72	48	–21.8	.081	53	.54	–47
3.5	.44	145	7.5	2.37	37	–20.8	.092	50	.55	–55
4.0	.44	134	6.4	2.10	27	–19.8	.102	45	.56	–62
4.5	.43	121	5.5	1.88	17	–18.9	.114	42	.58	–69
5.0	.44	106	4.6	1.71	7	–18.2	.123	38	.59	–76
5.5	.47	92	3.8	1.56	–1	–17.5	.134	33	.59	–81
6.0	.52	81	3.1	1.42	–11	–16.8	.145	29	.57	–88

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

AT-60535
Up to 6 GHz Low Noise Silicon Bipolar Transistor

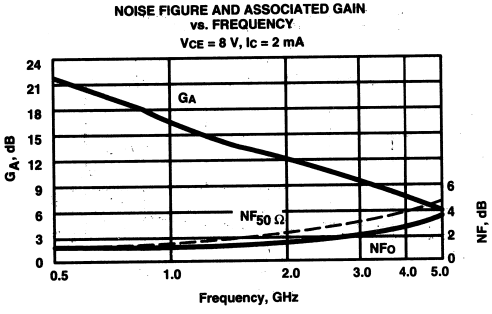
Features

- **Low Bias Current Operation:**
- **Low Noise Figure: 1.8 dB typical at 2.0 GHz**
  2.8 dB typical at 4.0 GHz
- **High Associated Gain: 12.0 dB typical at 2.0 GHz**
  7.5 dB typical at 4.0 GHz
- **High Gain-Bandwidth Product: 8.0 GHz typical f_T**
- **Cost Effective Ceramic Microstrip Package**

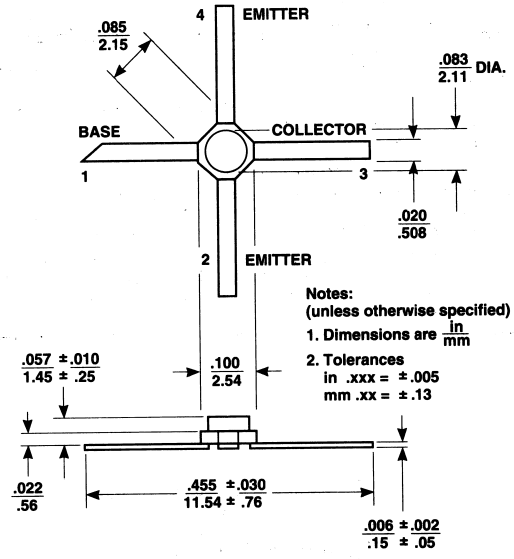
Description

The AT-60535 is a high performance NPN silicon bipolar transistor housed in a cost-effective, microstrip package. This device is designed for use in low noise, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.



35 micro-X Package



Noise Parameters: V_{CE} = 8 V, I_C = 2 mA

Freq. GHz	NFO dB	Gamma Opt Mag	Gamma Opt Ang	RN/50
1.0	1.4	.50	55	0.32
2.0	1.8	.40	114	0.38
4.0	2.8	.38	–153	0.40

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NFO	Optimum Noise Figure: V_{CE} = 8 V, I_C = 2 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		1.4 1.8 2.8	2.1
GA	Gain @ NFO: V_{CE} = 8 V, I_C = 2 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB	11.0	16.5 12.0 7.5	
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz f = 4.0 GHz	dB		11.5 6.0	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz	dBm		16.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz	dB		11.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 10 mA		GHz		8.0	
hFE	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 10 mA			30	150	300
ICBO	Collector Cutoff Current: V_{CB} = 8 V		µA			0.2
IEBO	Emitter Cutoff Current: V_{EB} = 1 V		µA			1.0
CCB	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		0.15	

Note: 1. For this test the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	40 mA
Power Dissipation[2,3]	P_T	400 mW
Junction Temperature	T_j	200°C
Storage Temperature[4]	T_{STG}	−65°C to 200°C
Thermal Resistance[2,5]:	θ_{jc} = 225°C/W	

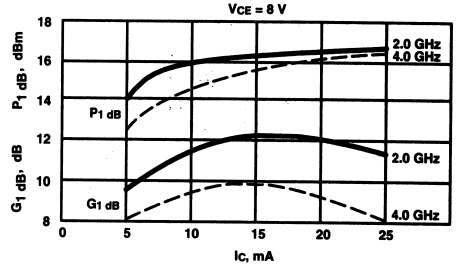
Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 4.4 mW/°C for T_C > 110°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safely stored up to 200°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

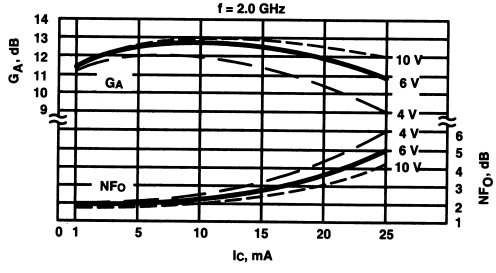
Typical Performance, T_A = 25°C

(unless otherwise noted)

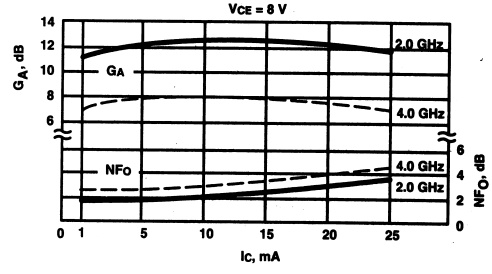
OUTPUT POWER AND 1 dB COMPRESSED GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



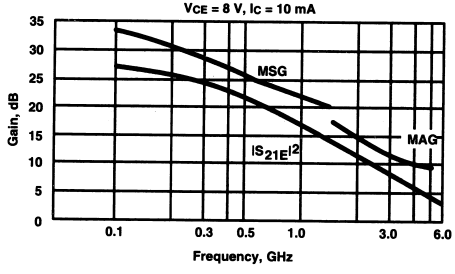
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN
vs. COLLECTOR CURRENT AND COLLECTOR VOLTAGE
f = 2.0 GHz



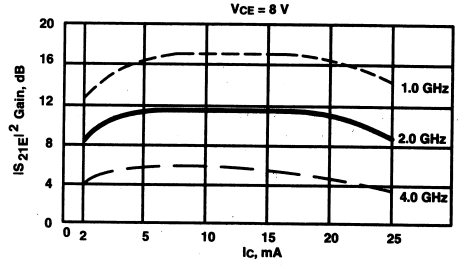
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



INSERTION POWER GAIN, MAXIMUM AVAILABLE
GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{CE} = 8 V, I_C = 10 mA



INSERTION POWER GAIN
vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



Typical Scattering Parameters: Common Emitter, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 2$ mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.94	–10	16.6	6.77	171	–39.2	.011	92	.99	–4
0.5	.83	–47	15.3	5.80	139	–27.6	.042	63	.92	–17
1.0	.64	–84	12.7	4.33	109	–23.8	.065	44	.81	–27
1.5	.50	–111	10.6	3.38	90	–22.4	.075	41	.74	–33
2.0	.42	–137	8.7	2.73	74	–21.6	.083	37	.70	–38
2.5	.37	–156	7.5	2.33	64	–21.0	.090	38	.67	–40
3.0	.37	–177	7.4	2.02	51	–20.8	.092	43	.66	–47
3.5	.37	164	5.0	1.77	39	–19.7	.103	41	.66	–56
4.0	.36	148	4.0	1.57	27	–19.2	.110	42	.67	–64
4.5	.37	131	3.0	1.42	17	–18.3	.121	42	.69	–70
5.0	.38	113	2.2	1.29	6	–17.1	.140	43	.69	–76
5.5	.43	93	1.5	1.19	–3	–15.9	.159	39	.69	–82
6.0	.50	80	0.8	1.09	–14	–15.0	.178	36	.66	–91

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 10$ mA

0.1	.77	–24	27.0	22.31	160	–41.0	.009	76	.96	–8
0.5	.47	–90	22.0	12.51	113	–31.0	.028	58	.72	–22
1.0	.33	–131	17.0	7.08	89	–27.2	.044	60	.63	–25
1.5	.28	–159	13.8	4.90	74	–25.0	.056	57	.60	–28
2.0	.27	176	11.5	3.77	63	–23.0	.070	58	.59	–33
2.5	.28	162	9.9	3.11	56	–21.6	.083	62	.57	–35
3.0	.30	149	8.4	2.64	46	–20.4	.096	60	.56	–43
3.5	.32	136	7.2	2.31	36	–19.1	.111	57	.57	–52
4.0	.33	124	6.2	2.04	26	–17.8	.129	53	.58	–60
4.5	.34	110	5.2	1.83	16	–16.7	.147	50	.60	–67
5.0	.36	95	4.4	1.67	6	–15.6	.166	45	.61	–73
5.5	.41	81	3.7	1.53	–2	–14.9	.180	40	.61	–79
6.0	.49	72	3.0	1.41	–12	–14.2	.196	36	.57	–87

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

AT-60570
Up to 6 GHz Low Noise Silicon Bipolar Transistor

Features

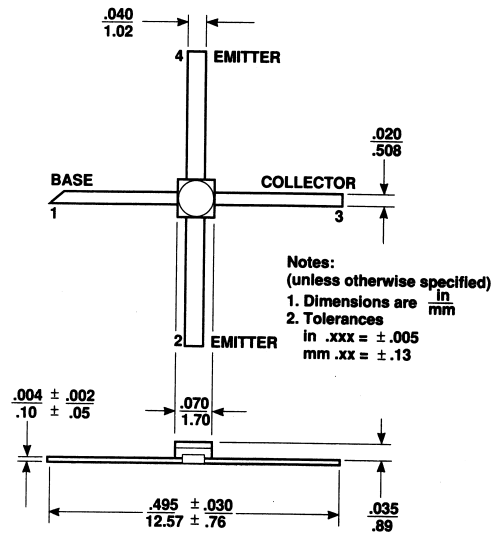
- **Low Bias Current Operation:**
- **Low Noise Figure: 1.8 dB typical at 2.0 GHz**
  2.8 dB typical at 4.0 GHz
- **High Associated Gain: 12.5 dB typical at 2.0 GHz**
  8.0 dB typical at 4.0 GHz
- **High Gain-Bandwidth Product: 8.0 GHz typical f_T**
- **Hermetic Gold-ceramic Microstrip Package**

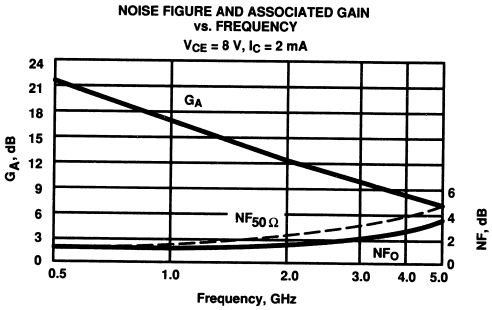
Description

The AT-60570 is a high performance NPN silicon bipolar transistor housed in a hermetic, high reliability package. This device is designed for use in low noise, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

70 mil Package





Noise Parameters: V_{CE} = 8 V, I_C = 2 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
1.0	1.4	.54	48	0.20
2.0	1.8	.44	98	0.28
4.0	2.8	.40	180	0.28

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 2 mA	f = 1.0 GHz	dB		1.4	
		f = 2.0 GHz			1.8	2.1
		f = 4.0 GHz			2.8	
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 2 mA	f = 1.0 GHz	dB		16.5	
		f = 2.0 GHz		11.0	12.5	
		f = 4.0 GHz			8.0	
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz	dB		12.0	
		f = 4.0 GHz			6.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz	dBm		16.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz	dB		12.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 10 mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 10 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		μA			1.0
C_{CB}	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		0.15	

Note: 1. For this test the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	40 mA
Power Dissipation[2,3]	P_T	400 mW
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 200°C/W

Notes:

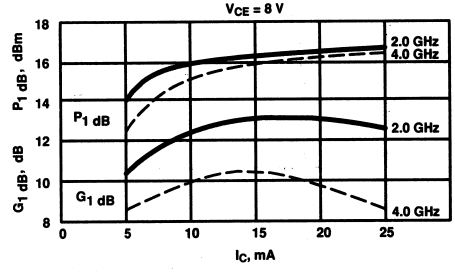
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 5 mW/°C for T_C > 120°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)

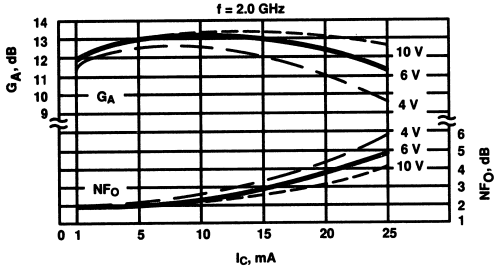
OUTPUT POWER AND 1 dB COMPRESSED GAIN vs. COLLECTOR CURRENT AND FREQUENCY

V_{CE} = 8 V



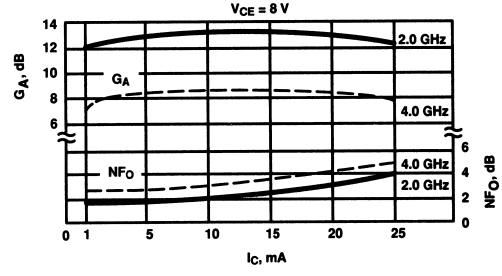
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN vs. COLLECTOR CURRENT AND COLLECTOR VOLTAGE

f = 2.0 GHz



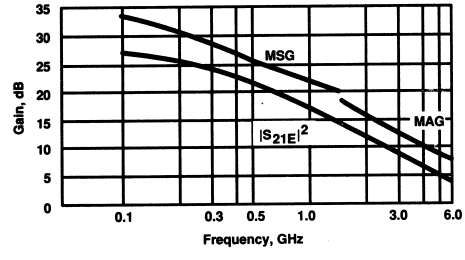
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN vs. COLLECTOR CURRENT AND FREQUENCY

V_{CE} = 8 V



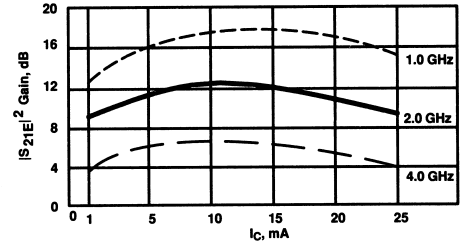
INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY

V_{CE} = 8 V, I_C = 10 mA



INSERTION POWER GAIN vs. COLLECTOR CURRENT AND FREQUENCY

V_{CE} = 8 V



Typical Scattering Parameters: Common Emitter, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 2$ mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.95	–10	16.6	6.74	171	–38.4	.012	86	.99	–4
0.5	.86	–48	15.3	5.81	141	–27.2	.044	63	.92	–19
1.0	.72	–83	12.8	4.38	113	–23.0	.070	43	.81	–30
1.5	.62	–108	10.7	3.42	95	–22.0	.080	35	.74	–37
2.0	.56	–128	8.8	2.75	80	–21.2	.088	28	.70	–43
2.5	.52	–141	7.4	2.34	72	–20.6	.094	28	.67	–44
3.0	.51	–153	6.1	2.02	61	–20.8	.092	27	.66	–51
3.5	.51	–164	4.9	1.75	50	–20.4	.095	24	.67	–58
4.0	.49	–172	3.8	1.55	40	–20.0	.099	25	.67	–65
4.5	.48	179	2.8	1.38	31	–19.8	.102	22	.69	–71
5.0	.46	169	2.1	1.27	22	–19.5	.106	21	.69	–76
5.5	.44	158	1.5	1.19	14	–19.2	.110	22	.70	–80
6.0	.44	145	0.9	1.11	4	–18.4	.120	20	.69	–86

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 10$ mA

0.1	.77	–26	27.3	23.25	161	–39.2	.011	79	.96	–9
0.5	.57	–98	22.6	13.51	116	–31.0	.028	49	.69	–27
1.0	.49	–136	17.8	7.72	92	–27.8	.041	45	.58	–31
1.5	.45	–156	14.6	5.36	79	–26.2	.049	45	.54	–34
2.0	.44	–171	12.3	4.10	69	–24.6	.059	48	.53	–39
2.5	.44	–177	10.5	3.35	63	–23.0	.070	51	.52	–39
3.0	.45	174	9.1	2.84	55	–23.0	.071	52	.52	–47
3.5	.45	167	7.8	2.46	46	–21.4	.086	52	.53	–56
4.0	.44	160	6.7	2.16	37	–20.2	.097	50	.55	–63
4.5	.42	153	5.7	1.92	29	–19.3	.108	47	.57	–70
5.0	.40	144	4.9	1.75	21	–18.7	.116	44	.59	–75
5.5	.40	132	4.2	1.62	13	–18.1	.124	41	.60	–79
6.0	.41	121	3.5	1.49	4	–17.3	.137	38	.60	–86

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

AT-60585
Up to 6 GHz Low Noise Silicon Bipolar Transistor

Features

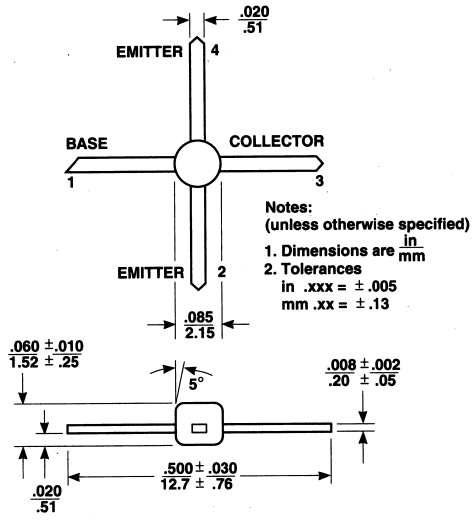
- **Low Bias Current Operation**
- **Low Noise Figure: 1.4 dB typical at 1.0 GHz**
  1.9 dB typical at 2.0 GHz
- **High Associated Gain: 16.5 dB typical at 1.0 GHz**
  11.5 dB typical at 2.0 GHz
- **High Gain-Bandwidth Product: 8.0 GHz typical f_T**
- **Low Cost Plastic Package**

Description

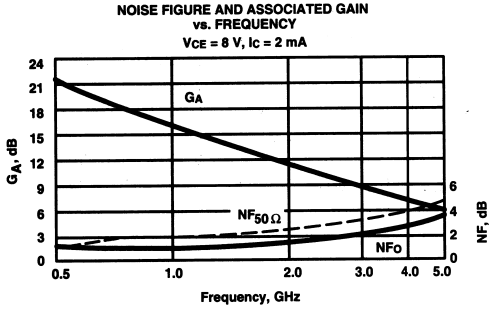
The AT-60585 is a high performance NPN silicon bipolar transistor housed in a low cost pastic package. This device is designed for use in low noise, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

85 Plastic Package



Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
   in .xxx = ±.005
   mm .xx = ±.13



Noise Parameters: V_{CE} = 8 V, I_C = 2 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
1.0	1.4	.50	53	0.32
2.0	1.9	.44	108	0.34
4.0	2.9	.40	–144	0.46

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 2 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		1.4 1.9 2.9	1.8
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 2 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB	15.0	16.5 11.5 7.5	
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 10 mA	f = 1.0 GHz f = 2.0 GHz	dB		17.0 11.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz	dBm		15.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz	dB		11.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 10 mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 10 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		μA			1.0
C_{CB}	Collector Base Capacitance[1]: V_{CB} = 8 V, f = 1 MHz		pF		0.2	

Note: 1. For this test the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	40 mA
Power Dissipation[2,3]	P_T	400 mW
Junction Temperature	T_j	150°C
Storage Temperature	T_{STG}	–65°C to 150°C

Thermal Resistance[2,4]: θ_{jc} = 180°C/W

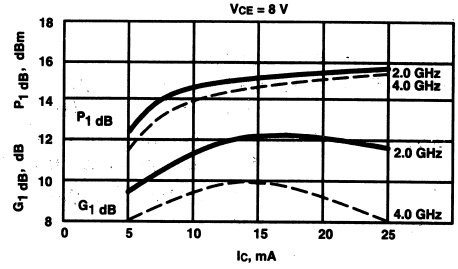
Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 5.6 mW/°C for T_C > 78°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

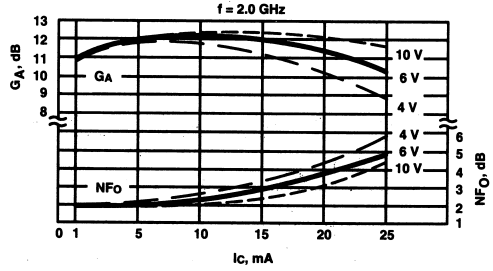
Typical Performance, T_A = 25°C

(unless otherwise noted)

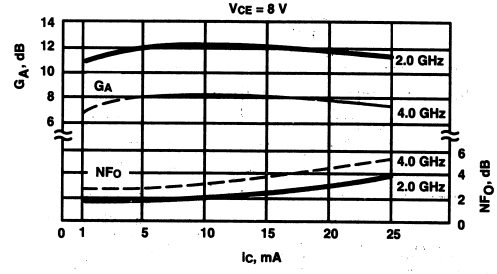
OUTPUT POWER AND 1 dB COMPRESSED GAIN vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



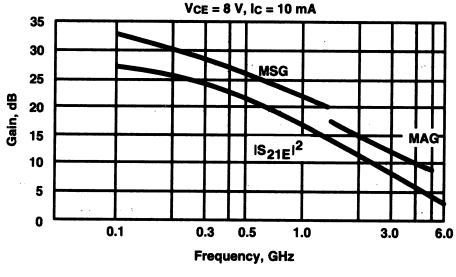
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN vs. COLLECTOR CURRENT AND COLLECTOR VOLTAGE
f = 2.0 GHz



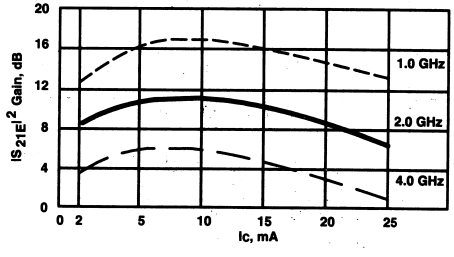
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{CE} = 8 V, I_C = 10 mA



INSERTION POWER GAIN vs. COLLECTOR CURRENT AND FREQUENCY
V_{CE} = 8 V



Typical Scattering Parameters: Common Emitter, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 2$ mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.95	–10	16.3	6.56	171	–38.5	.012	82	.99	–4
0.5	.84	–30	15.1	5.66	139	–26.0	.050	61	.90	–18
1.0	.67	–86	12.5	4.22	110	–22.6	.074	43	.78	–29
1.5	.55	–114	10.4	3.29	90	–21.1	.088	35	.70	–35
2.0	.48	–139	8.4	2.64	74	–20.3	.096	29	.65	–41
2.5	.44	–155	7.0	2.25	65	–20.4	.096	31	.63	–41
3.0	.44	–174	5.7	1.92	53	–19.9	.101	32	.60	–48
3.5	.44	171	4.5	1.67	42	–19.7	.104	28	.62	–54
4.0	.44	157	3.3	1.47	30	–19.2	.109	29	.63	–61
4.5	.44	144	2.3	1.31	20	–18.8	.115	30	.65	–66
5.0	.44	128	1.5	1.19	11	–18.2	.124	29	.66	–70
5.5	.47	110	0.8	1.10	1	–17.4	.135	29	.64	–74
6.0	.52	94	0.1	1.01	–9	–16.7	.146	27	.62	–80

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 10$ mA

0.1	.73	–28	27.0	22.47	160	–39.5	.011	84	.96	–9
0.5	.52	–105	21.9	12.44	113	–30.8	.029	49	.68	–23
1.0	.44	–145	16.9	7.00	90	–28.1	.039	51	.58	–25
1.5	.41	–168	13.7	4.85	76	–25.8	.051	57	.55	–28
2.0	.41	174	11.4	3.70	65	–24.2	.061	57	.53	–33
2.5	.42	165	9.7	3.06	60	–22.8	.072	58	.51	–34
3.0	.44	155	8.1	2.56	51	–21.3	.086	64	.50	–42
3.5	.46	145	7.0	2.23	41	–20.2	.098	60	.50	–50
4.0	.46	136	5.8	1.96	32	–18.8	.114	58	.52	–59
4.5	.46	127	4.9	1.75	23	–17.7	.130	57	.53	–65
5.0	.47	115	4.0	1.58	14	–17.0	.141	52	.54	–71
5.5	.50	103	3.3	1.46	5	–16.0	.159	47	.54	–75
6.0	.55	91	2.5	1.34	–3	–15.0	.177	42	.51	–84

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

AT-60586
Up to 6 GHz Low Noise Silicon Bipolar Transistor

Features

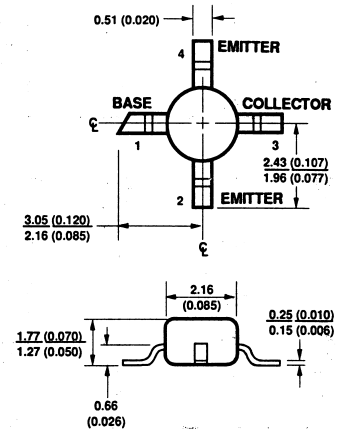
- **Low Bias Current Operation**
- **Low Noise Figure: 1.4 dB typical at 1.0 GHz**
  1.9 dB typical at 2.0 GHz
- **High Associated Gain: 16.0 dB typical at 1.0 GHz**
  11.0 dB typical at 2.0 GHz
- **High Gain-Bandwidth Product: 8.0 GHz typical f_T**
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Description

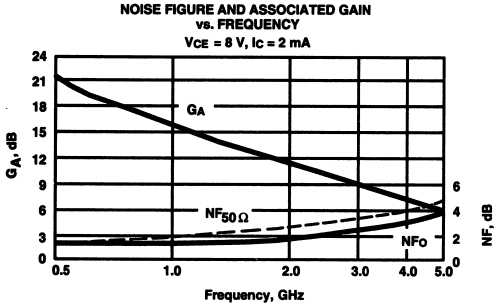
The AT-60586 is a high performance NPN silicon bipolar transistor housed in a low cost, surface mount plastic package. This device is designed for use in low noise, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices.

86 Plastic Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{CE} = 8 V, I_C = 2 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB		1.4 1.9 2.9	1.8
G_A	Gain @ NF_O: V_{CE} = 8 V, I_C = 2 mA	f = 1.0 GHz f = 2.0 GHz f = 4.0 GHz	dB	14.5	16.0 11.0 7.0	
$\|S_{21E}\|^2$	Insertion Power Gain: V_{CE} = 8 V, I_C = 10 mA	f = 1.0 GHz f = 2.0 GHz	dB		17.0 11.5	
$P_{1\ dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz	dBm		14.5	
$G_{1\ dB}$	1 dB Compressed Gain: V_{CE} = 8 V, I_C = 10 mA	f = 2.0 GHz	dB		10.5	
f_T	Gain Bandwidth Product: V_{CE} = 8 V, I_C = 10 mA		GHz		8.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 10 mA			30	150	300
I_{CBO}	Collector Cutoff Current: V_{CB} = 8 V		μA			0.2
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		μA			1.0
C_{CB}	Collector Base Capacitance[2]: V_{CB} = 8 V, f = 1 MHz		pF		0.2	

Notes: 1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices."
2. For this test, the emitter is grounded.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	1.5 V
Collector-Base Voltage	V_{CBO}	20 V
Collector-Emitter Voltage	V_{CEO}	12 V
Collector Current	I_C	40 mA
Power Dissipation[2,3]	P_T	400 mW
Junction Temperature	T_j	150°C
Storage Temperature	T_{STG}	–65°C to 150°C

Thermal Resistance[2,4]: θ_{jc} = 190°C/W

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 5.3 mW/°C for T_C > 74°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Part Number Ordering Information

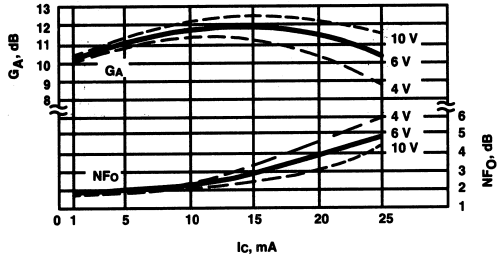
Part Number	Devices Per Reel	Reel Size
AT-60586-TR1	1000	7"
AT-60586-TR2	4000	13"

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

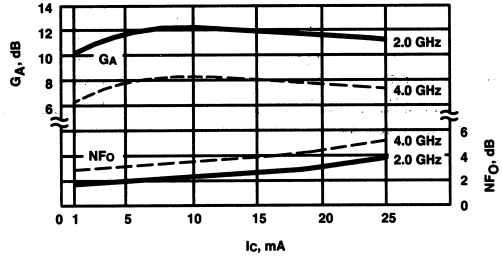
Typical Performance, T_A = 25°C

(unless otherwise noted)

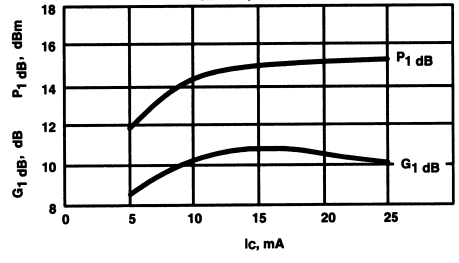
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN vs. COLLECTOR CURRENT AND COLLECTOR VOLTAGE
f = 2.0 GHz



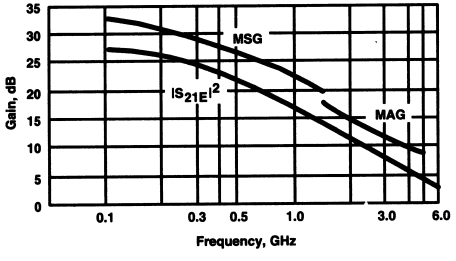
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN vs. COLLECTOR CURRENT AND FREQUENCY
VCE = 8 V



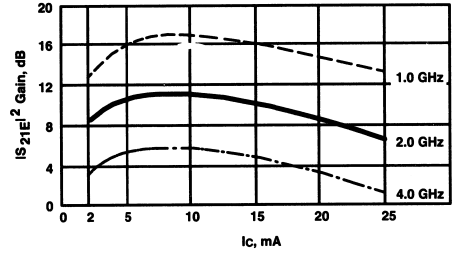
OUTPUT POWER AND 1 dB COMPRESSED GAIN vs. COLLECTOR CURRENT
VCE = 8 V, f = 2.0 GHz



INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
VCE = 8 V, IC = 10 mA



INSERTION POWER GAIN vs. COLLECTOR CURRENT AND FREQUENCY
VCE = 8 V



Typical Scattering Parameters: Common Emitter, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 2$ mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.95	–10	16.4	6.60	171	–39.7	.010	81	.99	–4
0.5	.83	–50	15.2	5.76	139	–25.8	.051	63	.90	–18
1.0	.65	–91	12.6	4.26	110	–21.7	.082	43	.76	–29
1.5	.55	–125	10.5	3.36	88	–20.6	.093	33	.67	–36
2.0	.50	–153	8.5	2.64	71	–20.1	.099	29	.61	–42
2.5	.49	–173	7.1	2.27	60	–19.6	.105	29	.58	–45
3.0	.49	166	5.8	1.94	46	–19.6	.105	24	.55	–51
3.5	.51	151	4.6	1.69	34	–18.8	.114	25	.54	–59
4.0	.54	138	3.4	1.48	23	–18.5	.119	24	.52	–68
4.5	.58	127	2.5	1.34	12	–18.0	.125	25	.51	–77
5.0	.61	117	1.7	1.22	1	–17.3	.137	24	.51	–89
5.5	.63	109	1.0	1.12	–8	–16.7	.146	22	.50	–102
6.0	.65	102	0.3	1.03	–19	–15.9	.161	22	.50	–116

$T_A = 25°C$, $V_{CE} = 8$ V, $I_C = 10$ mA

0.1	.76	–28	27.0	22.34	160	–40.8	.009	76	.95	–10
0.5	.51	–105	22.1	12.77	112	–30.2	.031	49	.66	–26
1.0	.42	–149	17.0	7.08	88	–26.5	.047	48	.54	–27
1.5	.42	–175	13.8	4.92	73	–24.9	.057	50	.49	–31
2.0	.44	165	11.5	3.75	60	–23.0	.071	51	.47	–36
2.5	.46	155	9.8	3.08	52	–21.3	.086	53	.45	–40
3.0	.48	143	8.2	2.56	42	–20.6	.093	48	.44	–46
3.5	.52	134	7.1	2.27	32	–19.1	.111	46	.42	–55
4.0	.55	125	6.0	2.00	22	–18.4	.120	44	.40	–64
4.5	.59	117	5.0	1.77	13	–17.3	.136	41	.39	–75
5.0	.62	110	4.1	1.61	3	–16.4	.151	36	.38	–88
5.5	.64	104	3.3	1.45	–5	–15.9	.160	34	.38	–100
6.0	.66	98	2.5	1.34	–15	–15.0	.178	30	.38	–117

A model for this device is available in the DEVICE MODELS section.

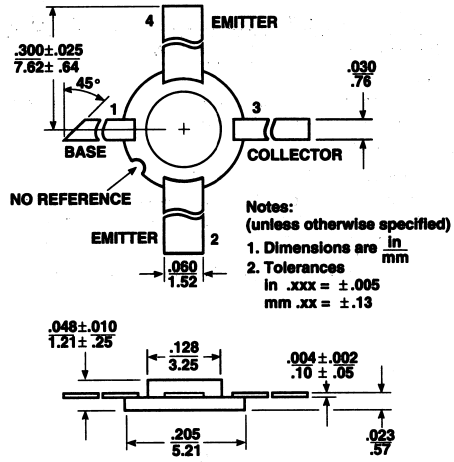
HEWLETT PACKARD

AT-64020
Up to 4 GHz Linear Power Silicon Bipolar Transistor

Features

- **High Output Power:**
  28.0 dBm typical $P_{1\,dB}$ at 2.0 GHz
  27.0 dBm typical $P_{1\,dB}$ at 4.0 GHz
- **High Gain at 1 dB Compression:**
  10.0 dB typical $G_{1\,dB}$ at 2.0 GHz
  6.5 dB typical $G_{1\,dB}$ at 4.0 GHz
- **35% Total Efficiency**
- **Emitter Ballast Resistors**
- **Hermetic, Metal/Beryllia Microstrip Package**

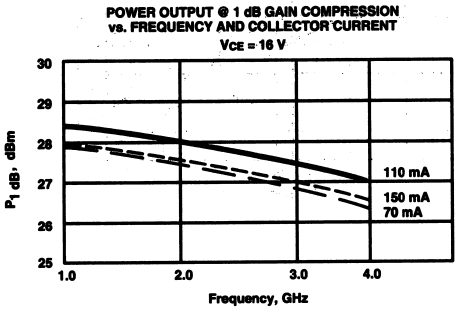
200 mil BeO Package



Description

The AT-64020 is a high performance NPN silicon bipolar transistor housed in a hermetic BeO disk package for good thermal characteristics. This device is designed for use in medium power, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices. The use of ion-implanted ballast resistors ensures uniform current distribution through the multiple emitter fingers.



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 16 V, I_C = 110 mA	f = 2.0 GHz f = 4.0 GHz	dBm	27.0	28.0 27.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 16 V, I_C = 110 mA	f = 2.0 GHz f = 4.0 GHz	dB	9.0	10.0 6.5	
η_T	Total Efficiency[1] at 1 dB Compression: V_{CE} = 16 V, I_C = 110 mA	f = 4.0 GHz	%		35.0	
$\lvert S_{21E}\rvert^2$	Insertion Power Gain: V_{CE} = 16 V, I_C = 110 mA	f = 2.0 GHz f = 4.0 GHz	dB		7.0 2.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 110 mA			20	50	200
I_{CBO}	Collector Cutoff Current: V_{CB} = 16 V		μA			100
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		μA			5.0

Note: 1. $\eta_T = \frac{\text{RF Output Power}}{\text{RF Input Power} + V_{CE}I_C}$

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	2 V
Collector-Base Voltage	V_{CBO}	40 V
Collector-Emitter Voltage	V_{CEO}	20 V
Collector Current	I_C	200 mA
Power Dissipation[2,3]	P_T	3 W
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	−65°C to 200°C

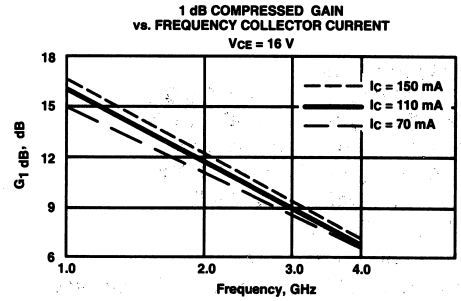
Thermal Resistance[2,4]: θ_{jc} = 40°C/W

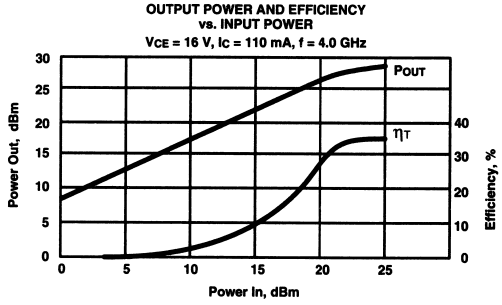
Notes:

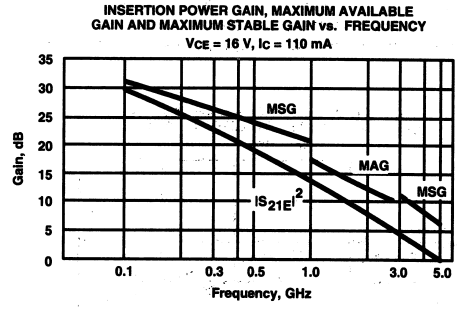
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 25 mW/°C for T_C > 80°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)







Typical Scattering Parameters: Common Emitter, Z_O = 50 Ω

T_A = 25°C, V_{CE} = 16 V, I_C = 110 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.61	−116	30.0	31.51	130	−33.1	.022	57	.67	−48
0.5	.75	−173	18.4	8.27	86	−28.8	.036	41	.23	−88
1.0	.75	171	12.5	4.23	66	−27.4	.043	49	.20	−100
1.5	.74	159	9.2	2.90	50	−23.5	.067	48	.21	−110
2.0	.74	148	7.0	2.23	35	−21.6	.083	46	.25	−120
2.5	.73	141	5.2	1.82	26	−19.8	.103	47	.27	−127
3.0	.73	130	3.8	1.56	12	−17.5	.133	41	.32	−135
3.5	.74	119	2.7	1.37	−2	−16.1	.157	35	.35	−146
4.0	.73	107	1.8	1.23	−16	−14.7	.186	26	.38	−158
4.5	.72	93	0.9	1.11	−30	−13.3	.217	18	.41	−168
5.0	.71	79	0.1	1.01	−43	−11.8	.256	8	.42	179

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

AT-64023
Up to 4 GHz Linear Power Silicon Bipolar Transistor

Features

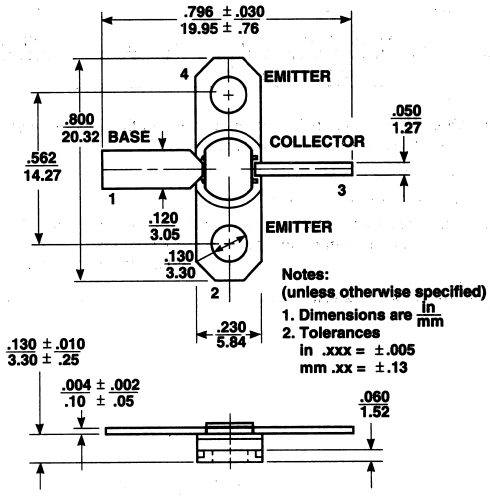
- **High Output Power:**
  28.0 dBm typical $P_{1\,dB}$ at 2.0 GHz
  27.0 dBm typical $P_{1\,dB}$ at 4.0 GHz
- **High Gain at 1 dB Compression:**
  12.5 dB typical $G_{1\,dB}$ at 2.0 GHz
  9.5 dB typical $G_{1\,dB}$ at 4.0 GHz
- **35% Total Efficiency**
- **Emitter Ballast Resistors**
- **Hermetic, Metal/Beryllia Stripline Package**

Description

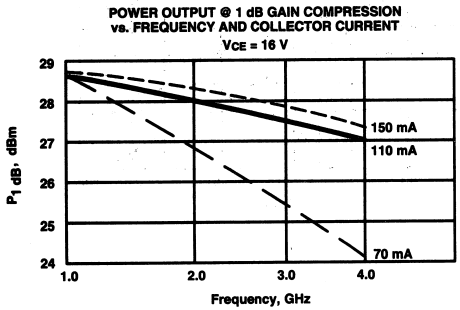
The AT-64023 is a high performance NPN silicon bipolar transistor housed in a hermetic BeO flange package for good thermal characteristics. This device is designed for use in medium power, wide band amplifier and oscillator applications operating over VHF, UHF and microwave frequencies.

Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metallization in the fabrication of these devices. The use of ion-implanted ballast resistors ensures uniform current distribution through the multiple emitter fingers.

230 mil BeO Flange Package



Outline 23A



Electrical Specifications, $T_A = 25°C$

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{CE} = 16 V, I_C = 110 mA	f = 2.0 GHz f = 4.0 GHz	dBm	 25.5	28.0 27.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{CE} = 16 V, I_C = 110 mA	f = 2.0 GHz f = 4.0 GHz	dB	 7.0	12.5 9.5	
η_T	Total Efficiency[1] at 1 dB Compression: V_{CE} = 16 V, I_C = 110 mA	f = 4.0 GHz	%		35.0	
$\lvert S_{21E}\rvert^2$	Insertion Power Gain: V_{CE} = 16 V, I_C = 110 mA	f = 2.0 GHz f = 4.0 GHz	dB		6.5 2.0	
h_{FE}	Forward Current Transfer Ratio: V_{CE} = 8 V, I_C = 110 mA			20	50	200
I_{CBO}	Collector Cutoff Current: V_{CB} = 16 V		μA			100
I_{EBO}	Emitter Cutoff Current: V_{EB} = 1 V		μA			5.0

Note: 1. $\eta_T = \frac{\text{RF Output Power}}{\text{RF Input Power} + V_{CE}I_C}$

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Emitter-Base Voltage	V_{EBO}	2.2 V
Collector-Base Voltage	V_{CBO}	40 V
Collector-Emitter Voltage	V_{CEO}	20 V
Collector Current	I_C	200 mA
Power Dissipation[2,3]	P_T	3 W
Junction Temperature	T_j	200°C
Storage Temperature	T_{STG}	–65°C to 200°C

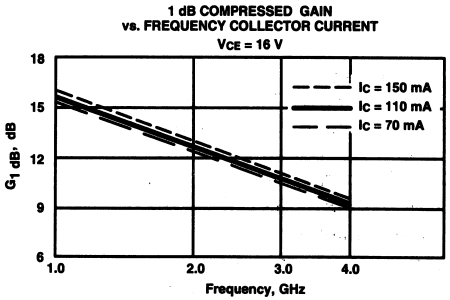
Thermal Resistance[2,4]: θ_{jc} = 40°C/W

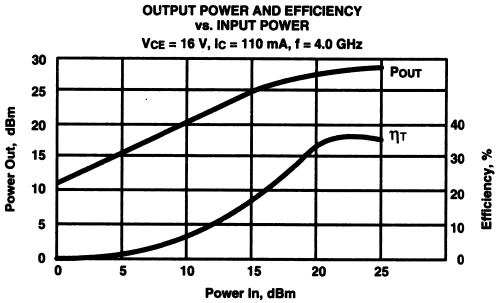
Notes:

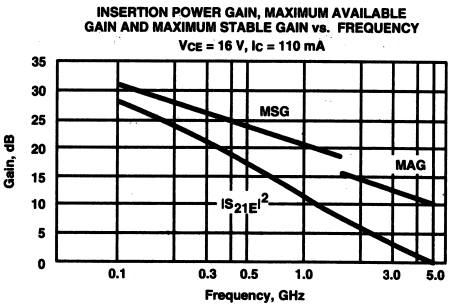
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 25 mW/°C for T_C > 80°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)







Typical Scattering Parameters: Common Emitter, Z_O = 50 Ω

T_A = 25°C, V_{CE} = 16 V, I_C = 110 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.54	–124	28.2	25.71	135	–33.3	.022	42	.72	–51
0.5	.80	–178	17.6	7.57	78	–29.5	.034	18	.33	–119
1.0	.80	162	11.9	3.92	47	–28.6	.037	10	.33	–142
1.5	.80	147	8.6	2.70	21	–27.9	.040	12	.40	–156
2.0	.78	133	6.3	2.07	–4	–27.6	.042	1	.48	–169
2.5	.77	127	5.1	1.80	–24	–25.5	.053	–5	.58	–178
3.0	.73	116	3.8	1.56	–51	–25.0	.056	–20	.67	170
3.5	.66	106	2.9	1.40	–79	–25.8	.051	–28	.78	156
4.0	.60	99	2.2	1.28	–109	–27.2	.044	–49	.86	142
4.5	.55	98	1.4	1.18	–141	–31.2	.028	–70	.93	127
5.0	.54	99	0.6	1.07	–175	–40.9	.009	–144	.93	112

A model for this device is available in the DEVICE MODELS section.

Gallium Arsenide Field Effect Transistors



Gallium Arsenide Field Effect Transistors

The Gallium Arsenide field effect transistor is a semiconductor device with amplification due to voltage gain. The advantages GaAs FETs have over other transistor types stem from the intrinsic high mobility of electrons in gallium arsenide. This high mobility translates into semiconductors with superior high performance characteristics in the microwave region, including high f_T, high f_{MAX}, and very low noise figure.

GaAs FETs find wide applications as the semiconductor device of choice at frequencies above 4 GHz (where the gain of most microwave silicon processes is diminishing) both as amplifiers and oscillators, or as low noise amplifiers in applications demanding optimum noise performance.

The performance of a GaAs FET is determined primarily by the gate width and length. The gate *length* is the short dimension of the gate and sets the "high frequency" aspects of performance. In general, shorter gate lengths result in superior performance (although the gate must have sufficient thickness to support the current density necessary for reliability). The gate length is a primary feature of the process used. The gate *width* determines the active periphery, and sets the transconductance (g_m) and saturated drain current (I_{DSS}) of the FET. In addition to establishing the power producing capability, the gate width also sets the s-parameters of the device, and therefore the optimum frequency of operation. In general, shorter widths work better at high frequencies. The gate width is set by the geometry or mask design. It is fairly common for the same mask type to be used with different processes to create FETs with the same gate width but different performance characteristics.

Product Families

Hewlett-Packard manufactures FETs using a series of processes tailored for the end application. Part numbers for these devices begin with the alpha characters "ATF". The first digit of the part number delineates process. The second digit defines the geometry. The third digit represents an assembly sort, e.g. for noise figure. The final two digits indicate the package type.

ATF-1x series

The ATF-1x process is optimized for low noise figure. This process uses vapor phase epi and a nominal 0.25 micron gate length to produce MESFETs with superior noise figures for LNA applications such as TVRO or GPS receivers, and all kinds of communications receivers. This process also results in devices with phase noise approximately 10 dB lower than that produced by the gain (ATF-2x) process. The relatively delicate gate needed for best noise performance results in a device not recommended for applications calling for operation in saturation. The nominal figures of merit for this process are an f_T of 40 GHz and an f_{MAX} of 100 GHz.

Two geometries are available:

- ATF-10xxx: 500 micron gate width device optimum for 2-8 GHz applications
- ATF-13xxx: 250 micron gate width device optimum for 4-16 GHz applications

ATF-2x series

The ATF-2x process is optimized for gain. This process uses ion implantation and a nominal 0.25 micron gate length to produce MESFETs with good gain and power. Typical uses include gain stages and medium power oscillator applications. The robust gate used results in a device with superior longevity. The nominal figures of merit for this process are an f_T of 40 GHz and an f_{MAX} of 100 GHz.

Three geometries are available:

- ATF-21xxx: 750 micron gate width device optimum for 1-6 GHz applications
- ATF-25xxx: 500 micron gate width device optimum for 2-8 GHz applications
- ATF-26xxx: 250 micron gate width device optimum for 4-16 GHz applications

ATF-3x series

The ATF-3x process is Hewlett-Packard's high performance Pseudomorphic High Electron Mobility Transistor (PHEMT) process. This process uses MBE material to create a GaAs - AlGaAs - InAlGaAs structure that results in superior mobility to standard MESFET or HEMT devices. This process is optimized to give the lowest noise figure for critical receiver applications such as DBS block converters. The nominal figures

of merit for this process are an f_T of 60 GHz and an f_{MAX} of 150 GHz.

The geometry available is:

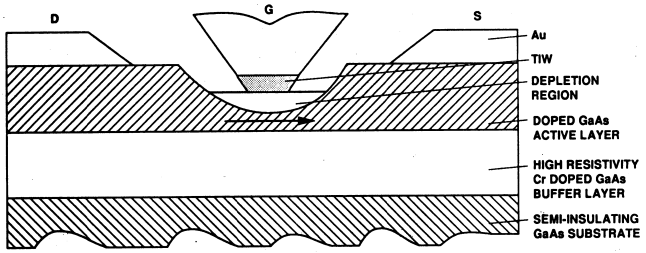
- ATF-35xxx: 200 micron gate width device optimum for 2-18 GHz applications

ATF-4x series

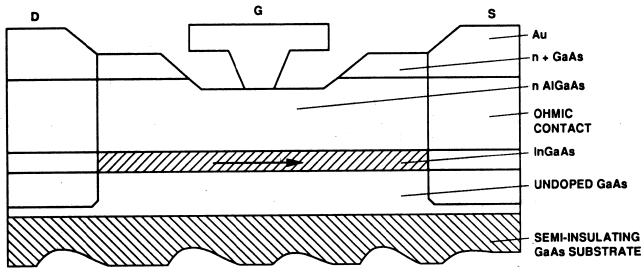
The ATF-4x process is optimized for power. This process uses a double recessed 0.5 micron gate length to produce MESFETs with high breakdowns and superior power producing capability. Typical uses include driver and power amplifiers up to several watts. The nominal figures of merit for this process are an f_T of 20 GHz and an f_{MAX} of 50 GHz.

Three geometries are available:

- ATF-44xxx: 5000 micron gate width device for 2-8 GHz applications
- ATF-45xxx: 2500 micron gate width device for 2-8 GHz applications
- ATF-46xxx: 1250 micron gate width device for 2-10 GHz applications



MESFET STRUCTURE



PHEMT STRUCTURE

Gallium Arsenide (GaAs) Field Effect Transistors (FETs)

Low Noise GaAs FETs (Typical Specifications at +25°C Case Temperature)

Part Number	Gate Width (μm)	Optimum Freq. Range (GHz)	Test Freq. (GHz)	NF_o (dB)	G_a (dB)	P_{1dB} (dBm)	Package	Page
ATF-10100	500	0.5-12	4	0.5	13.0	+20.0	chip	7-6
ATF-13100	250	2-18	12	1.1	9.5	+17.5	chip	7-20
ATF-21100	750	0.5-6	4	0.9	13.0	+23.0	chip	7-40
ATF-25100	500	0.5-10	4	0.8	14.0	+21.0	chip	7-51
ATF-10170	500	0.5-12	4	0.5	13.0	+20.0	70 mil stripline	7-11
ATF-13170	250	2-16	12	1.1	9.5	+17.5	70 mil stripline	7-24
ATF-21170	750	0.5-6	4	0.9	13.0	+23.0	70 mil stripline	7-43
ATF-25170	500	0.5-10	4	0.8	14.0	+21.0	70 mil stripline	7-54
ATF-10136	500	0.5-12	4	0.5	13.0	+20.0	trim lead micro-X SM	7-9
ATF-10236	500	0.5-12	4	0.8	13.0	+20.0	micro-X ceramic SM	7-13
ATF-13036	250	2-16	12	1.1	9.5	+17.5	micro-X ceramic SM	7-18
ATF-13136	250	2-16	12	1.2	9.5	+17.5	micro-X ceramic SM	7-22
ATF-13336	250	2-16	12	1.4	9.0	+17.5	micro-X ceramic SM	7-28
ATF-13284	250	1-16	4	0.7	15.0	+18.0	85 mil plastic	7-26
ATF-13484	250	1-16	4	1.0	14.0	+18.0	85 mil plastic	7-30
ATF-13786	250	1-12	10	–	–	+16.5	85 mil plastic SM	7-36

Low Noise PHEMTs (Typical Specifications at +25°C Case Temperature)

Part Number	Gate Width (μm)	Optimum Freq. Range (GHz)	Test Freq. (GHz)	NF_o (dB)	G_a (dB)	Package	Page
ATF-35076	200	4-18	12	0.75	10.5	70 mil ceramic	7-73
ATF-35176	200	4-18	12	0.85	10.0	70 mil ceramic	7-73
ATF-35376	200	4-18	12	1.0	10.0	70 mil ceramic	7-73
ATF-35576	200	4-18	12	1.5	12.0	70 mil ceramic	7-76

General Purpose GaAs FETs (Typical Specifications at +25°C Case Temperature)

Part Number	Gate Width (μm)	Optimum Freq. Range (GHz)	Test Freq. (GHz)	NF_o (dB)	G_a (dB)	P_{1dB} (dBm)	Package	Page
ATF-21100	750	0.5-6	4	0.9	13.0	+23.0	chip	7-40
ATF-25100	500	0.5-10	4	0.8	14.0	+21.0	chip	7-51
ATF-26100	250	2-18	12	1.6	9.0	+18.0	chip	7-60
ATF-21170	750	0.5-6	4	0.9	13.0	+23.0	70 mil stripline	7-43
ATF-21186	750	0.5-6	2	0.6	13.5	+19.0	85 mil SM plastic	7-45
ATF-25170	500	0.5-10	4	0.8	14.0	+21.0	70 mil stripline	7-54
ATF-25570	500	0.5-10	4	1.0	14.0	+20.5	70 mil stripline	7-56
ATF-26150	250	2-16	12	1.5	9.0	+18.0	50 mil stripline	7-63
ATF-26350	250	2-16	12	1.7	9.0	+18.0	50 mil stripline	7-65
ATF-26550	250	2-16	12	2.1	8.5	+18.0	50 mil stripline	7-67
ATF-25735	500	0.5-10	4	1.2	12.5	+19.0	micro-X ceramic SM	7-58
ATF-10736	500	0.5-12	4	1.2	12.5	+20.0	trim lead micro-X SM	7-15
ATF-13736	250	2-16	12	1.8	9.0	+17.5	trim lead micro-X SM	7-33
ATF-26836	250	2-16	12	2.2	6.0	+18.0	trim lead micro-X SM	7-69
ATF-13484	250	1-16	4	1.0	14.0	+18.0	85 mil plastic	7-30
ATF-26884	250	2-16	12	2.2	9.0	+18.0	85 mil plastic	7-71

Gallium Arsenide (GaAs) Field Effect Transistors (FETs) (cont.)

Medium Power GaAs FETs (Typical Specifications at +25°C Case Temperature)

Part Number	Optimum Freq. Range (GHz)	Test Frequency (GHz)	P_{1dB} (dBm)	G_{1dB} (dBm)	Package	Page
ATF-44100	2-8	4	+32.0	9.0	chip	7-78
ATF-45100	2-12	4	+29.0	11.0	chip	7-82
ATF-46100	2-14	4	+27.0	12.0	chip	7-88
ATF-44101	2-8	4	+32.0	9.0	100 mil flange	7-80
ATF-45101	2-8	4	+29.0	10.0	100 mil flange	7-84
ATF-45171	2-8	4	+29.0	10.5	70 mil flange	7-86
ATF-46101	2-10	4	+27.0	10.0	100 mil flange	7-90
ATF-46171	2-10	4	+27.0	11.0	70 mil flange	7-92

HEWLETT PACKARD

ATF-10100
0.5-12 GHz Low Noise Gallium Arsenide FET

Features

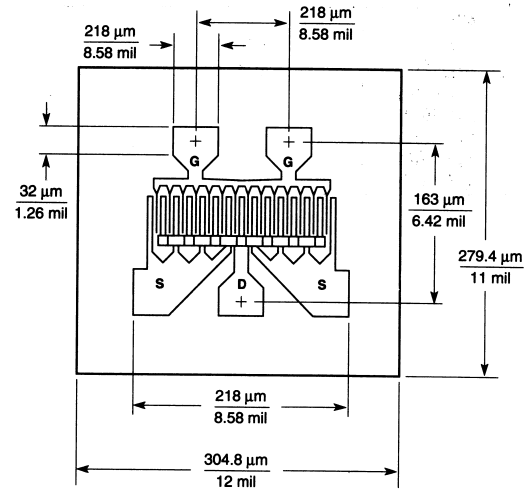
- **Low Noise Figure: 0.5 dB typical at 4 GHz**
- **Low Bias: VDS = 2 V, IDS = 25 mA**
- **High Assosiated Gain: 14.0 dB typical at 4 GHz**
- **High Output Power: 21.0 dBm typical $P_{1\ dB}$ at 4 GHz**

Description

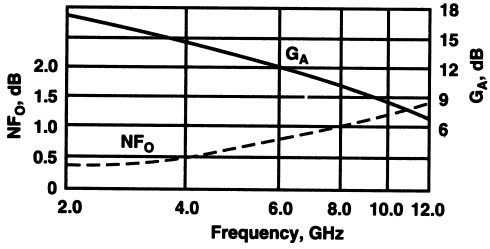
The ATF-10100 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor chip. Its premium noise figure makes this device appropriate for use in the first stage of low noise amplifiers operating in the 0.5-12 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length interconnects between drain fingers. Total gate periphery is 500 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device .

Chip Outline



Optimum Noise Figure and Associated Gain vs. Frequency
V_{DS} = 2 V, I_{DS} = 25 mA, T_A = 25°C



Noise Parameters: V_{DS} = 2 V, I_{DS} = 25 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
1.0	0.4	.78	13	.40
2.0	0.4	.55	27	.29
4.0	0.55	.39	65	.22
6.0	0.8	.41	105	.16
8.0	1.0	.46	144	.10

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 2 V, I_{DS} = 25 mA	f = 2.0 GHz f = 4.0 GHz f = 6.0 GHz	dB dB dB		0.4 0.55 0.8	0.7
G_A	Gain @ NF_O: V_{DS} = 2 V, I_{DS} = 25 mA	f = 2.0 GHz f = 4.0 GHz f = 6.0 GHz	dB dB dB	12.0	17.0 14.0 12.0	
$P_{1\ dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 4 V, I_{DS} = 70 mA	f = 4.0 GHz	dBm		21.0	
$G_{1\ dB}$	1dB Compressed Gain: V_{DS} = 4 V, I_{DS} = 70 mA	f = 4.0 GHz	dB		15.0	
g_m	Transconductance: V_{DS} = 2 V, V_{GS} = 0 V		mmho	80	140	
I_{DSS}	Saturated Drain Current: V_{DS} = 2 V, V_{GS} = 0 V		mA	70	130	180
V_P	Pinchoff Voltage: V_{DS} = 2 V, I_{DS} = 1 mA		V	-3.0	-1.3	-0.8

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum
Drain-Source Voltage	V_{DS}	+5 V
Gate-Source Voltage	V_{GS}	-4V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	430mW
Channel Temperature	T_{CH}	175°C
Storage Temperature[4]	T_{STG}	-65 to +175°C

Thermal Resistance: θ_{jc} = 225°C/W TCH = 150°C
Liquid Crystal Measurement; 1μm Spot Size[4]

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 4.4 mW/°C for T_{case} > 78°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See APPLICATIONS PRIMER IIIA for more information.

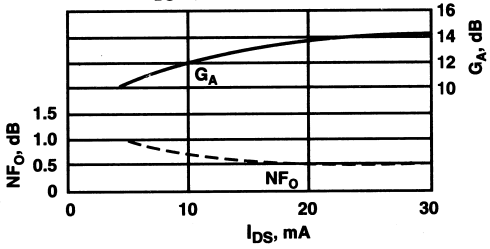
Part Number Ordering Information

Part Number	Devices Per Tray
ATF-10100-GP1	5
ATF-10100-GP3	50
ATF-10100-GP6	Up to 300

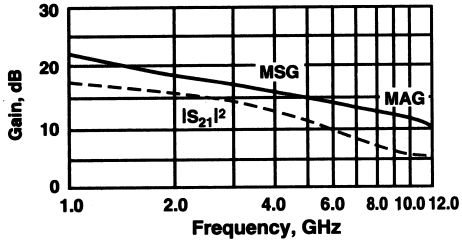
Typical Performance, T_A = 25°C

(Unless otherwise noted)

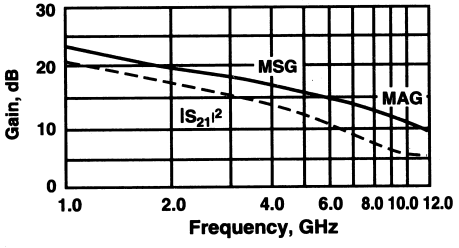
Optimum Noise Figure and Associated Gain vs. I_{DS}
V_{DS} = 2 V, f = 4.0 GHz



Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency
V_{DS} = 2 V, I_{DS} = 25 mA



Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency
V_{DS} = 4 V, I_{DS} = 70 mA



Typical Scattering Parameters: Common Source $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{DS} = 2$ V, $I_{DS} = 25$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
MHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
1.0	.93	-46	17.7	7.63	148	-25.5	.053	64	.33	-56
2.0	.83	-78	15.6	6.08	127	-21.4	.085	52	.31	-63
3.0	.78	-94	13.9	4.97	114	-19.8	.102	45	.30	-72
4.0	.72	-104	12.4	4.18	103	-18.7	.116	41	.29	-80
5.0	.70	-120	11.2	3.65	92	-17.9	.127	36	.25	-90
6.0	.68	-139	10.0	3.18	80	-17.6	.132	31	.19	-113
7.0	.71	-157	8.6	2.69	69	-17.5	.133	25	.18	-156
8.0	.72	168	7.4	2.35	60	-17.5	.133	22	.20	-178
9.0	.71	-177	6.5	2.12	53	-17.4	.135	19	.22	174
10.0	.70	175	6.0	1.99	46	-16.9	.143	17	.22	169
11.0	.70	167	5.5	1.88	38	-16.6	.148	15	.23	164
12.0	.70	162	5.0	1.77	31	-16.3	.154	13	.24	153
13.0	.70	159	4.5	1.68	25	-15.8	.162	11	.26	143
14.0	.70	155	4.1	1.61	20	-15.5	.168	10	.28	133
15.0	.73	149	3.9	1.56	14	-15.0	.177	8	.30	123
16.0	.77	138	3.2	1.45	5	-14.7	.184	6	.32	119
17.0	.76	134	1.8	1.23	0	-14.4	.190	5	.35	114
18.0	.77	134	1.3	1.16	-1	-13.9	.201	4	.38	106

$T_A = 25°C$, $V_{DS} = 4$ V, $I_{DS} = 70$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
MHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
1.0	.87	-60	20.6	10.72	136	-26.4	.048	55	.33	-59
2.0	.74	-96	17.5	7.50	113	-23.5	.067	43	.29	-66
3.0	.72	-112	15.2	5.77	101	-22.2	.078	39	.28	-69
4.0	.67	-122	13.4	4.68	91	-21.3	.086	38	.27	-72
5.0	.67	-137	12.0	3.97	81	-20.6	.093	36	.24	-77
6.0	.68	-154	10.5	3.36	70	-20.3	.097	35	.17	-95
7.0	.73	-168	9.0	2.81	61	-20.1	.099	33	.13	-127
8.0	.74	-177	7.7	2.44	54	-19.8	.102	31	.12	-159
9.0	.75	175	6.8	2.19	47	-19.6	.105	31	.12	-165
10.0	.75	166	6.2	2.04	39	-18.9	.113	29	.13	-171
11.0	.75	156	5.6	1.90	32	-18.4	.120	27	.13	-177
12.0	.74	150	5.1	1.79	25	-17.9	.128	26	.14	173
13.0	.74	148	4.6	1.69	19	-16.9	.143	25	.15	166
14.0	.75	145	4.2	1.62	14	-16.2	.155	24	.17	154
15.0	.76	140	3.9	1.57	9	-15.7	.164	21	.21	142
16.0	.77	135	3.2	1.45	-1	-15.5	.168	18	.24	133
17.0	.79	130	1.8	1.23	-6	-15.3	.171	18	.28	125
18.0	.80	125	1.3	1.16	-6	-14.4	.191	18	.32	117

HEWLETT PACKARD

ATF-10136
0.5-12 GHz Low Noise Gallium Arsenide FET

Features

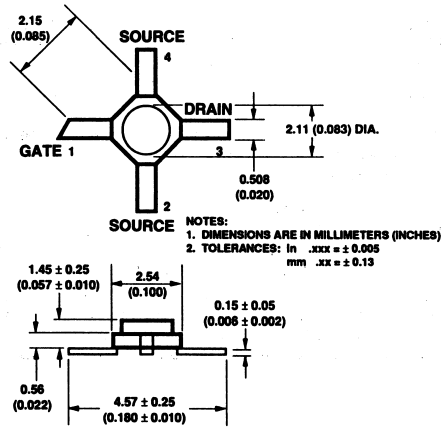
- **Low Noise Figure: 0.5 dB typical at 4 GHz**
- **Low Bias: V_{DS} = 2 V, I_{DS} = 20 mA**
- **High Associated Gain: 13.0 dB typical at 4 GHz**
- **High Output Power: 20.0 dBm typical $P_{1\,dB}$ at 4 GHz**
- **Cost Effective Ceramic Microstrip Package**
- **Tape-and-Reel Packaging Option Available[2]**

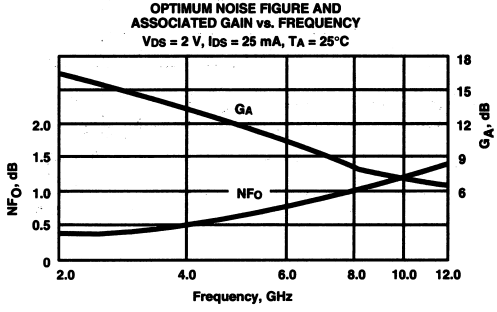
Description

The ATF-10136 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a cost effective microstrip package. Its premium noise figure makes this device appropriate for use in the first stage of low noise amplifiers operating in the 0.5-12 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length using airbridge interconnects between drain fingers. Total gate periphery is 500 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

36 micro-X Package[1]





Noise Parameters: V_{DS} = 2 V, I_{DS} = 25 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
1.0	0.4	.85	24	.70
2.0	0.4	.70	47	.46
4.0	0.5	.39	126	.36
6.0	0.8	.36	–170	.12
8.0	1.1	.45	–100	.38

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 2 V, I_{DS} = 25 mA	f = 2.0 GHz f = 4.0 GHz f = 6.0 GHz	dB dB dB		0.4 0.5 0.8	 0.6
G_A	Gain @ NF_O: V_{DS} = 2 V, I_{DS} = 25 mA	f = 2.0 GHz f = 4.0 GHz f = 6.0 GHz	dB dB dB	 12.0 	16.5 13.0 11.0	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 4 V, I_{DS} = 70 mA	f = 4.0 GHz	dBm		20.0	
$G_{1\,dB}$	1dB Compressed Gain: V_{DS} = 4 V, I_{DS} = 70 mA	f = 4.0 GHz	dB		12.0	
gm	Transconductance: V_{DS} = 2 V, V_{GS} = 0 V		mmho	70	140	
I_{DSS}	Saturated Drain Current: V_{DS} = 2 V, V_{GS} = 0 V		mA	70	130	180
V_P	Pinchoff Voltage: V_{DS} = 2 V, I_{DS} = 1 mA		V	–4.0	–1.3	–0.5

Notes: 1. Long leaded 35 Package available upon request.
2. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors".

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+5 V
Gate-Source Voltage	V_{GS}	–4 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	430 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature[4]	T_{STG}	–65°C to +175°C

Thermal Resistance: θ_{jc} = 350°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm Spot Size[5]

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 2.9 mW/°C for T_{CASE} > 25°C.
4. Storage above +150°C may tarnish the leads of this package difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safety stored up to 175°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

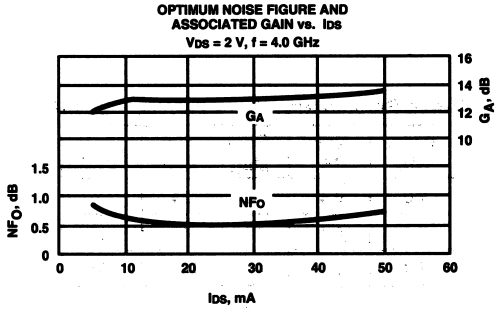
Part Number Ordering Information

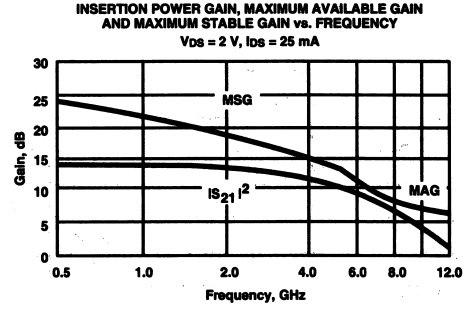
Part Number	Devices Per Reel	Reel Size
ATF-10136-TR1	1000	7"
ATF-10136-TR2	4000	13"
ATF-10136-STR	1	STRIP

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

Typical Performance, T_A = 25°C

(unless otherwise noted)





Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 2 V, I_{DS} = 25 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.5	.98	–18	14.5	5.32	163	–34.0	.020	78	.35	–9
1.0	.93	–33	14.3	5.19	147	–28.4	.038	67	.36	–19
2.0	.79	–66	13.3	4.64	113	–22.6	.074	59	.30	–31
3.0	.64	–94	12.2	4.07	87	–19.2	.110	44	.27	–42
4.0	.54	–120	11.1	3.60	61	–17.3	.137	31	.22	–49
5.0	.47	–155	10.1	3.20	37	–15.5	.167	13	.16	–54
6.0	.45	162	9.2	2.88	13	–14.3	.193	–2	.08	–17
7.0	.50	120	8.0	2.51	–10	–13.9	.203	–19	.16	45
8.0	.60	87	6.4	2.09	–32	–13.6	.210	–36	.32	48
9.0	.68	61	4.9	1.75	–51	–13.6	.209	–46	.44	38
10.0	.73	42	3.6	1.52	–66	–13.7	.207	–58	.51	34
11.0	.77	26	2.0	1.26	–82	–13.8	.205	–73	.54	27
12.0	.80	14	1.0	1.12	–97	–14.0	.200	–82	.54	15

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

ATF-10170
0.5-12 GHz Low Noise Gallium Arsenide FET

Features

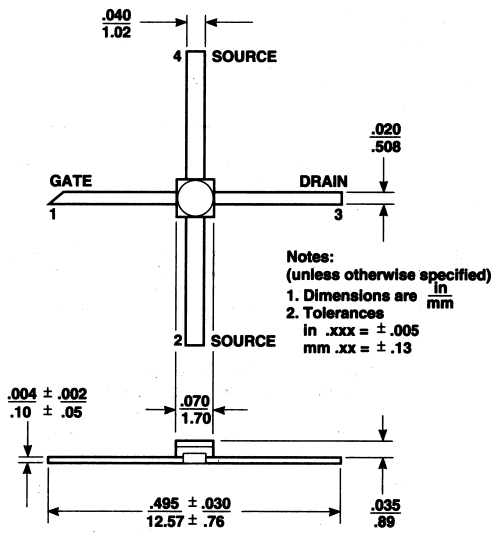
- **Low Noise Figure: 0.5 dB typical at 4 GHz**
- **Low Bias: V_{DS} = 2 V, I_{DS} = 25 mA**
- **High Associated Gain: 14.0 dB typical at 4 GHz**
- **High Output Power: 21.0 dBm typical $P_{1\ dB}$ at 4 GHz**
- **Hermetic Gold-Ceramic Microstrip Package**

Description

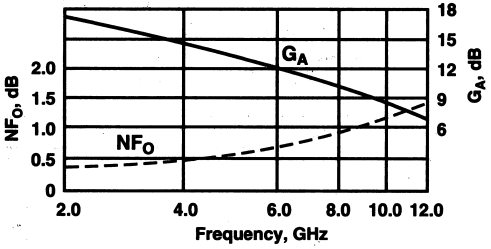
The ATF-10170 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a hermetic, high reliability package. Its noise figure makes this device appropriate for use in the first stage of low noise amplifiers operating in the 0.5-12 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length using airbridge interconnects between drain fingers. Total gate periphery is 500 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

70 mil Package



Optimum Noise Figure and Associated Gain vs. Frequency
V_{DS} = 2 V, I_{DS} = 25 mA, T_A = 25°C



Noise Parameters: V_{DS} = 2 V, I_{DS} = 25 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
1.0	0.4	.87	23	.42
2.0	0.4	.73	47	.34
4.0	0.5	.46	95	.17
6.0	0.7	.44	131	.30
8.0	0.9	.43	162	.44

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 2 V, I_{DS} = 25 mA	f = 2.0 GHz f = 4.0 GHz f = 6.0 GHz	dB dB dB		0.4 0.5 0.7	0.6
G_A	Gain @ NF_O: V_{DS} = 2 V, I_{DS} = 25 mA	f = 2.0 GHz f = 4.0 GHz f = 6.0 GHz	dB dB dB	12.5	17.0 14.0 12.0	
$P_{1\ dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 4 V, I_{DS} = 70 mA	f = 4.0 GHz	dBm		21.0	
$G_{1\ dB}$	1dB Compressed Gain: V_{DS} = 4 V, I_{DS} = 70 mA	f = 4.0 GHz	dB		15.0	
g_m	Transconductance: V_{DS} = 2 V, V_{GS} = 0 V		mmho	80	140	
I_{DSS}	Saturated Drain Current: V_{DS} = 2 V, V_{GS} = 0 V		mA	70	130	180
V_P	Pinchoff Voltage: V_{DS} = 2 V, I_{DS} = 1 mA		V	-3.0	-1.3	-0.8

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum
Drain-Source Voltage	V_{DS}	+5 V
Gate-Source Voltage	V_{GS}	-4 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	430mW
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	-65 to +175°C

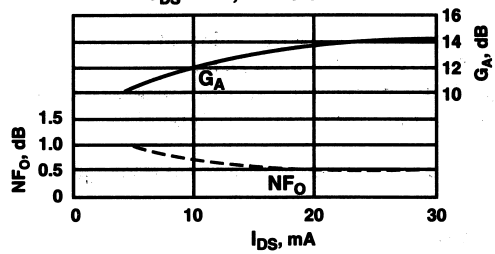
Thermal Resistance: θ_{jc} = 325°C/W TCH = 150°C
Liquid Crystal Measurement; 1µm Spot Size[4]

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 3.1 mW/°C for T_{case} > 35°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See APPLICATIONS PRIMER IIIA for more information.

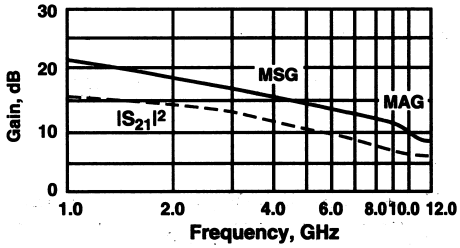
Typical Performance, T_A = 25°C

(Unless otherwise noted)

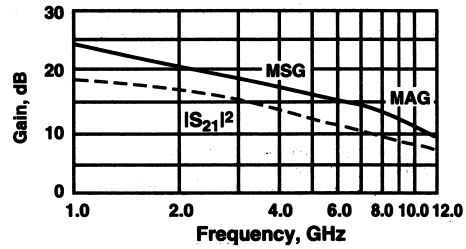
Optimum Noise Figure and Associated Gain vs. I_{DS}
V_{DS} = 2 V, f = 4.0 GHz



Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency
V_{DS} = 2 V, I_{DS} = 25 mA



Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency
V_{DS} = 4 V, I_{DS} = 70 mA



Typical Scattering Parameters: Common Source Z_O = 50 Ω

T_A = 25°C, V_{DS} = 2 V, I_{DS} = 25 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
MHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
1.0	.95	-40	15.6	6.05	148	-27.3	.043	66	.27	-39
2.0	.88	-74	14.4	5.27	121	-22.5	.075	47	.24	-74
3.0	.81	-100	13.1	4.54	100	-20.2	.097	34	.22	-100
4.0	.74	-125	11.8	3.87	79	-19.0	.112	22	.20	-125
5.0	.70	-146	10.5	3.35	61	-18.2	.123	11	.18	-146
6.0	.66	-165	9.5	2.97	45	-17.5	.134	1	.17	-166
7.0	.64	180	8.6	2.70	29	-16.8	.144	-8	.16	177
8.0	.63	169	8.0	2.52	18	-16.3	.153	-13	.15	166
9.0	.60	153	7.4	2.35	2	-15.8	.163	-23	.14	153
10.0	.57	138	6.8	2.19	-13	-15.1	.175	-34	.13	140
11.0	.55	121	6.4	2.09	-28	-14.7	.185	-44	.12	123
12.0	.54	104	6.2	2.05	-43	-14.1	.197	-56	.11	105

T_A = 25°C, V_{DS} = 4 V, I_{DS} = 70 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
MHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
1.0	.93	-44	18.2	8.13	145	-29.1	.035	64	.32	-35
2.0	.83	-81	16.7	6.81	116	-24.6	.059	47	.27	-63
3.0	.76	-108	15.1	5.68	96	-22.5	.075	38	.23	-82
4.0	.70	-132	13.5	4.73	76	-21.2	.087	27	.20	-102
5.0	.65	-153	12.1	4.03	59	-20.2	.098	18	.18	-120
6.0	.62	-170	11.0	3.55	43	-19.4	.107	10	.16	-135
7.0	.60	174	10.1	3.20	27	-18.7	.116	2	.15	-145
8.0	.58	163	9.4	2.95	17	-18.0	.126	-2	.14	-151
9.0	.56	148	8.7	2.73	2	-17.2	.138	-11	.14	-161
10.0	.54	133	8.2	2.56	-13	-16.5	.149	-21	.14	-171
11.0	.52	117	7.7	2.43	-28	-15.9	.161	-131	.13	-179
12.0	.51	101	7.4	2.35	-43	-14.6	.174	-43	.12	172

HEWLETT PACKARD

ATF-10236
0.5-12 GHz Low Noise Gallium Arsenide FET

Features

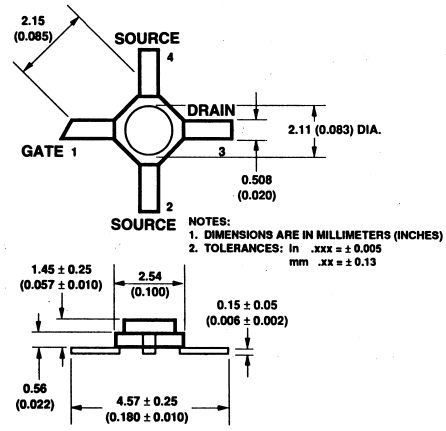
- **Low Noise Figure: 0.8 dB typical at 4 GHz**
- **Low Bias: V_{DS} = 2V, I_{DS} = 20 mA**
- **High Associated Gain: 13.0 dB typical at 4 GHz**
- **High Output Power: 20.0 dBm typical $P_{1\,dB}$ at 4 GHz**
- **Cost Effective Ceramic Microstrip Package**
- **Tape-And-Reel Packaging Option Available[2]**

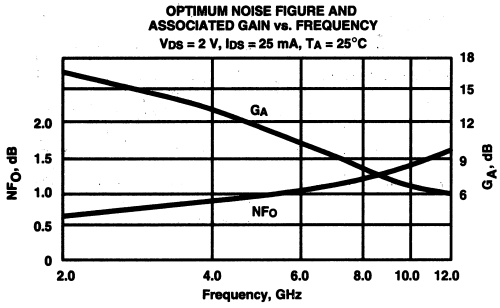
Description

The ATF-10236 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a cost effective microstrip package. Its low noise figure makes this device appropriate for use in the second stage of low noise amplifiers operating in the 0.5-12 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length using airbridge interconnects between drain fingers. Total gate periphery is 500 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

36 micro-X Package[1]





Noise Parameters: V_{DS} = 2 V, I_{DS} = 25 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
1.0	0.5	.87	36	.63
2.0	0.6	.73	74	.33
4.0	0.8	.45	148	.15
6.0	1.0	.42	–137	.12
8.0	1.3	.49	–80	.45

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 2 V, I_{DS} = 25 mA	f = 2.0 GHz f = 4.0 GHz f = 6.0 GHz	dB dB dB		0.6 0.8 1.0	 1.0
G_A	Gain @ NF_O: V_{DS} = 2 V, I_{DS} = 25 mA	f = 2.0 GHz f = 4.0 GHz f = 6.0 GHz	dB dB dB	 12.0 	16.5 13.0 10.5	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 4 V, I_{DS} = 70 mA	f = 4.0 GHz	dBm		20.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 4 V, I_{DS} = 70 mA	f = 4.0 GHz	dB		12.0	
g_m	Transconductance: V_{DS} = 2 V, V_{GS} = 0 V		mmho	80	140	
I_{DSS}	Saturated Drain Current: V_{DS} = 2 V, V_{GS} = 0 V		mA	70	130	180
V_P	Pinchoff Voltage: V_{DS} = 2 V, I_{DS} = 1 mA		V	–3.0	–1.3	–0.8

Notes: 1. Long leaded 35 package available upon request.
2. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors".

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+5 V
Gate-Source Voltage	V_{GS}	–4 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	430 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature[4]	T_{STG}	175°C

Thermal Resistance: θ_{jc} = 350°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 µm Spot Size[5]

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 2.9 mW/°C for T_{CASE} > 25°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safely stored up to 175°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

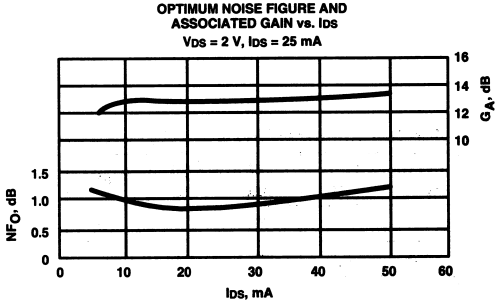
Part Number Ordering Information

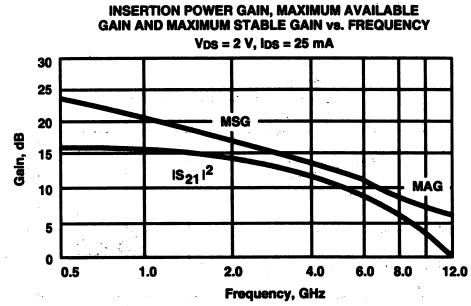
Part Number	Devices Per Reel	Reel Size
ATF-10236-TR1	1000	7"
ATF-10236-TR2	4000	13"
ATF-10236-STR	1	STRIP

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

Typical Performance, T_A = 25°C

(unless otherwise noted)





Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 2 V, I_{DS} = 25 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.5	.97	–20	15.1	5.68	162	–32.8	.023	76	.47	–11
1.0	.93	–41	14.9	5.58	143	–26.0	.050	71	.45	–23
2.0	.77	–81	13.6	4.76	107	–21.3	.086	51	.36	–38
3.0	.59	–114	12.2	4.06	80	–18.4	.120	35	.30	–51
4.0	.48	–148	10.9	3.51	52	–16.5	.149	18	.23	–67
5.0	.46	166	9.6	3.03	26	–15.3	.172	3	.10	–67
6.0	.53	125	8.5	2.65	1	–14.5	.189	–14	.09	48
7.0	.62	96	6.9	2.22	–20	–14.4	.191	–28	.24	55
8.0	.71	73	4.9	1.75	–39	–14.5	.189	–41	.37	51
9.0	.75	54	3.3	1.47	–55	–14.7	.184	–46	.46	42
10.0	.78	39	2.1	1.28	–72	–14.9	.180	–59	.51	34
11.0	.82	26	0.3	1.04	–86	–14.9	.179	–71	.54	26
12.0	.84	12	–0.5	0.95	–101	–15.0	.177	–82	.54	17

A model for this device is available in the DEVICE MODELS section.

ATF-10736 (ATF-20136)
0.5-12 GHz General Purpose Gallium Arsenide FET

Features

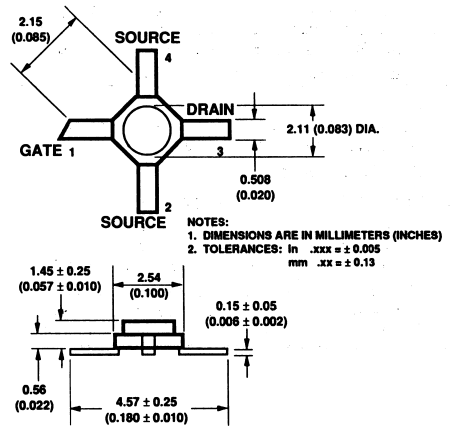
- **High Associated Gain: 12.5 dB typical at 4 GHz**
- **Low Bias: V_{DS} = 2 V, I_{DS} = 20 mA**
- **High Output Power: 20.0 dBm typical $P_{1\,dB}$ at 4 GHz**
- **Low Noise Figure: 1.2 dB typical at 4 GHz**
- **Cost Effective Ceramic Microstrip Package**
- **Tape-and-Reel Packaging Option Available[2]**

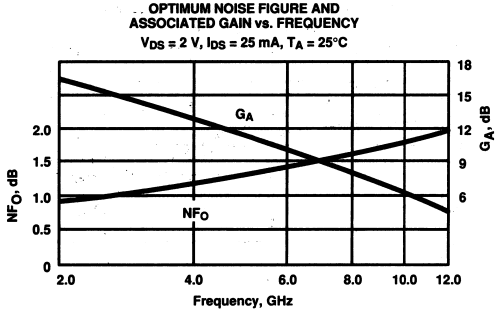
Description

The ATF-10736 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a cost effective microstrip package. Its noise figure makes this device appropriate for use in the gain stages of low noise amplifiers operating in the 0.5-12 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length using airbridge interconnects between drain fingers. Total gate periphery is 500 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

36 micro-X Package[1]





Noise Parameters: V_{DS} = 2 V, I_{DS} = 25 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
1.0	0.8	.88	41	.52
2.0	0.9	.75	85	.27
4.0	1.2	.48	159	.08
6.0	1.4	.46	–122	.08
8.0	1.7	.53	–71	.43

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 2 V, I_{DS} = 25 mA	f = 2.0 GHz f = 4.0 GHz f = 6.0 GHz	dB dB dB		0.9 1.2 1.4	 1.4
G_A	Gain @ NF_O: V_{DS} = 2 V, I_{DS} = 25 mA	f = 2.0 GHz f = 4.0 GHz f = 6.0 GHz	dB dB dB	 12.0 	16.5 13.0 10.5	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 4 V, I_{DS} = 70 mA	f = 4.0 GHz	dBm		20.0	
$G_{1\,dB}$	1dB Compressed Gain: V_{DS} = 4 V, I_{DS} = 70 mA	f = 4.0 GHz	dB		12.0	
g_m	Transconductance: V_{DS} = 2 V, V_{GS} = 0 V		mmho	70	140	
I_{DSS}	Saturated Drain Current: V_{DS} = 2 V, V_{GS} = 0 V		mA	70	130	180
V_P	Pinchoff Voltage: V_{DS} = 2 V, I_{DS} = 1 mA		V	–4.0	–1.3	–0.5

Notes: 1. Long leaded 35 Package available upon request.
2. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors".

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+5 V
Gate-Source Voltage	V_{GS}	–4 V
Drain Current	I_{DS}	I_{DSS}
Total Power Dissipation[2,3]	P_T	430 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature[4]	T_{STG}	–65°C to +175°C

Thermal Resistance: θ_{jc} = 350°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm Spot Size[5]

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 2.9 mW/°C for T_{CASE} > 25°C.
4. Storage above +150°C may tarnish the leads of this package difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safety stored up to 175°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

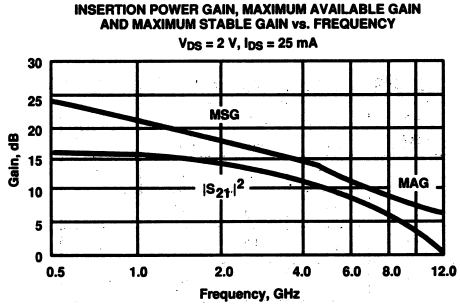
Part Number Ordering Information

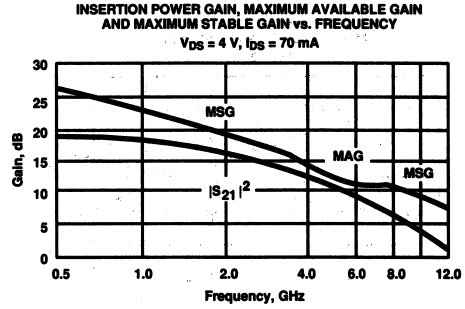
Part Number	Devices Per Reel	Reel Size
ATF-10736-TR1	1000	7"
ATF-10736-TR2	4000	13"
ATF-10736-STR	1	STRIP

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

Typical Performance, T_A = 25°C

(unless otherwise noted)





Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 2 V, I_{DS} = 25 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.5	.96	–20	15.4	5.90	162	–32.4	.024	77	.50	–10
1.0	.92	–40	15.2	5.77	144	–26.7	.046	66	.48	–21
2.0	.77	–76	13.8	4.92	109	–21.3	.086	52	.39	–34
3.0	.59	–107	12.5	4.20	83	–20.0	.111	40	.33	–45
4.0	.49	–136	11.2	3.64	57	–17.3	.137	24	.26	–61
5.0	.43	–179	10.0	3.15	32	–15.5	.167	9	.14	–65
6.0	.49	138	8.6	2.74	8	–14.9	.179	–5	.05	22
7.0	.57	106	7.3	2.32	–13	–14.8	.183	–18	.19	60
8.0	.68	81	5.6	1.92	–32	–14.7	.185	–33	.33	57
9.0	.73	62	4.2	1.62	–50	–14.8	.183	–40	.42	46
10.0	.77	47	3.0	1.41	–66	–14.8	.182	–52	.46	38
11.0	.82	36	1.0	1.12	–81	–14.6	.186	–67	.50	27
12.0	.85	22	–0.2	0.98	–97	–14.5	.189	–75	.51	15

T_A = 25°C, V_{DS} = 4 V, I_{DS} = 70 mA

0.5	.90	–32	19.0	8.95	147	–34.9	.018	77	.40	–7
1.0	.79	–53	18.0	7.96	128	–28.6	.037	70	.38	–17
2.0	.57	–96	15.5	5.99	90	–22.5	.075	56	.34	–38
3.0	.43	–129	13.3	4.60	64	–19.5	.106	43	.31	–50
4.0	.36	–163	11.6	3.78	39	–17.3	.136	31	.28	–51
5.0	.35	156	10.1	3.21	16	–15.6	.166	14	.22	–45
6.0	.47	110	8.8	2.76	–11	–14.5	.189	–5	.15	–4
7.0	.65	78	7.0	2.23	–36	–14.2	.196	–23	.28	35
8.0	.77	58	5.1	1.80	–56	–14.1	.198	–38	.42	37
9.0	.83	44	3.5	1.50	–72	–14.2	.195	–48	.51	33
10.0	.86	30	2.4	1.32	–88	–14.5	.188	–64	.55	26
11.0	.87	16	1.1	1.13	–106	–14.8	.182	–77	.60	18
12.0	.91	1	–0.1	0.99	–123	–15.3	.171	–91	.65	7

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

ATF-13036
2-16 GHz Low Noise Gallium Arsenide FET

Features

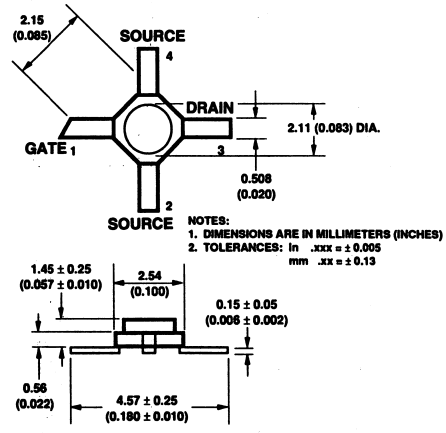
- **Low Noise Figure: 1.1 dB typical at 12 GHz**
- **High Associated Gain: 9.5 dB typical at 12 GHz**
- **High Output Power: 17.5 dBm typical $P_{1\,dB}$ at 12 GHz**
- **Cost Effective Ceramic Microstrip Package**
- **Tape-and-Reel Packaging Option Available[2]**

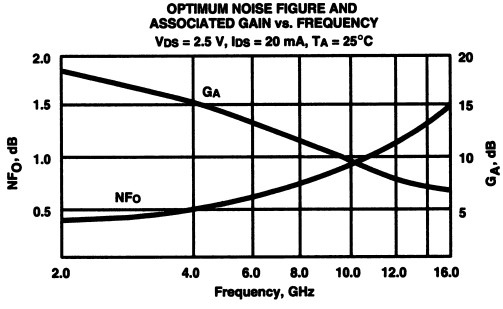
Description

The ATF-13036 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a cost effective microstrip package. Its premium noise figure makes this device appropriate for use in the first stage of low noise amplifiers operating in the 2-16 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery is 250 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

36 micro-X Package[1]





Noise Parameters: V_{DS} = 2.5 V, I_{DS} = 20 mA

Freq. GHz	NFO dB	Gamma Opt Mag	Gamma Opt Ang	RN/50
2.0	0.4	.80	29	0.23
4.0	0.5	.54	70	0.22
6.0	0.7	.47	107	0.13
8.0	0.8	.27	164	0.17
12.0	1.1	.33	–55	0.32
14.0	1.3	.42	–12	0.38

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NFO	Optimum Noise Figure:	f = 8.0 GHz	dB		0.8	
	V_{DS} = 2.5 V, I_{DS} = 15 - 30 mA	f = 12.0 GHz	dB		1.1	1.2
		f = 14.0 GHz	dB		1.3	
GA	Gain @ NFO: V_{DS} = 2.5 V, I_{DS} = 15 - 30 mA	f = 8.0 GHz	dB		11.5	
		f = 12.0 GHz	dB	9.0	9.5	
		f = 14.0 GHz	dB		8.0	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 4 V, I_{DS} = 40 mA	f = 12.0 GHz	dBm		17.5	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 4 V, I_{DS} = 40 mA	f = 12.0 GHz	dB		8.5	
gm	Transconductance: V_{DS} = 2.5 V, V_{GS} = 0 V		mmho	25	55	
IDSS	Saturated Drain Current: V_{DS} = 2.5 V, V_{GS} = 0 V		mA	40	50	90
VP	Pinchoff Voltage: V_{DS} = 2.5 V, I_{DS} = 1 mA		V	–4.0	–1.5	–0.5

Notes: 1. Long leaded 35 package available upon request.
2. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors".

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+5 V
Gate-Source Voltage	V_{GS}	–4 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	225 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature[4]	T_{STG}	–65°C to +175°C

Thermal Resistance: θ_{jc} = 400°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm Spot Size[5]

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 2.5 mW/°C for T_{CASE} > 85°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safely stored up to 175°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

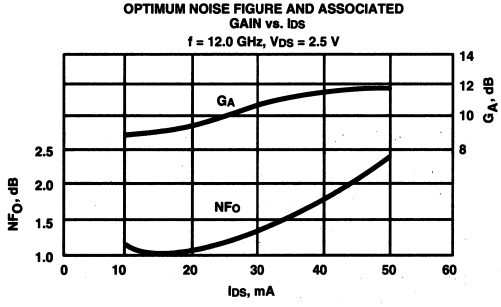
Part Number Ordering Information

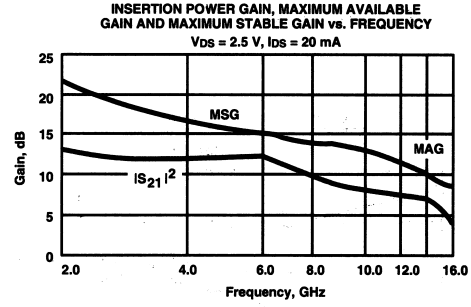
Part Number	Devices Per Reel	Reel Size
ATF-13036-TR1	1000	7"
ATF-13036-TR2	4000	13"
ATF-13036-STR	1	STRIP

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

Typical Performance, T_A = 25°C

(unless otherwise noted)





Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 2.5 V, I_{DS} = 20 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
2.0	.96	–40	12.4	4.19	134	–28.0	.040	67	.56	–20
3.0	.88	–52	11.4	3.72	112	–25.5	.053	58	.58	–27
4.0	.81	–66	11.5	3.77	93	–22.7	.073	50	.55	–34
5.0	.68	–98	12.0	3.99	73	–20.1	.099	31	.43	–54
6.0	.55	–137	11.5	3.75	52	–19.0	.112	14	.30	–80
7.0	.53	–168	11.0	3.53	27	–18.1	.125	0	.21	–103
8.0	.51	161	10.3	3.27	2	–17.1	.139	–11	.14	–135
9.0	.51	120	10.2	3.25	–19	–16.1	.156	–25	.10	163
10.0	.56	84	9.2	2.87	–41	–16.1	.157	–43	.18	110
11.0	.60	50	8.3	2.61	–61	–16.2	.155	–55	.24	87
12.0	.62	44	7.8	2.45	–84	–16.7	.147	–62	.26	64
13.0	.64	36	7.3	2.32	–102	–17.0	.141	–73	.27	46
14.0	.67	16	6.6	2.14	–120	–17.9	.128	–85	.30	20
15.0	.73	–6	5.2	1.83	–139	–19.2	.110	–97	.36	–4
16.0	.77	–22	4.2	1.62	–157	–20.6	.093	–112	.39	–14

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

ATF-13100
2-18 GHz Low Noise Gallium Arsenide FET

Features

- **Low Noise Figure: 1.1 dB typical at 12 GHz**
- **High Associated Gain: 9.5 dB typical at 12 GHz**
- **High Output Power: 17.5 dBm typical $P_{1\,dB}$ at 12 GHz**

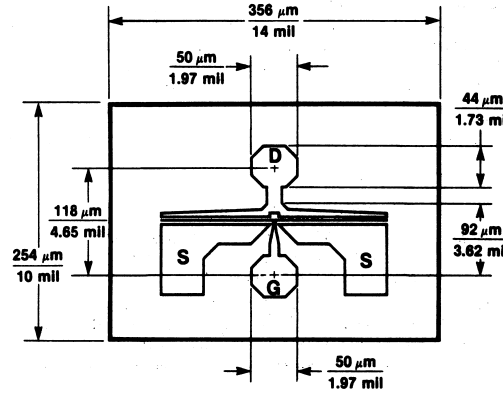
Description

The ATF-13100 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor chip. This device is designed for use in low noise, wideband amplifier and oscillator applications in the 2-18 GHz frequency range.

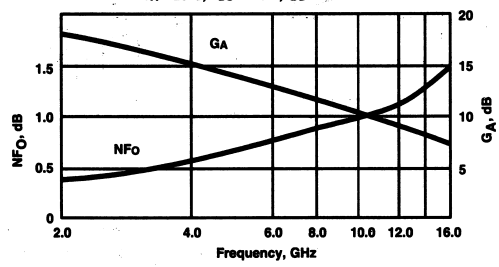
This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery of 250 microns. Proven gold based metalization systems and nitride passivation assure a rugged, reliable device.

The recommended mounting procedure is to die attach at a stage temperature of 300°C using a gold-tin preform under forming gas. Assembly can be preformed with either wedge or ball bonding using 0.7 mil gold wire. See also "Chip Use" in the APPLICATIONS section.

Chip Outline



OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN vs. FREQUENCY
T_A = 25°C, V_{DS} = 2.5 V, I_{DS} = 20 mA



Noise Parameters: V_{DS} = 2.5 V, I_{DS} = 20 mA

Freq. GHz	NFO dB	Gamma Opt Mag	Gamma Opt Ang	RN/50
4.0	0.5	.60	30	.32
6.0	0.7	.32	68	.21
8.0	0.8	.25	102	.15
12.0	1.1	.23	–165	.09
15.0	1.5	.32	–112	.21

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
NFO	Optimum Noise Figure: V_{DS} = 2.5 V, I_{DS} = 15 - 30 mA	f = 8.0 GHz	dB		0.8	
		f = 12.0 GHz	dB		1.1	1.2
		f = 15.0 GHz	dB		1.5	
GA	Gain @ NFO: V_{DS} = 2.5 V, I_{DS} = 15 - 30 mA	f = 8.0 GHz	dB		12.0	
		f = 12.0 GHz	dB	9.0	9.5	
		f = 15.0 GHz	dB		8.0	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 4 V, I_{DS} = 40 mA	f = 12.0 GHz	dBm		17.5	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 4 V, I_{DS} = 40 mA	f = 12.0 GHz	dB		8.5	
gm	Transconductance: V_{DS} = 2.5 V, V_{GS} = 0 V		mmho	30	55	
IDSS	Saturated Drain Current: V_{DS} = 2.5 V, V_{GS} = 0 V		mA	40	50	90
VP	Pinchoff Voltage: V_{DS} = 2.5 V, I_{DS} = 1 mA		V	–3.0	–1.5	–0.8

Note: 1. RF Performance is determined by assembling and testing 10 samples per wafer.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+5 V
Gate-Source Voltage	V_{GS}	–4 V
Drain Current	I_{DS}	I_{DSS}
Total Power Dissipation[2,3]	P_T	225 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	–65°C to +175°C

Thermal Resistance: θ_{jc} = 250°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm Spot Size[4]

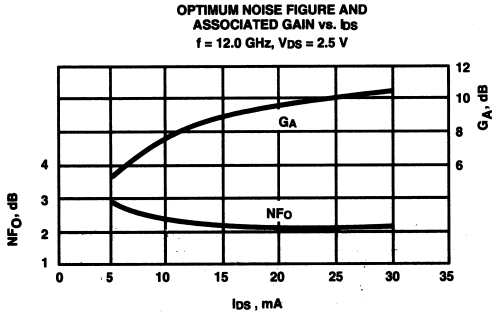
Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Mounting Surface Temperature = 25°C.
3. Derate at 4 mW/°C for $T_{MOUNTING\ SURFACE}$ > 119°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Part Number Ordering Information

Part Number	Devices Per Tray
ATF-13100-GP1	5
ATF-13100-GP3	50
ATF-13100-GP6	up to 300

Typical Performance, T_A = 25°C

(unless otherwise noted)



Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 2.5 V, I_{DS} = 20 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
2.0	.96	–27	13.4	4.68	153	–26.9	.045	75	.55	–16
3.0	.92	–41	13.4	4.65	140	–23.6	.066	67	.52	–24
4.0	.85	–58	13.1	4.54	126	–21.4	.085	59	.49	–33
5.0	.79	–76	12.9	4.40	113	–19.8	.102	50	.44	–41
6.0	.73	–95	12.4	4.19	100	–18.7	.116	42	.38	–48
7.0	.68	–113	12.0	3.97	87	–18.0	.126	34	.30	–54
8.0	.63	–132	11.4	3.71	75	–17.5	.134	25	.24	–64
9.0	.62	–151	10.9	3.51	63	–17.1	.140	18	.18	–75
10.0	.59	–167	10.3	3.27	53	–16.8	.144	11	.13	–84
11.0	.59	173	9.7	3.07	40	–16.5	.149	2	.08	–104
12.0	.57	155	9.0	2.83	30	–16.5	.150	–9	.02	160
13.0	.60	136	8.6	2.69	19	–16.4	.151	–16	.08	106
14.0	.64	116	7.9	2.47	7	–16.4	.151	–25	.15	103
15.0	.67	98	7.1	2.26	–6	–16.4	.152	–34	.23	100
16.0	.73	83	5.8	1.96	–16	–16.9	.143	–40	.31	90
17.0	.77	72	4.6	1.70	–26	–17.0	.141	–45	.36	82
18.0	.80	63	3.5	1.50	–35	–17.4	.135	–48	.40	72

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

ATF-13136
2-16 GHz Low Noise Gallium Arsenide FET

Features

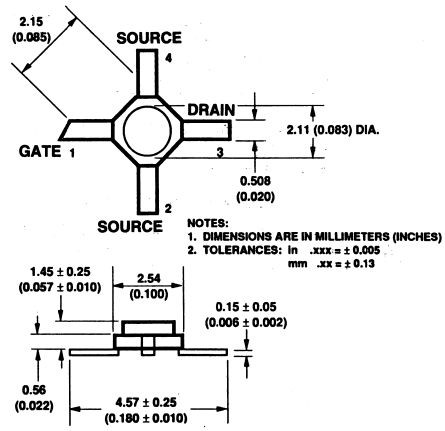
- **Low Noise Figure: 1.2 dB typical at 12 GHz**
- **High Associated Gain: 9.5 dB typical at 12 GHz**
- **High Output Power: 17.5 dBm typical $P_{1\,dB}$ at 12 GHz**
- **Cost Effective Ceramic Microstrip Package**
- **Tape-and-Reel Packaging Option Available[2]**

Description

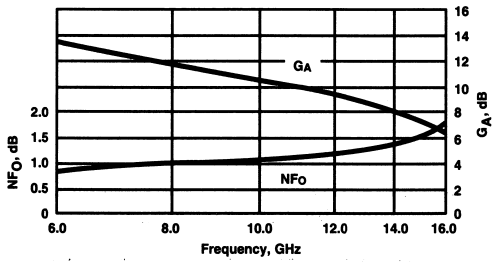
The ATF-13136 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a cost effective microstrip package. Its premium noise figure makes this device appropriate for use in the first stage of low noise amplifiers operating in the 2-16 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery of 250 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

36 micro-X Package[1]



OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN vs. FREQUENCY
V_{DS} = 2.5 V, I_{DS} = 20 mA, T_A = 25°C



Noise Parameters: V_{DS} = 3 V, I_{DS} = 20 mA

Freq. GHz	NFO dB	Gamma Opt Mag	Gamma Opt Ang	RN/50
4.0	0.5	.58	87	.22
6.0	0.8	.47	130	.18
8.0	1.0	.37	–163	.17
12.0	1.2	.47	–65	.80
14.0	1.4	.52	–15	1.20

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NFO	Optimum Noise Figure:	f = 8.0 GHz	dB		1.0	
	V_{DS} = 2.5 V, I_{DS} = 15 - 30 mA	f = 12.0 GHz	dB		1.2	1.4
		f = 14.0 GHz	dB		1.4	
GA	Gain @ NFO: V_{DS} = 2.5 V, I_{DS} = 15 - 30 mA	f = 8.0 GHz	dB		11.5	
		f = 12.0 GHz	dB	8.5	9.5	
		f = 14.0 GHz	dB		8.0	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 4 V, I_{DS} = 40 mA	f = 12.0 GHz	dBm		17.5	
$G_{1\,dB}$	1dB Compressed Gain: V_{DS} = 4 V, I_{DS} = 40 mA	f = 12.0 GHz	dB		8.5	
gm	Transconductance: V_{DS} = 2.5 V, V_{GS} = 0 V		mmho	25	55	
IDSS	Saturated Drain Current: V_{DS} = 2.5 V, V_{GS} = 0 V		mA	40	50	90
VP	Pinchoff Voltage: V_{DS} = 2.5 V, I_{DS} = 1 mA		V	–4.0	–1.5	–0.5

Notes: 1. Long leaded 35 package available upon request.
2. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors".

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+5 V
Gate-Source Voltage	V_{GS}	–4 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	225 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature[4]	T_{STG}	–65°C to +175°C

Thermal Resistance: θ_{jc} = 400°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm Spot Size[5]

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 2.5 mW/°C for T_{CASE} > 85°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safety stored up to 175°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Part Number Ordering Information

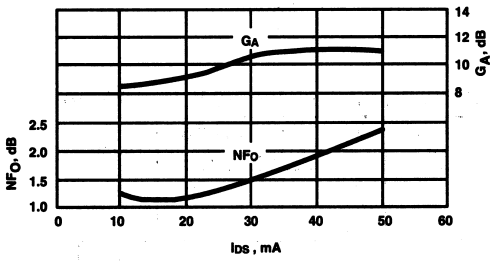
Part Number	Devices Per Reel	Reel Size
ATF-13136-TR1	1000	7"
ATF-13136-TR2	4000	13"
ATF-13136-STR	1	STRIP

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

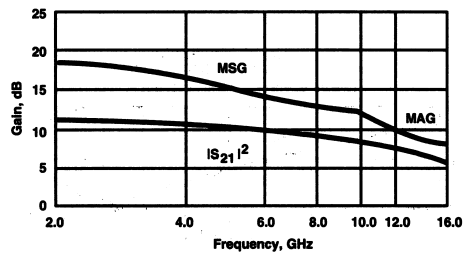
Typical Performance, T_A = 25°C

(unless otherwise noted)

OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN vs. I_{DS}
V_{DS} = 2.5 V, f = 12.0 GHz



INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{DS} = 2.5 V, I_{DS} = 20 mA



Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 2.5 V, I_{DS} = 20 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
2.0	.95	–42	11.2	3.65	134	–26.7	.046	62	.56	–37
3.0	.87	–65	10.7	3.43	112	–24.2	.062	40	.53	–47
4.0	.84	–85	10.3	3.28	93	–22.3	.077	31	.53	–54
5.0	.78	–104	10.1	3.21	73	–20.3	.097	18	.48	–62
6.0	.69	–128	10.4	3.30	52	–18.6	.117	7	.43	–76
7.0	.59	–163	10.4	3.32	27	–17.3	.137	–12	.35	–95
8.0	.54	157	9.8	3.10	2	–17.0	.142	–27	.26	–110
9.0	.55	121	9.2	2.89	–19	–16.3	.153	–43	.15	–119
10.0	.54	93	8.7	2.71	–41	–16.0	.159	–58	.07	–142
11.0	.56	64	8.1	2.54	–61	–16.2	.155	–73	.06	92
12.0	.61	37	7.4	2.34	–84	–16.8	.144	–89	.15	46
13.0	.65	19	6.8	2.18	–102	–17.6	.132	–100	.18	23
14.0	.65	7	6.4	2.09	–120	–18.0	.126	–114	.19	–2
15.0	.67	–6	5.9	1.98	–139	–18.2	.123	–119	.16	–27
16.0	.68	–25	5.3	1.84	–170	–18.4	.120	–134	.13	–30

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

ATF-13170
2-16 GHz Low Noise Gallium Arsenide FET

Features

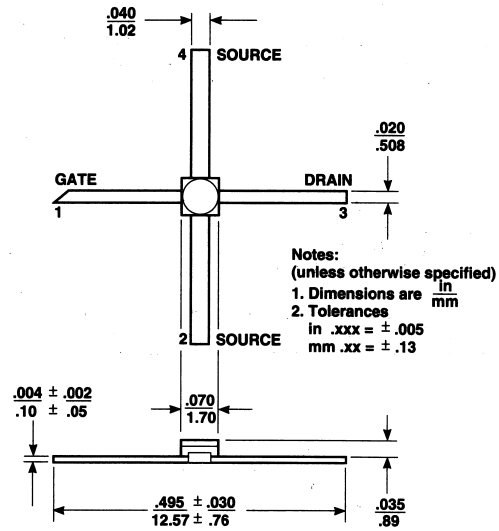
- **Low Noise Figure: 1.0 dB typical at 12 GHz**
- **High Associated Gain: 10.0 dB typical at 12 GHz**
- **High Output Power: 17.5 dBm typical $P_{1\,dB}$ at 12 GHz**
- **Hermetic Gold-Ceramic Microstrip Package**

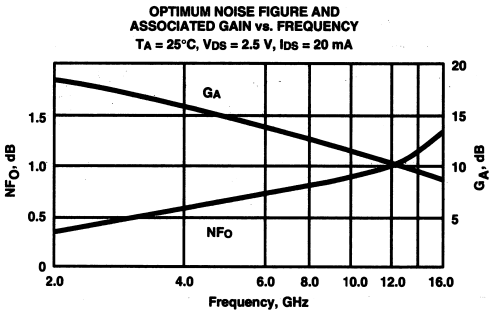
Description

The ATF-13170 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a hermetic, high reliability package. Its premium noise figure makes this device appropriate for use in low noise amplifiers operating in the 2-16 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery of 250 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

70 mil Package





Noise Parameters: V_{DS} = 3 V, I_{DS} = 20 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
4.0	0.5	.62	56	.44
6.0	0.7	.47	81	.34
8.0	0.8	.53	116	.19
12.0	1.0	.44	157	.12
14.0	1.3	.43	179	.07

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 2.5 V, I_{DS} = 20 mA	f = 8.0 GHz	dB		0.8	
		f = 12.0 GHz	dB		1.0	1.1
		f = 14.0 GHz	dB		1.3	
G_A	Gain @ NF_O: V_{DS} = 2.5 V, I_{DS} = 20 mA	f = 8.0 GHz	dB		12.0	
		f = 12.0 GHz	dB	9.0	10.0	
		f = 14.0 GHz	dB		8.5	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 4 V, I_{DS} = 40 mA	f = 12.0 GHz	dBm		17.5	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 4 V, I_{DS} = 40 mA	f = 12.0 GHz	dB		8.5	
g_m	Transconductance: V_{DS} = 2.5 V, V_{GS} = 0 V		mmho	30	55	
I_{DSS}	Saturated Drain Current: V_{DS} = 2.5 V, V_{GS} = 0 V		mA	40	50	90
V_P	Pinchoff Voltage: V_{DS} = 2.5 V, I_{DS} = 1 mA		V	–3.0	–1.5	–0.8

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+5 V
Gate-Source Voltage	V_{GS}	–4 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	225 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	–65°C to +175°C

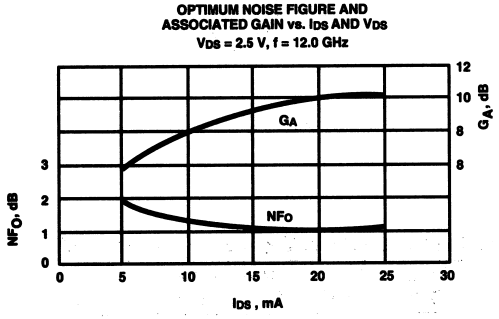
Thermal Resistance: θ_{jc} = 350°C/W; T_{CH} = 150°C
Liquid Crystal Measuremen; 1 μm Spot Size[4]

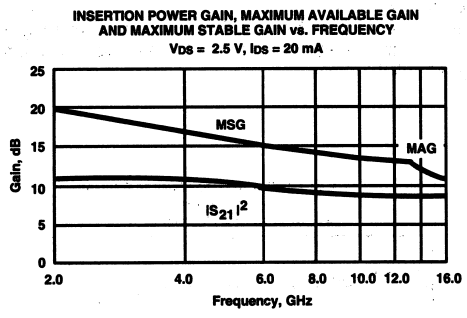
Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 2.9 mW/°C for T_{CASE} > 96°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)





Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 2.5 V, I_{DS} = 20 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
2.0	.97	–36	11.4	3.73	143	–28.4	.038	65	.48	–28
3.0	.94	–51	11.2	3.63	128	–25.3	.054	55	.47	–39
4.0	.90	–69	10.9	3.51	111	–23.1	.070	43	.45	–53
5.0	.86	–85	10.5	3.34	94	–21.6	.083	32	.44	–67
6.0	.82	–101	10.1	3.20	78	–20.6	.093	20	.42	–79
7.0	.77	–116	9.7	3.06	63	–19.8	.102	10	.41	–91
8.0	.74	–127	9.3	2.92	50	–19.3	.108	2	.40	–99
9.0	.70	–140	8.9	2.79	37	–18.7	.116	–7	.40	–109
10.0	.67	–153	8.7	2.73	23	–18.2	.123	–17	.41	–120
11.0	.64	–167	8.6	2.69	8	–17.7	.131	–28	.41	–130
12.0	.60	179	8.4	2.64	–7	–17.2	.137	–39	.40	–139
13.0	.57	166	8.3	2.59	–21	–16.8	.144	–50	.39	–148
14.0	.53	153	8.3	2.60	–33	–16.3	.153	–59	.38	–155
15.0	.48	136	8.3	2.61	–49	–15.6	.166	–73	.37	–167
16.0	.41	112	8.4	2.62	–67	–14.9	.180	–88	.34	180
17.0	.36	79	8.3	2.61	–86	–14.4	.191	–105	.26	170
18.0	.35	34	8.2	2.56	–107	–14.0	.200	–124	.17	170

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

ATF-13284
1-16 GHz Low Noise Gallium Arsenide FET

Features

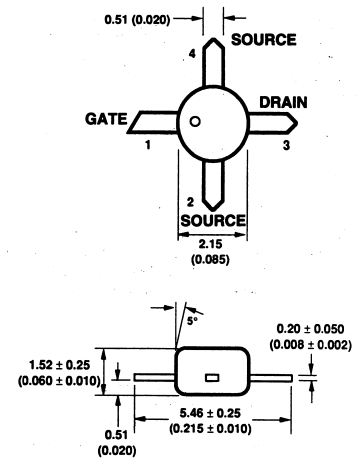
- **Low Noise Figure: 0.7 dB typical at 4 GHz**
- **High Associated Gain: 15.0 dB typical at 4 GHz**
- **High Output Power: 18.0 dBm typical $P_{1\,dB}$ at 4 GHz**
- **Low Cost Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Description

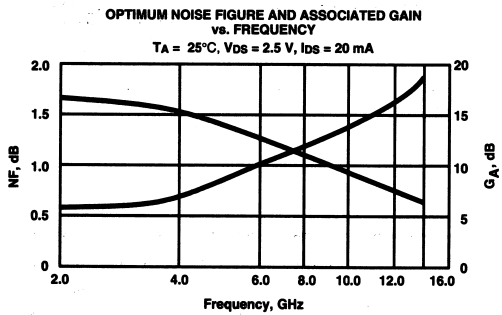
The ATF-13284 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a low cost plastic package. Its low noise figure makes this device appropriate for use in the first or second stages of low noise amplifiers operating in the 1-16 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery of 250 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

84 Plastic Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)



Noise Parameters: V_{DS} = 2.5 V, I_{DS} = 20 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_n/50$
1.0	0.6	.92	10	1.3
2.0	0.6	.85	21	1.2
4.0	0.7	.75	54	1.0
8.0	1.2	.57	144	0.3
12.0	1.6	.51	–118	0.1

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 2.5 V, I_{DS} = 15 - 30 mA	f = 4.0 GHz f = 12.0 GHz	dB dB		0.7 1.6	0.8
G_A	Gain @ NF_O: V_{DS} = 2.5 V, I_{DS} = 15 - 30 mA	f = 4.0 GHz f = 12.0 GHz	dB dB	13.0	15.0 8.5	
$P_{1\,dB}$	Power Output @ 1 dB Gain Compression: V_{DS} = 4 V, I_{DS} = 40 mA	f = 4.0 GHz	dBm		18.0	
$G_{1\,dB}$	1dB Compressed Gain: V_{DS} = 4 V, I_{DS} = 40 mA	f = 4.0 GHz	dB		15.0	
g_m	Transconductance: V_{DS} = 2.5 V, V_{GS} = 0 V		mmho	25	55	
I_{DSS}	Saturated Drain Current: V_{DS} = 2.5 V, V_{GS} = 0 V		mA	40	50	90
V_P	Pinchoff Voltage: V_{DS} = 2.5 V, I_{DS} = 1 mA		V	–4.0	–1.5	–0.5

Note: 1. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors".

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+5 V
Gate-Source Voltage	V_{GS}	–4 V
Drain Current	I_{DS}	I_{DSS}
Total Power Dissipation[2,3]	P_T	225 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	–65°C to +150°C

Thermal Resistance: θ_{jc} = 325°C/W; T_{CH} = 150°C
Liquid Crystal Measurment: 1 μm Spot Size[4]

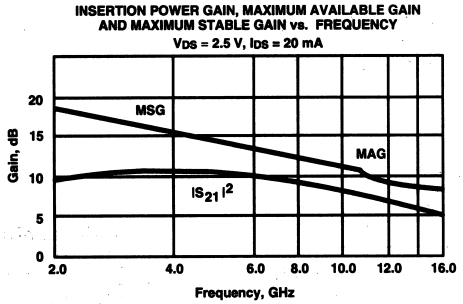
Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 3.1 mW/°C for T_C > 102°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Part Number Ordering Information

Part Number	Devices Per Reel	Reel Size
ATF-13284-TR1	1000	7"
ATF-13284-TR2	4000	13"
ATF-13284-STR	1	strip

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

Typical Performance, T_A = 25°C
(unless otherwise noted)



Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 2.5 V, I_{DS} = 20 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.5	.99	–11	10.2	3.22	169	–36.5	.015	80	.50	–11
1.0	.98	–21	10.2	3.24	157	–32.8	.023	74	.50	–17
2.0	.97	–33	10.3	3.26	145	–26.9	.045	67	.50	–24
3.0	.91	–52	10.4	3.30	127	–23.2	.069	55	.49	–37
4.0	.84	–73	10.5	3.36	108	–20.7	.092	42	.47	–50
5.0	.77	–91	10.2	3.23	91	–19.3	.109	31	.46	–61
6.0	.70	–108	9.8	3.08	76	–18.3	.121	22	.45	–71
7.0	.64	–123	9.3	2.93	62	–17.6	.132	14	.43	–79
8.0	.59	–142	9.1	2.85	47	–16.9	.153	5	.39	–89
9.0	.54	–166	8.8	2.74	30	–16.3	.153	–5	.33	–104
10.0	.51	168	8.3	2.59	14	–16.0	.159	–15	.25	–123
11.0	.51	147	7.4	2.34	–2	–16.2	.155	–22	.19	–151
12.0	.48	127	7.0	2.25	–12	–16.0	.159	–30	.14	–171
13.0	.51	108	6.7	2.17	–26	–15.9	.161	–35	.12	177
14.0	.57	87	6.1	2.02	–41	–16.0	.160	–46	.12	144
15.0	.59	70	5.6	1.90	–57	–16.1	.158	–53	.15	102
16.0	.62	58	5.1	1.79	–66	–16.1	.157	–59	.21	74
17.0	.63	46	4.6	1.69	–80	–16.1	.157	–67	.28	60
18.0	.64	35	3.7	1.53	–93	–16.1	.157	–84	.36	47

HEWLETT PACKARD

ATF-13336
2-16 GHz Low Noise Gallium Arsenide FET

Features

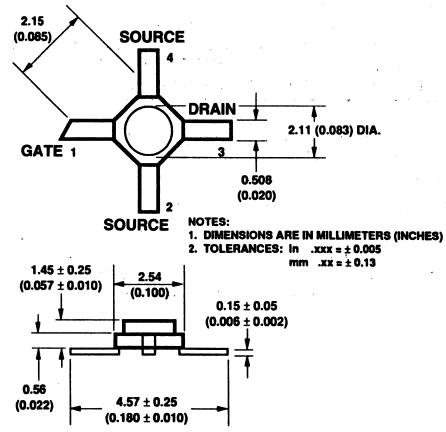
- **Low Noise Figure: 1.4 dB typical at 12 GHz**
- **High Associated Gain: 9.0 dB typical at 12 GHz**
- **High Output Power: 17.5 dBm typical $P_{1\,dB}$ at 12 GHz**
- **Cost Effective Ceramic Microstrip Package**
- **Tape-and-Reel Packaging Option Available[2]**

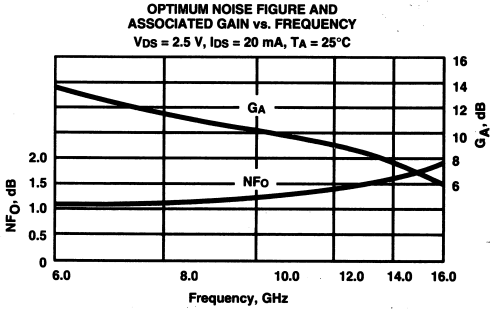
Description

The ATF-13336 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a cost effective microstrip package. Its premium noise figure makes this device appropriate for use in the second stage of low noise amplifiers operating in the 2-16 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery of 250 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

36 micro-X Package[1]





Noise Parameters: V_{DS} = 2.5 V, I_{DS} = 20 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
4.0	0.8	.63	93	.27
6.0	1.1	.47	138	.10
8.0	1.2	.40	–153	.20
12.0	1.4	.52	–45	.88
14.0	1.6	.57	–2	1.3

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 2.5 V, I_{DS} = 15 - 30 mA	f = 8.0 GHz f = 12.0 GHz f = 14.0 GHz	dB dB dB		1.2 1.4 1.6	1.6
G_A	Gain @ NF_O: V_{DS} = 2.5 V, I_{DS} = 15 - 30 mA	f = 8.0 GHz f = 12.0 GHz f = 14.0 GHz	dB dB dB	8.0	11.5 9.0 7.5	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 4 V, I_{DS} = 40 mA	f = 12.0 GHz	dBm		17.5	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 4 V, I_{DS} = 40 mA	f = 12.0 GHz	dB		8.5	
gm	Transconductance: V_{DS} = 2.5 V, V_{GS} = 0 V		mmho	25	55	
I_{DSS}	Saturated Drain Current: V_{DS} = 2.5 V, V_{GS} = 0 V		mA	40	50	90
V_P	Pinchoff Voltage: V_{DS} = 2.5 V, I_{DS} = 1 mA		V	–4.0	–1.5	–0.5

Notes: 1. Long leaded 35 Package available upon request.
2. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors".

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+5 V
Gate-Source Voltage	V_{GS}	–4 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	225 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature[4]	T_{STG}	–65°C to +175°C

Thermal Resistance: θ_{jc} = 400°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 µm Spot Size[5]

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 2.5 mW/°C for T_{CASE} > 85°C.
4. Storage above +150°C may tarnish the leads of this package difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safety stored up to 175°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

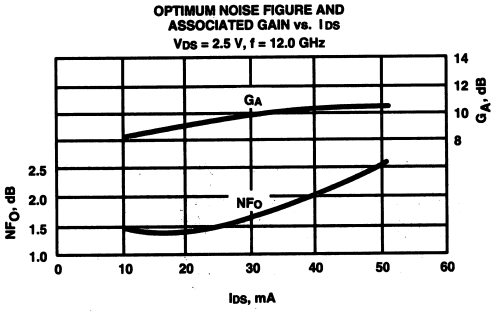
Part Number Ordering Information

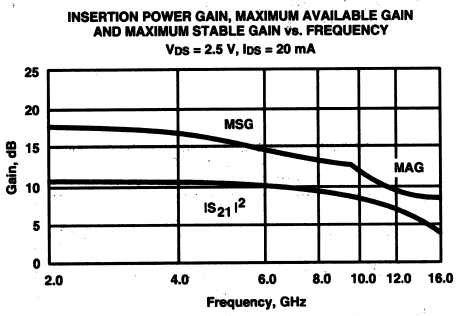
Part Number	Devices Per Reel	Reel Size
ATF-13336-TR1	1000	7"
ATF-13336-TR2	4000	13"
ATF-13336-STR	1	STRIP

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

Typical Performance, T_A = 25°C

(unless otherwise noted)





Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 2.5 V, I_{DS} = 20 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
2.0	.96	–51	10.6	3.39	127	–27.1	.044	57	.61	–41
3.0	.88	–75	10.3	3.28	106	–23.4	.060	33	.58	–51
4.0	.86	–96	10.1	3.19	86	–22.6	.074	25	.57	–57
5.0	.79	–117	9.9	3.13	66	–20.6	.093	12	.54	–65
.6.0	.69	–142	10.2	3.22	46	–18.9	.114	1	.49	–79
7.0	.60	–178	10.1	3.21	21	–17.6	.132	–18	.42	–97
8.0	.54	141	9.8	3.10	–4	–17.3	.137	–33	.31	–112
9.0	.56	103	8.9	2.80	–26	–16.7	.147	–48	.21	–121
10.0	.56	74	8.3	2.60	–48	–16.5	.150	–63	.09	–145
11.0	.58	44	7.6	2.39	–68	–16.8	.145	–78	.07	89
12.0	.63	20	6.7	2.17	–90	–17.5	.133	–95	.16	43
13.0	.65	3	6.0	2.00	–108	–18.3	.121	–107	.19	21
14.0	.66	–7	5.5	1.89	–126	–18.9	.114	–121	.19	–4
15.0	.70	–19	4.9	1.76	–144	–19.0	.112	–129	.16	–28
16.0	.72	–34	4.4	1.66	–175	–19.2	.110	–142	.14	–32

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

ATF-13484
1-16 GHz Low Noise Gallium Arsenide FET

Features

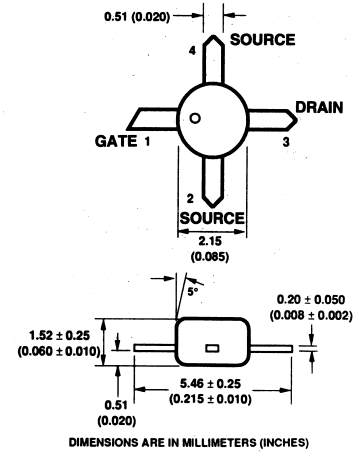
- **Low Noise Figure: 1.0 dB typical at 4 GHz**
- **High Associated Gain: 14.0 dB typical at 4 GHz**
- **High Output Power: 18.0 dBm typical $P_{1\,dB}$ at 4 GHz**
- **Low Cost Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Description

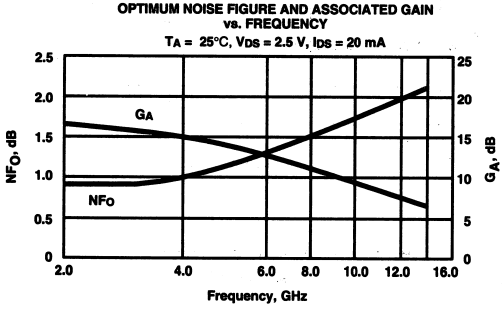
The ATF-13484 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a low cost plastic package. Its low noise figure makes this device appropriate for use in the first or second stages of low noise amplifiers operating in the 1-16 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery of 250 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

84 Plastic Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)



Noise Parameters: V_{DS} = 2.5 V, I_{DS} = 20 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_n/50$
1.0	0.8	.92	14	1.3
2.0	0.8	.85	28	1.1
4.0	1.0	.76	61	0.9
8.0	1.5	.60	152	0.2
12.0	2.0	.55	–104	0.2

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 2.5 V, I_{DS} = 15 - 30 mA	f = 4.0 GHz f = 12.0 GHz	dB dB		1.0 2.0	1.2
G_A	Gain @ NF_O: V_{DS} = 2.5 V, I_{DS} = 15 - 30 mA	f = 4.0 GHz f = 12.0 GHz	dB dB	12.0	14.0 7.5	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 4 V, I_{DS} = 40 mA	f = 4.0 GHz	dBm		18.0	
$G_{1\,dB}$	1dB Compressed Gain: V_{DS} = 4 V, I_{DS} = 40 mA	f = 4.0 GHz	dB		14.5	
gm	Transconductance: V_{DS} = 2.5 V, V_{GS} = 0 V		mmho	25	55	
I_{DSS}	Saturated Drain Current: V_{DS} = 2.5 V, V_{GS} = 0 V		mA	40	50	90
V_P	Pinchoff Voltage: V_{DS} = 2.5 V, I_{DS} = 1 mA		V	–4.0	–1.5	–0.5

Note: 1. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors".

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+5 V
Gate-Source Voltage	V_{GS}	–4 V
Drain Current	I_{DS}	I_{DSS}
Total Power Dissipation[2,3]	P_T	225 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	–65°C to +150°C

Thermal Resistance: θ_{jc} = 325°C/W; T_{CH} = 150°C
Liquid Crystal Measurement: 1 μm Spot Size[4]

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 3.1 mW/°C for T_C > 102°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Part Number Ordering Information

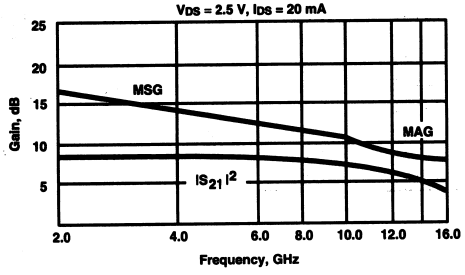
Part Number	Devices Per Reel	Reel Size
ATF-13484-TR1	1000	7"
ATF-13484-TR2	4000	13"
ATF-13484-STR	1	strip

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

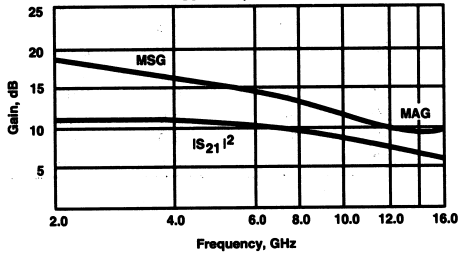
Typical Performance, T_A = 25°C

(unless otherwise noted)

INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{DS} = 2.5 V, I_{DS} = 20 mA



INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{DS} = 4.0 V, I_{DS} = 40 mA



Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 2.5 V, I_{DS} = 20 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.5	.99	–12	8.9	2.79	170	–37.1	.014	81	.50	–10
1.0	.99	–22	8.5	2.67	158	–32.4	.024	78	.50	–18
2.0	.97	–35	8.2	2.56	143	–26.2	.049	63	.50	–26
3.0	.92	–53	8.4	2.64	126	–23.1	.070	51	.49	–38
4.0	.87	–73	8.5	2.66	107	–20.4	.095	38	.45	–55
5.0	.80	–91	8.4	2.62	90	–18.9	.113	28	.41	–69
6.0	.75	–109	8.2	2.57	74	–17.3	.136	16	.38	–81
7.0	.69	–127	8.0	2.52	57	–16.6	.148	5	.34	–91
8.0	.64	–148	7.7	2.43	41	–15.7	.164	–5	.31	–102
9.0	.61	–173	7.4	2.35	23	–15.4	.169	–14	.25	–117
10.0	.58	163	6.8	2.20	6	–15.4	.170	–28	.20	–134
11.0	.57	140	6.2	2.03	–11	–15.3	.172	–38	.16	–165
12.0	.56	119	5.8	1.95	–23	–15.4	.170	–49	.11	161
13.0	.60	97	5.6	1.90	–41	–15.5	.168	–59	.09	121
14.0	.64	79	5.3	1.84	–56	–15.6	.166	–75	.12	74
15.0	.67	66	4.6	1.70	–69	–15.7	.164	–79	.17	52
16.0	.71	49	3.9	1.57	–81	–15.8	.162	–82	.22	30
17.0	.73	38	3.1	1.43	–94	–15.9	.160	–85	.28	20
18.0	.75	27	2.3	1.30	–106	–16.0	.158	–89	.34	14

T_A = 25°C, V_{DS} = 4.0 V, I_{DS} = 40 mA

1.0	.98	–19	11.2	3.61	160	–33.2	.022	74	.61	–11
2.0	.94	–40	11.3	3.67	141	–27.1	.044	65	.58	–25
3.0	.88	–59	11.4	3.71	121	–23.4	.068	48	.54	–38
4.0	.80	–80	11.3	3.65	102	–21.6	.083	38	.48	–55
5.0	.72	–99	10.9	3.50	84	–20.2	.098	27	.44	–68
6.0	.65	–118	10.5	3.34	68	–19.1	.111	19	.40	–80
7.0	.59	–137	10.1	3.20	51	–18.1	.124	7	.37	–89
8.0	.54	–159	9.7	3.04	36	–17.3	.136	0	.34	–100
9.0	.52	175	9.1	2.86	19	–17.1	.140	–12	.29	–112
10.0	.50	151	8.5	2.65	2	–16.5	.150	–21	.23	–127
11.0	.50	129	7.7	2.43	–13	–16.4	.152	–31	.17	–150
12.0	.51	108	7.3	2.32	–25	–16.4	.151	–40	.12	–175
13.0	.55	87	7.0	2.25	–42	–16.4	.151	–47	.09	163
14.0	.62	70	6.8	2.20	–56	–16.5	.150	–58	.09	106
15.0	.67	60	6.3	2.06	–66	–16.5	.149	–65	.11	89
16.0	.69	44	5.6	1.90	–81	–16.7	.147	–72	.15	64
17.0	.66	30	4.5	1.68	–95	–16.1	.156	–82	.19	57
18.0	.62	18	3.8	1.55	–112	–15.0	.178	–100	.31	51

HEWLETT PACKARD

ATF-13736
2-16 GHz General Purpose Gallium Arsenide FET

Features

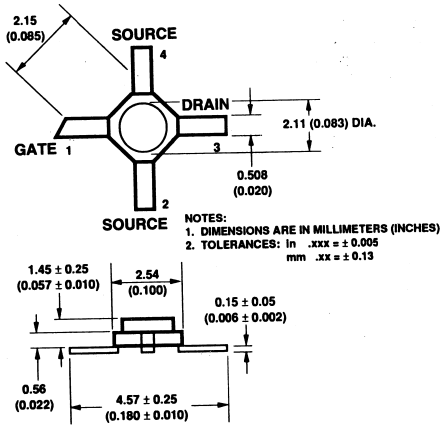
- **High Associated Gain: 9.0 dB typical at 12 GHz**
- **High Output Power: 17.5 dBm typical $P_{1\,dB}$ at 12 GHz**
- **Low Noise Figure: 1.8 dB typical at 12 GHz**
- **Cost Effective Ceramic Microstrip Package**
- **Tape-and-Reel Packaging Option Available[2]**

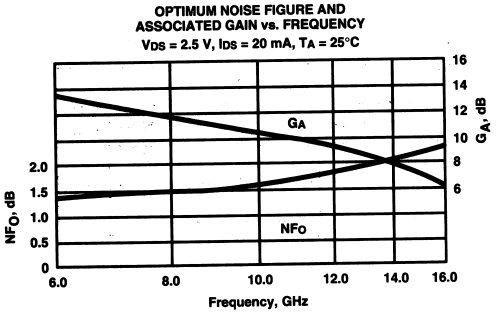
Description

The ATF-13736 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a cost effective microstrip package. Its noise figure makes this device appropriate for use in the gain stages of low noise amplifiers operating in the 2-16 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery of 250 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

36 micro-X Package[1]





Noise Parameters: V_{DS} = 3 V, I_{DS} = 20 mA

Freq. GHz	NFO dB	Gamma Opt Mag	Gamma Opt Ang	RN/50
4.0	1.1	.71	102	.10
6.0	1.3	.55	147	.07
8.0	1.5	.46	–144	.19
12.0	1.8	.50	–40	.88
14.0	2.1	.52	–2	1.17

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NFO	Optimum Noise Figure: VDS = 2.5 V, IDS = 15 - 30 mA	f = 8.0 GHz f = 12.0 GHz f = 14.0 GHz	dB dB dB		1.5 1.8 2.1	2.2
GA	Gain @ NFO: VDS = 2.5 V, IDS = 15 - 30 mA	f = 8.0 GHz f = 12.0 GHz f = 14.0 GHz	dB dB dB	8.0	11.5 9.0 7.0	
P1 dB	Output Power @ 1 dB Gain Compression: VDS = 4 V, IDS = 40 mA	f = 12.0 GHz	dBm		17.5	
G1 dB	1dB Compressed Gain: VDS = 4 V, IDS = 40 mA	f = 12.0 GHz	dB		8.5	
gm	Transconductance: VDS = 2.5 V, VGS = 0 V		mmho	25	55	
IDSS	Saturated Drain Current: VDS = 2.5 V, VGS = 0 V		mA	40	50	90
VP	Pinchoff Voltage: VDS = 2.5 V, IDS = 1 mA		V	–4.0	–1.5	–0.5

Notes: 1. Long leaded 35 package available upon request.
2. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors".

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+5 V
Gate-Source Voltage	V_{GS}	–4 V
Drain Current	I_{DS}	I_{DSS}
Total Power Dissipation[2,3]	P_T	225 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature[4]	T_{STG}	–65°C to +175°C

Thermal Resistance: θ_{jc} = 400°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm Spot Size[5]

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 2.5 mW/°C for T_{CASE} > 85°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safety stored up to 175°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

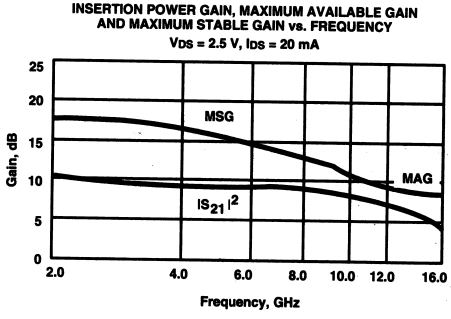
Part Number Ordering Information

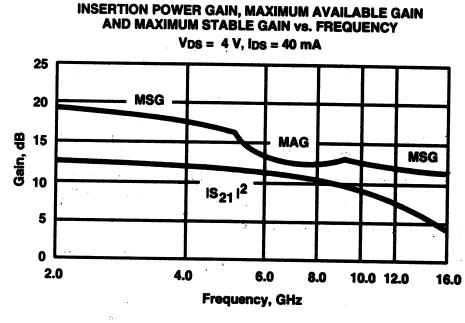
Part Number	Devices Per Reel	Reel Size
ATF-13736-TR1	1000	7"
ATF-13736-TR2	4000	13"
ATF-13736-STR	1	STRIP

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

Typical Performance, T_A = 25°C

(unless otherwise noted)





Typical Scattering Parameters: Common Source, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{DS} = 2.5$ V, $I_{DS} = 20$ mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
2.0	.94	–46	11.0	3.56	128	–26.4	.048	55	.59	–36
3.0	.86	–70	10.2	3.23	109	–25.2	.055	40	.57	–47
4.0	.84	–90	9.8	3.08	91	–23.1	.070	31	.56	–55
5.0	.77	–110	9.6	3.02	69	–20.9	.090	18	.52	–63
6.0	.68	–135	9.9	3.14	51	–19.3	.109	7	.47	–75
7.0	.59	–170	9.9	3.13	24	–18.0	.126	–12	.39	–92
8.0	.54	149	9.5	2.99	–1	–17.6	.132	–27	.30	–112
9.0	.56	112	8.8	2.75	–22	–16.9	.143	–43	.19	–121
10.0	.58	86	8.1	2.53	–43	–16.4	.152	–58	.11	–140
11.0	.60	63	7.6	2.41	–66	–16.5	.149	–73	.09	92
12.0	.64	39	7.0	2.24	–90	–17.1	.140	–81	.15	47
13.0	.68	20	6.4	2.08	–106	–17.6	.132	–90	.19	21
14.0	.70	9	6.0	1.99	–130	–18.0	.126	–97	.19	–3
15.0	.72	–1	5.2	1.83	–145	–18.2	.123	–111	.15	–26
16.0	.74	–17	4.6	1.70	–177	–18.4	.120	–129	.11	–34

$T_A = 25°C$, $V_{DS} = 4$ V, $I_{DS} = 40$ mA

2.0	.88	–44	13.5	4.73	130	–26.4	.048	64	.67	–28
3.0	.76	–68	13.0	4.47	107	–24.9	.057	52	.61	–39
4.0	.68	–90	12.4	4.19	86	–22.5	.075	39	.57	–46
5.0	.56	–113	12.0	4.00	66	–21.0	.089	32	.52	–52
6.0	.42	–145	11.8	3.90	44	–19.8	.102	21	.44	–61
7.0	.37	161	11.5	3.74	20	–18.6	.117	9	.31	–75
8.0	.47	116	10.5	3.36	–3	–17.9	.128	–5	.17	–95
9.0	.57	90	9.4	2.96	–23	–17.2	.138	–19	.05	–143
10.0	.63	70	8.9	2.77	–41	–17.4	.135	–28	.06	128
11.0	.69	51	7.9	2.47	–63	–17.7	.131	–39	.17	100
12.0	.77	33	7.1	2.26	–82	–18.0	.126	–52	.26	75
13.0	.82	21	6.0	2.00	–101	–18.6	.118	–65	.35	62
14.0	.85	13	5.4	1.86	–117	–19.2	.110	–75	.39	54
15.0	.83	1	4.8	1.73	–134	–19.7	.104	–83	.41	49
16.0	.81	–17	4.4	1.65	–154	–19.8	.102	–103	.42	41

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

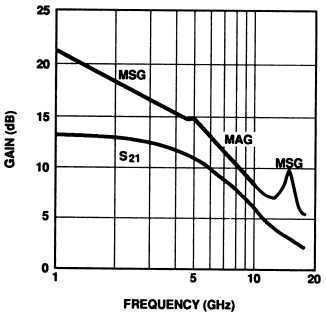
Surface Mount Gallium Arsenide FET for Oscillators

Technical Data

ATF-13786

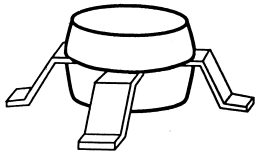
Features

- **Low Cost Surface Mount Plastic Package**
- **High f_{MAX}: 60 GHz Typical**
- **Low Phase Noise at 10 GHz: -110 dBc/Hz @ 100 kHz Typical**
- **Output Power at 10 GHz: up to 10 dBm**
- **Tape-and-Reel Packaging Option Available**

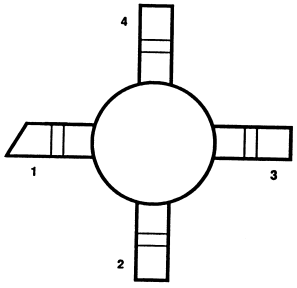


Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency. V_{DS} = 3 V, I_{DS} = 40 mA.

85 mil Plastic Surface Mount Package



Pin Configuration



Pin Description
1 Gate
2 Source
3 Drain
4 Source

Description

Hewlett-Packard's ATF-13786 is a low cost Gallium Arsenide Schottky barrier-gate field effect transistor housed in a surface mount plastic package. This device is designed for use in low cost, surface mount oscillators operating over the RF and microwave frequency ranges. The ATF-13786 has sufficient gain for easy use as a negative R cell, without excess gain that can lead to unwanted oscillations and mode jumping. The gate structure used in the fabrication of this device results in phase noise performance superior to that of most other MESFETs. These features make this device particularly well suited for low power (< +10 dBm) commercial oscillator applications such as are encountered in DBS, TVRO, and MMDS television receivers, or hand-held transceivers operating in the 900 MHz, 2.4 GHz, and 5.7 GHz ISM bands.

This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery of 250 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

Absolute Maximum Ratings for the ATF-13786[1]

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain-Source Voltage	V	4
V_{GS}	Gate-Source Voltage	V	-4
I_{DS}	Drain Current	mA	I_{DSS}
P_t	Power Dissipation[2,3]	mW	225
T_{ch}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to +150

Thermal Resistance[2]: Θ_{jc} = 325°C/W

Notes:
1. Operation of this device above any one of these conditions may cause permanent damage.
2. T_{case} = 25°C (T_{case} is defined to be the temperature at the ends of pins 2 and 4 where they contact the circuit board).
3. Derate at 3.1 mW/°C for T_C > 60°C.

Electrical Specifications for the ATF-13786, T_C = 25°C, V_{DS} = 3 V, I_{DS} = 40 mA[4] (unless noted)

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$\|S_{21}\|^2$	Insertion Power Gain	f = 10 GHz	dB		6.0	
$P_{1\,dB}$	Power at 1 dB Gain Compression	f = 10 GHz	dBm	15	16.5	
$G_{1\,dB}$	1 dB Compressed Gain	f = 10 GHz	dB	6.5	7.5	
PN	Phase Noise (100 kHz offset)[5]	f = 10 GHz	dBc/Hz		-110	
g_m	Transconductance	V_{DS} = 3 V, V_{GS} = 0 V	mS	25	55	
I_{DSS}	Saturated Drain Current	V_{DS} = 3 V, V_{GS} = 0 V	mA	50	70	100
V_P	Pinchoff Voltage	V_{DS} = 3 V, I_{DS} = 1 mA	V	-2.0	-1.5	-0.5
V_{BDG}	Gate - Drain Breakdown Voltage	I_{DG} = 0.1 mA	V	6.5	7	

Notes:
4. Recommended maximum bias conditions for use as an oscillator.
5. The superior phase noise of this product results from the use of a gate structure optimized for noise performance. Typical performance of 10 GHz parallel resonated, lightly coupled oscillator using high Q dielectric resonator.

Typical Scattering Parameters, Common Source, $Z_o = 50\Omega$

$V_{DS} = 3$ V, $I_{DS} = 40$ mA

Frequency GHz	S_{11}		S_{21}		S_{12}		S_{22}	
	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.
1	0.97	-23	4.80	157	0.03	77	0.46	-13
2	0.88	-46	4.60	135	0.06	66	0.42	-25
3	0.78	-68	4.35	117	0.08	58	0.36	-35
4	0.67	-95	4.02	95	0.11	47	0.28	-48
5	0.57	-125	3.61	75	0.12	37	0.19	-65
6	0.52	-157	3.20	57	0.13	28	0.12	-93
7	0.53	176	2.84	41	0.14	21	0.08	-147
8	0.57	160	2.54	31	0.14	18	0.10	171
9	0.60	143	2.27	16	0.14	12	0.15	148
10	0.63	130	2.04	4	0.15	6	0.19	134
11	0.64	117	1.82	-9	0.14	0	0.25	122
12	0.67	107	1.65	-19	0.14	-4	0.30	113
13	0.72	99	1.55	-29	0.14	-8	0.35	109
14	0.76	97	1.47	-35	0.14	-9	0.39	111
15	0.78	90	1.40	-46	0.14	-14	0.41	108
16	0.77	83	1.32	-58	0.14	-20	0.42	104
17	0.74	77	1.26	-68	0.14	-28	0.43	98
18	0.73	69	1.23	-80	0.14	-36	0.42	93

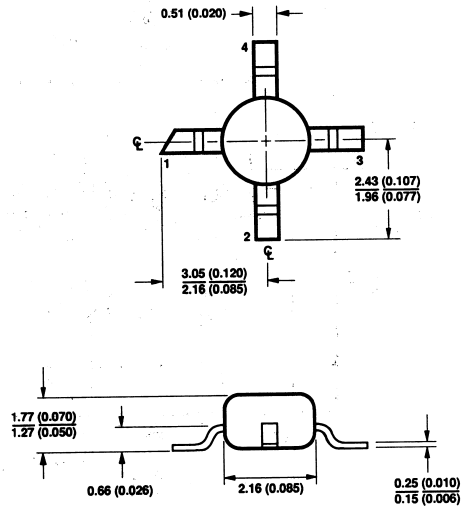
Part Number Ordering Information

Part Number	Devices per Reel	Reel Size
ATF-13786-TR1	1000	7"
ATF-13786-TR2	4000	13"
ATF-13786-STR	1	strip

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

Package Dimensions

85 mil Plastic Package



OUTLINE 86

DIMENSIONS ARE IN MILLIMETERS (INCHES)

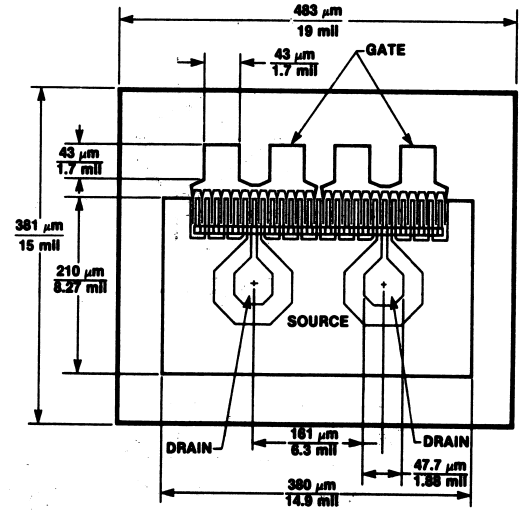
HEWLETT PACKARD

ATF-21100 (AT-8111)
0.5-6 GHz Low Noise Gallium Arsenide FET

Features

- **Low Noise Figure: 0.9 dB typical at 4 GHz**
- **High Associated Gain: 13.0 dB typical at 4 GHz**
- **High Output Power: 23.0 dBm typical $P_{1\,dB}$ at 4 GHz**

Chip Outline



Description

The ATF-21100 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor chip. This device is designed for use in low noise or medium power amplifier applications in the 0.5-6 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length using airbridge interconnects between drain fingers. Total gate periphery is 750 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

The recommended mounting procedure is to die attach at a stage temperature of 300 C using a gold-tin preform under forming gas. Assembly can be performed with either wedge or ball bonding using 0.7 mil gold wire. See also "Chip Use" in the APPLICATIONS section.

Noise Parameters: V_{DS} = 3 V, I_{DS} = 20 mA

Freq. GHz	NFo dB	Gamma Opt Mag	Gamma Opt Ang	RN/50
0.5	0.4	.93	10	.92
1.0	0.5	.86	20	.83
2.0	0.6	.72	42	.64
4.0	0.9	.61	104	.28
6.0	1.2	.55	160	.07

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
NFO	Optimum Noise Figure: V_{DS} = 3 V, I_{DS} = 20 mA	f = 2.0 GHz	dB		0.6	
		f = 4.0 GHz	dB		0.9	1.1
		f = 6.0 GHz	dB		1.2	
GA	Gain @ NFO: V_{DS} = 3 V, I_{DS} = 20 mA	f = 2.0 GHz	dB		16.0	
		f = 4.0 GHz	dB	12.0	13.0	
		f = 6.0 GHz	dB		10.0	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 5 V, I_{DS} = 80 mA	f = 4.0 GHz	dBm		23.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 5 V, I_{DS} = 80 mA	f = 4.0 GHz	dB		13.0	
gm	Transconductance: V_{DS} = 3 V, V_{GS} = 0 V		mmho	70	120	
IDSS	Saturated Drain Current: V_{DS} = 3 V, V_{GS} = 0 V		mA	80	120	200
VP	Pinchoff Voltage: V_{DS} = 3 V, I_{DS} = 1 mA		V	–3.0	–1.5	–0.8

Note: 1. RF performance is determined by assembling and testing 10 samples per wafer.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain Source Voltage	V_{DS}	+7 V
Gate-Source Voltage	V_{GS}	–4 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	600 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	–65°C to +175°C

Thermal Resistance: θ_{jc} = 150° C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm Spot Size[4]

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Mounting Surface Temperature = 25°C.
3. Derate at 6.7 mW/°C for $T_{MOUNTING\ SURFACE}$ > 85°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

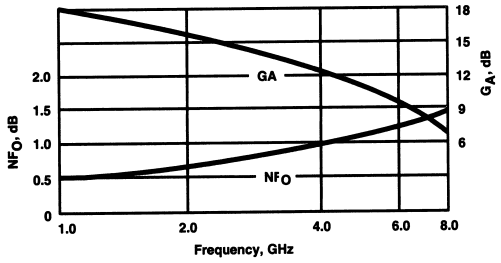
Part Number Ordering Information

Part Number	Devices Per Tray
ATF-21100-GP1	5
ATF-21100-GP3	50
ATF-21100-GP6	up to 300

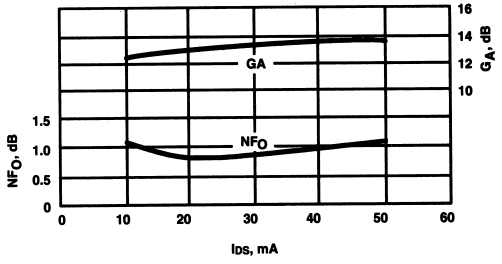
Typical Performance, T_A = 25°C

(unless otherwise noted)

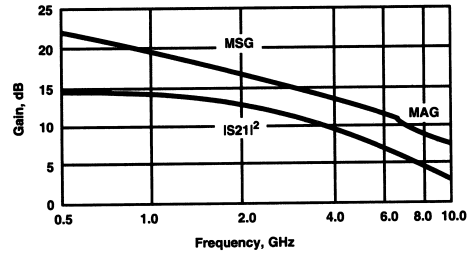
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN vs. FREQUENCY
V_{DS} = 3 V, I_{DS} = 20 mA



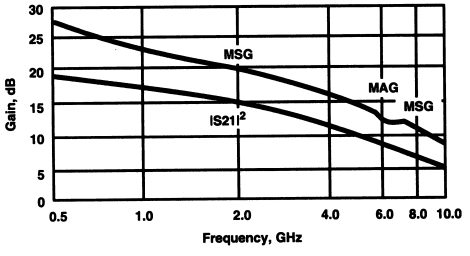
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN vs. I_{DS}
V_{DS} = 3 V, f = 4.0 GHz



INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{DS} = 3 V, I_{DS} = 20 mA



INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{DS} = 5 V, I_{DS} = 80 mA



Typical Scattering Parameters: Common Source, $Z_O = 50\ \Omega$

$T_A = 25°C$, $V_{DS} = 3$ V, $I_{DS} = 20$ mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.5	.97	–20	14.0	5.00	166	–30.8	.029	77	.52	–11
1.0	.95	–34	13.7	4.82	152	–24.7	.058	73	.48	–28
2.0	.83	–69	12.6	4.26	130	–20.2	.098	56	.43	–52
3.0	.70	–101	11.1	3.59	105	–18.2	.123	45	.39	–74
4.0	.63	–129	9.5	2.97	88	–17.3	.136	39	.36	–92
5.0	.60	–152	7.9	2.47	74	–17.1	.139	36	.33	–107
6.0	.60	–169	6.4	2.10	62	–17.0	.141	34	.32	–122
7.0	.63	177	5.1	1.81	53	–17.0	.142	33	.33	–134
8.0	.66	167	4.1	1.60	44	–16.8	.145	32	.33	–145
9.0	.68	160	3.1	1.44	36	–16.4	.152	31	.34	–154
10.0	.70	155	2.1	1.32	28	–15.7	.164	27	.33	–166

$T_A = 25°C$, $V_{DS} = 5$ V, $I_{DS} = 80$ mA

0.5	.96	–25	18.2	8.10	161	–34.4	.019	80	.50	–9
1.0	.90	–50	17.4	7.41	144	–29.1	.035	71	.46	–17
2.0	.76	–89	15.1	5.72	117	–25.0	.056	62	.37	–26
3.0	.68	–116	13.0	4.48	99	–23.1	.070	60	.31	–32
4.0	.65	–137	11.3	3.66	85	–21.6	.083	61	.26	–38
5.0	.63	–156	9.7	3.06	72	–20.3	.097	61	.23	–49
6.0	.62	–172	8.3	2.61	61	–18.9	.113	62	.20	–65
7.0	.64	175	7.2	2.29	51	–17.8	.129	61	.19	–86
8.0	.66	163	6.2	2.04	41	–16.7	.146	60	.20	–103
9.0	.68	151	5.2	1.82	32	–15.7	.165	57	.22	–119
10.0	.71	139	4.2	1.63	23	–14.7	.184	54	.26	–135

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

ATF-21170 (AT-8110)
0.5-6 GHz Low Noise Gallium Arsenide FET

Features

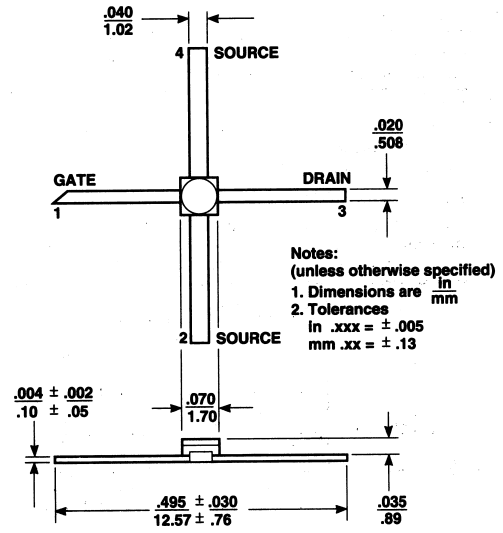
- **Low Noise Figure: 0.9 dB typical at 4 GHz**
- **High Associated Gain: 13.0 dB typical at 4 GHz**
- **High Output Power: 23.0 dBm typical $P_{1\,dB}$ at 4 GHz**
- **Hermetic Gold-Ceramic Microstrip Package**

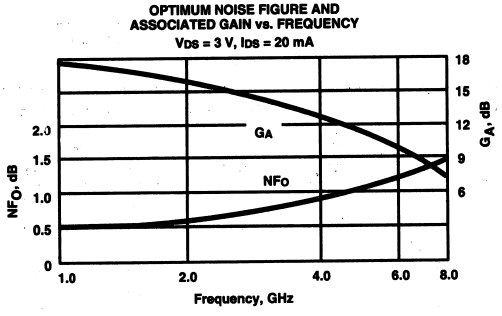
Description

The ATF-21170 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a hermetic, high reliability package. This device is designed for use in low noise or medium power amplifier applications in the 0.5-6 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length using airbridge interconnects between drain fingers. Total gate periphery is 750 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

70 mil Package





Noise Parameters: V_{DS} = 3 V, I_{DS} = 20 mA

Freq. GHz	NFO dB	Gamma Opt Mag	Gamma Opt Ang	RN/50
0.5	0.4	.93	17	.90
1.0	0.5	.85	35	.70
2.0	0.6	.70	70	.46
4.0	0.9	.59	148	.14
8.0	1.2	.54	–177	.09

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NFO	Optimum Noise Figure: VDS = 3 V, IDS = 20 mA	f = 2.0 GHz f = 4.0 GHz f = 6.0 GHz	dB dB dB		0.6 0.9 1.2	1.1
GA	Gain @ NFO: VDS = 3 V, IDS = 20 mA	f = 2.0 GHz f = 4.0 GHz f = 6.0 GHz	dB dB dB	12.0	16.0 13.0 10.0	
P1 dB	Output Power @ 1 dB Gain Compression: VDS = 5 V, IDS = 80 mA	f = 4.0 GHz	dBm		23.0	
G1 dB	1dB Compressed Gain: VDS = 5 V, IDS = 80 mA	f = 4.0 GHz	dB		13.0	
gm	Transconductance: VDS = 3 V, VGS = 0 V		mmho	70	120	
IDSS	Saturated Drain Current: VDS = 3 V, VGS = 0 V		mA	80	120	200
VP	Pinchoff Voltage: VDS = 3 V, IDS = 1 mA		V	–3.0	–1.5	–0.8

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+7 V
Gate-Source Voltage	V_{GS}	–4 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	600 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	–65°C to +175°C

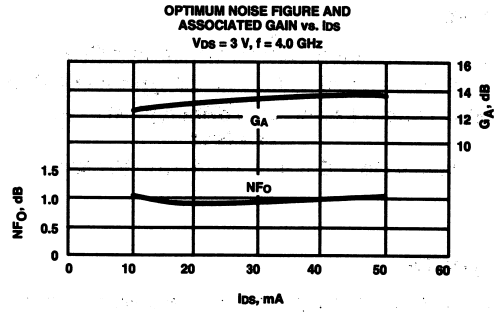
Thermal Resistance: θ_{jc} = 250°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 µm Spot Size[4]

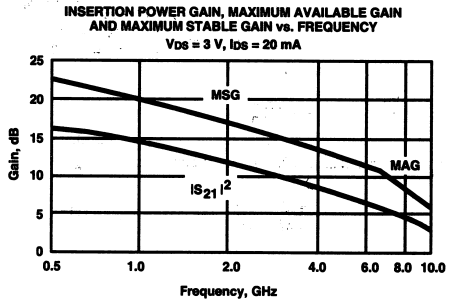
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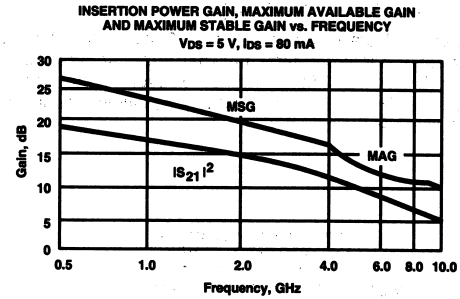
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 4 mW/°C for T_{CASE} > 25°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)







Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 3 V, I_{DS} = 20 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.5	.96	–31	15.5	5.93	157	–29.4	.034	72	.46	–23
1.0	.91	–55	14.2	5.14	137	–24.3	.061	56	.42	–42
2.0	.82	–95	12.1	4.05	106	–20.4	.096	36	.39	–70
3.0	.74	–123	10.2	3.23	82	–19.5	.106	21	.35	–91
4.0	.70	–147	8.8	2.74	61	–18.7	.116	9	.33	–109
5.0	.65	–170	7.3	2.33	41	–18.2	.123	–1	.30	–127
6.0	.64	167	6.3	2.07	22	–17.7	.131	–10	.29	–145
7.0	.65	146	5.4	1.86	4	–17.5	.134	–17	.26	–167
8.0	.66	126	4.5	1.67	–13	–17.0	.141	–28	.26	164
9.0	.66	107	3.4	1.48	–30	–16.6	.148	–39	.26	140
10.0	.67	87	2.2	1.29	–47	–16.2	.155	–50	.25	114

T_A = 25°C, V_{DS} = 5 V, I_{DS} = 80 mA

0.5	.95	–43	18.3	8.24	149	–32.4	.024	67	.49	–17
1.0	.89	–64	17.4	7.28	133	–29.9	.032	59	.46	–26
2.0	.78	–106	14.6	5.36	101	–25.2	.055	44	.40	–45
3.0	.69	–133	12.4	4.18	79	–23.4	.068	34	.38	–60
4.0	.64	–160	10.7	3.42	56	–22.7	.073	31	.36	–81
5.0	.60	175	9.1	2.85	37	–21.7	.082	24	.35	–100
6.0	.61	154	7.9	2.47	18	–20.4	.095	19	.33	–115
7.0	.61	136	6.9	2.22	2	–19.3	.108	12	.31	–132
8.0	.63	120	6.2	2.05	–14	–17.9	.127	7	.27	–152
9.0	.64	102	5.3	1.85	–32	–16.6	.148	0	.27	–179
10.0	.64	86	4.5	1.68	–48	–15.3	.172	–13	.29	165

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

0.5 to 6 GHz General Purpose Gallium Arsenide FET

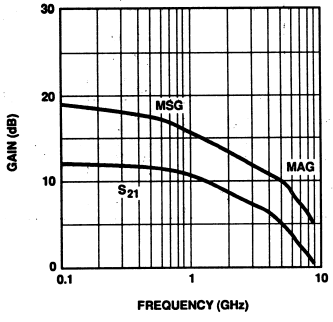
Technical Data

ATF-21186

Features

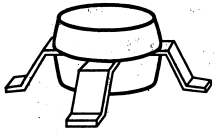
- **Low Noise Figure: 0.6 dB Typ. @ 2 GHz**
- **High Output Power: 19 dBm Typ. P_{1dB} @ 2 GHz**
- **High MSG: 13.5 dB Typ. @ 2 GHz**
- **Low Cost Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Note:
1. Refer to "Tape-and-Reel Packaging for Surface Mount Semiconductors".

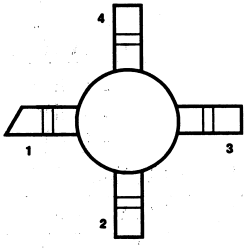


ATF-21186 Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency.
V_{DS} = 2 V, I_{DS} = 15 mA.

85 mil Plastic Surface Mount Package



Pin Configuration



Pin Description

1	Gate
2	Source
3	Drain
4	Source

Description

Hewlett–Packard's ATF-21186 is a low cost Gallium Arsenide Schottky barrier-gate field effect transistor housed in a surface mount plastic package. This general purpose device is designed for use in low noise amplifiers, gain stages, driver amplifiers, and oscillators operating over the VHF, UHF, and microwave frequency ranges. High gain with two Volt operation makes this part attractive for low voltage, battery operated systems. The low noise figure is appropriate for commercial systems demanding good sensitivity, such as GPS receiver front-ends and MMDS television receivers. The output power is sufficient for use as the driver stage in many hand-held transceivers operating in the 900 MHz through 2.4 GHz bands, including in cellular phones, PCN, and ISM band spread spectrum applications.

This GaAs FET device has a nominal 0.3 micron gate length using airbridge interconnects between drain fingers. Total gate periphery is 750 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

ATF-21186 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain-Source Voltage	V	5
V_{GS}	Gate-Source Voltage	V	-4
I_{DS}	Drain Current	mA	I_{DSS}
P_t	Power Dissipation[2,3]	mW	400
T_{ch}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to +150

Thermal Resistance[2]: Θ_{jc} = 225°C/W

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{case} = 25°C (T_{case} is defined to be the temperature at the ends of pins 2 and 4 where they contact the circuit board).
3. Derate at 4.4 mW/°C for T_C > 60°C.

ATF-21186 Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_o	Optimum Noise Figure V_{DS} = 2 V, I_{DS} = 15 mA	f = 1 GHz f = 2 GHz f = 4 GHz	dB		0.55 0.65 0.84	0.75
G_A	Associated Gain V_{DS} = 2 V, I_{DS} = 15 mA	f = 1 GHz f = 2 GHz f = 4 GHz	dB	 12.0 	15.0 13.0 9.0	
$P_{1\,dB}$	Power at 1 dB Gain Compression V_{DS} = 3 V, I_{DS} = 70 mA	f = 1 GHz f = 2 GHz f = 4 GHz	dBm		19.0 19.0 18.0	
$G_{1\,dB}$	1 dB Compressed Gain V_{DS} = 3 V, I_{DS} = 70 mA	f = 1 GHz f = 2 GHz f = 4 GHz	dB		18.0 14.0 8.5	
g_m	Transconductance	V_{DS} = 3 V, V_{GS} = 0 V	mS	70	120	
I_{DSS}	Saturated Drain Current	V_{DS} = 3 V, V_{GS} = 0 V	mA	80	120	200
V_P	Pinchoff Voltage	V_{DS} = 3 V, I_{DS} = 1 mA	V	-3.0	-1.5	-0.8

Typical Performance, for the ATF-21186, T_A = 25°C

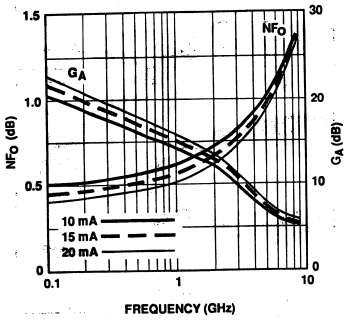


Figure 1. ATF-21186 Optimum Noise Figure and Associated Gain vs. Frequency and I_{DS} - V_{DS} = 2 V.

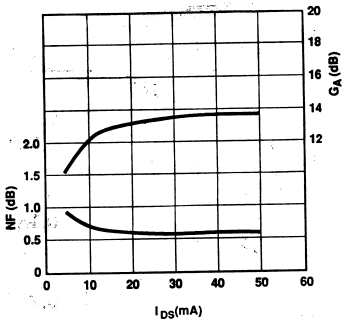


Figure 2. ATF-21186 Optimum Noise Figure and Associated Gain vs. I_{DS}, f = 2 GHz, V_{DS} = 2 V.

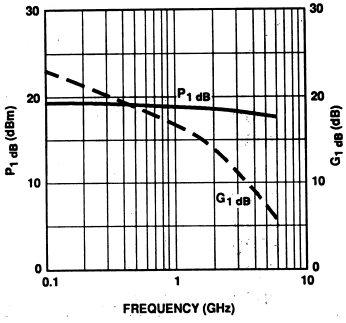


Figure 3. ATF-21186 Power Output at 1 dB Compression and 1 dB Compressed Gain vs. Frequency. V_{DS} = 3 V, I_S = 70 mA.

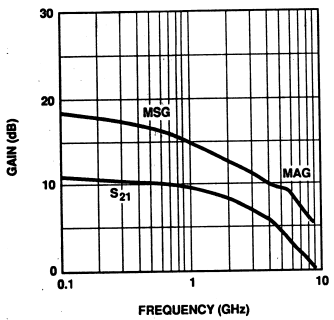


Figure 4. ATF-21186 Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency. V_{DS} = 2 V, I_{DS} = 10 mA.

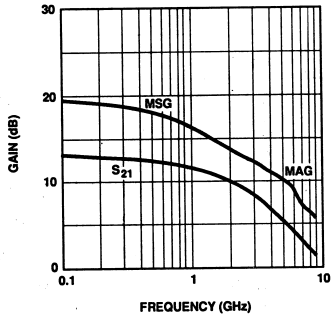


Figure 5. ATF-21186 Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency. V_{DS} = 2 V, I_{DS} = 20 mA.

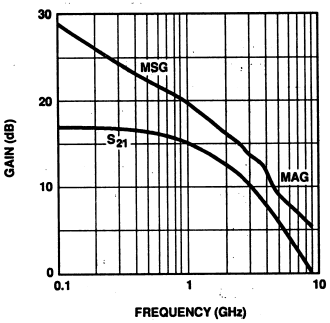


Figure 6. ATF-21186 Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency. V_{DS} = 3 V, I_{DS} = 70 mA.

ATF-21186 Typical Scattering Parameters,

Common Source, Zo = 50 Ω, V_{DS} = 2 V, I_{DS} = 10 mA

Frequency (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.
500	0.98	-46	3.21	148	0.072	63	0.40	-46
1000	0.93	-58	2.93	135	0.099	54	0.39	-54
2000	0.83	-83	2.47	110	0.142	37	0.38	-74
3000	0.74	-109	2.12	85	0.174	22	0.35	-97
4000	0.67	-138	1.89	62	0.192	9	0.30	-125
5000	0.63	-167	1.67	40	0.197	-4	0.28	-158
6000	0.63	167	1.46	19	0.194	-14	0.30	173
7000	0.63	145	1.28	1	0.191	-21	0.35	152
8000	0.65	127	1.15	-15	0.192	-26	0.39	137

ATF-21186 Typical Scattering Parameters,

Common Source, Zo = 50 Ω, V_{DS} = 2 V, I_{DS} = 15 mA

Frequency MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.
500	0.98	-49	3.77	147	0.069	62	0.34	-55
1000	0.92	-61	3.42	133	0.092	54	0.33	-63
2000	0.81	-87	2.85	108	0.131	39	0.32	-81
3000	0.72	-114	2.41	84	0.159	25	0.29	-105
4000	0.64	-143	2.11	61	0.178	13	0.26	-135
5000	0.62	-172	1.83	39	0.186	1	0.25	-170
6000	0.61	162	1.59	19	0.189	-8	0.28	162
7000	0.63	140	1.39	2	0.192	-15	0.33	144
8000	0.65	123	1.25	-14	0.200	-20	0.37	129

ATF-21186 Typical Scattering Parameters,

Common Source, Zo = 50 Ω, V_{DS} = 2 V, I_{DS} = 20 mA

Frequency MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.
500	0.98	-51	4.17	146	0.066	61	0.31	-62
1000	0.91	-64	3.78	132	0.087	54	0.30	-69
2000	0.80	-90	3.11	107	0.123	40	0.28	-87
3000	0.70	-118	2.60	83	0.150	27	0.26	-111
4000	0.63	-147	2.25	60	0.169	16	0.23	-142
5000	0.61	-176	1.94	39	0.180	5	0.23	-178
6000	0.61	159	1.68	20	0.187	-4	0.28	155
7000	0.62	137	1.47	2	0.193	-11	0.33	138
8000	0.64	120	1.32	-13	0.205	-17	0.36	125

ATF-21186 Typical Scattering Parameters,

Common Source, Zo = 50 Ω, V_{DS} = 3 V, I_{DS} = 70 mA

Frequency MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.
500	0.95	-30	6.69	156	0.04	74	0.31	-26
1000	0.87	-57	5.74	136	0.06	63	0.20	-58
2000	0.69	-105	4.30	102	0.10	48	0.18	-109
3000	0.63	-139	3.36	80	0.12	41	0.18	-149
4000	0.62	-170	2.63	60	0.14	33	0.22	-178
5000	0.63	165	2.12	42	0.15	28	0.27	161
6000	0.67	147	1.76	26	0.17	23	0.33	146
7000	0.71	133	1.49	13	0.18	18	0.39	136
8000	0.74	126	1.29	5	0.19	16	0.43	131

ATF-21186 Typical Noise Parameters,
Common Source, Zo = 50 Ω, V_{DS} = 2 V, I_{DS} = 10 mA

Frequency	NF_o	Γ_{opt}		RN/50 Ω
MHz	dB	Mag.	Ang.	-
500	0.57	0.83	30	0.78
1000	0.61	0.80	39	0.58
2000	0.71	0.76	61	0.48
4000	0.90	0.72	109	0.23
6000	1.09	0.71	168	0.04
8000	1.29	0.73	-145	0.10

ATF-21186 Typical Noise Parameters,
Common Source, Zo = 50 Ω, V_{DS} = 2 V, I_{DS} = 15 mA

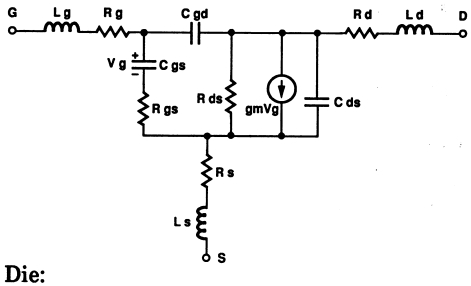
Frequency	NF_o	Γ_{opt}		RN/50 Ω
MHz	dB	Mag.	Ang.	-
500	0.50	0.91	31	0.68
1000	0.55	0.87	40	0.49
2000	0.65	0.77	63	0.40
4000	0.84	0.66	111	0.29
6000	1.13	0.65	171	0.04
8000	1.23	0.79	-141	0.11

ATF-21186 Typical Noise Parameters,
Common Source, Zo = 50 Ω, V_{DS} = 2 V, I_{DS} = 20 mA

Frequency	NF_o	Γ_{opt}		RN/50 Ω
MHz	dB	Mag.	Ang.	-
500	0.45	0.88	31	0.56
1000	0.50	0.84	41	0.43
2000	0.60	0.75	64	0.35
4000	0.82	0.65	113	0.16
6000	1.03	0.65	174	0.03
8000	1.24	0.69	-139	0.11

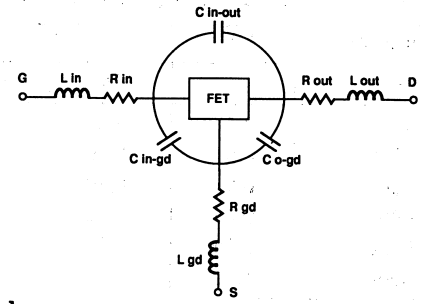
ATF-21186 Linear Equivalent Circuit

V_{DS} = 2 V, I_{DS} = 15 mA



Die:

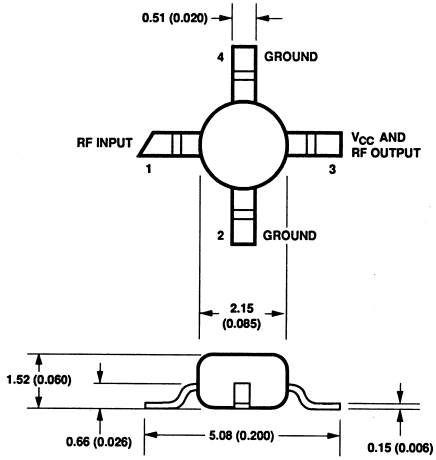
gm = 62 mS	R s = 1.38 Ω
C gs = 0.642 pF	R g = 0.98 Ω
C ds = 0.271 pF	R d = 0.62 Ω
C gd = 0.181 pF	Tau = 1.16
R gs = 3.90 Ω	L g = 0.60 nH
R ds = 110 Ω	L s = 0.20 nH
	L d = 0.63 nH



Package:

R in = R out = R gd = 0.03 Ω
L in = 0.13 nH
L out = 0.23 nH
L gd = 0.02 nH
C in-gd = C o-gd = 0.169 pF
C in-out = 0.022 pF

Package Dimensions



TYPICAL DIMENSIONS ARE IN MM (IN)

85 mil Plastic Package

Part Number Ordering Information

Part Number	Devices per Reel	Reel Size
ATF-21186-TR1	1000	7""
ATF-21186-TR2	4000	13"
ATF-21186-STR	1	strip

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

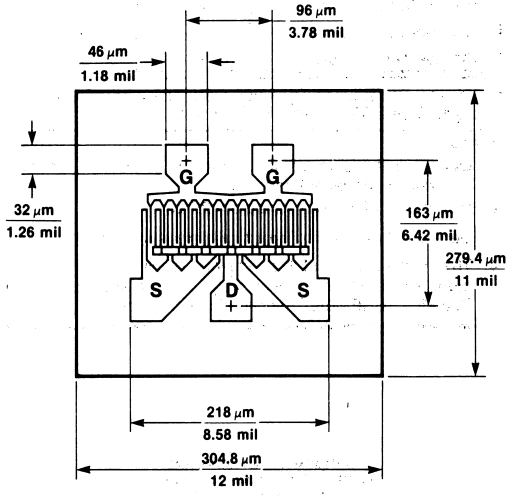
HEWLETT PACKARD

ATF-25100 (AT-8251)
0.5-10 GHz Low Noise Gallium Arsenide FET

Features

- **Low Noise Figure: 0.8 dB typical at 4 GHz**
- **High Associated Gain: 14.0 dB typical at 4 GHz**
- **High Output Power: 21.0 dBm typical $P_{1\,dB}$ at 4 GHz**

Chip Outline



Description

The ATF-25100 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor chip. Its noise figure makes this device appropriate for use in low noise amplifiers operating in the 0.5-10 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length using airbridge interconnects between drain fingers. Total gate periphery is 500 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

The recommended mounting procedure is to die attach at a stage temperature of 300°C using a gold-tin preform under forming gas. Assembly can be performed with either wedge or ball bonding using 0.7 mil gold wire. See also "Chip Use" in the APPLICATIONS section.

Noise Parameters: V_{DS} = 3 V, I_{DS} = 20 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
1.0	0.5	.91	11	1.03
2.0	0.6	.83	22	.79
4.0	0.8	.57	63	.67
6.0	1.0	.50	101	.23
8.0	1.2	.47	135	.34

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 3 V, I_{DS} = 20 mA	f = 4.0 GHz f = 6.0 GHz f = 8.0 GHz	dB dB dB		0.8 1.0 1.2	1.0
G_A	Gain @ NF_O: V_{DS} = 3 V, I_{DS} = 20 mA	f = 4.0 GHz f = 6.0 GHz f = 8.0 GHz	dB dB dB	13.0	14.0 11.5 9.0	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 5 V, I_{DS} = 50 mA	f = 4.0 GHz	dBm		21.0	
$G_{1\,dB}$	1dB Compressed Gain: V_{DS} = 5 V, I_{DS} = 50 mA	f = 4.0 GHz	dB		15.0	
g_m	Transconductance: V_{DS} = 3 V, V_{GS} = 0 V		mmho	50	80	
I_{DSS}	Saturated Drain Current: V_{DS} = 3 V, V_{GS} = 0 V		mA	50	100	150
V_P	Pinchoff Voltage: V_{DS} = 3 V, I_{DS} = 1 mA		V	–3.0	–2.0	–0.8

Note: 1. RF Performance is determined by assembling and testing 10 samples per wafer.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+7 V
Gate-Source Voltage	V_{GS}	–4 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	450 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	–65°C to +175°C

Thermal Resistance: θ_{jc} = 200°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm Spot Size[4]

Notes:

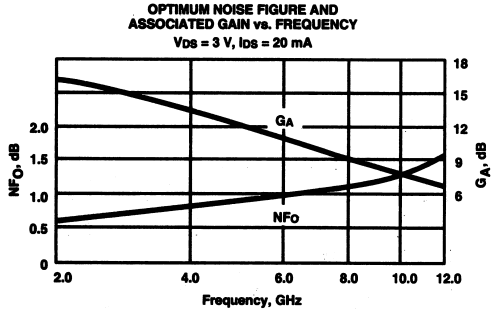
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Mounting Surface Temperature = 25°C.
3. Derate at 5 mW/°C for $T_{MOUNTING\ SURFACE}$ > 85°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

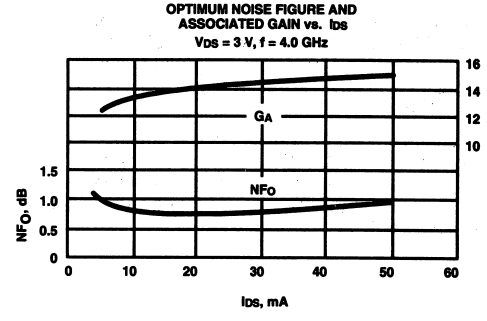
Part Number Ordering Information

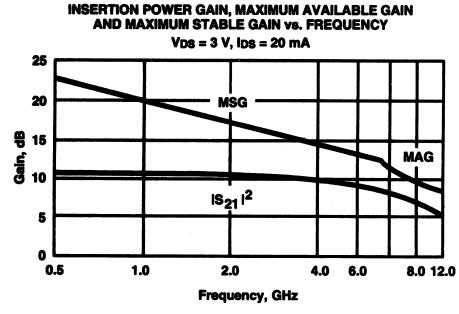
Part Number	Devices Per Tray
ATF-25100-GP1	5
ATF-25100-GP3	50
ATF-25100-GP6	up to 300

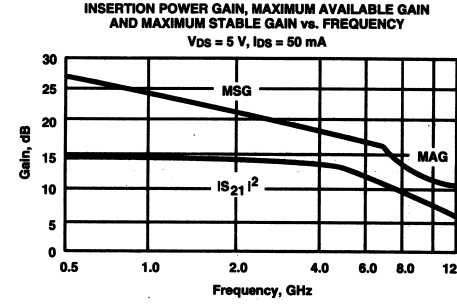
Typical Performance, T_A = 25°C

(unless otherwise noted)









Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 3 V, I_{DS} = 20 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.5	.98	–11	10.4	3.30	173	–34.9	.018	89	.53	–3
1.0	.98	–19	10.4	3.30	165	–29.9	.032	84	.52	–6
2.0	.96	–35	10.3	3.29	150	–24.3	.061	74	.47	–12
3.0	.94	–53	10.1	3.22	134	–21.0	.089	64	.41	–23
4.0	.87	–74	9.9	3.13	117	–19.0	.112	55	.32	–33
5.0	.79	–94	9.2	2.88	103	–18.1	.125	49	.24	–43
6.0	.74	–115	8.6	2.68	89	–17.0	.141	39	.13	–60
7.0	.70	–134	7.7	2.43	77	–16.7	.146	35	.03	–167
8.0	.66	–151	6.8	2.20	67	–16.3	.153	32	.07	155
9.0	.66	–163	6.4	2.09	57	–15.9	.160	25	.13	138
10.0	.67	–176	5.7	1.93	46	–15.8	.163	23	.17	135
11.0	.68	171	5.2	1.81	37	–15.5	.167	18	.23	132
12.0	.68	162	4.5	1.68	24	–15.4	.170	9	.24	130

T_A = 25°C, V_{DS} = 5 V, I_{DS} = 50 mA

0.5	.98	–14	14.6	5.40	173	–39.2	.011	88	.69	–1
1.0	.98	–25	14.5	5.32	163	–34.0	.020	82	.67	–5
2.0	.93	–47	14.3	5.16	144	–28.4	.038	71	.60	–12
3.0	.89	–70	13.7	4.82	127	–25.0	.056	65	.53	–17
4.0	.82	–94	13.0	4.48	110	–23.4	.068	52	.46	–20
5.0	.75	–117	11.8	3.88	97	–22.5	.075	50	.40	–24
6.0	.71	–137	10.9	3.51	83	–21.9	.080	46	.31	–29
7.0	.70	–159	9.7	3.07	71	–21.6	.083	42	.22	–35
8.0	.71	–169	8.7	2.73	63	–21.3	.086	41	.16	–42
9.0	.72	180	8.1	2.53	54	–20.9	.090	40	.12	–46
10.0	.73	172	7.3	2.31	44	–20.6	.093	39	.09	–55
11.0	.74	162	6.6	2.13	35	–20.2	.098	36	.05	–131
12.0	.73	150	6.4	2.08	21	–19.7	.104	34	.08	–170

A model for this device is available in the DEVICE MODELS section.

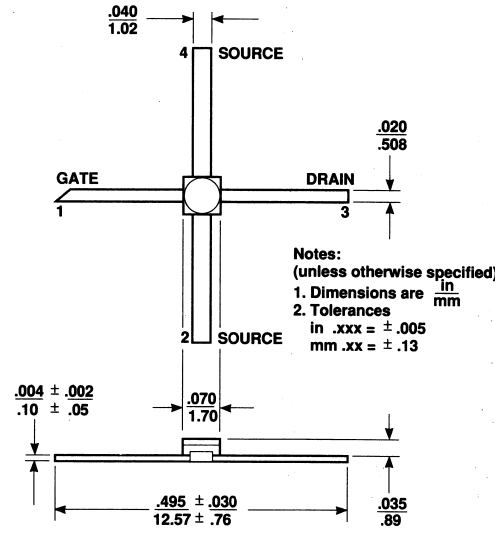
HEWLETT PACKARD

ATF-25170 (AT-8250)
0.5-10 GHz Low Noise Gallium Arsenide FET

Features

- **Low Noise Figure: 0.8 dB typical at 4 GHz**
- **High Associated Gain: 14.0 dB typical at 4 GHz**
- **High Output Power: 21.0 dBm typical $P_{1\,dB}$ at 4 GHz**
- **Hermetic Gold-Ceramic Microstrip Package**

70 mil Package



Description

The ATF-25170 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a hermetic, high reliability package. Its noise figure makes this device appropriate for use in low noise amplifiers operating in the 0.5-10 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length using airbridge interconnects between drain fingers. Total gate periphery is 500 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

Noise Parameters: V_{DS} = 3 V, I_{DS} = 20 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
1.0	0.6	.89	24	.78
2.0	0.7	.77	50	.53
4.0	0.8	.63	105	.33
6.0	1.0	.66	147	.06
8.0	1.2	.62	–159	.11

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 3 V, I_{DS} = 20 mA	f = 4.0 GHz	dB		0.8	1.0
		f = 6.0 GHz	dB		1.0	
		f = 8.0 GHz	dB		1.2	
G_A	Gain @ NF_O: V_{DS} = 3 V, I_{DS} = 20 mA	f = 4.0 GHz	dB	13.0	14.0	
		f = 6.0 GHz	dB		11.5	
		f = 8.0 GHz	dB		9.0	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 5 V, I_{DS} = 50 mA	f = 4.0 GHz	dBm		21.0	
$G_{1\,dB}$	1dB Compressed Gain: V_{DS} = 5 V, I_{DS} = 50 mA	f = 4.0 GHz	dB		15.0	
g_m	Transconductance: V_{DS} = 3 V, V_{GS} = 0 V		mmho	50	80	
I_{DSS}	Saturated Drain Current: V_{DS} = 3 V, V_{GS} = 0 V		mA	50	100	150
V_P	Pinchoff Voltage: V_{DS} = 3 V, I_{DS} = 1 mA		V	–3.0	–2.0	–0.8

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+7 V
Gate-Source Voltage	V_{GS}	–4 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	450 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	–65°C to +175°C

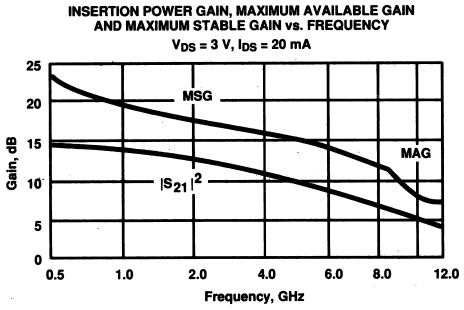
Thermal Resistance: θ_{jc} = 300°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm Spot Size[4]

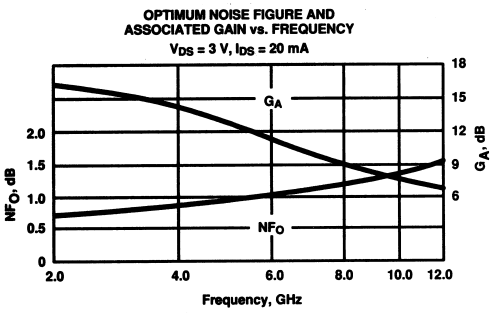
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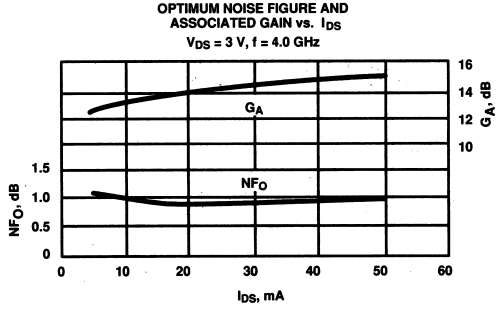
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Mounting Surface Temperature = 25°C.
3. Derate at 3.3 mW/°C for $T_{MOUNTING\ SURFACE}$ > 40°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)







Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 3 V, I_{DS} = 20 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.5	.98	–23	13.6	4.80	160	–32.8	.023	76	.50	–23
1.0	.96	–38	13.0	4.46	147	–23.6	.037	67	.48	–30
2.0	.88	–66	11.5	3.75	121	–23.6	.066	50	.44	–45
3.0	.80	–86	10.2	3.23	102	–21.8	.081	41	.41	–55
4.0	.77	–106	9.3	2.93	82	–19.7	.103	28	.38	–65
5.0	.71	–127	8.5	2.66	62	–18.6	.118	17	.35	–78
6.0	.65	–149	7.9	2.47	42	–17.7	.130	6	.30	–93
7.0	.60	–173	7.3	2.33	24	–16.5	.149	–4	.26	–111
8.0	.56	161	6.8	2.20	5	–15.8	.162	–16	.22	–134
9.0	.56	136	6.2	2.05	–14	–15.1	.175	–26	.21	–166
10.0	.55	118	5.4	1.87	–31	–15.0	.178	–35	.21	173
11.0	.53	108	4.9	1.76	–46	–14.9	.180	–42	.22	164
12.0	.53	95	4.7	1.71	–62	–14.8	.183	–52	.23	159

A model for this device is available in the DEVICE MODELS section.

ATF-25570 (AT-12570-5)
0.5-10 GHz General Purpose Gallium Arsenide FET

Features

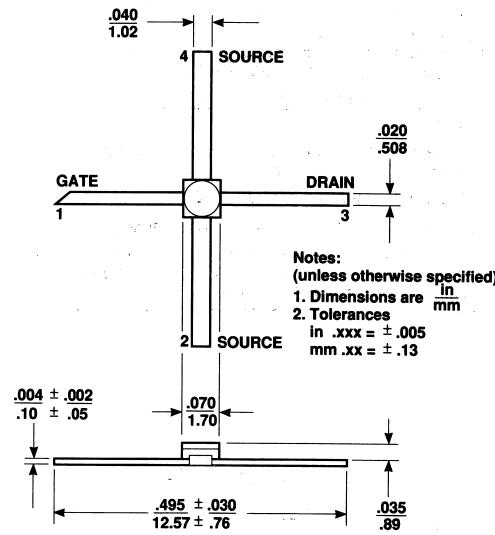
- **High Output Power: 20.5 dBm typical $P_{1\,dB}$ at 4 GHz**
- **High Associated Gain: 14.0 dB typical at 4 GHz**
- **Low Noise Figure: 1.0 dB typical at 4 GHz**
- **Hermetic Gold-Ceramic Microstrip Package**

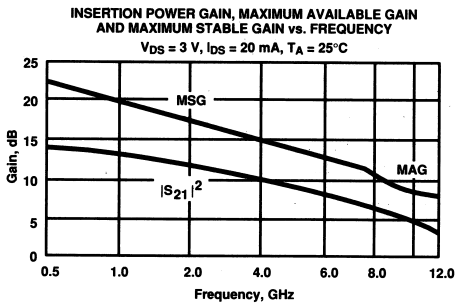
Description

The ATF-25570 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a hermetic, high reliability package. This device is designed for use in general purpose amplifier and oscillator applications in the 0.5-10 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length using airbridge interconnects between drain fingers. Total gate periphery is 500 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

70 mil Package





Electrical Specifications, $T_A = 25°C$

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 3 V, I_{DS} = 20 mA	f = 4.0 GHz f = 6.0 GHz f = 8.0 GHz	dB		1.0 1.2 1.4	1.3
G_A	Gain @ NF_O: V_{DS} = 3 V, I_{DS} = 20 mA	f = 4.0 GHz f = 6.0 GHz f = 8.0 GHz	dB	13.0	14.0 11.0 8.5	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 5 V, I_{DS} = 50 mA	f = 4.0 GHz	dBm		20.5	
$G_{1\,dB}$	1dB Compressed Gain: V_{DS} = 5 V, I_{DS} = 50 mA	f = 4.0 GHz	dB		13.0	
g_m	Transconductance: V_{DS} = 3 V, V_{GS} = 0 V		mmho	50	80	
I_{DSS}	Saturated Drain Current: V_{DS} = 3 V, V_{GS} = 0 V		mA	50	100	150
V_P	Pinchoff Voltage: V_{DS} = 3 V, I_{DS} = 1 mA		V	–3.0	–2.0	–0.8

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+7 V
Gate-Source Voltage	V_{GS}	–4 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	450 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	–65°C to +175°C

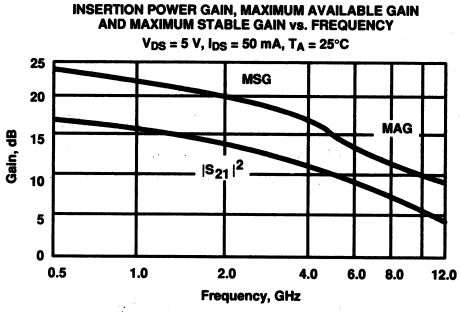
Thermal Resistance: θ_{jc} = 300°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm Spot Size[4]

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 3.3 mW/°C for T_{CASE} > 40°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)



Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 3 V, I_{DS} = 20 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.5	.98	–24	14.0	5.02	160	–28.9	.036	71	.56	–24
1.0	.96	–41	13.4	4.70	145	–26.2	.049	62	.55	–33
2.0	.84	–76	12.3	4.14	115	–22.5	.075	44	.49	–51
3.0	.78	–100	10.8	3.48	94	–20.9	.090	33	.46	–60
4.0	.72	–123	9.6	3.01	73	–19.8	.102	20	.42	–76
5.0	.68	–142	8.5	2.67	54	–18.8	.114	9	.38	–88
6.0	.63	–162	7.8	2.45	36	–18.3	.121	0	.35	–101
7.0	.60	175	7.2	2.30	18	–17.5	.133	–7	.30	–118
8.0	.58	150	6.3	2.06	–1	–17.0	.141	–16	.26	–138
9.0	.59	128	5.6	1.90	–19	–16.7	.146	–28	.25	–167
10.0	.60	113	4.7	1.72	–36	–16.4	.151	–35	.26	172
11.0	.60	104	4.1	1.61	–48	–16.1	.157	–40	.28	155
12.0	.59	91	3.9	1.56	–68	–15.9	.160	–44	.30	146

T_A = 25°C, V_{DS} = 5 V, I_{DS} = 50 mA

0.5	.97	–27	16.2	6.49	156	–32.0	.025	63	.59	–21
1.0	.94	–45	15.5	5.95	141	–29.9	.032	57	.60	–28
2.0	.81	–82	13.5	4.72	111	–26.2	.049	45	.58	–39
3.0	.73	–105	11.7	3.86	91	–24.9	.057	41	.55	–50
4.0	.66	–128	10.3	3.29	70	–23.4	.068	37	.52	–62
5.0	.61	–148	9.2	2.88	52	–22.5	.075	32	.49	–72
6.0	.57	–170	8.5	2.65	34	–21.6	.083	30	.48	–84
7.0	.56	167	7.6	2.41	16	–20.2	.097	28	.45	–98
8.0	.57	145	6.8	2.19	–1	–19.2	.110	18	.42	–115
9.0	.59	127	6.0	2.00	–18	–18.5	.119	12	.40	–136
10.0	.60	115	5.2	1.82	–35	–17.8	.129	4	.40	–159
11.0	.60	108	4.7	1.72	–47	–17.5	.134	1	.42	–176
12.0	.57	93	4.5	1.67	–64	–16.9	.143	–10	.44	173

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

ATF-25735 (AT-12535)
0.5-10 GHz General Purpose Gallium Arsenide FET

Features

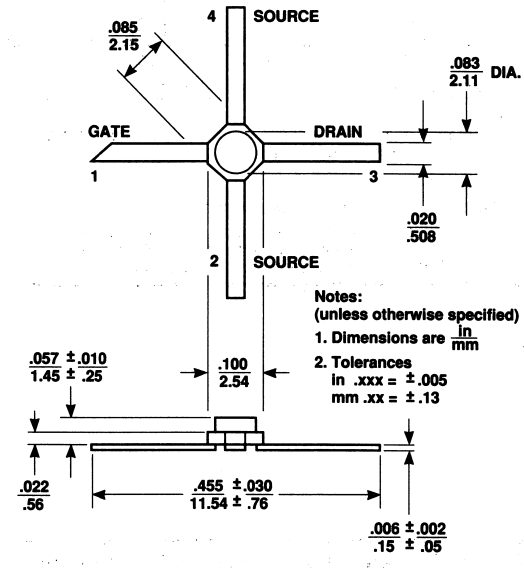
- **High Output Power: 19.0 dBm typical $P_{1\,dB}$ at 4 GHz**
- **High Gain: 12.5 dB typical $G_{1\,dB}$ at 4 GHz**
- **Low Noise Figure: 1.2 dB typical at 4 GHz**
- **Cost Effective Ceramic Microstrip Package**

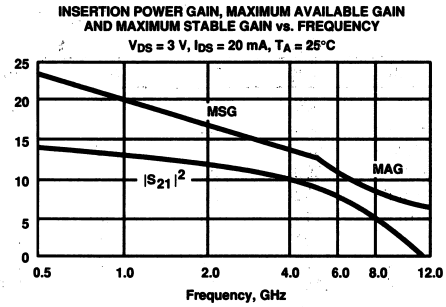
Description

The ATF-25735 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a cost effective microstrip package. This device is designed for use in general purpose amplifier and oscillator applications in the 0.5-10 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length using airbridge interconnects between drain fingers. Total gate periphery is 500 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

35 micro-X Package





Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 3 V, I_{DS} = 20 mA	f = 2.0 GHz f = 4.0 GHz f = 6.0 GHz	dB		1.0 1.2 1.4	1.5
G_A	Gain @ NF_O: V_{DS} = 3 V, I_{DS} = 20 mA	f = 2.0 GHz f = 4.0 GHz f = 6.0 GHz	dB	 11.5 	15.0 13.0 10.5	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 5 V, I_{DS} = 50 mA	f = 4.0 GHz	dBm		19.0	
$G_{1\,dB}$	1dB Compressed Gain: V_{DS} = 5 V, I_{DS} = 50 mA	f = 4.0 GHz	dB		12.5	
g_m	Transconductance: V_{DS} = 3 V, V_{GS} = 0 V		mmho	50	80	
I_{DSS}	Saturated Drain Current: V_{DS} = 3 V, V_{GS} = 0 V		mA	50	100	150
V_P	Pinchoff Voltage: V_{DS} = 3 V, I_{DS} = 1 mA		V	–3.0	–2.0	–0.8

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+7 V
Gate-Source Voltage	V_{GS}	–4 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	450 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature[4]	T_{STG}	–65°C to +175°C

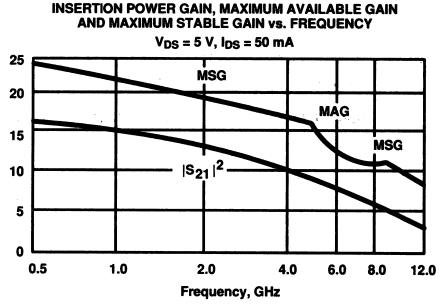
Thermal Resistance: θ_{jc} = 325°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm Spot Size[5]

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 3 mW/°C for T_{CASE} > 29°C.
4. Storage above +150°C may tarnish the leads of this package difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safety stored up to 175°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)



Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 3 V, I_{DS} = 20 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.5	.98	–22	13.9	4.95	159	–32.0	.025	77	.52	–12
1.0	.94	–45	13.3	4.61	142	–27.1	.044	64	.52	–20
2.0	.85	–82	12.2	4.06	110	–21.6	.083	45	.46	–41
3.0	.70	–116	11.0	3.54	81	–19.3	.109	24	.38	–61
4.0	.58	–152	10.0	3.17	54	–17.7	.131	12	.35	–81
5.0	.50	165	8.9	2.78	27	–16.7	.146	–7	.29	–97
6.0	.52	122	7.7	2.43	1	–16.1	.156	–20	.18	–112
7.0	.59	90	6.3	2.06	–23	–15.8	.162	–34	.07	–161
8.0	.65	66	5.1	1.79	–43	–15.5	.167	–46	.09	107
9.0	.69	44	3.8	1.55	–63	–15.3	.172	–53	.15	76
10.0	.73	32	2.7	1.36	–82	–15.4	.170	–65	.18	53
11.0	.79	20	1.1	1.14	–100	–15.5	.168	–78	.21	24
12.0	.84	7	–0.2	.98	–119	–15.7	.161	–93	.26	–5

T_A = 25°C, V_{DS} = 5 V, I_{DS} = 50 mA

0.5	.93	–21	16.0	6.29	156	–34.0	.020	69	.56	–10
1.0	.88	–42	15.4	5.89	140	–29.6	.033	62	.53	–21
2.0	.78	–81	14.1	5.08	108	–24.4	.060	49	.47	–43
3.0	.65	–112	12.6	4.27	83	–22.6	.074	39	.44	–55
4.0	.55	–142	11.4	3.73	58	–21.0	.089	28	.41	–64
5.0	.48	–176	10.6	3.37	36	–19.7	.104	20	.37	–69
6.0	.47	142	9.7	3.04	10	–18.3	.122	6	.28	–83
7.0	.56	104	8.4	2.64	–14	–17.5	.134	–6	.14	–105
8.0	.65	80	7.0	2.25	–35	–16.7	.146	–17	.07	172
9.0	.73	61	5.8	1.94	–53	–16.1	.157	–26	.14	113
10.0	.78	47	4.7	1.71	–72	–15.4	.169	–40	.20	94
11.0	.80	34	3.6	1.51	–90	–15.1	.176	–53	.27	68
12.0	.85	18	2.7	1.36	–109	–14.8	.181	–64	.36	45

A model for this device is available in the DEVICE MODELS section.

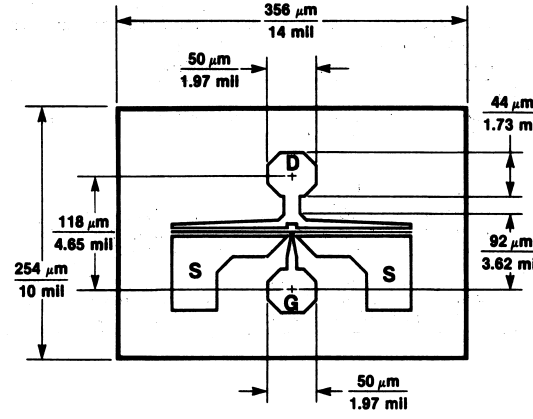
HEWLETT PACKARD

ATF-26100 (AT-10600)
2-18 GHz General Purpose Gallium Arsenide FET

Features

- **Low Noise Figure: 1.8 dB typical at 12 GHz**
- **High Associated Gain: 9.0 dB typical at 12 GHz**
- **High Output Power: 18.0 dBm typical $P_{1\,dB}$ at 12 GHz**

Chip Outline



Description

The ATF-26100 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor chip. This device is designed for use in low noise, wideband amplifier and oscillator applications in the 2-18 GHz frequency range.

This GaAs FET chip has a nominal 0.3 micron gate length with a total gate periphery of 250 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

The recommended mounting procedure is to die attach at a stage temperature of 300 C using a gold-tin preform under forming gas. Assembly can be performed with either wedge or ball bonding using 0.7 mil gold wire. See also "Chip Use" in the APPLICATIONS section.

Noise Parameters: V_{DS} = 3 V, I_{DS} = 10 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
6.0	1.3	.67	52	1.08
8.0	1.5	.45	84	1.03
12.0	1.8	.22	–158	.84
14.0	2.0	.33	–136	.91

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 3 V, I_{DS} = 10 mA	f = 8.0 GHz	dB		1.5	
		f = 12.0 GHz	dB		1.8	2.2
		f = 14.0 GHz	dB		2.0	
G_A	Gain @ NF_O: V_{DS} = 3 V, I_{DS} = 10 mA	f = 8.0 GHz	dB		12.0	
		f = 12.0 GHz	dB	8.0	9.0	
		f = 14.0 GHz	dB		8.0	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 5 V, I_{DS} = 30 mA	f = 12.0 GHz	dBm		18.0	
$G_{1\,dB}$	1dB Compressed Gain: V_{DS} = 5 V, I_{DS} = 30 mA	f = 12.0 GHz	dB		8.0	
g_m	Transconductance: V_{DS} = 3 V, V_{GS} = 0 V		mmho	20	40	
I_{DSS}	Saturated Drain Current: V_{DS} = 3 V, V_{GS} = 0 V		mA	30	50	90
V_P	Pinchoff Voltage: V_{DS} = 3 V, I_{DS} = 1 mA		V	–3.0	–1.7	–0.8

Note: 1. RF performance is determined by assembling and testing 10 samples per wafer.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+7 V
Gate-Source Voltage	V_{GS}	–4 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	275 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	–65°C to +175°C

Thermal Resistance: θ_{jc} = 225°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm Spot Size[4]

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Mounting Surface Temperature = 25°C.
3. Derate at 4.4 mW/°C for $T_{MOUNTING\ SURFACE}$ > 113°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

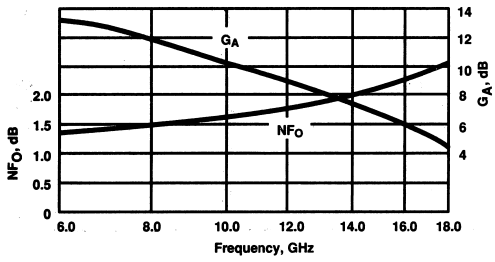
Part Number Ordering Information

Part Number	Devices Per Tray
ATF-26100-GP1	5
ATF-26100-GP3	50
ATF-26100-GP6	up to 300

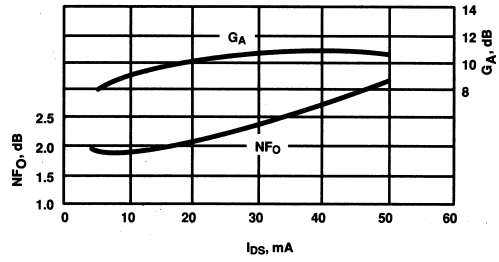
Typical Performance, T_A = 25°C

(unless otherwise noted)

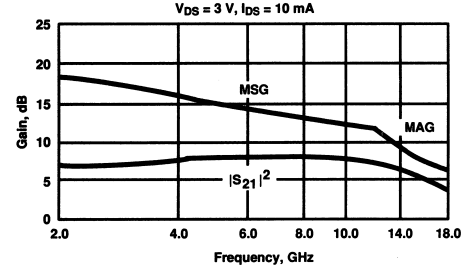
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN vs. FREQUENCY
V_{DS} = 3 V, I_{DS} = 10 mA



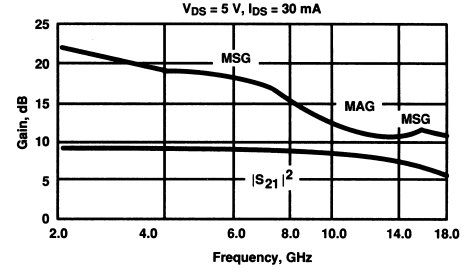
OPTIMUM NOISE FIGURE AND ASSOCIATED GAIN vs. I_{DS}
V_{DS} = 3 V, f = 12 GHz



INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{DS} = 3 V, I_{DS} = 10 mA



INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{DS} = 5 V, I_{DS} = 30 mA



Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 3 V, I_{DS} = 10 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
2.0	.98	–19	6.5	2.11	161	–29.4	.034	82	.68	–4
3.0	.96	–28	6.5	2.11	151	–25.8	.051	78	.67	–6
4.0	.93	–37	6.6	2.15	142	–23.5	.067	74	.64	–9
5.0	.90	–47	6.9	2.22	131	–21.5	.084	69	.61	–13
6.0	.86	–59	7.1	2.27	120	–19.9	.101	64	.57	–17
7.0	.80	–72	7.2	2.29	110	–18.6	.117	59	.52	–23
8.0	.74	–83	7.3	2.32	100	–17.7	.130	54	.48	–28
9.0	.68	–97	7.3	2.33	89	–16.9	.143	48	.43	–36
10.0	.61	–114	7.3	2.31	77	–16.1	.156	42	.38	–46
11.0	.55	–133	7.1	2.27	66	–15.6	.166	35	.33	–56
12.0	.52	–153	6.8	2.18	54	–15.2	.174	28	.28	–66
13.0	.49	–174	6.4	2.10	44	–14.9	.180	21	.24	–78
14.0	.49	165	6.0	2.00	33	–14.7	.184	10	.17	–99
15.0	.52	144	5.3	1.84	21	–14.6	.186	6	.15	–109
16.0	.54	131	4.6	1.69	12	–14.6	.187	3	.13	–121
17.0	.57	117	4.0	1.58	3	–14.5	.189	–6	.10	–177
18.0	.58	105	3.2	1.45	–6	–14.4	.190	–12	.13	145

T_A = 25°C, V_{DS} = 5 V, I_{DS} = 30 mA

2.0	.98	–22	9.6	3.01	158	–33.2	.022	85	.71	–3
3.0	.93	–34	9.5	2.98	146	–30.8	.029	81	.70	–5
4.0	.87	–45	9.6	3.02	136	–28.2	.039	78	.68	–8
5.0	.81	–59	9.7	3.05	124	–25.8	.051	76	.65	–11
6.0	.74	–72	9.5	2.98	112	–24.7	.058	74	.62	–14
7.0	.68	–86	9.1	2.86	101	–23.4	.068	72	.60	–18
8.0	.63	–100	8.9	2.80	91	–22.5	.075	70	.57	–22
9.0	.56	–113	8.8	2.76	82	–21.7	.082	69	.55	–26
10.0	.51	–130	8.4	2.62	72	–20.6	.096	68	.53	–30
11.0	.46	–143	8.0	2.52	62	–20.0	.100	66	.51	–40
12.0	.42	–156	7.8	2.45	54	–19.6	.105	64	.47	–49
13.0	.41	–168	7.5	2.37	46	–18.9	.114	60	.46	–54
14.0	.40	164	7.2	2.29	38	–17.8	.129	56	.44	–60
15.0	.41	145	6.6	2.15	29	–16.9	.143	52	.42	–65
16.0	.44	132	6.2	2.04	21	–15.5	.167	45	.40	–72
17.0	.47	120	5.9	1.97	11	–14.7	.185	40	.35	–80
18.0	.51	104	5.2	1.83	2	–14.6	.187	34	.30	–93

A model for this device is available in the DEVICE MODELS section.

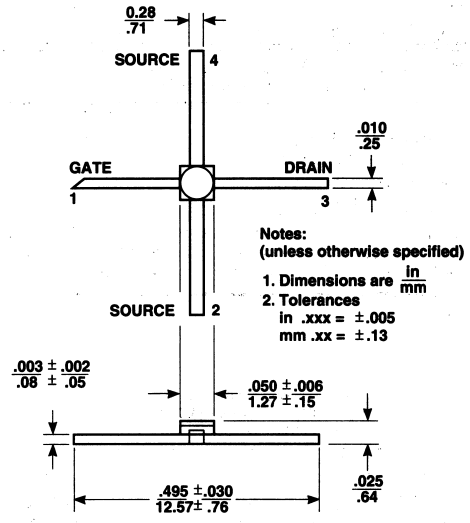
HEWLETT PACKARD

ATF-26150 (AT-10650-1)
2-16 GHz General Purpose Gallium Arsenide FET

Features

- **Low Noise Figure: 1.8 dB typical at 12 GHz**
- **High Associated Gain: 9.0 dB typical at 12 GHz**
- **High Output Power: 18.0 dBm typical $P_{1\,dB}$ at 12 GHz**
- **Hermetic Gold-Ceramic Microstrip Package**

50 mil Package



Description

The ATF-26150 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a hermetic, high reliability package. Its noise figure makes this device appropriate for use in low noise amplifiers operating in the 2-16 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery of 250 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

Noise Parameters: V_{DS} = 3 V, I_{DS} = 10 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
6.0	1.3	.59	74	.77
8.0	1.5	.57	110	.56
12.0	1.8	.63	178	.06
14.0	2.0	.70	–134	.73

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 3 V, I_{DS} = 10 mA	f = 8.0 GHz f = 12.0 GHz f = 14.0 GHz	dB dB dB		1.5 1.8 2.0	2.2
G_A	Gain @ NF_O: V_{DS} = 3 V, I_{DS} = 10 mA	f = 8.0 GHz f = 12.0 GHz f = 14.0 GHz	dB dB dB	8.0	11.5 9.0 8.0	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 5 V, I_{DS} = 30 mA	f = 12.0 GHz	dBm		18.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 5 V, I_{DS} = 30 mA	f = 12.0 GHz	dB		8.0	
g_m	Transconductance: V_{DS} = 3 V, V_{GS} = 0 V		mmho	20	40	
I_{DSS}	Saturated Drain Current: V_{DS} = 3 V, V_{GS} = 0 V		mA	30	50	90
V_P	Pinchoff Voltage: V_{DS} = 3 V, I_{DS} = 1 mA		V	–3.0	–1.7	–0.8

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+7 V
Gate-Source Voltage	V_{GS}	–4 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	275 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	–65°C to +175°C

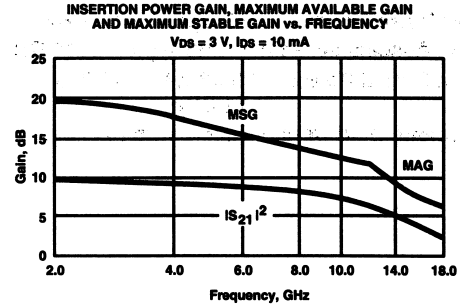
Thermal Resistance: θ_{jc} = 325°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm Spot Size[4]

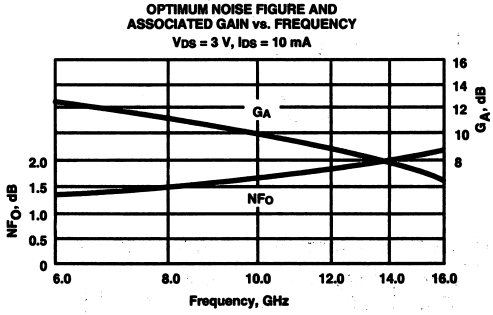
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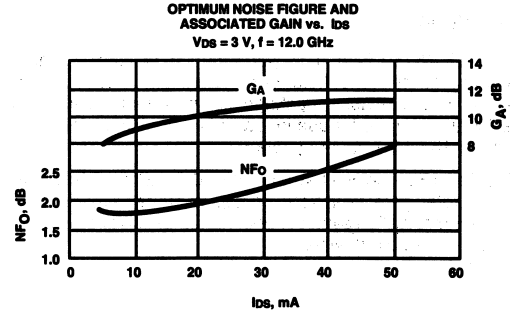
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 3 mW/°C for T_{CASE} > 86°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)







Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 3 V, I_{DS} = 10 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
2.0	.96	–35	8.7	2.73	153	–28.0	.040	73	.76	–20
3.0	.93	–50	8.4	2.64	139	–26.2	.049	62	.72	–29
4.0	.91	–64	8.1	2.54	122	–24.7	.058	51	.68	–38
5.0	.88	–79	7.7	2.42	105	–23.5	.067	40	.64	–47
6.0	.85	–94	7.2	2.30	89	–22.4	.076	29	.60	–56
7.0	.81	–110	7.1	2.27	75	–21.4	.085	18	.56	–65
8.0	.76	–129	7.0	2.25	60	–20.3	.097	7	.51	–75
9.0	.73	–147	6.8	2.20	44	–19.4	.107	–3	.46	–89
10.0	.69	–164	6.5	2.11	27	–19.2	.110	–14	.44	–105
11.0	.67	–178	5.9	1.98	14	–19.1	.111	–20	.41	–123
12.0	.64	166	5.7	1.93	–1	–19.0	.112	–30	.39	–137
13.0	.62	151	5.3	1.85	–15	–18.9	.114	–32	.37	–152
14.0	.59	135	5.1	1.81	–29	–18.7	.116	–46	.34	–173
15.0	.56	120	4.5	1.68	–43	–18.6	.117	–54	.35	160
16.0	.54	109	3.8	1.55	–58	18.5	.119	–67	.41	137
17.0	.51	99	3.1	1.43	–71	18.4	.120	–72	.46	125
18.0	.48	86	2.3	1.31	–85	18.1	.125	–77	.51	114

A model for this device is available in the DEVICE MODELS section.

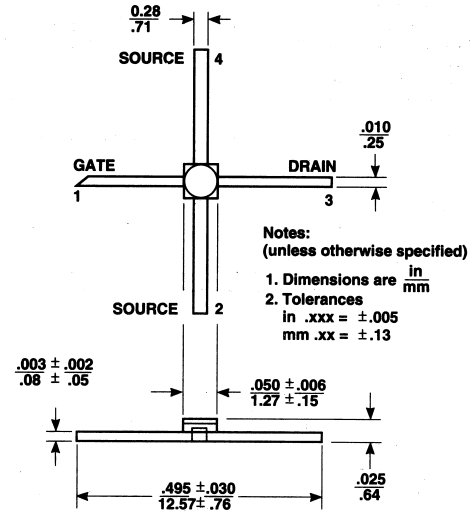
HEWLETT PACKARD

ATF-26350 (AT-10650-3)
2-16 GHz General Purpose Gallium Arsenide FET

Features

- **Low Noise Figure: 2.3 dB typical at 12 GHz**
- **High Associated Gain: 8.0 dB typical at 12 GHz**
- **High Output Power: 18.0 dBm typical $P_{1\,dB}$ at 12 GHz**
- **Hermetic Gold-Ceramic Microstrip Package**

50 mil Package



Description

The ATF-26350 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a hermetic, high reliability package. Its noise figure makes this device appropriate for use in low noise amplifiers operating in the 2-16 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery of 250 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

Noise Parameters: V_{DS} = 3 V, I_{DS} = 10 mA

Freq. GHz	NF_O dB	Gamma Opt Mag	Gamma Opt Ang	$R_N/50$
6.0	1.8	.49	82	.72
8.0	2.0	.50	118	.52
12.0	2.3	.55	–165	.13
14.0	2.5	.72	–119	.96

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 3 V, I_{DS} = 10 mA	f = 8.0 GHz f = 12.0 GHz f = 14.0 GHz	dB dB dB		2.0 2.3 2.5	2.5
G_A	Gain @ NF_O: V_{DS} = 3 V, I_{DS} = 10 mA	f = 8.0 GHz f = 12.0 GHz f = 14.0 GHz	dB dB dB	7.0	11.0 8.0 7.0	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 5 V, I_{DS} = 30 mA	f = 14.0 GHz	dBm		18.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 5 V, I_{DS} = 30 mA	f = 14.0 GHz	dB		8.0	
gm	Transconductance: V_{DS} = 3 V, V_{GS} = 0 V		mmho	20	40	
I_{DSS}	Saturated Drain Current: V_{DS} = 3 V, V_{GS} = 0 V		mA	30	50	90
V_P	Pinchoff Voltage: V_{DS} = 3 V, I_{DS} = 1 mA		V	–3.0	–1.7	–0.8

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+7 V
Gate-Source Voltage	V_{GS}	–4 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	275 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	–65°C to +175°C

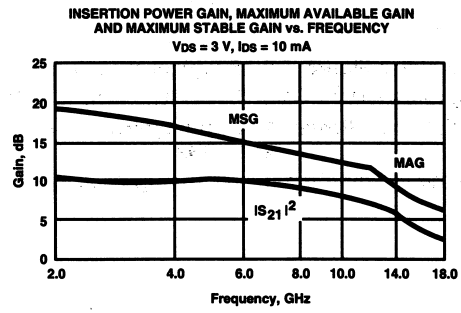
Thermal Resistance: θ_{jc} = 325°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm Spot Size[4]

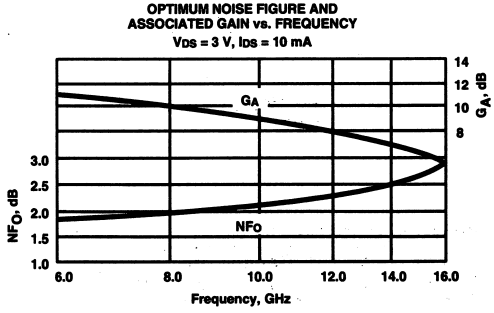
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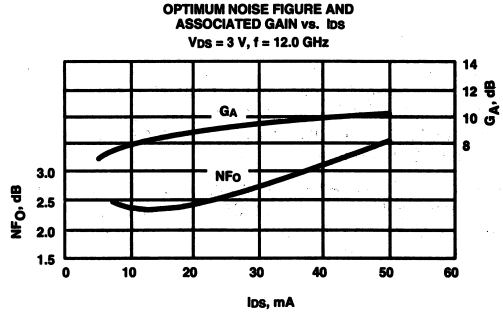
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 3 mW/°C for T_{CASE} > 86°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)







Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 3 V, I_{DS} = 10 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
2.0	.94	–38	10.2	3.24	145	–27.3	.043	59	.76	–22
3.0	.88	–56	10.0	3.18	129	–25.4	.054	49	.73	–30
4.0	.86	–73	9.9	3.12	113	–23.9	.064	37	.70	–41
5.0	.81	–91	9.7	3.06	97	–22.5	.075	27	.66	–51
6.0	.77	–108	9.5	3.00	81	–21.4	.085	19	.63	–62
7.0	.71	–129	9.3	2.92	65	–20.1	.099	9	.58	–72
8.0	.65	–153	9.0	2.82	48	–19.3	.109	–6	.52	–83
9.0	.63	–176	8.6	2.68	31	–18.9	.114	–19	.48	–96
10.0	.62	164	7.8	2.45	14	–18.7	.116	–23	.44	–112
11.0	.61	148	7.0	2.25	0	–18.8	.115	–29	.42	–128
12.0	.61	130	6.5	2.12	–14	–18.9	.113	–36	.40	–140
13.0	.60	114	6.0	1.99	–28	–19.2	.110	–49	.39	–152
14.0	.60	98	5.5	1.88	–42	–19.3	.108	–57	.36	–171
15.0	.60	85	4.7	1.71	–56	–19.5	.106	–63	.36	165
16.0	.59	73	3.9	1.57	–69	–19.3	.108	–73	.40	141
17.0	.59	65	3.2	1.44	–81	–19.2	.110	–79	.45	131
18.0	.58	54	2.5	1.33	–95	–18.8	.115	–85	.49	123

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

ATF-26550 (AT-10650-5)
2-16 GHz General Purpose Gallium Arsenide FET

Features

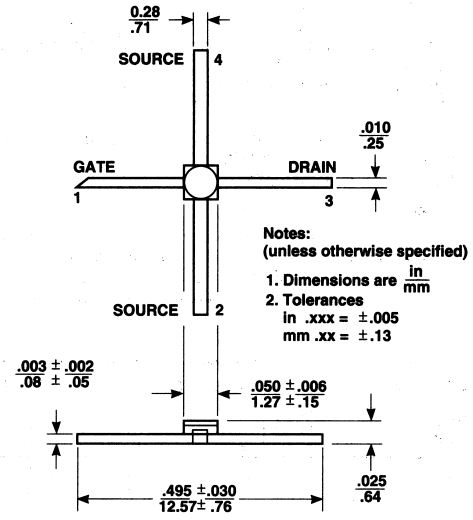
- **High Associated Gain: 8.0 dB typical at 12 GHz**
- **High Output Power: 18.0 dBm typical $P_{1\,dB}$ at 12 GHz**
- **Low Noise Figure: 2.5 dB typical at 12 GHz**
- **Hermetic Gold-Ceramic Microstrip Package**

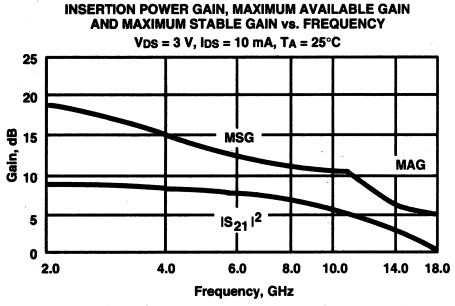
Description

The ATF-26550 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a hermetic, high reliability package. Its noise figure makes this device appropriate for use in the gain stages of low noise amplifiers operating in the 2-16 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery of 250 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

50 mil Package





Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_O	Optimum Noise Figure: V_{DS} = 3 V, I_{DS} = 10 mA	f = 8.0 GHz f = 12.0 GHz f = 14.0 GHz	dB		2.2 2.5 2.7	2.8
G_A	Gain @ NF_O: V_{DS} = 3 V, I_{DS} = 10 mA	f = 8.0 GHz f = 12.0 GHz f = 14.0 GHz	dB	7.0	10.0 8.0 7.0	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 5 V, I_{DS} = 30 mA	f = 12.0 GHz	dBm		18.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 5 V, I_{DS} = 30 mA	f = 12.0 GHz	dB		7.5	
g_m	Transconductance: V_{DS} = 3 V, V_{GS} = 0 V		mmho	20	40	
I_{DSS}	Saturated Drain Current: V_{DS} = 3 V, V_{GS} = 0 V		mA	30	50	90
V_P	Pinchoff Voltage: V_{DS} = 3 V, I_{DS} = 1 mA		V	–3.0	–1.7	–0.8

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+7 V
Gate-Source Voltage	V_{GS}	–4 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	275 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	–65°C to +175°C

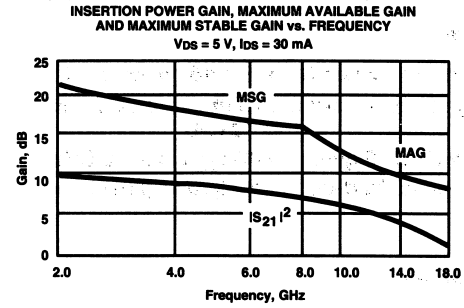
Thermal Resistance: θ_{jc} = 325°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 µm Spot Size[4]

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 3 mW/°C for T_{CASE} > 86°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)



Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 3 V, I_{DS} = 10 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
2.0	.95	–36	8.1	2.53	148	–28.0	.040	64	.75	–18
3.0	.92	–51	7.6	2.41	133	–24.7	.058	55	.71	–26
4.0	.90	–67	7.2	2.30	118	–22.4	.076	43	.68	–39
5.0	.87	–82	6.8	2.18	102	–20.5	.094	34	.64	–49
6.0	.84	–97	6.3	2.06	87	–19.0	.112	24	.60	–58
7.0	.80	–118	6.4	2.08	70	–18.2	.123	7	.55	–71
8.0	.73	–140	6.2	2.04	53	–17.4	.135	–5	.47	–85
9.0	.71	–161	5.8	1.95	35	–17.0	.142	–17	.43	–103
10.0	.67	–178	5.2	1.81	18	–16.7	.146	–27	.42	–120
11.0	.66	167	4.4	1.66	5	–16.8	.144	–39	.41	–134
12.0	.64	150	4.0	1.59	–10	–17.1	.140	–49	.40	–144
13.0	.63	133	3.6	1.51	–23	–17.4	.135	–59	.38	–154
14.0	.63	115	3.0	1.42	–38	–17.5	.133	–66	.36	–172
15.0	.62	99	2.5	1.34	–53	–17.7	.130	–74	.35	158
16.0	.62	89	1.7	1.22	–67	–17.9	.128	–88	.40	134
17.0	.63	81	1.0	1.11	–79	–17.9	.127	–91	.44	123
18.0	.62	70	0.1	1.01	–92	–17.8	.129	–94	.48	118

T_A = 25°C, V_{DS} = 5 V, I_{DS} = 30 mA

2.0	.96	–38	9.0	2.82	144	–32.8	.023	69	.75	–20
3.0	.92	–52	8.4	2.62	130	–30.2	.031	70	.75	–28
4.0	.89	–66	7.9	2.48	116	–27.5	.042	68	.76	–36
5.0	.85	–82	7.8	2.46	100	–25.4	.054	65	.76	–47
6.0	.78	–102	7.7	2.43	84	–24.0	.063	46	.71	–57
7.0	.71	–124	7.5	2.38	66	–23.9	.064	30	.66	–68
8.0	.68	–144	7.2	2.30	52	–23.6	.066	25	.63	–78
9.0	.64	–163	7.0	2.23	37	–23.2	.069	19	.62	–86
10.0	.62	–178	6.4	2.08	21	–23.2	.069	12	.61	–99
11.0	.60	165	5.7	1.93	8	–23.1	.070	5	.61	–112
12.0	.60	149	5.2	1.82	–6	–23.1	.070	–3	.60	–124
13.0	.59	131	4.7	1.71	–21	–23.1	.070	–8	.60	–138
14.0	.59	122	4.1	1.60	–34	–22.5	.075	–15	.60	–152
15.0	.62	105	3.3	1.47	–48	–21.9	.080	–20	.59	–162
16.0	.61	93	3.0	1.42	–60	–21.5	.084	–25	.58	175
17.0	.62	83	2.2	1.29	–74	–21.1	.088	–31	.60	161
18.0	.63	73	1.1	1.13	–85	–20.3	.097	–40	.65	145

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

ATF-26836
2-16 GHz General Purpose Gallium Arsenide FET

Features

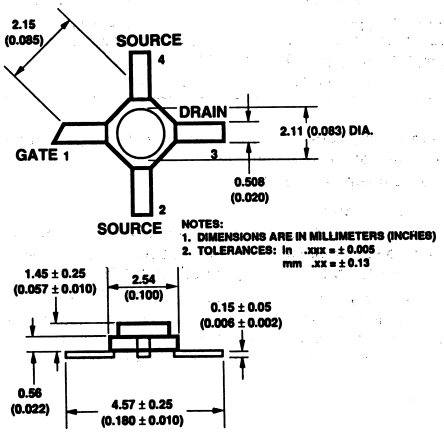
- **High f_{MAX}: 60 GHz typical**
- **High Output Power: 18.0 dBm typical $P_{1\,dB}$ at 12 GHz**
- **High Gain: 9.0 dB typical G_{SS} at 12 GHz**
- **Cost Effective Ceramic Microstrip Package**
- **Tape-and-Reel Packaging Option Available[2]**

Description

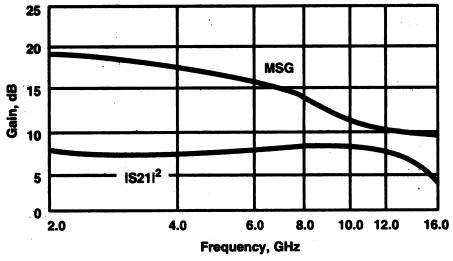
The ATF-26836 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a cost effective microstrip package. This device is designed for use in oscillator applications up to 25 GHz and general purpose amplifier applications in the 2-16 GHz frequency range.

This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery of 250 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

36 micro-X Package[1]



INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{DS} = 5 V, I_{DS} = 30 mA, T_A = 25°C



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
f_{MAX}	Maximum Frequency of Oscillation: V_{DS} = 5 V, I_{DS} = 30 mA		GHz		60	
G_{SS}	Tuned Small Signal Gain: V_{DS} = 5 V, I_{DS} = 30 mA	f = 12.0 GHz	dB	7.0	9.0	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 5 V, I_{DS} = 30 mA	f = 12.0 GHz	dBm	15.0	18.0	
NF_O	Optimum Noise Figure: V_{DS} = 3 V, I_{DS} = 10 mA	f = 12.0 GHz	dB		2.2	
G_A	Gain @ NF_O: V_{DS} = 3 V, I_{DS} = 10 mA	f = 12.0 GHz	dB		6.0	
g_m	Transconductance: V_{DS} = 3 V, V_{GS} = 0 V		mmho	15	35	
I_{DSS}	Saturated Drain Current: V_{DS} = 3 V, V_{GS} = 0 V		mA	30	50	90
V_P	Pinchoff Voltage: V_{DS} = 3 V, I_{DS} = 1 mA		V	–3.5	–1.5	–0.5

Notes: 1. Long leaded 35 micro-X package available upon request.
2. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors".

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+7 V
Gate-Source Voltage	V_{GS}	–4 V
Drain Current	I_{DS}	I_{DSS}
Total Power Dissipation[2,3]	P_T	275 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature[4]	T_{STG}	–65°C to +175°C

Thermal Resistance: θ_{jc} = 350°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm Spot Size[5]

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 2.9 mW/°C for T_{CASE} > 79°C.
4. Storage above +150°C may tarnish the leads of this package difficult to solder into a circuit. After a device has been soldered into a circuit, it may be safety stored up to 175°C.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

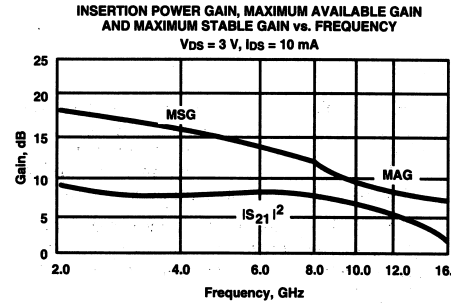
Part Number Ordering Information

Part Number	Devices Per Reel	Reel Size
ATF-26836-TR1	1000	7"
ATF-26836-TR2	4000	13"
ATF-26836-STR	1	STRIP

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

Typical Performance, T_A = 25°C

(unless otherwise noted)



Typical Scattering Parameters: Common Emitter, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 3 V, I_{DS} = 10 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	K
2.0	.94	–38	8.2	2.57	138	–27.1	.044	60	.74	–26	0.39
3.0	.90	–55	7.8	2.45	120	–24.9	.057	51	.71	–35	0.51
4.0	.84	–72	7.6	2.41	102	–22.9	.072	44	.71	–44	0.59
5.0	.75	–92	8.0	2.50	82	–20.6	.093	30	.66	–53	0.76
6.0	.64	–117	8.1	2.55	61	–19.3	.109	15	.60	–64	0.91
7.0	.52	–155	8.3	2.60	37	–18.1	.124	5	.51	–78	0.98
8.0	.49	163	7.9	2.47	14	–17.5	.133	–12	.41	–92	1.05
9.0	.52	126	7.2	2.30	–7	–16.9	.143	–21	.30	–106	1.07
10.0	.56	100	6.4	2.10	–28	–16.8	.144	–32	.24	–125	1.11
11.0	.61	78	5.6	1.91	–47	–17.1	.140	–41	.18	–154	1.16
12.0	.67	58	4.7	1.71	–66	–17.1	.139	–49	.15	168	1.16
13.0	.69	45	3.9	1.57	–83	–17.3	.137	–61	.17	134	1.20
14.0	.72	35	3.0	1.42	–98	–17.2	.138	–66	.19	107	1.20
15.0	.72	22	2.5	1.33	–115	–17.2	.138	–77	.23	89	1.24
16.0	.72	13	2.0	1.26	–128	–17.4	.135	–85	.27	71	1.31

T_A = 25°C, V_{DS} = 5 V, I_{DS} = 30 mA

2.0	.94	–44	9.0	2.82	130	–30.2	.031	65	.80	–31	0.28
3.0	.86	–63	8.5	2.65	110	–28.4	.038	56	.80	–43	0.49
4.0	.78	–81	8.0	2.51	89	–26.9	.045	47	.79	–52	0.72
5.0	.68	–97	7.9	2.49	71	–25.5	.053	41	.78	–58	0.89
6.0	.57	–118	8.1	2.53	51	–24.4	.060	39	.76	–67	0.98
7.0	.43	–151	8.5	2.65	28	–22.4	.076	38	.73	–80	0.90
8.0	.37	165	8.5	2.66	3	–20.6	.093	30	.69	–99	0.82
9.0	.40	122	8.0	2.52	–20	–18.0	.126	15	.64	–119	0.67
10.0	.47	96	7.7	2.42	–42	–16.4	.152	3	.66	–140	0.47
11.0	.55	75	7.5	2.37	–66	–15.1	.176	–4	.63	–166	0.39
12.0	.61	53	7.4	2.35	–88	–13.8	.205	–19	.64	168	0.30
13.0	.71	33	7.4	2.34	–116	–13.2	.220	–39	.71	132	0.11
14.0	.71	10	6.7	2.17	–143	–13.5	.212	–56	.78	104	0.06
15.0	.65	–10	5.7	1.93	–170	–14.0	.200	–72	.85	79	0.04
16.0	.58	–30	4.2	1.62	166	–14.9	.180	–93	.98	61	–0.23

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

ATF-26884
2-16 GHz General Purpose Gallium Arsenide FET

Features

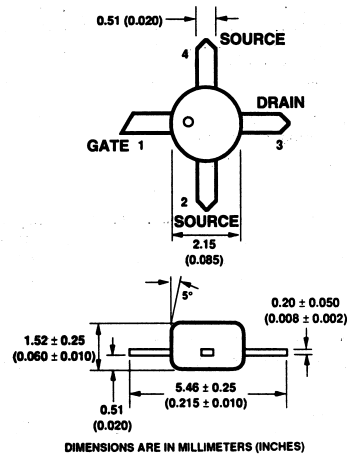
- **High f_{MAX}: 60 GHz typical**
- **High Output Power: 18.0 dBm typical $P_{1\,dB}$ at 12 GHz**
- **High Gain: 9.0 dB typical G_{SS} at 12 GHz**
- **Low Cost Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Description

The ATF-26884 is a high performance gallium arsenide Schottky-barrier-gate field effect transistor housed in a low cost effective plastic package. This device is designed for use in oscillator applications up to 25 GHz and general purpose amplifier applications in the 2-16 GHz frequency range.

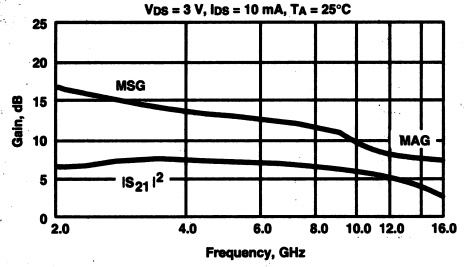
This GaAs FET device has a nominal 0.3 micron gate length with a total gate periphery of 250 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

84 Plastic Package

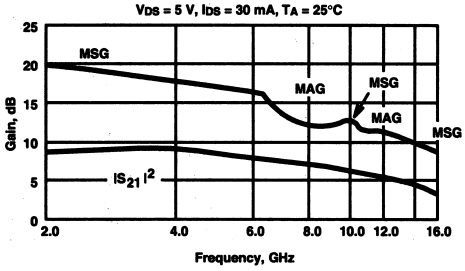


DIMENSIONS ARE IN MILLIMETERS (INCHES)

INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{DS} = 3 V, I_{DS} = 10 mA, T_A = 25°C



INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{DS} = 5 V, I_{DS} = 30 mA, T_A = 25°C



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
f_{MAX}	Maximum Frequency of Oscillation: V_{DS} = 5 V, I_{DS} = 30 mA		GHz		60	
G_{SS}	Tuned Small Signal Gain: V_{DS} = 5 V, I_{DS} = 30 mA	f = 12.0 GHz	dB	7.0	9.0	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 5 V, I_{DS} = 30 mA	f = 12.0 GHz	dBm	15.0	18.0	
NF_O	Optimum Noise Figure: V_{DS} = 3 V, I_{DS} = 10 mA	f = 12.0 GHz	dB		2.2	
G_A	Gain @ NF_O: V_{DS} = 3 V, I_{DS} = 10 mA	f = 12.0 GHz	dB		6.0	
g_m	Transconductance: V_{DS} = 3 V, V_{GS} = 0 V		mmho	15	35	
I_{DSS}	Saturated Drain Current: V_{DS} = 3 V, V_{GS} = 0 V		mA	30	50	90
V_P	Pinchoff Voltage: V_{DS} = 3 V, I_{DS} = 1 mA		V	–3.5	–1.5	–0.5

Note: 1. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors".

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+7 V
Gate-Source Voltage	V_{GS}	–4 V
Drain Current	I_{DS}	I_{DSS}
Total Power Dissipation[2,3]	P_T	275 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	–65°C to +150°C

Thermal Resistance: θ_{jc} = 300°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm Spot Size[4]

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 3.3 mW/°C for T_C > 92.5°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Part Number Ordering Information

Part Number	Devices Per Reel	Reel Size
ATF-26884-TR1	1000	7"
ATF-26884-TR2	4000	13"
ATF-26884-STR	1	STRIP

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 3 V, I_{DS} = 10 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	K
2.0	.96	–36	6.9	2.21	142	–26.6	.047	64	.81	–25	0.22
3.0	.91	–56	7.4	2.35	123	–23.0	.071	50	.77	–38	0.33
4.0	.86	–78	7.6	2.39	103	–20.6	.093	36	.70	–50	0.44
5.0	.79	–97	7.2	2.30	86	–19.5	.106	25	.66	–61	0.57
6.0	.73	–113	6.8	2.20	71	–18.9	.114	16	.62	–70	0.70
7.0	.67	–127	6.4	2.10	56	–18.4	.120	9	.61	–78	0.81
8.0	.62	–144	6.4	2.08	41	–17.9	.128	1	.58	–88	0.88
9.0	.57	–168	6.2	2.03	23	–17.5	.134	–8	.54	–101	0.94
10.0	.53	168	5.8	1.96	6	–17.3	.136	–16	.47	–116	1.07
11.0	.52	147	5.2	1.81	–10	–17.2	.138	–22	.41	–133	1.19
12.0	.49	124	4.9	1.76	–22	–17.1	.140	–26	.39	–143	1.26
13.0	.52	103	4.6	1.70	–36	–16.7	.146	–31	.37	–154	1.21
14.0	.56	80	4.0	1.58	–54	–16.3	.153	–37	.35	–171	1.17
15.0	.60	65	3.3	1.46	–72	–16.3	.153	–42	.35	173	1.16
16.0	.65	52	2.9	1.40	–83	–16.3	.153	–48	.37	132	1.10
17.0	.68	40	2.3	1.30	–99	–16.0	.158	–56	.41	101	1.07
18.0	.69	30	1.3	1.16	–112	–15.9	.159	–72	.47	87	1.03
									T_A = 25°C, V_{DS} = 5 V, I_{DS} = 30 mA		
2.0	.94	–41	9.2	2.88	138	–30.8	.029	65	.84	–23	0.29
3.0	.87	–65	9.5	2.97	118	–27.3	.043	51	.80	–34	0.43
4.0	.79	–89	9.3	2.93	97	–25.5	.053	40	.74	–44	0.63
5.0	.71	–109	8.7	2.73	79	–24.9	.057	35	.71	–53	0.82
6.0	.64	–126	8.1	2.54	64	–24.4	.060	33	.69	–60	0.99
7.0	.57	–142	7.5	2.38	50	–24.0	.063	31	.69	–67	1.12
8.0	.52	–162	7.2	2.30	35	–23.1	.070	30	.69	–76	1.07
9.0	.48	174	6.9	2.21	18	–21.9	.080	28	.67	–87	1.05
10.0	.48	149	6.5	2.11	1	–20.4	.095	24	.63	–100	0.98
11.0	.48	130	5.9	1.97	–14	–19.7	.104	22	.57	–114	1.10
12.0	.49	108	5.6	1.91	–25	–18.1	.125	20	.55	–122	0.96
13.0	.53	88	5.2	1.82	–39	–16.2	.155	18	.54	–132	0.78
14.0	.57	69	4.7	1.71	–55	–15.2	.173	5	.52	–146	0.72
15.0	.62	56	4.1	1.60	–75	–14.8	.182	–1	.52	–165	0.65
16.0	.70	44	3.7	1.53	–87	–13.8	.205	–16	.52	165	0.51
17.0	.75	33	3.0	1.41	–103	–12.9	.226	–28	.54	135	0.45
18.0	.74	24	2.3	1.30	–117	–13.6	.210	–44	.63	114	0.41

A model for this device is available in the DEVICE MODELS section.

ATF-35076, -35176, -35376
2-18 GHz Low Noise Pseudomorphic HEMT

Features

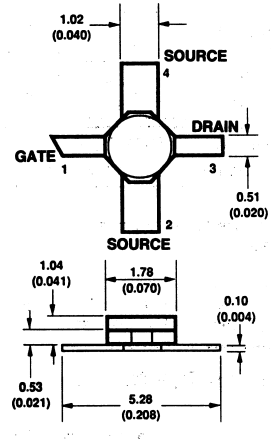
- **PHEMT Technology**
- **Low Noise Figure: 0.75 Typical at 12 GHz**
- **High Associated Gain: 11 dB Typical at 12 GHz**
- **Cost Effective Ceramic Microstrip Package**
- **Tape-and-Reel Packaging Option Available[1]**

Description

The ATF-35076, -35176, and -35376 are noise performance differentiated versions of the high performance ATF-35 Pseudomorphic High Electron Mobility Transistor (PHEMT), housed in the Style 76 cost effective, ceramic microstrip package. The ATF-35076 offers premium noise figure and is an ideal choice for use in the first stage of extremely low noise cascades. The slightly higher noise figure of the ATF-35176 makes it appropriate for use in the second stage of premium cascades or as the first stage in amplifiers that have less critical noise requirements. The moderate noise performance of the ATF-35376 makes this part suitable for second stage use in low noise cascades. Although developed for use in Ku band DBS systems, these devices are also appropriate for use in C band TVRO LNAs or other low noise amplifiers operating in the 2 to 18 GHz frequency range.

These GaAs PHEMT devices have a nominal 0.25 micron gate length with a total gate periphery of 200 microns. Proven gold based metallization systems and nitride passivation assure rugged, reliable devices.

76 Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Typical Noise Parameters: V_{DS} = 1.5 V, I_{DS} = 10 mA

FREQ GHz	ATF-35076 NFO dB	ATF-35176 NFO dB	ATF-35376 NFO dB	ΓOPT MAG	ΓOPT ANG	RN/ZO -
2.0	.13	.14	.17	.82	23	.23
4.0	.25	.28	.33	.74	43	.19
6.0	.38	.43	.50	.62	69	.13
8.0	.50	.57	.67	.57	89	.10
10.0	.63	.71	.83	.51	115	.07
12.0	.75	.85	1.00	.44	140	.05
14.0	.88	.99	1.17	.42	164	.04

ΓOPT and RN/ZO apply equally to the ATF-35076, ATF-35176, and ATF-35376.

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Product	Unit	Min.	Typ.	Max.
NFO	Optimum Noise Figure: V_{DS} = 1.5 V, I_{DS} = 10 mA	f = 4.0 GHz	ATF-35076	dB		0.25	
		f = 12 GHz		dB		0.75	0.80
GA	Gain @ NFO: V_{DS} = 1.5 V, I_{DS} = 10 mA	f = 4.0 GHz		dB		16.0	
		f = 12 GHz		dB	10.0	11.0	
NFO	Optimum Noise Figure: V_{DS} = 1.5 V, I_{DS} = 10 mA	f = 4.0 GHz	ATF-35176	dB		0.30	
		f = 12 GHz		dB		0.85	0.90
GA	Gain @ NFO: V_{DS} = 1.5 V, I_{DS} = 10 mA	f = 4.0 GHz		dB		16.0	
		f = 12 GHz		dB	10.0	11.0	
NFO	Optimum Noise Figure: V_{DS} = 1.5 V, I_{DS} = 10 mA	f = 4.0 GHz	ATF-35376	dB		0.40	
		f = 12 GHz		dB		1.0	1.2
GA	Gain @ NFO: V_{DS} = 1.5 V, I_{DS} = 10 mA	f = 4.0 GHz		dB		15.0	
		f = 12 GHz		dB	9.5	10.0	
gm	Transconductance: V_{DS} = 1.5 V, V_{GS} = 0 V			mS	40	65	
Idss	Saturated Drain Current: V_{DS} = 1.5 V, V_{GS} = 0 V			mA	20	50	70
VP	Pinchoff Voltage: V_{DS} = 1.5 V, I_{DS} = 1 mA			V	-2.0	-0.4	

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+4 V
Gate-Source Voltage	V_{GS}	-3 V
Drain Current	I_D	I_{dss}
Total Power Dissipation [2,3]	P_T	225 mW
RF Input Power	$P_{IN\ max}$	+10 dBm
Channel Temperature	T_{CH}	150°C
Storage Temperature	T_{STG}	-65 to 150°C

Thermal Resistance 2: θ_{jc}=325 °C/W; T_{CH}=150°C
Liquid Crystal Measurement: 1 µm Spot Size 4

Notes:
1. Operation of this device above any one of these limits may cause permanent damage.
2. T_{case} = 25°C
3. Derate at 3.2 mW/ °C for T_C>102°C
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than alternate methods.

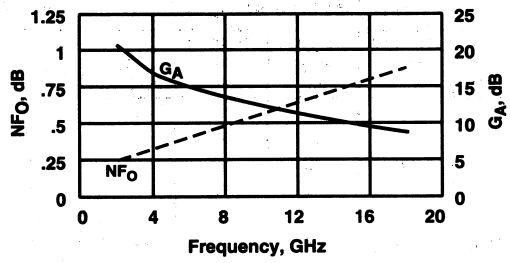
Part Number Order Information

Part Number	Devices Per Reel	Reel Size
ATF-35076-TR1	1000	7"
ATF-35076-TR2	4000	13"
ATF-35076-STR	1	strip
ATF-35176-TR1	1000	7"
ATF-35176-TR2	4000	13"
ATF-35176-STR	1	strip
ATF-35376-TR1	1000	7"
ATF-35376-TR2	4000	13"
ATF-35376-STR	1	strip

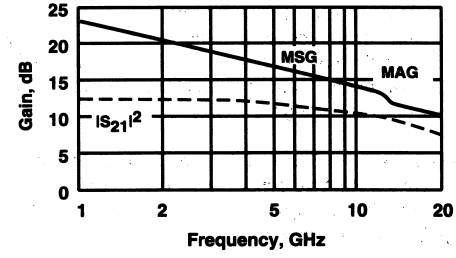
For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

Typical Performance, T_A = 25°C, (Unless otherwise noted)

Noise Figure and Associated Gain vs. Frequency (ATF-35076) V_{DS} = 1.5 V, I_{DS} = 10 mA



Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency V_{DS} = 1.5 V, I_{DS} = 10 mA



Typical Scattering Parameters: Common Source, Z_o = 50 Ω T_A = 25°C, V_{DS} = 1.5 V, I_{DS} = 10 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
2.0	.98	-31	12.69	4.10	149	-29.11	.035	67	.49	-24
3.0	.95	-43	12.13	4.04	137	-25.85	.051	59	.47	-33
4.0	.92	-60	12.06	4.01	122	-23.48	.067	48	.45	-45
5.0	.88	-76	11.84	3.91	106	-21.94	.080	36	.41	-58
6.0	.83	-92	11.51	3.76	91	-20.82	.091	26	.38	-70
7.0	.79	-108	11.22	3.64	77	-20.00	.100	16	.35	-83
8.0	.76	-119	10.95	3.53	67	-19.33	.108	10	.32	-90
9.0	.73	-134	10.66	3.41	53	-18.86	.114	0	.29	-102
10.0	.70	-149	10.32	3.28	39	-18.42	.120	-10	.27	-114
11.0	.66	-164	10.01	3.17	26	-18.20	.123	-20	.24	-127
12.0	.63	-179	9.75	3.07	13	-17.86	.128	-29	.22	-139
13.0	.61	166	9.57	3.01	09	-17.79	.129	-39	.20	-150
14.0	.60	155	9.37	2.94	-83	-17.65	.131	-43	.16	-158
15.0	.59	140	9.17	2.88	-22	-17.52	.133	-54	.14	-170
16.0	.57	124	8.91	2.79	-35	-17.46	.134	-65	.11	178
17.0	.55	108	8.82	2.76	-50	-17.20	.138	-76	.07	166
18.0	.54	88	8.77	2.75	-64	-17.02	.141	-89	.04	131

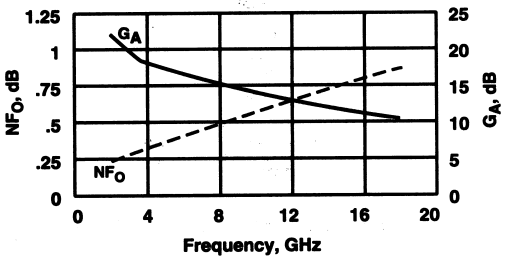
The above S parameter description applies equally to the ATF-35076, -35176, and -35376.

ATF-35 Series Pseudomorphic HEMT

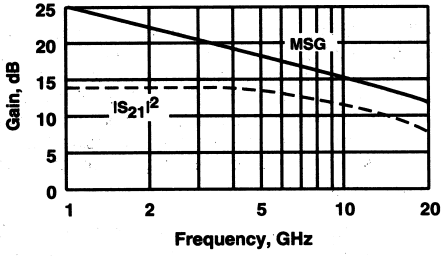
For the ATF-35 Series PHEMTs, increasing I_{ds} from 10 mA to 20 mA has the effect of increasing gain at 12 GHz by approximately 1 dB without significantly altering noise performance. Designers having the flexibility to operate at this higher bias current may want to take advantage of this feature. 20 mA S parameter data follows. Since device capacitances vary little with bias current, the 10 mA noise parameters may also be used to describe 20 mA noise performance.

Typical Performance, T_A = 25°C, (Unless otherwise noted)

Noise Figure and Associated Gain vs. Frequency (ATF-35076) V_{DS} = 1.5 V, I_{DS} = 20 mA



Insertion Power Gain and Maximum Stable Gain vs. Frequency V_{DS} = 1.5 V, I_{DS} = 20 mA



Typical Scattering Parameters: Common Source, Z_o = 50 Ω

T_A = 25°C, V_{DS} = 1.5 V, I_{DS} = 20 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
2.0	.97	-33	13.89	4.95	147	-29.62	.033	68	.41	-24
3.0	.95	-45	13.76	4.88	135	-26.56	.047	60	.40	-33
4.0	.91	-62	13.57	4.77	119	-24.44	.060	50	.37	-45
5.0	.86	-79	13.20	4.57	103	-22.73	.073	38	.33	-57
6.0	.80	-95	12.75	4.34	88	-21.72	.082	28	.30	-69
7.0	.76	-110	12.34	4.14	74	-20.82	.091	19	.27	-82
8.0	.74	-121	12.07	4.01	65	-20.09	.099	14	.24	-90
9.0	.71	-135	11.75	3.87	51	-19.66	.104	5	.22	-102
10.0	.67	-150	11.35	3.70	37	-19.17	.110	-5	.20	-113
11.0	.62	-164	10.95	3.53	24	-18.86	.114	-14	.17	-123
12.0	.59	-178	10.63	3.40	11	-18.42	.120	-23	.15	-138
13.0	.57	167	10.47	3.34	-2	-18.20	.123	-33	.14	-152
14.0	.56	156	10.32	3.28	-9	-17.99	.126	-37	.12	-164
15.0	.54	140	10.10	3.20	-23	-17.92	.127	-47	.10	-173
16.0	.52	125	9.82	3.10	-37	-17.65	.131	-58	.06	-179
17.0	.49	107	9.70	3.05	-51	-17.39	.135	-70	.03	165
18.0	.50	88	9.72	3.06	-66	-17.08	.140	-82	.03	53

The above S parameter description applies equally to the ATF-35076, -35176, and -35376.

HEWLETT PACKARD

ATF-35576
2-18 GHz Low Noise Pseudomorphic HEMT

Features

- **PHEMT Technology**
- **High Gain at Moderate Noise Figure:**
  G = 12 dB Typ, NF = 2.0 dB Max @ 12 GHz
- **Cost Effective Ceramic Microstrip Package**
- **Tape-and-Reel Packaging Option Available[1]**

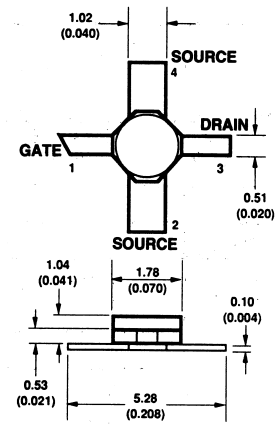
Description

The ATF-35576 is a high performance Pseudomorphic High Electron Mobility Transistor (PHEMT), housed in a cost effective ceramic microstrip package. This device is a superior choice for use as the third stage of Ku band DBS low noise cascades where high gain to mask mixer noise contributions is more important than an extremely low noise figure. The ATF-35576 is also suitable for general gain applications in the 2 to 18 GHz frequency range.

For optimum performance in low noise cascades, this device should be matched primarily for gain, with only a small offset in tuning for noise figure. Designers having the flexibiltiy to operate with an I_{DS} of 20 mA rather than 10 mA will find that at 12 GHz the higher bias results in approximately 1 dB of additional gain with no significant alteration in noise performance.

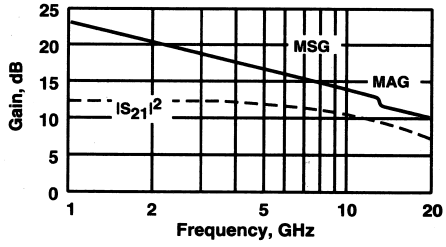
This GaAs PHEMT device has a nominal 0.25 micron gate length with a total gate periphery of 200 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

76 Package

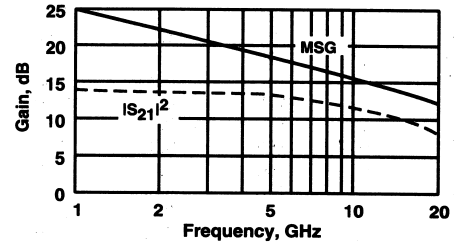


DIMENSIONS ARE IN MILLIMETERS (INCHES)

Insertion Power Gain, Maximum Available Gain and Maximum Stable Gain vs. Frequency
V_{DS} = 1.5 V, I_{DS} = 10 mA



Insertion Power Gain and Maximum Stable Gain vs. Frequency
V_{DS} = 1.5 V, I_{DS} = 20 mA



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
G	Gain @ NF: V_{DS} = 1.5 V, I_{DS} = 10 mA	f = 4.0 GHz	dB		17.0	
		f = 12 GHz[2]	dB	11.0	12.0	
NF	Noise Figure: V_{DS} = 1.5 V, I_{DS} = 10 mA	f = 4.0 GHz	dB		1.0	
		f = 12 GHz[2]	dB		1.5	2.0
gm	Transconductance: V_{DS} = 1.5 V, V_{GS} = 0 V		mS	40	65	
Idss	Saturated Drain Current: V_{DS} = 1.5 V, V_{GS} = 0 V		mA	20	50	70
VP	Pinchoff Voltage: V_{DS} = 1.5 V, I_{DS} = 1 mA		V	-2.0	-0.4	

Notes: 1. Refer to AB-0008: "Tape-and-Reel Packaging for Surface Mount Semiconductors"
2. Tested with generator impedance, offset slightly from maximum gain setting to provide improved noise performance.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+4 V
Gate-Source Voltage	V_{GS}	-3 V
Drain Current	I_D	I_{dss}
Total Power Dissipation [2,3]	P_T	225 mW
RF Input Power	$P_{IN\ max}$	+10 dBm
Channel Temperature	T_{CH}	150°C
Storage Temperature	T_{STG}	-65 to 150°C

Thermal Resistance [2]: θ_{jc}=325 °C/W; T_{CH}=150°C
Liquid Crystal Measurement: 1μm Spot Size [4]

Notes:
1. Operation of this device above any one of these limits may cause permanent damage.
2. T_{case} = 25°C
3. Derate at 3.2 mW/ °C for T_C>102°C
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than alternate methods.

Part Number Order Information

Part Number	Devices Per Reel	Reel Size
ATF-35576-TR1	1000	7"
ATF-35576-TR2	4000	13"
ATF-35576-STR	1	strip

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

Typical Scattering Parameters: Common Source, Z_o = 50 Ω

T_A = 25°C, V_{DS} = 1.5 V, I_{DS} = 10 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
2.0	.98	-31	12.69	4.10	149	-29.11	.035	67	.49	-24
3.0	.95	-43	12.13	4.04	137	-25.85	.051	59	.47	-33
4.0	.92	-60	12.06	4.01	122	-23.48	.067	48	.45	-45
5.0	.88	-76	11.84	3.91	106	-21.94	.080	36	.41	-58
6.0	.83	-92	11.51	3.76	91	-20.82	.091	26	.38	-70
7.0	.79	-108	11.22	3.64	77	-20.00	.100	16	.35	-83
8.0	.76	-119	10.95	3.53	67	-19.33	.108	10	.32	-90
9.0	.73	-134	10.66	3.41	53	-18.86	.114	0	.29	-102
10.0	.70	-149	10.32	3.28	39	-18.42	.120	-10	.27	-114
11.0	.66	-164	10.01	3.17	26	-18.20	.123	-20	.24	-127
12.0	.63	-179	9.75	3.07	13	-17.86	.128	-29	.22	-139
13.0	.61	166	9.57	3.01	09	-17.79	.129	-39	.20	-150
14.0	.60	155	9.37	2.94	-83	-17.65	.131	-43	.16	-158
15.0	.59	140	9.17	2.88	-22	-17.52	.133	-54	.14	-170
16.0	.57	124	8.91	2.79	-35	-17.46	.134	-65	.11	178
17.0	.55	108	8.82	2.76	-50	-17.20	.138	-76	.07	166
18.0	.54	88	8.77	2.75	-64	-17.02	.141	-89	.04	131

Typical Scattering Parameters: Common Source, Z_o = 50 Ω

T_A = 25°C, V_{DS} = 1.5 V, I_{DS} = 20 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
2.0	.97	-33	13.89	4.95	147	-29.62	.033	68	.41	-24
3.0	.95	-45	13.76	4.88	135	-26.56	.047	60	.40	-33
4.0	.91	-62	13.57	4.77	119	-24.44	.060	50	.37	-45
5.0	.86	-79	13.20	4.57	103	-22.73	.073	38	.33	-57
6.0	.80	-95	12.75	4.34	88	-21.72	.082	28	.30	-69
7.0	.76	-110	12.34	4.14	74	-20.82	.091	19	.27	-82
8.0	.74	-121	12.07	4.01	65	-20.09	.099	14	.24	-90
9.0	.71	-135	11.75	3.87	51	-19.66	.104	5	.22	-102
10.0	.67	-150	11.35	3.70	37	-19.17	.110	-5	.20	-113
11.0	.62	-164	10.95	3.53	24	-18.86	.114	-14	.17	-123
12.0	.59	-178	10.63	3.40	11	-18.42	.120	-23	.15	-138
13.0	.57	167	10.47	3.34	-2	-18.20	.123	-33	.14	-152
14.0	.56	156	10.32	3.28	-9	-17.99	.126	-37	.12	-164
15.0	.54	140	10.10	3.20	-23	-17.92	.127	-47	.10	-173
16.0	.52	125	9.82	3.10	-37	-17.65	.131	-58	.06	-179
17.0	.49	107	9.70	3.05	-51	-17.39	.135	-70	.03	165
18.0	.50	88	9.72	3.06	-66	-17.08	.140	-82	.03	53

HEWLETT PACKARD

ATF-44100 (AT-8141)
2-8 GHz Medium Power
Gallium Arsenide FET

Features

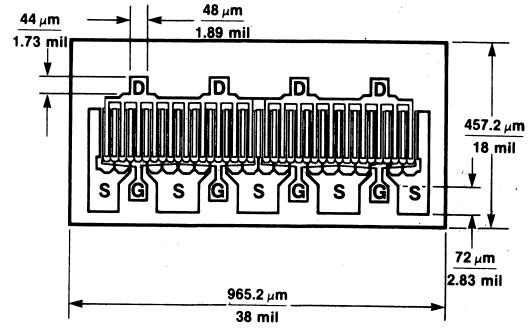
- **High Output Power:**
  32.0 dBm typical $P_{1\,dB}$ at 4 GHz
- **High Gain at 1 dB Compression:**
  9.0 dB typical $G_{1\,dB}$ at 4 GHz
- **High Power Efficiency:**
  36% typical at 4 GHz

Description

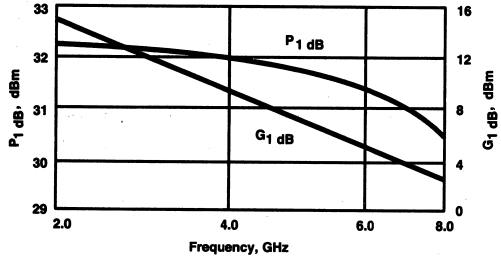
The ATF-44100 is a gallium arsenide Schottky-barrier-gate field effect transistor designed for medium power, linear amplification in the 2 to 8 GHz frequency range. This nominally 0.5 micron gate length GaAs FET is an interdigitated four-cell structure using airbridge interconnects between source fingers. Total gate periphery is 5 millimeters. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

The recommended mounting procedure is to die attach at a stage temperature of 300° C using a gold-tin preform under forming gas. Assembly should be performed with wedge bonding using either 0.7 mil of 1.0 mil gold wire. See also "Chip Use" in the APPLICATIONS section.

Chip Outline



POWER OUTPUT @ 1 dB GAIN COMPRESSION AND
1 dB COMPRESSED GAIN vs. FREQUENCY
V_{DS} = 9 V, I_{DS} = 500 mA



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression:	f = 4.0 GHz	dBm		32.0	
	V_{DS} = 9 V, I_{DS} = 500 mA	f = 6.0 GHz			31.5	
		f = 8.0 GHz			31.0	
$G_{1\,dB}$	1 dB Compressed Gain:	f = 4.0 GHz	dB	8.0	9.0	
	V_{DS} = 9 V, I_{DS} = 500 mA	f = 6.0 GHz			6.0	
		f = 8.0 GHz			3.0	
η_{add}	Efficiency @ $P_{1\,dB}$: V_{DS} = 9 V, I_{DS} = 500 mA	f = 4.0 GHz	%		36	
g_m	Transconductance: V_{DS} = 2.5 V, I_{DS} = 500 mA		mmho		300	
I_{DSS}	Saturated Drain Current: V_{DS} = 1.75 V, V_{GS} = 0 V		mA	800	1300	1500
V_P	Pinchoff Voltage: V_{DS} = 2.5 V, I_{DS} = 5 mA		V	–5.4	–4.5	–2.0

Note: 1. RF Performance is determined by assembling and testing 10 samples per wafer.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+14 V
Gate-Source Voltage	V_{GS}	–7 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	8.3 W
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	–65°C to +175°C

Thermal Resistance: θ_{jc} = 18°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm Spot Size[4]

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Mounting Surface Temperature = 25°C.
3. Derate at 55.6 mW/°C for $T_{MOUNTING\ SURFACE}$ > 26°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

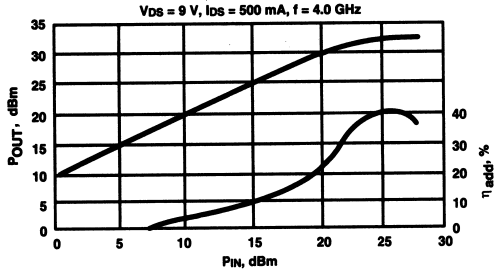
Part Number Ordering Information

Part Number	Devices Per Tray
ATF-44100-GP1	5
ATF-44100-GP3	50
ATF-44100-GP6	up to 300

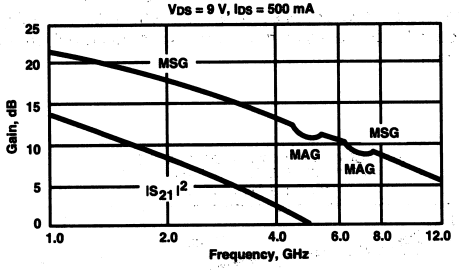
Typical Performance, T_A = 25°C

(unless otherwise noted)

OUTPUT POWER AND POWER ADDED EFFICIENCY vs. INPUT POWER
V_{DS} = 9 V, I_{DS} = 500 mA, f = 4.0 GHz



INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{DS} = 9 V, I_{DS} = 500 mA



Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 9 V, I_{DS} = 500 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
1.0	.88	–117	13.1	4.52	111	–28.0	.040	34	.37	–162
2.0	.89	–149	8.1	2.55	88	–26.0	.050	36	.41	–168
3.0	.89	–163	5.1	1.80	72	–25.4	.054	38	.44	–170
4.0	.90	–172	2.4	1.32	60	–24.7	.058	44	.47	–173
5.0	.91	–179	0.3	1.04	49	–24.3	.061	46	.52	–176
6.0	.92	175	–1.4	.85	39	–23.5	.067	47	.56	–178
7.0	.92	170	–3.2	.69	30	–23.0	.071	49	.60	180
8.0	.93	167	–4.4	.60	24	–22.6	.074	50	.64	176
9.0	.93	162	–5.7	.52	15	–22.2	.078	51	.67	175
10.0	.94	158	–6.7	.46	10	–21.7	.082	52	.70	173
11.0	.95	153	–7.7	.41	3	–21.3	.086	50	.73	172
12.0	.95	145	–9.1	.35	–4	–20.7	.092	49	.76	171

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

ATF-44101 (AT-8140)
2-8 GHz Medium Power
Gallium Arsenide FET

Features

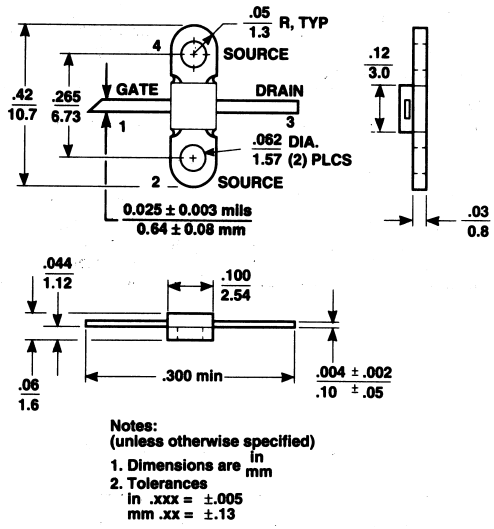
- **High Output Power:**
  32.0 dBm typical $P_{1\,dB}$ at 4 GHz
- **High Gain at 1 dB Compression:**
  9.0 dB typical $G_{1\,dB}$ at 4 GHz
- **High Power Efficiency:**
  36% typical at 4 GHz
- **Hermetic Metal-Ceramic Stripline Package**

Description

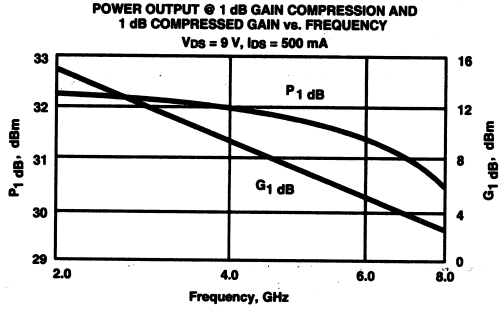
The ATF-44101 is a gallium arsenide Schottky-barrier-gate field effect transistor designed for medium power, linear amplification in the 2 to 8 GHz frequency range. This nominally .5 micron gate length GaAs FET is an interdigitated four-cell structure using airbridge interconnects between source fingers. Total gate periphery is 5 millimeters. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

This device is suitable for applications in space, airborne, military ground and shipboard, and commercial environments. It is supplied in a hermetic high reliability package with low parasitic reactance and minimum thermal resistance.

100 mil Flange



Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
   in .xxx = ±.005
   mm .xx = ±.13



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression:	f = 4.0 GHz	dBm	31.0	32.0	
	V_{DS} = 9 V, I_{DS} = 500 mA	f = 6.0 GHz			31.5	
$G_{1\,dB}$	1 dB Compressed Gain:	f = 4.0 GHz	dB	8.0	9.0	
	V_{DS} = 9 V, I_{DS} = 500 mA	f = 6.0 GHz			5.5	
η_{add}	Efficiency @ $P_{1\,dB}$: V_{DS} = 9 V, I_{DS} = 500 mA	f = 4.0 GHz	%		36	
g_m	Transconductance: V_{DS} = 2.5 V, I_{DS} = 500 mA		mmho		300	
I_{DSS}	Saturated Drain Current: V_{DS} = 1.75 V, V_{GS} = 0 V		mA	800	1300	1500
V_P	Pinchoff Voltage: V_{DS} = 2.5 V, I_{DS} = 5 mA		V	–5.4	–4.0	–2.0

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+14 V
Gate-Source Voltage	V_{GS}	–7 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	6.5 W
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	–65°C to +175°C

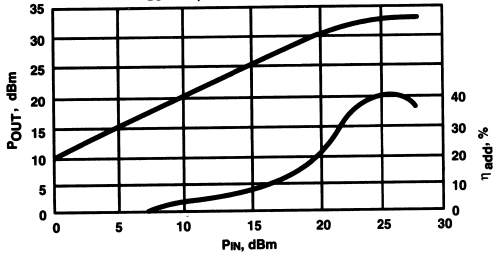
Thermal Resistance: θ_{jc} = 23°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 µm Spot Size[4]

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 43 mW/°C for T_{CASE} > 25°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

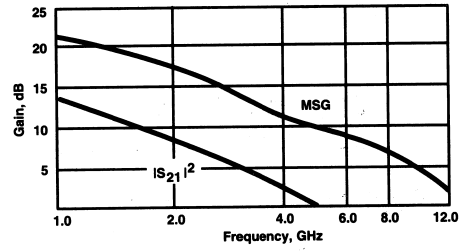
Typical Performance, T_A = 25°C

(unless otherwise noted)

OUTPUT POWER AND POWER ADDED EFFICIENCY vs. INPUT POWER
V_{DS} = 9 V, I_{DS} = 500 mA, f = 4.0 GHz



INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{DS} = 9 V, I_{DS} = 500 mA



Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 9 V, I_{DS} = 500 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
1.0	.88	–125	13.4	4.69	104	–28.2	.039	31	.29	–154
2.0	.87	–161	8.1	2.53	74	–26.7	.046	21	.38	–164
3.0	.87	–178	4.8	1.73	54	–26.7	.046	22	.44	–167
4.0	.87	168	2.5	1.34	35	–25.7	.052	17	.47	–175
5.0	.88	153	0.8	1.10	16	–25.5	.053	13	.49	175
6.0	.88	136	–0.8	.91	–5	–23.6	.066	0	.52	160
7.0	.89	122	–2.5	.75	–25	–23.4	.068	–7	.56	144
8.0	.89	114	–4.2	.62	–39	–22.7	.073	–13	.62	132
9.0	.88	109	–5.5	.53	–52	–22.2	.078	–18	.68	124
10.0	.86	103	–6.7	.46	–64	–20.9	.090	–24	.72	118
11.0	.81	91	–6.9	.45	–78	–19.3	.108	–33	.73	112
12.0	.77	74	–7.5	.42	–95	–17.2	.138	–49	.73	101

A model for this device is available in the DEVICE MODELS section.

ATF-45100 (AT-8151)
2-12 GHz Medium Power Gallium Arsenide FET

Features

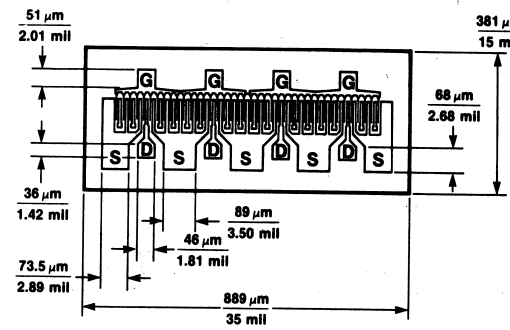
- **High Output Power:**
  29.0 dBm typical $P_{1\,dB}$ at 4 GHz
- **High Gain at 1 dB Compression:**
  11.0 dB typical $G_{1\,dB}$ at 4 GHz
- **High Power Efficiency:**
  38% typical at 4 GHz

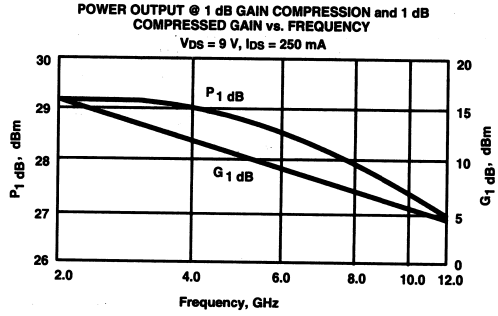
Description

The ATF-45100 is a gallium arsenide Schottky-barrier-gate field effect transistor designed for medium power, linear amplification in the 2 to 12 GHz frequency range. This nominally 0.5 micron gate length GaAs FET is an interdigitated four-cell structure using airbridge interconnects between drain fingers. Total gate periphery is 2.5 millimeters. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device. All metal surfaces are gold plated for ease of bonding and die attach.

The recommended mounting procedure is to die attach temperature of 300° C using a gold-tin preform under forming gas. Assembly should be performed with wedge bonding using either 0.7 mil of 1.0 mil gold wire. See also "Chip Use" in the APPLICATIONS section.

Chip Outline





Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 9 V, I_{DS} = 250 mA	f = 4.0 GHz f = 8.0 GHz f = 12.0 GHz	dBm	28.0	29.0 28.0 27.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 9 V, I_{DS} = 250 mA	f = 4.0 GHz f = 8.0 GHz f = 12.0 GHz	dB	10.0	11.0 6.5 4.5	
η_{add}	Efficiency @ $P_{1\,dB}$: V_{DS} = 9 V, I_{DS} = 250 mA	f = 4.0 GHz	%		38	
g_m	Transconductance: V_{DS} = 2.5 V, I_{DS} = 250 mA		mmho		200	
I_{DSS}	Saturated Drain Current: V_{DS} = 1.75 V, V_{GS} = 0 V		mA	400	600	800
V_P	Pinchoff Voltage: V_{DS} = 2.5 V, I_{DS} = 5 mA		V	–5.4	–4.0	–2.0

Note: 1. RF Performance is determined by packaging and testing 10 samples per wafer.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+14 V
Gate-Source Voltage	V_{GS}	–7 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	4.0 W
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	–65°C to +175°C

Thermal Resistance: θ_{jc} = 38°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 µm Spot Size[4]

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Mounting Surface Temperature = 25°C.
3. Derate at 26 mW/°C for $T_{MOUNTING\ SURFACE}$ > 23°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

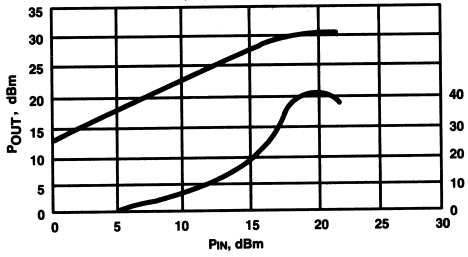
Part Number Ordering Information

Part Number	Devices Per Tray
ATF-45100-GP1	5
ATF-45100-GP3	50
ATF-45100-GP6	up to 300

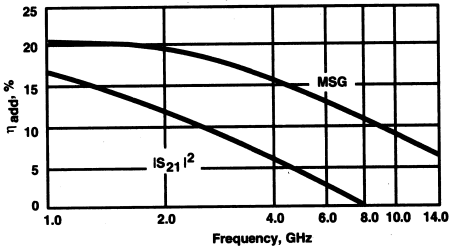
Typical Performance, T_A = 25°C

(unless otherwise noted)

OUTPUT POWER AND POWER ADDED EFFICIENCY vs. INPUT POWER
V_{DS} = 9 V, I_{DS} = 250 mA, f = 4.0 GHz



INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{DS} = 9 V, I_{DS} = 250 mA



Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 9 V, I_{DS} = 250 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
1.0	.92	–88	16.1	6.41	124	–27.3	.043	36	.32	–45
2.0	.85	–127	12.1	4.01	96	–26.0	.050	38	.29	–68
3.0	.84	–147	9.3	2.93	78	–25.4	.054	40	.29	–87
4.0	.85	–159	6.8	2.19	64	–24.9	.057	43	.31	–102
5.0	.87	–169	4.8	1.74	51	–24.3	.061	48	.37	–118
6.0	.88	–177	3.1	1.43	38	–23.9	.064	53	.43	–130
7.0	.88	177	1.3	1.17	27	–23.5	.067	57	.50	–139
8.0	.89	173	0.0	1.00	19	–22.4	.076	60	.57	–149
9.0	.90	167	–1.3	.86	8	–21.7	.082	63	.63	–157
10.0	.90	162	–2.6	.74	1	–21.2	.087	60	.68	–162
11.0	.91	157	–4.0	.63	–9	–20.4	.096	57	.72	–169
12.0	.91	148	–5.4	.54	–18	–19.9	.101	54	.75	–171
13.0	.90	145	–6.0	.50	–25	–19.6	.105	48	.79	–175
14.0	.90	135	–6.9	.45	–35	–19.7	.104	41	.82	–179

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

ATF-45101 (AT-8150)
2-8 GHz Medium Power Gallium Arsenide FET

Features

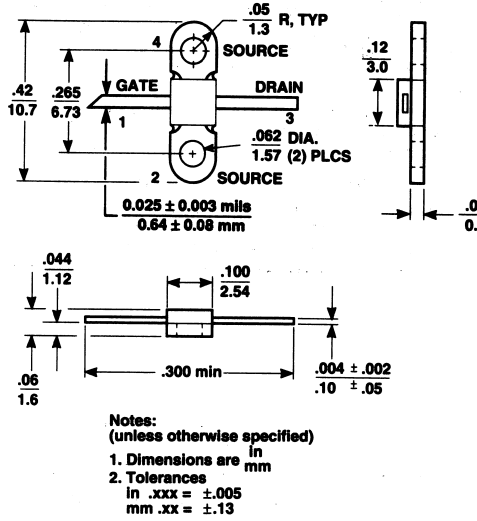
- **High Output Power:**
  29.0 dBm typical $P_{1\,dB}$ at 4 GHz
- **High Gain at 1 dB Compression:**
  10.0 dB typical $G_{1\,dB}$ at 4 GHz
- **High Power Efficiency:**
  38% typical at 4 GHz
- **Hermetic Metal-Ceramic Stripline Package**

Description

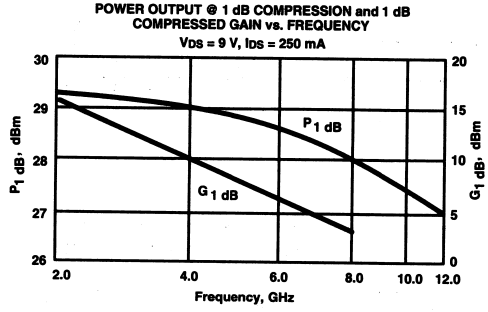
The ATF-45101 is a gallium arsenide Schottky-barrier-gate field effect transistor designed for medium power, linear amplification in the 2 to 8 GHz frequency range. This nominally 0.5 micron gate length GaAs FET is an interdigitated four-cell structure using airbridge interconnects between drain fingers. Total gate periphery is 2.5 millimeters. Proven gold based metalization systems and nitride passivation assure a rugged, reliable device.

This device is suitable for applications in space, airborne, military ground and shipboard, and commercial environments. It is supplied in a hermetic high reliability package with low parasitic reactance and minimum thermal resistance.

100 mil Flange Package



Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
   in .xxx = ±.005
   mm .xx = ±.13



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 9 V, I_{DS} = 250 mA	f = 4.0 GHz f = 8.0 GHz	dBm	28.0	29.0 28.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 9 V, I_{DS} = 250 mA	f = 4.0 GHz f = 8.0 GHz	dB	9.0	10.0 4.0	
η_{add}	Efficiency @ $P_{1\,dB}$: V_{DS} = 9 V, I_{DS} = 250 mA	f = 4.0 GHz	%		38	
g_m	Transconductance: V_{DS} = 2.5 V, I_{DS} = 250 mA		mmho		200	
I_{DSS}	Saturated Drain Current: V_{DS} = 1.75 V, V_{GS} = 0 V		mA	400	600	800
V_P	Pinchoff Voltage: V_{DS} = 2.5 V, I_{DS} = 5 mA		V	–5.4	–4.0	–2.0

Absolute Maximum Ratings

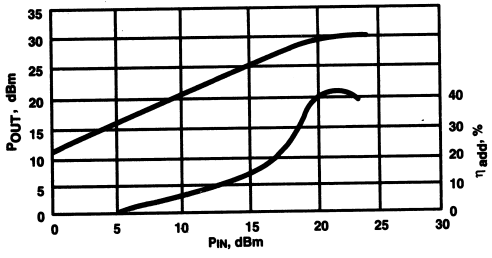
Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+14 V
Gate-Source Voltage	V_{GS}	–7 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	3.6 W
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	–65°C to +175°C

Thermal Resistance: θ_{jc} = 42°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm Spot Size[4]

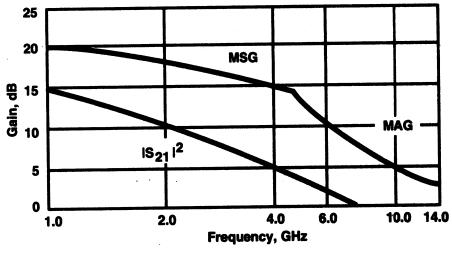
Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 24 mW/°C for T_{CASE} > 24°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Typical Performance, T_A = 25°C
(unless otherwise noted)

OUTPUT POWER AND POWER ADDED EFFICIENCY vs. INPUT POWER
V_{DS} = 9 V, I_{DS} = 250 mA, f = 4.0 GHz



INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{DS} = 9 V, I_{DS} = 250 mA



Typical Scattering Parameters: Common Source, Z_O = 50 Ω
T_A = 25°C, V_{DS} = 9 V, I_{DS} = 125 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
1.0	.89	–88	14.9	5.54	119	–26.2	.049	43	.31	–63
2.0	.83	–135	10.8	3.48	82	–26.0	.050	18	.33	–108
3.0	.81	–158	7.6	2.40	58	–25.8	.051	7	.39	–129
4.0	.84	–174	5.4	1.86	38	–25.5	.053	3	.46	–144
5.0	.82	170	3.8	1.55	18	–25.2	.055	–2	.50	–154
6.0	.81	152	2.6	1.36	–2	–24.4	.060	–8	.52	–168
7.0	.81	133	1.2	1.15	–25	–23.9	.064	–15	.55	173
8.0	.81	122	–0.3	.97	–42	–23.5	.067	–20	.59	154
9.0	.80	113	–1.8	.81	–60	–22.6	.074	–31	.64	137
10.0	.79	107	–3.2	.69	–73	–22.0	.079	–40	.68	123
11.0	.77	94	–4.6	.59	–91	–21.5	.084	–45	.72	113
12.0	.73	82	–5.8	.51	–106	–20.3	.097	–55	.76	99
13.0	.68	69	–6.7	.46	–123	–18.3	.121	–63	.78	89
14.0	.64	56	–7.1	.44	–137	–15.9	.161	–79	.80	79

A model for this device is available in the DEVICE MODELS section.

ATF-45171 (AT-11571)
2-8 GHz Medium Power Gallium Arsenide FET

Features

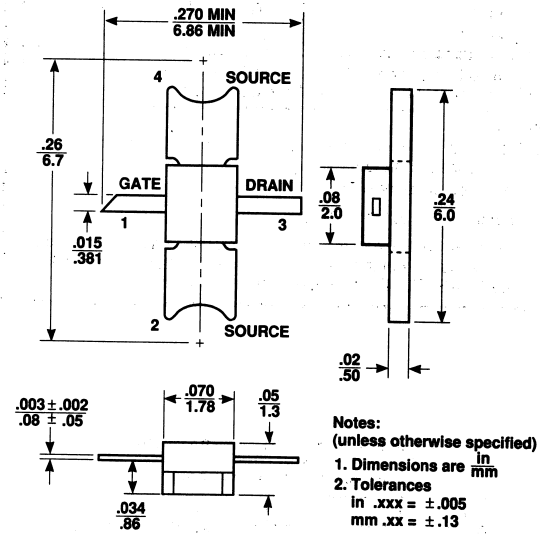
- **High Output Power: 29.0 dBm typical $P_{1\,dB}$ at 4 GHz**
- **High Gain at 1 dB Compression: 10.5 dB typical $G_{1\,dB}$ at 4 GHz**
- **High Power Efficiency: 38% typical at 4 GHz**
- **Hermetic Metal-Ceramic Stripline Package**

Description

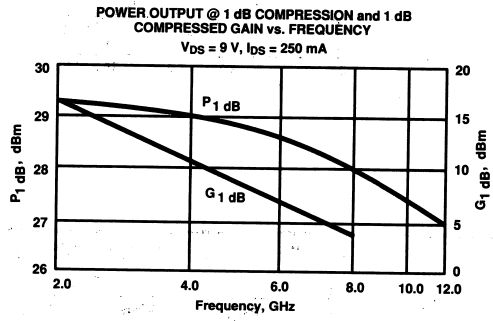
The ATF-45171 is a gallium arsenide Schottky-barrier-gate field effect transistor designed for medium power, linear amplification in the 2 to 8 GHz frequency range. This nominally 0.5 micron gate length GaAs FET is an interdigitated four-cell structure using airbridge interconnects between drain fingers. Total gate periphery is 2.5 millimeters. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

This device is suitable for applications in space, airborne, military ground and shipboard, and commercial environments. It is supplied in a hermetic high reliability package with low parasitic reactance and minimum thermal resistance.

70 mil Flange Package



Notes:
(unless otherwise specified)
1. Dimensions are $\frac{in}{mm}$
2. Tolerances
   in .xxx = ±.005
   mm .xx = ±.13



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 9 V, I_{DS} = 250 mA	f = 4.0 GHz f = 8.0 GHz	dBm	28.0	29.0 28.0	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 9 V, I_{DS} = 250 mA	f = 4.0 GHz f = 8.0 GHz	dB	9.5	10.5 4.5	
η_{add}	Efficiency @ $P_{1\,dB}$: V_{DS} = 9 V, I_{DS} = 250 mA	f = 4.0 GHz	%		38	
g_m	Transconductance: V_{DS} = 2.5 V, I_{DS} = 250 mA		mmho		200	
I_{DSS}	Saturated Drain Current: V_{DS} = 1.75 V, V_{GS} = 0 V		mA	400	600	800
V_P	Pinchoff Voltage: V_{DS} = 2.5 V, I_{DS} = 5 mA		V	–5.4	–4.0	–2.0

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+14 V
Gate-Source Voltage	V_{GS}	–7 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	3.6 W
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	–65°C to +175°C

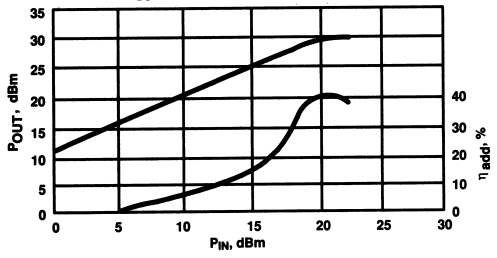
Thermal Resistance: θ_{jc} = 42°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm Spot Size[4]

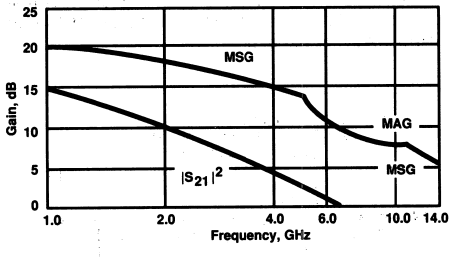
Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 24 mW/°C for T_{CASE} > 24°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)





Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 9 V, I_{DS} = 250 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
1.0	.91	–83	14.5	5.30	122	–26.7	.046	46	.37	–46
2.0	.83	–137	10.8	3.45	83	–26.4	.048	19	.26	–91
3.0	.83	–167	7.4	2.34	54	–26.0	.050	5	.31	–131
4.0	.86	174	4.4	1.66	32	–25.5	.053	2	.43	–155
5.0	.86	162	2.1	1.28	12	–25.1	.055	0	.52	–167
6.0	.85	152	0.7	1.09	–3	–24.7	.058	–2	.56	–176
7.0	.84	138	0.1	1.01	–22	–24.4	.060	–6	.59	173
8.0	.84	124	–0.9	.90	–40	–23.8	.064	–13	.62	154
9.0	.85	114	–2.5	.75	–59	–23.4	.068	–19	.66	135
10.0	.85	106	–4.3	.61	–70	–22.5	.075	–25	.71	123
11.0	.85	100	–5.2	.55	–81	–21.6	.083	–30	.76	119
12.0	.83	95	–6.2	.49	–90	–20.8	.091	–39	.79	111
13.0	.80	76	–6.7	.46	–107	–19.3	.109	–50	.81	98
14.0	.77	59	–8.0	.40	–125	–18.9	.113	–61	.83	78

A model for this device is available in the DEVICE MODELS section.

ATF-46100 (AT-8161)
2-14 GHz Medium Power Gallium Arsenide FET

Features

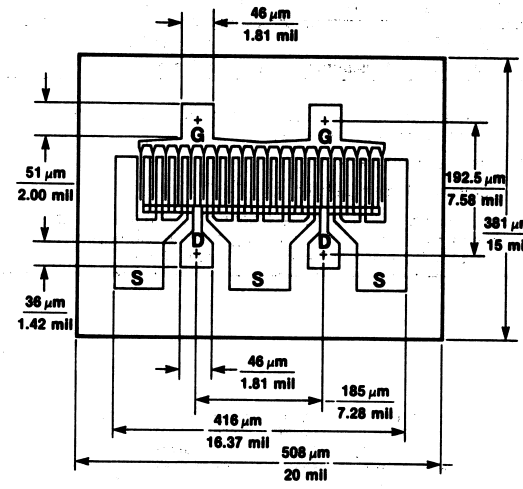
- **High Output Power:**
  27.0 dBm typical $P_{1\,dB}$ at 4 GHz
- **High Gain at 1 dB Compression:**
  12.0 dB typical $G_{1\,dB}$ at 4 GHz
- **High Power Efficiency:**
  38% typical at 4 GHz

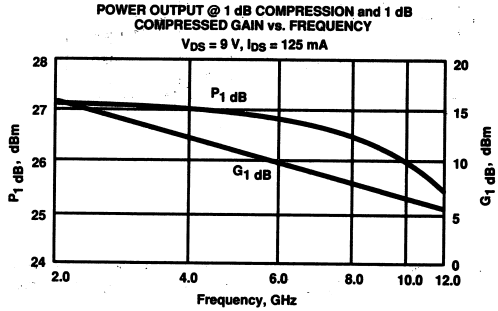
Description

The ATF-46100 is a gallium arsenide Schottky-barrier-gate field effect transistor designed for medium power, linear amplification in the 2 to 14 GHz frequency range. This nominally 0.5 micron gate length GaAs FET is an interdigitated four-cell structure using airbridge interconnects between drain fingers. Total gate periphery is 1.25 millimeters. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device. All metal surfaces are gold plated for ease of bonding and die attach.

The recommended mounting procedure is to die attach temperature of 300°C using a gold-tin preform under forming gas. Assembly should be performed with wedge bonding using either 0.7 mil of 1.0 mil gold wire. See also "Chip Use" in the APPLICATIONS section.

Chip Outline





Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions[1]		Units	Min.	Typ.	Max.
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 9 V, I_{DS} = 125 mA	f = 4.0 GHz f = 8.0 GHz f = 12.0 GHz	dBm	26.0	27.0 26.5 25.5	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 9 V, I_{DS} = 125 mA	f = 4.0 GHz f = 8.0 GHz f = 12.0 GHz	dB	11.0	12.0 8.0 6.0	
η_{add}	Efficiency @ $P_{1\,dB}$: V_{DS} = 9 V, I_{DS} = 125 mA	f = 4.0 GHz	%		38	
g_m	Transconductance: V_{DS} = 2.5 V, I_{DS} = 125 mA		mmho		100	
I_{DSS}	Saturated Drain Current: V_{DS} = 2.5 V, V_{GS} = 0 V		mA	200	330	450
V_P	Pinchoff Voltage: V_{DS} = 2.5 V, I_{DS} = 5 mA		V	–5.4	–3.5	–2.0

Note 1: RF Performance is determined by packaging and testing 10 samples per wafer.

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+14 V
Gate-Source Voltage	V_{GS}	–7 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	2.2 W
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	–65°C to +175°C

Thermal Resistance: θ_{jc} = 70°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm Spot Size[4]

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Mounting Surface Temperature = 25°C.
3. Derate at 14.3 mW/°C for $T_{MOUNTING\ SURFACE}$ > 21°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

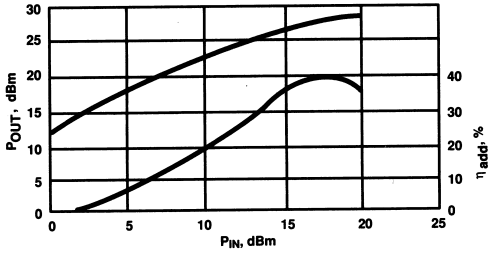
Part Number Ordering Information

Part Number	Devices Per Tray
ATF-46100-GP1	5
ATF-46100-GP3	50
ATF-46100-GP5	up to 300

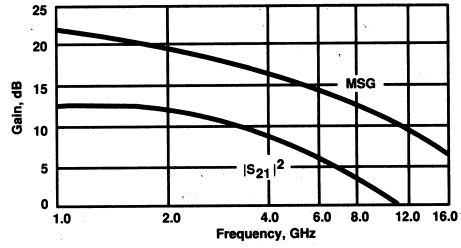
Typical Performance, T_A = 25°C

(unless otherwise noted)

OUTPUT POWER AND POWER ADDED EFFICIENCY vs. INPUT POWER
V_{DS} = 9 V, I_{DS} = 125 mA, f = 4.0 GHz



INSERTION POWER GAIN, MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN vs. FREQUENCY
V_{DS} = 9 V, I_{DS} = 125 mA



Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 9 V, I_{DS} = 125 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
1.0	.97	–44	13.0	4.48	148	–30.8	.029	70	.60	–15
2.0	.89	–80	11.3	3.69	121	–27.1	.044	70	.56	–26
3.0	.84	–106	9.9	3.13	101	–25.5	.053	69	.51	–36
4.0	.81	–129	8.3	2.59	83	–24.4	.060	68	.47	–45
5.0	.81	–147	6.8	2.20	67	–23.9	.064	66	.45	–59
6.0	.82	–161	5.6	1.90	53	–23.5	.067	64	.42	–74
7.0	.83	–172	4.2	1.63	40	–22.9	.072	62	.42	–89
8.0	.84	180	3.3	1.46	29	–22.0	.079	60	.45	–105
9.0	.85	171	2.3	1.31	16	–20.8	.091	58	.49	–125
10.0	.86	163	1.0	1.12	4	–19.8	.102	56	.55	–139
11.0	.88	156	0.3	1.03	–7	–18.9	.113	54	.61	–154
12.0	.89	149	–1.0	.89	–18	–18.5	.119	51	.66	–162
13.0	.90	142	–2.0	.79	–26	–17.7	.130	42	.72	–172
14.0	.91	135	–3.2	.69	–38	–17.4	.135	39	.76	180
15.0	.92	130	–4.3	.61	–45	–16.9	.143	33	.79	175
16.0	.93	126	–5.4	.54	–51	–16.4	.151	24	.82	167

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

ATF-46101 (AT-8160)
2-10 GHz Medium Power Gallium Arsenide FET

Features

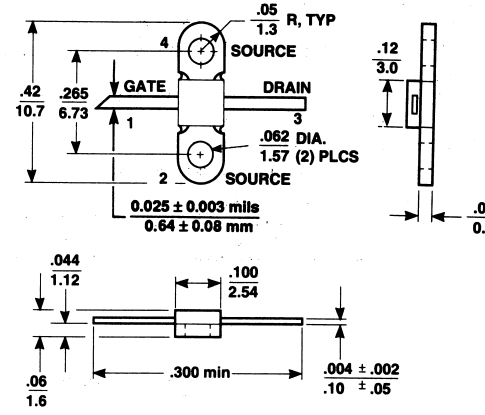
- **High Output Power: 27.0 dBm typical $P_{1\,dB}$ at 4 GHz**
- **High Gain at 1 dB Compression: 10.0 dB typical $G_{1\,dB}$ at 4 GHz**
- **High Power Efficiency: 38% typical at 4 GHz**
- **Hermetic Metal-Ceramic Stripline Package**

Description

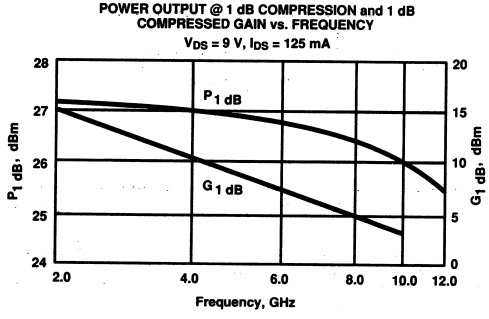
The ATF-46101 is a gallium arsenide Schottky-barrier-gate field effect transistor designed for medium power, linear amplification in the 2 to 10 GHz frequency range. This nominally 0.5 micron gate length GaAs FET is an interdigitated four-cell structure using airbridge interconnects between drain fingers. Total gate periphery is 1.25 millimeters. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

This device is suitable for applications in space, airborne, military ground and shipboard, and commercial environments. It is supplied in a hermetic high reliability package with low parasitic reactance and minimum thermal resistance.

100 mil Flange Package



Notes:
(unless otherwise specified)
1. Dimensions are in mm
2. Tolerances
   in .xxx = ±.005
   mm .xx = ±.13



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 9 V, I_{DS} = 125 mA	f = 4.0 GHz f = 8.0 GHz	dBm	26.0	27.0 26.5	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 9 V, I_{DS} = 125 mA	f = 4.0 GHz f = 8.0 GHz	dB	9.0	10.0 5.0	
η_{add}	Efficiency @ $P_{1\,dB}$: V_{DS} = 9 V, I_{DS} = 125 mA	f = 4.0 GHz	%		38	
g_m	Transconductance: V_{DS} = 2.5 V, I_{DS} = 125 mA		mmho		100	
I_{DSS}	Saturated Drain Current: V_{DS} = 2.5 V, V_{GS} = 0 V		mA	200	330	450
V_P	Pinchoff Voltage: V_{DS} = 2.5 V, I_{DS} = 5 mA		V	–5.4	–3.5	–2.0

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+14 V
Gate-Source Voltage	V_{GS}	–7 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	2.0 W
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	–65°C to +175°C

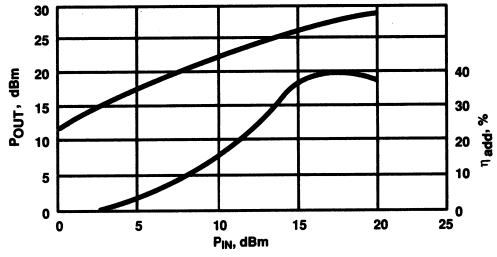
Thermal Resistance: θ_{jc} = 75°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm Spot Size[4]

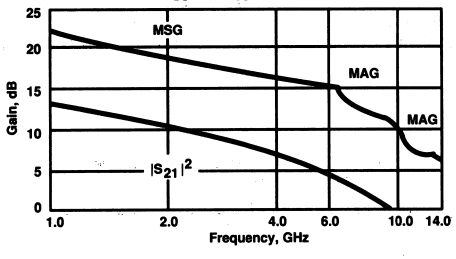
Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 13 mW/°C for T_{CASE} > 25°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)





Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 9 V, I_{DS} = 125 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
1.0	.94	–56	12.8	4.37	135	–31.4	.027	52	.64	–28
2.0	.86	–101	10.7	3.41	98	–27.3	.043	30	.59	–56
3.0	.82	–131	8.4	2.64	71	–26.9	.045	18	.58	–79
4.0	.82	–152	6.7	2.16	48	–26.4	.048	9	.62	–98
5.0	.80	–173	5.4	1.86	26	–26.0	.050	–1	.63	–112
6.0	.79	165	4.3	1.64	5	–25.8	.051	–12	.65	–126
7.0	.78	143	3.1	1.43	–18	–25.4	.054	–24	.65	–145
8.0	.78	131	1.6	1.20	–36	–24.7	.058	–37	.70	–166
9.0	.77	123	0.3	1.03	–55	–23.9	.064	–40	.73	173
10.0	.76	118	–1.2	.87	–72	–23.1	.070	–52	.76	158
11.0	.67	104	–2.0	.79	–91	–22.6	.074	–57	.79	146
12.0	.60	86	–2.7	.73	–110	–21.2	.087	–66	.83	136
13.0	.54	71	–3.5	.67	–133	–19.7	.104	–79	.87	124
14.0	.50	64	–4.0	.63	–154	–15.9	.160	–99	.92	115

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

ATF-46171 (AT-11671)
2-10 GHz Medium Power Gallium Arsenide FET

Features

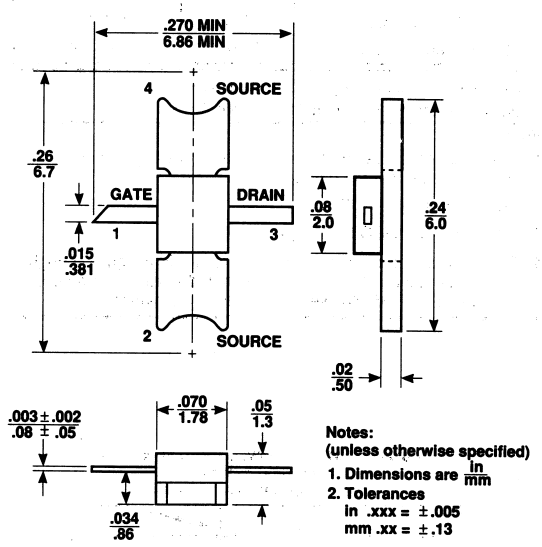
- **High Output Power: 27.0 dBm typical $P_{1\,dB}$ at 4 GHz**
- **High Gain at 1 dB Compression: 11.0 dB typical $G_{1\,dB}$ at 4 GHz**
- **High Power Efficiency: 38% typical at 4 GHz**
- **Hermetic Metal-Ceramic Stripline Package**

Description

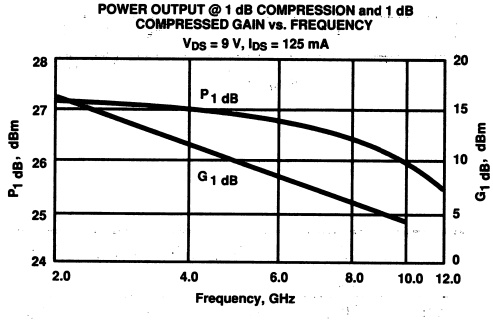
The ATF-46171 is a gallium arsenide Schottky-barrier-gate field effect transistor designed for medium power, linear amplification in the 2 to 10 GHz frequency range. This nominally 0.5 micron gate length GaAs FET is an interdigitated four-cell structure using airbridge interconnects between drain fingers. Total gate periphery is 1.25 millimeters. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

This device is suitable for applications in space, airborne, military ground and shipboard, and commercial environments. It is supplied in a hermetic high reliability package with low parasitic reactance and minimum thermal resistance.

70 mil Flange Package



Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
   in .xxx = ±.005
   mm .xx = ±.13



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression: V_{DS} = 9 V, I_{DS} = 125 mA	f = 4.0 GHz f = 8.0 GHz	dBm	26.0	27.0 26.5	
$G_{1\,dB}$	1 dB Compressed Gain: V_{DS} = 9 V, I_{DS} = 125 mA	f = 4.0 GHz f = 8.0 GHz	dB	10.0	11.0 6.0	
η_{add}	Efficiency @ $P_{1\,dB}$: V_{DS} = 9 V, I_{DS} = 125 mA	f = 4.0 GHz	%		38	
g_m	Transconductance: V_{DS} = 2.5 V, I_{DS} = 125 mA		mmho		100	
I_{DSS}	Saturated Drain Current: V_{DS} = 2.5 V, V_{GS} = 0 V		mA	200	330	450
V_P	Pinchoff Voltage: V_{DS} = 2.5 V, I_{DS} = 5 mA		V	–5.4	–3.5	–2.0

Absolute Maximum Ratings

Parameter	Symbol	Absolute Maximum[1]
Drain-Source Voltage	V_{DS}	+14 V
Gate-Source Voltage	V_{GS}	–7 V
Drain Current	I_{DS}	I_{DSS}
Power Dissipation[2,3]	P_T	2.0 W
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	–65°C to +175°C

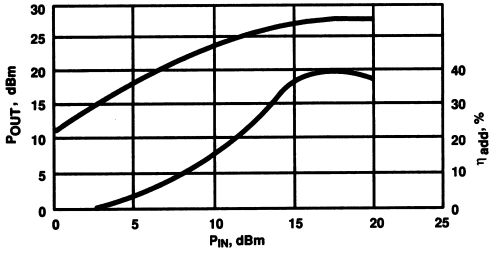
Thermal Resistance: θ_{jc} = 75°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm Spot Size[4]

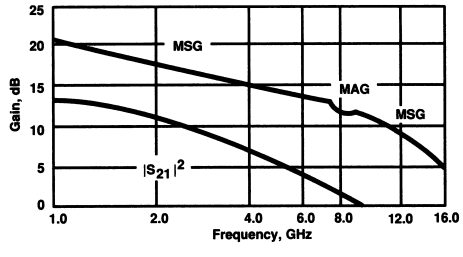
Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Case Temperature = 25°C.
3. Derate at 13 mW/°C for T_{CASE} > 25°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)





Typical Scattering Parameters: Common Source, Z_O = 50 Ω

T_A = 25°C, V_{DS} = 9 V, I_{DS} = 125 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
1.0	.95	–54	12.7	4.30	138	–29.4	.034	63	.71	–22
2.0	.84	–106	11.0	3.56	99	–26.7	.046	30	.60	–44
3.0	.81	–145	8.9	2.80	67	–25.7	.052	13	.52	–71
4.0	.81	–172	6.6	2.14	40	–25.0	.056	2	.52	–101
5.0	.80	171	4.6	1.70	18	–24.4	.060	–3	.58	–122
6.0	.79	159	3.1	1.44	1	–24.0	.063	–6	.63	–135
7.0	.78	141	2.2	1.29	–18	–23.5	.067	–10	.63	–147
8.0	.77	123	1.4	1.17	–36	–23.0	.071	–14	.64	–164
9.0	.79	108	–0.1	.99	–58	–22.5	.075	–17	.67	171
10.0	.79	100	–1.4	.85	–73	–22.0	.079	–21	.74	152
11.0	.78	93	–2.5	.75	–86	–21.6	.083	–24	.76	142
12.0	.76	85	–3.5	.67	–97	–20.6	.093	–32	.79	133
13.0	.73	67	–4.3	.61	–118	–19.5	.106	–49	.80	119
14.0	.71	47	–5.8	.51	–138	–19.0	.112	–66	.83	98
15.0	.73	35	–7.5	.42	–157	–18.6	.118	–71	.85	83
16.0	.75	26	–8.9	.36	–157	–18.3	.121	–78	.90	72

A model for this device is available in the DEVICE MODELS section.

Silicon IC Amplifiers, Mixers and Modulators, Prescalers



Silicon Bipolar RF and Microwave Integrated Circuits

Hewlett-Packard's state-of-the-art microwave bipolar technology is the basis for a broad line of RF and microwave integrated circuits. Complexity ranges from very simple MSA series of two-transistor Darlington gain blocks to multi-transistor function blocks such as the HPMX series of vector modulators. These devices are designed to work optimally in the 100 MHz to 3 GHz frequency range, although operation to much lower frequencies is possible, and individual offerings have excellent performance at frequencies as high as 5 GHz.

Processes

A number of processes are used to manufacture these devices.

SAT process: Hewlett-Packard's state-of-the-art 10 GHz f_T 25 GHz f_{MAX} bipolar process is also used to manufacture the AT line of discrete bipolar transistors. Diffused resistors are added to this joined-backside-collector process to allow the creation of simple ICs such as the MSA Darlington gain blocks.

ISOSAT process: Trench isolation is coupled with the SAT transistor engine to create a process optimized for high speed analog integrated circuits. Material and processing enhancements raise the nominal f_T of this process to above 15 GHz. Design flexibility is enhanced through the addition of second metal capability, and by the availability of such on-chip elements such as capacitors, diodes, and high valued resistors. This process also utilizes polyimide as an inter-metal dielectric and scratch protection.

HP-10 and HP-25: These processes result from enhancements to Hewlett-Packard's high speed digital silicon processes, to make them suitable for microwave applications. The HP-10 has a nominal f_T of 10 GHz while the HP-25 has a nominal f_T of 25 GHz.

Product Families

The MSA families are Darlington feedback 50 Ω gain blocks. These simple ICs provide the designer with a wide selection of easy to use broad-band, general purpose amplifiers suitable for many different RF and IF applications. Members of the family are differentiated by output power, noise figure, bias requirements, and speciality performance features such as bandwidth or dynamic range.

The MSF family of frequency converters provide one of the simplest receiver architectures available. The addition of parallel feedback to these devices will create a self-oscillating unbalanced mixer from a simple gain block. These devices are most suitable for down-conversion applications where the IF is well spaced from the LO and RF frequencies, and noise performance is not critical.

The INA family adds a low noise input stage to a Darlington output stage to create high gain, low noise matched amplifiers. Like the MSAs, this product family is broad-band, general-purpose in nature, and provides a simple solution to many IF and less critical LNA applications. With 25 dB gain at 8 mA, the INA-03184 is also the most current-efficient gain block in the silicon MMIC families.

The IAM family are Gilbert cell multiplier-based frequency converters. This structure works well as an active mixer in functions requiring load insensitive conversion gain, good spurious signal suppression, low LO power and moderate dynamic range. Applications include frequency down-conversion, up-conversion, modulation, demodulation, and phase detection, where the RF and LO frequencies can be up to 5 GHz and the IF (output) frequency can be up to 2 GHz.

The HPMX family are vector modulators. The "heart" of the transmit chain in a digital radio, these devices provide the means by which the in-phase (I) and quadrature (Q) data streams are combined and up-converted to the broadcast frequency. The basic product consists of two Gilbert cell multipliers and a summing amplifier on a single chip. Variants allow for dual conversion operation by adding a second mixer, or specialize the frequency of operation by adding on-chip 90 degree phase shifters.

Silicon Monolithic Integrated Circuits

General Purpose Amplifiers (Typical Specifications at +25°C Case Temperature.)

Part Number	GP @ 0.1 GHz (dB)	GP @ 1 GHz (dB)	NF @ 1 GHz (dB)	P_{1dB} (dBm)	Min. Supply Voltage[a] (V_{CC})	Device Voltage[a] (V_d)	Device Current[a] (mA)	Package	Page
MSA-0100	19.0	17.0	6.0	+1.5	7	5.0	17	chip	8-70
MSA-0200	12.5	12.0	6.5	+4.5	7	5.0	25	chip	8-82
MSA-0300	12.5	12.0	6.0	+10.0	7	5.0	35	chip	8-94
MSA-0170	19.0	16.5	6.0	+1.5	7	5.0	17	70 mil stripline	8-76
MSA-0270	12.5	12.0	6.5	+4.5	7	5.0	25	70 mil stripline	8-88
MSA-0370	12.5	12.0	6.0	+10.0	7	5.0	35	70 mil stripline	8-102
MSA-0135	19.0	16.5	6.0	+1.5	7	5.0	17	micro-X ceramic SM	8-74
MSA-0136	19.0	16.5	6.0	+1.5	7	5.0	17	trim lead micro-X SM	8-74
MSA-0235	12.5	12.0	6.5	+4.5	7	5.0	25	micro-X ceramic SM	8-86
MSA-0236	12.5	12.0	6.5	+4.5	7	5.0	25	trim lead micro-X SM	8-86
MSA-0335	12.5	12.0	6.0	+10.0	7	5.0	35	micro-X ceramic SM	8-100
MSA-0336	12.5	12.0	6.0	+10.0	7	5.0	35	trim lead micro-X SM	8-100
MSA-0104	18.5	15.0	6.0	+1.5	7	5.0	17	145 mil plastic	8-72
MSA-0185	18.5	15.0	6.0	+1.5	7	5.0	17	85 mil plastic	8-78
MSA-0204	12.5	11.0	6.5	+4.5	7	5.0	25	145 mil plastic	8-84
MSA-0285	12.5	12.0	6.5	+4.5	7	5.0	25	85 mil plastic	8-90
MSA-0304	12.5	11.0	6.0	+10.0	7	5.0	35	145 mil plastic	8-96
MSA-0385	12.5	12.0	6.0	+10.0	7	5.0	35	85 mil plastic	8-104
MSA-0186	18.5	15.0	6.0	+1.5	7	5.0	17	85 mil plastic	8-80
MSA-0286	12.5	12.0	6.5	+4.5	7	5.0	25	85 mil plastic	8-92
MSA-0311	11.5	11.0	6.0	+9.0	7	4.7	35	SOT-143 SM plastic	8-98
MSA-0386	12.5	12.0	6.0	+10.0	7	5.0	35	85 mil plastic	8-106
MSA-2011	18.5	16.5	5.0	+9.0	7	4.9	32	SOT-143 SM Plastic	8-189
MSA-2111	22.0	16.5	3.3	+10.0	5	3.6	29	SOT-143 SM plastic	8-195
MSA-3111	25.0	18.5	4.3	+9.0	7	5.0	29	SOT-143 SM Plastic	8-197

Low Noise Amplifers (Typical Specifications at +25°C Case Temperature.)

Part Number	G_P @ 0.1 GHz (dB)	G_P @ 1 GHz (dB)	NF @ 1 GHz (dB)	P_{1dB} (dBm)	Min. Supply Voltage[a] (V_{CC})	Device Voltage[a] (V_d)	Device Current[a] (mA)	Package	Page
INA-01100	32.5	24.0	1.7[b]	+10.0	5.5	5.5	35	chip	8-50
INA-02100	32.5	29.0	2.0[c]	+10.0	5.5	5.5	35	chip	8-54
INA-03100	31.5	26.0	2.3	+2.0	N/A	4.5	12	chip	8-62
MSA-0600	20.5	17.5	3.0	+1.5	5	3.5	16	chip	8-132
MSA-0700	13.5	13.0	4.5	+5.5	5	4.0	22	chip	8-144
MSA-0800	32.5	24.0	3.0	+12.5	10	7.8	36	chip	8-156
INA-01170	32.5	24.0	1.7[b]	+10.0	5.5	5.5	35	70 mil stripline	8-52
INA-02170	31.5	29.0	2.0[c]	+10.0	5.5	5.5	35	70 mil stripline	8-56
INA-03170	26.0	26.0	2.3	+2.0	4.5	4.5	12	70 mil stripline	8-64
MSA-0670	20.5	17.5	3.0	+1.5	5	3.5	16	70 mil stripline	8-138
MSA-0770	13.5	13.0	4.5	+5.5	5	4.0	22	70 mil stripline	8-150
MSA-0870	32.5	23.5	3.0	+12.5	10	7.8	36	70 mil stripline	8-160
MSA-0635	20.0	16.5	3.0	+1.5	5	3.5	15	micro-X ceramic SM	8-136
MSA-0636	20.0	16.5	3.0	+1.5	5	3.5	15	trim lead micro-X SM	8-136
MSA-0735	13.5	13.0	4.5	+5.5	5	4.0	22	micro-X ceramic SM	8-148
MSA-0736	13.5	13.0	4.5	+5.5	5	4.0	22	trim lead micro-X SM	8-148
MSA-0835	32.5	23.0	3.0	+12.5	10	7.8	36	micro-X ceramic SM	8-158
MSA-0836	32.5	23.0	3.0	+12.5	10	7.8	36	trim lead micro-X SM	8-158
INA-02184	32.0	28.5	2.0[c]	+11.0	5.5	5.5	35	85 mil plastic	8-58
INA-03184	25.5	25.0	2.6	-2.0	4.0	4.0	10	85 mil plastic	8-66
MSA-0685	20.0	16.5	3.2	+1.5	5	3.5	16	85 mil plastic	8-140
MSA-0785	13.5	12.5	5.0	+5.5	5	4.0	22	85 mil plastic	8-152
MSA-0885	32.5	22.5	3.3	+12.5	10	7.8	36	85 mil plastic	8-162

Silicon Monolithic Integrated Circuits (cont.)

Low Noise Amplifers (Typical Specifications at +25°C Case Temperature.) (cont.)

Part Number	G_P @ 0.1 GHz (dB)	G_P @ 1 GHz (dB)	NF @ 1 GHz (dB)	P_{1dB} (dBm)	Min. Supply Voltage[a] (V_{CC})	Device Voltage[a] (V_d)	Device Current[a] (mA)	Package	Page
INA-02186	31.5	28.5	2.0[c]	+11.0	5.5	5.5	35	85 mil SM plastic	8-58
INA-10386	25.0	25.0	3.7[d]	+11.0	6.0	6.0	50	85 mil SM plastic	8-68
MSA-0611	19.5	15.0	3.2	+2.0	5	3.3	16	SOT-143 SM plastic	8-134
MSA-0686	20.0	16.5	3.2	+1.0	5	3.5	16	85 mil SM plastic	8-142
MSA-0711	13.0	12.0	5.0	+5.5	5	3.8	22	SOT-143 SM plastic	8-146
MSA-0786	13.5	12.5	5.0	+5.5	5	4.0	22	85 mil SM plastic	8-154
MSA-0886	32.5	22.5	3.3	+12.5	10	7.8	36	85 mil SM plastic	8-164

Notes:
[a] Refer to schematic drawing on individual data sheet.
[b] Noise Figure at 0.1 GHz.
[c.] Noise Figure at 0.5 GHz.
[d.] Noise Figure at 0.5 GHz.

Medium Power Amplifiers (Typical Specifications at +25°C Case Temperature)

Part Number	G_P @ 0.1 GHz (dB)	G_P @ 1 GHz (dB)	NF @ 1 GHz (dB)	P_{1dB} (dBm)	Min. Supply Voltage[a] (V_{CC})	Device Voltage[a] (V_d)	Device Current[a] (mA)	Package	Page
MSA-0400	8.5	8.5	6.5	+16.0	10	6.3	90	chip	8-108
MSA-0500	9.0	8.5	6.5	+23.0	15	12.0	165	chip	8-123
MSA-1000	8.5	8.5	7.0	+27.0	20	15.0	325	chip	8-173
MSA-0420	8.5	8.5	6.5	+16.0	10	6.3	90	200 mil BeO disk	8-113
MSA-0470	8.5	8.3	6.5	+12.5	7	5.3	50	70 mil stripline	8-117
MSA-0520	9.0	8.5	6.5	+23.0	15	12.0	165	200 mil BeO disk	8-130
MSA-1023	8.5	8.5	7.0	+27.0	20	15.0	325	230 mil BeO flange	8-176
MSA-0435	8.5	8.3	6.5	+12.5	7	5.3	50	micro-X ceramic SM	8-115
MSA-0436	8.5	8.3	6.5	+12.5	7	5.3	50	trim lead micro-X SM	8-115
MSA-0404	8.3	7.7	7.0	+11.5	7	5.3	50	145 mil plastic	8-111
MSA-0485	8.3	8.0	7.0	+12.5	7	5.3	50	85 mil plastic	8-119
MSA-0504	8.0	7.0	6.5	+18.0	12	8.4	80	145 mil plastic	8-126
MSA-0486	8.3	8.0	7.0	+12.5	7	5.3	50	85 mil SM plastic	8-121
MSA-0505	8.0	7.0	6.5	+18.0	12	8.4	80	85 mil SM plastic	8-128

Wide Dynamic Range Amplifiers (Typical Specifications at +25°C Case Temperature)

Part Number	GP @ 0.1 GHz (dB)	GP @ 1 GHz (dB)	NF (dB)	P_{1dB} (dBm)	Min. Supply Voltage[a] (V_{CC})	Device Voltage[a] (V_d)	Device Current[a] (mA)	Package	Page
MSA-1100	12.5	11.0	4.0	+17.5	8	5.5	60	chip	8-178
MSA-1110	12.5	11.0	4.0	+17.5	8	5.5	60	100 mil stripline	8-185
MSA-1120	12.5	11.0	4.0	+17.5	8	5.5	60	200 mil BeO disk	8-187
MSA-1104	12.5	10.5	4.2	+17.5	8	5.5	60	145 mil plastic	8-181
MSA-1105	12.5	10.5	4.2	+17.5	8	5.5	60	85 mil SM plastic	8-183

High Frequency Amplifiers (Typical Specifications at +25°C Case Temperature)

Part Number	G_P @ 0.1 GHz (dB)	G_P @ 1 GHz (dB)	NF @ 1 GHz (dB)	P_{1dB} (dBm)	Min. Supply Voltage[a] (V_{CC})	Device Voltage[a] (V_d)	Device Current[a] (mA)	Package	Page
MSA-0900	8.0	8.0	6.0	+11.5	12	7.8	35	chip	8-166
MSA-0910	8.0	8.0	6.0	+11.5	12	7.8	35	100 mil stripline	8-169
MSA-0986	8.0	7.5	6.0	+11.0	12	7.8	35	85 mil SM plastic	8-171

Silicon Monolithic Integrated Circuits (cont)

Special Purpose/Minimal or No Feedback Amplifiers

(Typical Specifications at +25°C Case Temperature)

Part Number	G_P @ 0.1 GHz (dB)	G_P @ 1 GHz (dB)	NF @ 1 GHz (dB)	P_{1dB} (dBm)	Min. Supply Voltage[a] (V_{CC})	Device Voltage[a] (V_d)	Device Current[a] (mA)	Package	Page
MSA-9970	17.5	16.0		+14.5	10	7.8	35	70 mil stripline	8-203
MSA-0835	32.5	23.0	3.0	+12.5	10	7.8	36	micro-X ceramic SM	8-158
MSA-0836	32.5	23.0	3.0	+12.5	10	7.8	36	trim lead micro-X SM	8-158
MSA-0885	32.5	22.5	3.3	+12.5	10	7.8	36	85 mil plastic	8-162

Notes:
[a] Refer to schematic drawing on individual data sheet.

QPSK Modulators (Typical Specifications at +25°C Case Temperature.)

Part Number	LO Freq.	I/Q Freq.	P_{1dB} (dBm)	P_{SAT} (dBm)	Noise (dBm/Hz)	A_i (dB)	P_i (Deg.)	Package	Page
HPMX-2001	DC -2 GHz	DC -700 MHz	-9.5	-5.5	-135	±0.5	±1.0	SO-16, plastic	8-7
HPMX-2002	LO-1: 40-300 MHz LO-2: 250-2000 MHz	70 kHz	-12.5		-136	0.04	0.25	SO-20, plastic	8-13

3-Port Double-Balanced Mixers (Typical Specifications at +25°C Case Temperature)

Part Number	RF & LO Freq. (GHz)	Active Max. IF Freq. w/Gain (GHz)	RF-IF Gain (dB)	IP_3 (dBm)	LO-RF Iso. (dB)	Supply Voltage (V)	Device Current (mA)	Package	Page
IAM-81000	0.05-5.0	up to 1.0	8.5[a]	+3[a]	30[a]	5	12.5	chip	8-33
IAM-81018	0.05-5.0	up to 1.0	8.5[a]	+3[a]	30[a]	5	12.5	180 mil SM	8-37
IAM-82008	0.05-5.0	up to 2.0	15.0[b]	+18[b]	22[b]	10	55	SO-8 SM	8-39
IAM-82018	0.05-5.0	up to 2.0	15.0[b]	+18[b]	30[b]	10	50	180 mil SM	8-43
IAM-81008	0.05-5.0	up to 1.0	8.5[a]	+3[a]	25[a]	5	13	SO-8 SM	8-35

2-Port Self-Oscillating Mixers (Typical Specifications at +25°C Case Temperature)

Part Number	RF & LO Freq. (GHz)	IF Freq. w/Gain (GHz)	RF-IF Conversion Gain (dB)	IP_3 (dBm)	LO-RF Iso. (dB)	Supply Voltage (V)	Device Current (mA)	Package	Page
MSF-8670	0.1-2.0	up to 0.5	9.0[c]	+7[c]	0[c]	5	16	70 mil stripline	8-205
MSF-8870	0.5-8.0	up to 2.0	9.0[d]	+16[d]	0[d]	10	36	70 mil stripline	8-209
MSF-8635	0.1-2.0	up to 0.5	9.0[c]	+7[c]	0[c]	5	16	micro-X ceramic	8-205
MSF-8835	0.5-8.0	up to 2.0	9.0[d]	+16[d]	0[d]	10	36	micro-X ceramic	8-209
MSF-8685	0.1-2.0	up to 0.5	8.0[c]	+7[c]	0[c]	5	16	85 mil plastic	8-205
MSF-8885	0.5-8.0	up to 2.0	8.5[d]	+16[d]	0[d]	10	36	85 mil plastic	8-209

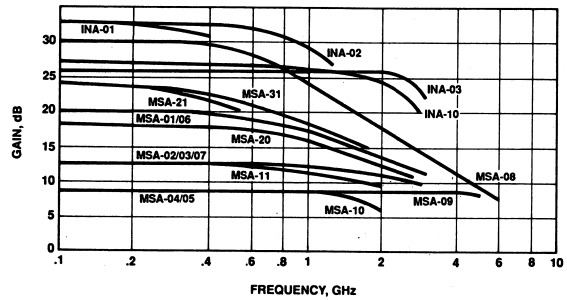
Notes:
[a] -20 dBm RF input, -5 dBm LO input, RF at 2.0 GHz, LO at 1.75 GHz.
[b] -20 dBm RF input, 0 dBm LO input, RF at 2.0 GHz, LO at 1.75 GHz.
[c] -20 dBm RF input, RF at 1.575 GHz, LO at 1.4 GHz.
[d] -20 dBm RF input, RF at 4.2 GHz, LO at 5.15 GHz.

High Frequency Prescalers (Typical Specifications at +25°C Case Temperature)

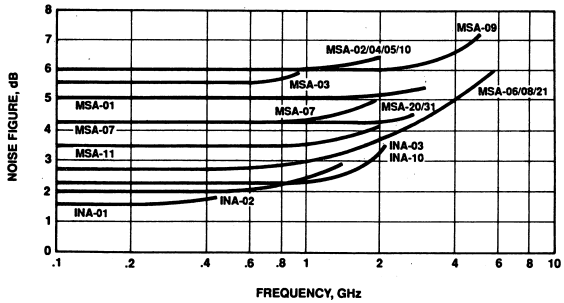
Part Number	Divide Ratio	F_{MAX} (GHz)	F_{MIN} (dB)	P_{IN} @ (dBm)	P_{OUT} @ (dB)	I_{CC} (V)	Package	Page
IFD-53010	4	6.0	0.15	-25 @ 5.0 GHz	-5 @ 0.15 to 5.0 GHz	43	100 mil stripline	8-45
IFD-53110	4	5.0	0.15	-25 @ 3.0 GHz	-5 @ 0.15 to 3.0 GHz	43	100 mil stripline	8-45

Performance Graphs for Silicon Monolithic Amplifiers

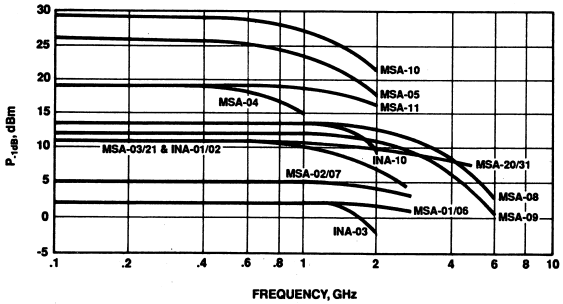
FIXED GAIN FEEDBACK AMPLIFIERS
GAIN VERSUS FREQUENCY



FIXED GAIN FEEDBACK AMPLIFIERS
NOISE FIGURE VERSUS FREQUENCY



FIXED GAIN FEEDBACK AMPLIFIERS
P_{1dB} VERSUS FREQUENCY



HEWLETT PACKARD

Silicon Bipolar Monolithic QPSK Modulator

Technical Data

HPMX-2001

Features

- **I/Q Bandwidth: DC - 700 MHz**
- **LO Frequency Range: DC-2000 MHz**
- **Standby Mode - P_d 10 mW**
- **Low Cost Plastic Surface Mount Package**

Applications

- **Digital Cellular Radio (eg., GSM, ADC)**
- **RF Data Links**
- **Vector Generators**
- **AM Modulator**
- **Single Sideband Mixer**

Description

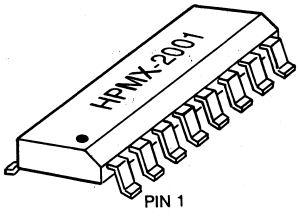
The HPMX-2001 is a silicon monolithic quadrature phase shift keyed modulator in a plastic surface mount SO-16 package. It is designed for wide or narrow band applications and has a typical LO operating frequency range of DC-2000 MHz and typical I/Q bandwidth of DC-700 MHz.

The modulator may be operated in any combination of single or differential input/output configurations. The LO inputs are self biasing and have 50 Ohm termination impedances. The I & Q inputs are open base and require 2.5 V DC bias. This allows direct coupling to the I & Q inputs. The RF output is designed to drive a 50 Ohm load and has a saturated output power level of -5.5 dBm.

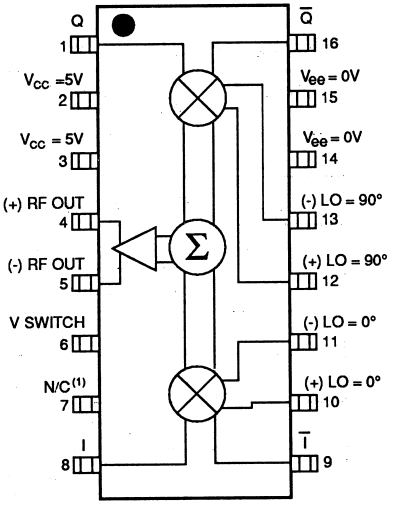
The internal signal paths of the modulator are fully differential to help reduce susceptibility to common mode noise. The small amplitude and phase imbalance of the device, 0.5 dB and 1 degree respectively, makes the modulator suitable for many communication applications. The HPMX-2001 also features a standby mode in which the device consumes only 10 mW of power.

The HPMX-2001 is manufactured using Hewlett-Packard's 13 GHz F_t, 25 GHz F_{max} silicon bipolar integrated circuit process.

Plastic SO-16 Package



Functional Block Diagram and Pin Configuration



NOTE 1: DO NOT GROUND PIN 7.

HPMX-2001 Absolute Maximum Ratings, T_A = 25°C*

Symbol	Parameter	Units	Maximum
V_{cc}	Supply Voltage	Volts	6
V_{in} I/Q	I/Q Input Voltage	Volts P-P	4
P_{in} LO	LO Input Power	dBm	10
V_{sw}	Standby Switch Voltage	Volts	6
T_{op}	Ambient Operating Temperature	°C	-55 to +85
T_{stg}	Storage Temperature	°C	-55 to +150

*Operation in excess of any one of these conditions may result in permanent damage to this device.

Care should be taken to prevent Electro Static Discharge (ESD) that could permanently damage the device. Class I device.

Notes: 1. A θ_{ja} of 200°C/W should be used for derating and junction temperature calculations: $T_j = (P_d \times \theta_{ja}) + T_a$

2. Maximum soldering temperature is 260°C for 5 seconds.

Electrical Parameters, T_A = 25°C, V_{cc} = 5V, Single Ended Operation

Symbol	Parameter/Test Condition: Z_o = 50 Ohms	Units	Typ.
I_{cc}	Supply Current	mA	20
P_{sw}	Standby Power, V_{sw} = +2.5 Volts	mW	10
–	LO Operating Frequency Range	MHz	DC to 2,000
–	I/Q Modulating Frequency Range	MHz	DC to 700
–	I/Q Input Impedance	Ohms pF	25K 1.0

RF Electrical Parameters, T_A = 25°C, V_{cc} = 5V, Single Ended Operation

Symbol	Parameters/Test Conditions: LO = -13 dBm, F = 100 MHz, I/Q = 70 KHz 1 Volt P-P, Z_o = 50 Ohms		Units	Typ.
P_{1dB}	Power Out at 1 dB Compression		dBm	-9.5
P_{sat}	Saturated Output Power		dBm	-5.5
Noise	Output Noise Floor		dBm/Hz	-135
–	LO Input SWR		SWR	2.3:1
–	RF Output SWR		SWR	1.6:1
A_i	I/Q Amplitude Imbalance		dB	±0.5
P_i	I/Q Phase Imbalance		Deg.	±1.0
–	Modulation products power level in dB relative to the desired sideband at the output	Residual LO Undesired Sideband	dBc dBc	-37(3) -33(4)

Notes: 3. Improved LO rejection may be obtained by adjusting I/Q bias voltages.

4. Undesired sideband and harmonic suppression may be improved by adjusting I/Q amplitude and phase and/or using differential operation.

RF Electrical Parameters, T_A = 25°C, V_{cc} = 5V, Single Ended Operation

Symbol	Parameters/Test Conditions: LO = -13 dBm, F = 900 MHz, I/Q = 70 KHz 1 Volt P-P, Z_o = 50 Ohms		Units	Typ.
P_{1dB}	Power Out at 1 dB Compression		dBm	-9.5
P_{sat}	Saturated Output Power		dBm	-6.0
Noise	Output Noise Floor		dBm/Hz	-135
–	LO Input SWR		SWR	2.3:1
–	RF Output SWR		SWR	1.6:1
A_i	I/Q Amplitude Imbalance		dB	±1.0
P_i	I/Q Phase Imbalance		Deg.	±1.0
–	Modulation products power level in dB relative to the desired sideband at the output	Residual LO Undesired Sideband	dBc dBc	-35(3) -30(4)

Notes: 3. Improved LO rejection may be obtained by adjusting I/Q bias voltages.

4. Undesired sideband and harmonic suppression may be improved by adjusting I/Q amplitude and phase and/or using differential operation.

Theory of Operation

Figure 1 shows the simplified schematic for the HPMX-2001. There are four differential input pairs (I, Q, LO = 0°, LO = 90°) and one differential output pair (RF). Any of the inputs or outputs can be used single-endedly with the proper terminations. The bias circuit for the LO inputs provides 50 Ohm matching of typically 2.3:1 in either differential or single-ended mode. The I and Q inputs are differentially mixed with the LO = 0° and LO = 90° signals respectively. The two mixer cells are double balanced to improve port isolation and reduce spurious signals at the RF output.

The outputs of the mixers are cross coupled into the summing amplifier circuit. This helps to reduce any internally generated offsets which tend to cause greater feedthrough of unwanted signals to the RF outputs.

The mixer and summing subcells utilize current sources that are controlled by the standby circuit. When the standby mode is activated, the control line turns off the current sources for all subcells. The resulting power dissipation is due only to the standby circuit.

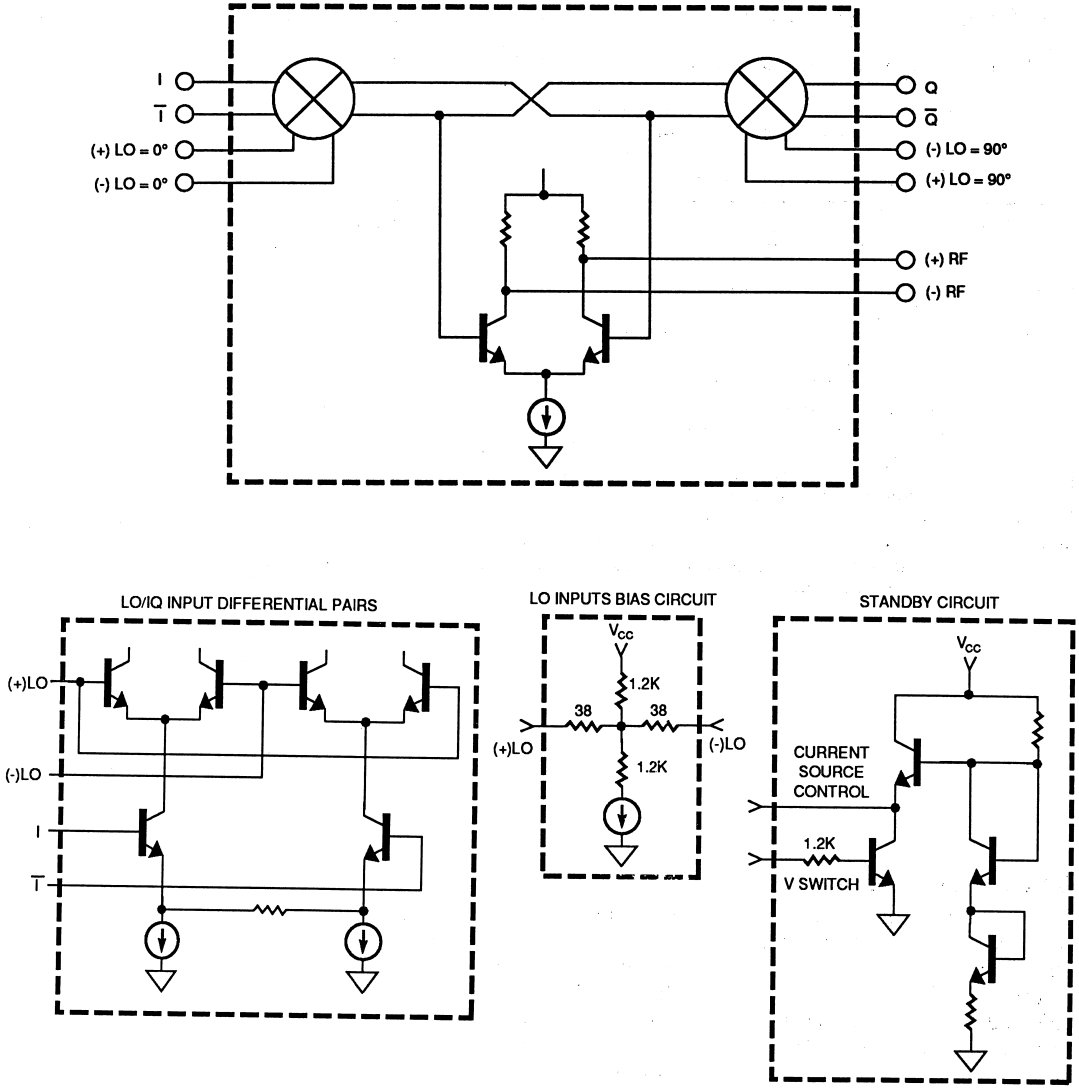
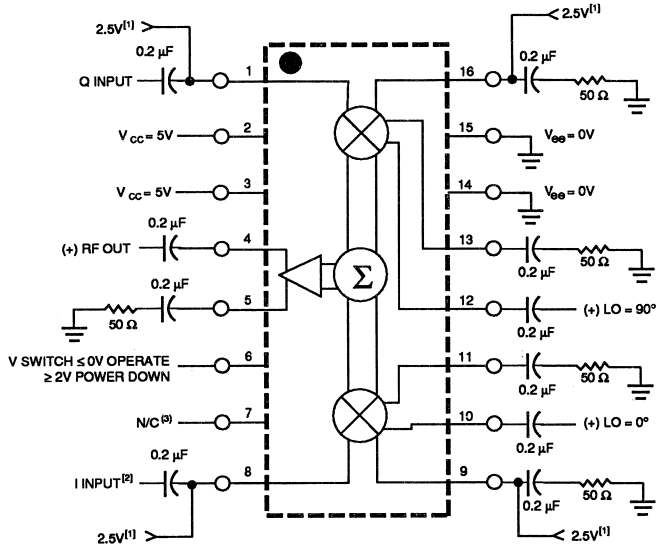


Figure 1. HPMX-2001 Simplified Schematic



NOTES:
1. IMPROVED LO REJECTION MAY BE OBTAINED BY ADJUSTING THE I/Q BIAS VOLTAGES.
2. UNDESIRED SIDEBAND AND HARMONIC SUPPRESSION MAY BE IMPROVED BY ADJUSTING I/Q AMPLITUDE AND PHASE AND/OR USING DIFFERENTIAL OPERATION.
3. DO NOT GROUND PIN 7.

Figure 2. HPMX-2001 Test Circuit, Single Ended Operation[2]

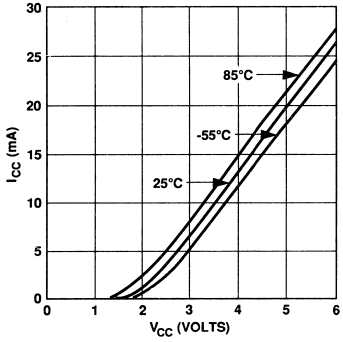


Figure 3. Typical I_{CC} vs. V_{CC} vs. Temperature

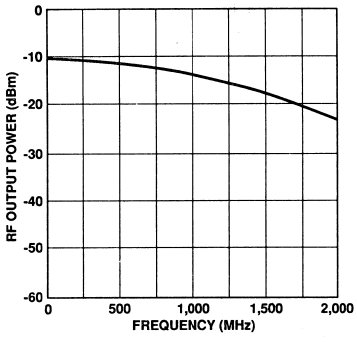


Figure 4. Typical RF-LO Frequency Response, LO = -13 dBm, I and Q = 70 KHz, 688 mV P-P

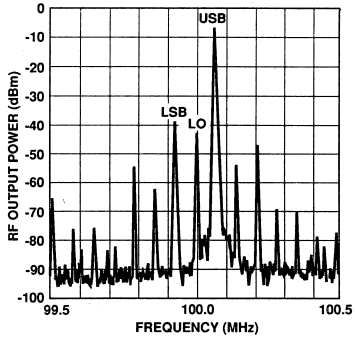


Figure 5. Typical Output Frequency spectrum, LO = 100 MHz -13 dBm, I/Q = 70 KHz 1 Volt P-P

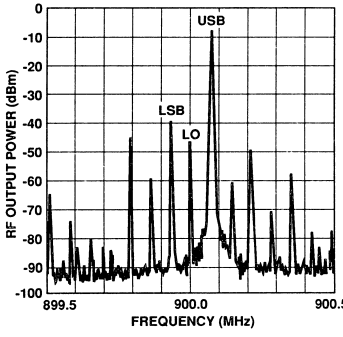


Figure 6. Typical Output Frequency spectrum, LO = 900 MHz -13 dBm, I/Q = 70 KHz 1 Volt P-P

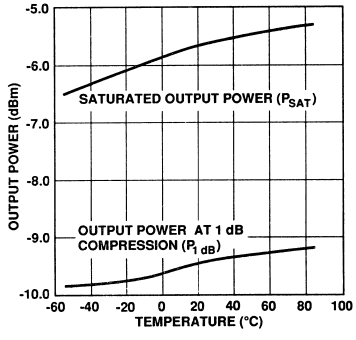


Figure 7. Output Power vs. Temperature, V_{CC} = 5 Volts, F = 100 MHz.

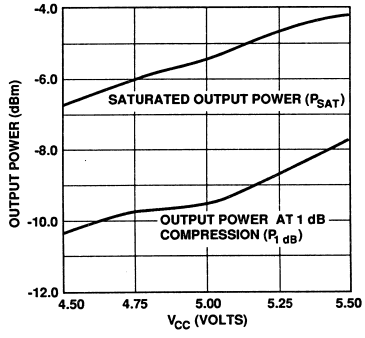
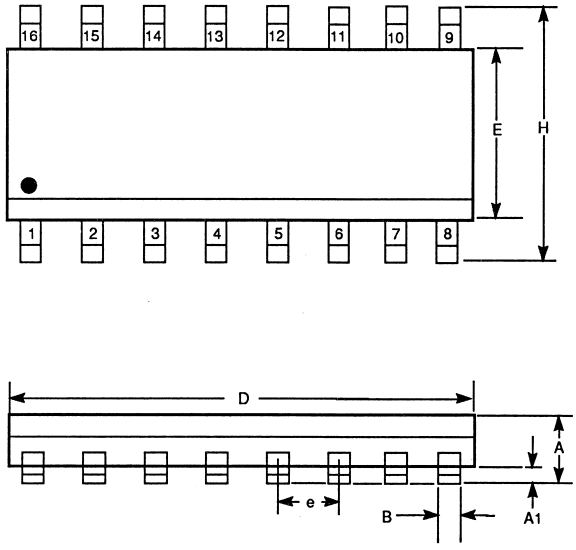
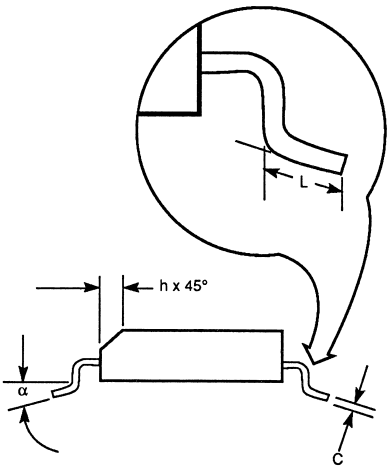


Figure 8. Output Power vs. V_{CC}, T_A = 25°C, F = 100 MHz.

Package Dimensions

Plastic SO-16 Package





Symbol	Dimensions	
	Min.	Max.
A	1.35 (0.053)	1.75 (0.068)
A1	0.10 (0.004)	0.25 (0.0098)
B	0.35 (0.0138)	0.49 (0.0192)
C	0.19 (0.007)	0.25 (0.0098)
D	9.80 (0.386)	10.00 (0.394)
E	3.80 (0.150)	4.00 (0.157)
e	1.27 BSC (0.050)	
H	5.80 (0.228)	6.20 (0.244)
h	0.25 (0.010)	0.50 (0.020)
L	0.40 (0.016)	1.27 (0.050)
α	0°	8°

Meets JEDEC outline dimensions.
Dimensions are in millimeters (inches)

HEWLETT PACKARD

Silicon Bipolar Monolithic Conversion Quadrature Modulator

Technical Data

HPMX-2002

Features

- **I/Q Bandwidth >10 MHz**
- **Wide Bandwidth**
  1st LO, 40-300 MHz
  2nd LO, 250-2,000 MHz
  RF 250-2,000 MHz
- **On Chip Mixer for Dual Conversion**
- **Low Power Dissipation**
  Standby, 50 μW
  Operating, 60 mW
- **Low Cost Plastic Surface Mount Package**

Applications

- **Digital Cellular Radio**
- **RF Data Links**
- **Vector Generators**

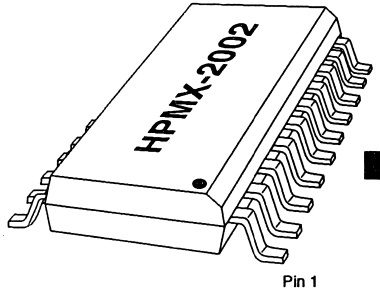
Description

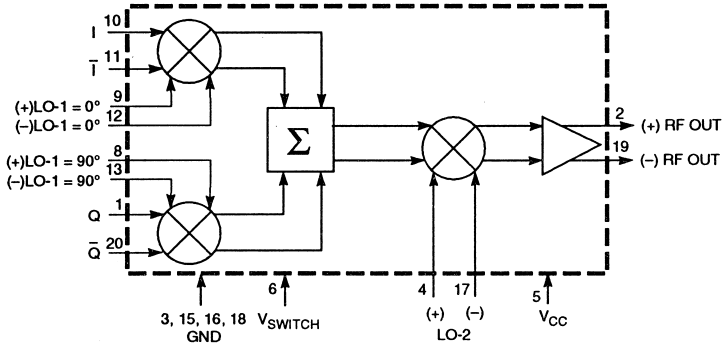
The HPMX-2002 is a silicon monolithic, dual conversion, quadrature modulator in a plastic surface mount SO-20 package. It has typical LO-1 operating frequency range of 40-300 and LO-2 of 250-2,000 MHz, and typical I/Q bandwidth of >10 MHz.

The LO inputs are self biased and have 50 Ohm termination impedances. The RF output has a -11 dBm output power level. The HPMX-2002 also features a standby mode in which the device consumes only 11 μA of current.

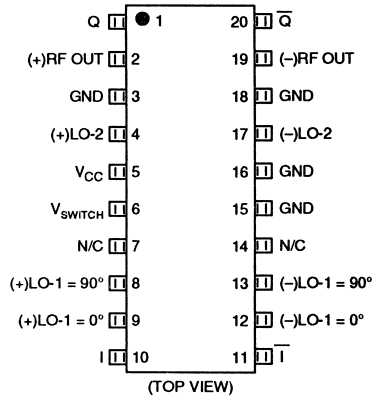
The device is manufactured using Hewlett-Packard's 13 GHz F_t, 25 GHz F_{max} silicon bipolar integrated circuit process.

Plastic SO-20 Package





Functional Block Diagram



Pin Configuration

Absolute Maximum Ratings, T_A = 25°C*

Symbol	Parameter	Units	Max.
V_{cc}	Supply Voltage	Volts	6
V_{in} I/Q	I/Q Input Voltage	Volts P-P	4
P_{in} L/O	Lo Input Power	dBm	+10
V_{switch}	Standby Switch Voltage	Volts	6
T_{op}	Ambient Operating Temperature	°C	-55 to +85
T_{stg}	Storage Temperature	°C	-55 to +150

* Operation in excess of any one of these conditions may result in permanent damage to this device. Care should be taken to prevent Electro Static Discharge (ESD) that could permanently damage the device. Class I device.

Notes:

1. A θ_{ja} of 200°C/W should be used for derating and junction temperature calculations:
   $T_j = (P_d \times \theta_{ja}) + T_A$
2. Maximum soldering temperature is 260°C for 5 seconds.

RF Electrical Parameters, T_A = 25°C, V_{CC} = 5V

Symbol	Parameter/Test Condition: LO-1 = -14 dBm F = 100 MHz, LO-2 = -3 dBm F = 900 MHz, I/Q = 70 kHz 1.2V P-P (Differential), Z_O = 50 Ohms, Test Circuit #2		Units	Min.	Typ.	Max.
P_{out}	RF Output Power at 800 MHz		dBm		-11	
	RF Output Power Flatness, 800 to 1,000 MHz		dB		±0.6	
P_{1dB}	Power Out at 1 dB Compression (I/Q Voltage Swept)		dBm		-12.5	
Noise	Output Noise Floor		dBm/Hz		-136	
	Modulation product power levels in dB relative to the desired sideband with filter at 1st carrier output	Residual L/O (800 MHz) [1]	dBc		-38	-30
		Undesired Sideband (799.93 MHz)[2]	dBc		-52	-30
		2nd Harmonic (800 ± 0.140 MHz)[3]	dBc		-47	-30
		3rd Harmonic (800 ± 0.210 MHz)[3]	dBc		-42	-30
		5th Harmonic (800 ± 0.350 MHz)[3]	dBc		-57	-50
	LO-1 Input SWR		SWR		1.5:1	
	LO-2 Input SWR		SWR		1.2:1	
	RF Output SWR (Operating)		SWR		1.5:1	
A_i	I/Q Amplitude Imbalance (Derived from undesired sideband data)		dB		0.04	
P_i	I/Q Phase Imbalance (Derived from undesired sideband data)		Deg.		0.25	

Notes:

1. Residual LO = (F_{L02} - F_{L01})
2. Undesired Sideband = (F_{L02} - F_{L01} - F_{IQ})
3. Nth Harmonic = (F_{L02} - F_{L01}) ± (N * F_{IQ})

Electrical Parameters, T_A = 25°C, V_{CC} = 5V

Symbol	Parameter/Test Condition: LO-1 = -14 dBm F=100 MHz, LO-2 = -3 dBm F = 900 MHz, I/Q = 70 kHz 1.2V P-P Z_O = 50 Ohms, Test Circuit #1 (unless noted)	Units	Typ.	Max.
I_{cc}	Supply Current	mA	12.2	15
I_{cc}	Standby Current, V_{switch} = +3.0 V	µA	10.5	15
	I/Q Input Impedance (Internally Biased with High Impedance Source to ≅ 2.3 Volts DC)	Ohms pF	8K 1.0	
	LO-1 Operating Frequency Range	MHz	40 to 300	
	LO-2 Operating Frequency Range	MHz	250 to 2,000	
	I/Q Modulating Frequency Range	MHz	DC to 10	
	RF Output Frequency Range	MHz	250 to 2,000	
T_{on}	Turn-on Time, within 0.5 dB Final Output Power (Test Circuit #4)	µs	1.2	
T_{off}	Turn-off Time, Output Power below Noise Floor (Test Circuit #4)	µs	0.4	

Theory of Operation

Figure 1 shows the simplified block diagram of the HPMX-2002. The device consists of 3 double balanced active "Gilbert cell" mixers and two amplifier stages. I and Q inputs are mixed with the LO-1 0° and LO-1 90° signals respectively. These signals are then amplified, level shifted, up-converted, and fed to the output through an amplifier stage.

Double balanced mixers are used to improve port isolation and reduce spurious signals at the output. All signal inputs (except V_{switch}) are differentially balanced and RF ports are matched to 50 Ohms. I and Q inputs have high impedances to ensure that they can be driven from high impedance sources. All of the signal inputs can be used either single endedly or differentially with proper terminations.

The mixers and amplifiers use current sources that are controlled by the standby circuit. When the standby circuit is activated, the control line turns off the current sources for all subcells. The remaining power dissipation is due only to the standby circuit.

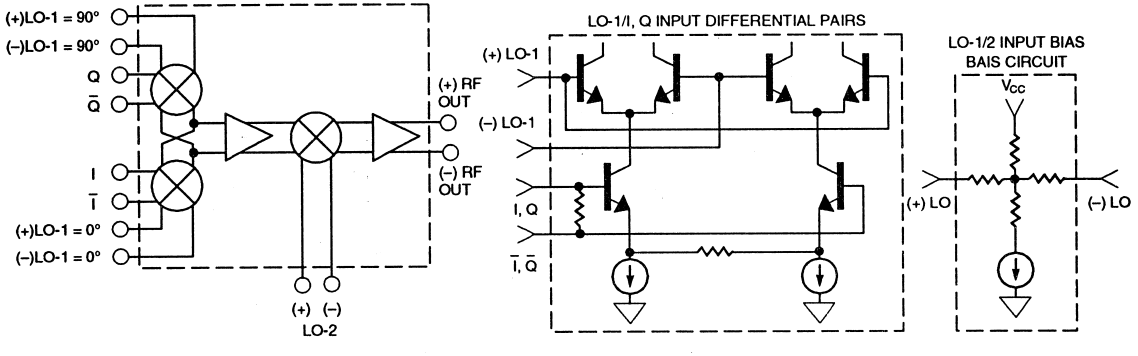


Figure 1. HPMX-2002 Simplified Schematic

High Frequency Performance

The dual conversion architecture and the wideband nature of the Gilbert cell allows an excellent performance to 2 GHz. The output stage gain has been kept low which gives wide bandwidth to allow this device to be used over a wide range of LO-2 frequencies. For equal input signals, harmonic suppression will generally improve at higher LO-2 frequencies. RF performance at 1.9 GHz is similar to performance at 800 MHz but with reduced output power.

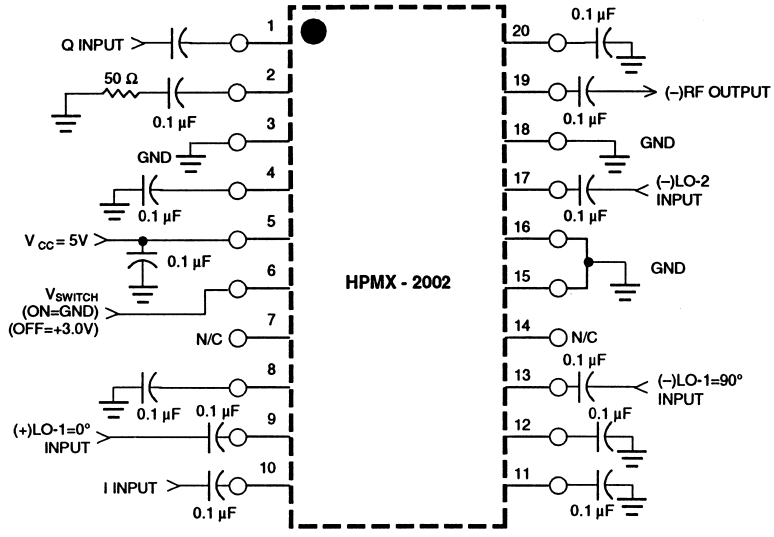


Figure 2. HPMX-2002 Test Circuit #1, Broadband Operation

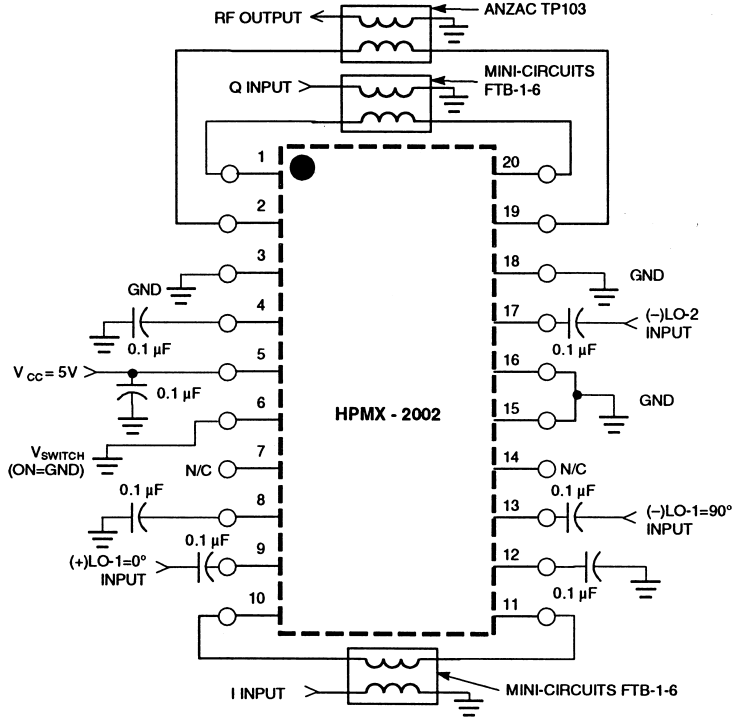


Figure 3. HPMX-2002 Test Circuit #2, Differential Operation

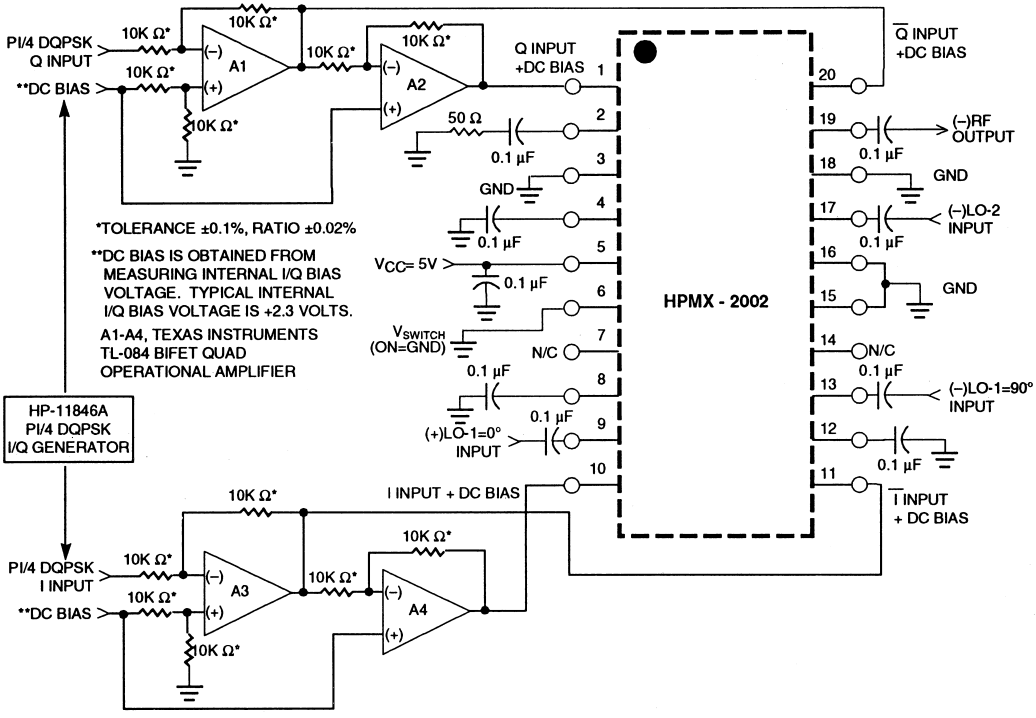


Figure 4. HPMX-2002 Test Circuit #3, Spectral Mask.

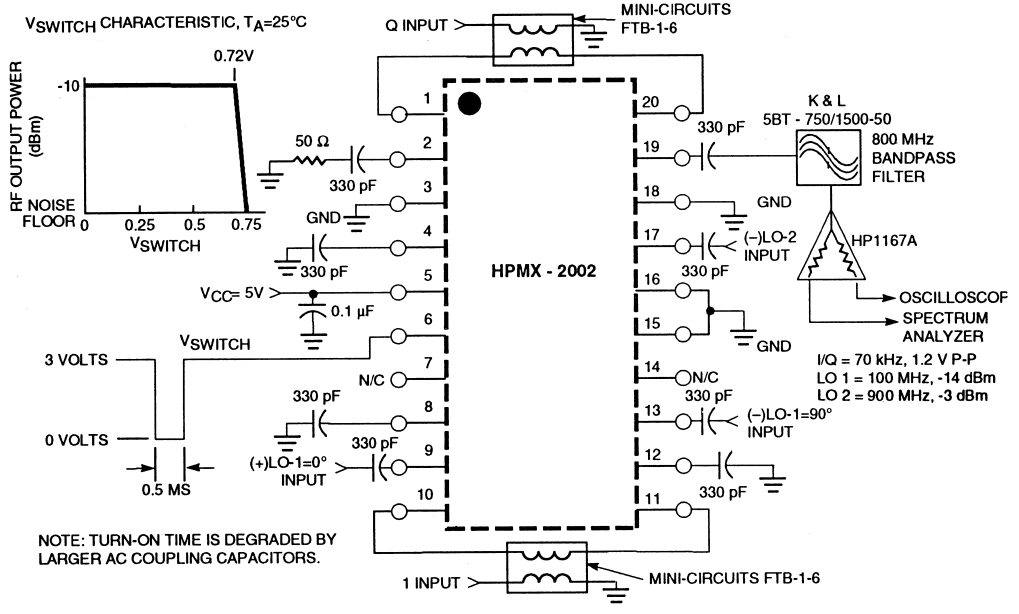


Figure 5. HPMX-2002 Test Circuit #4, Turn-On Time.

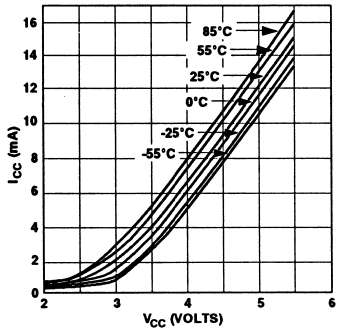


Figure 6. Typical I_{CC} vs. V_{CC} vs. Temperature

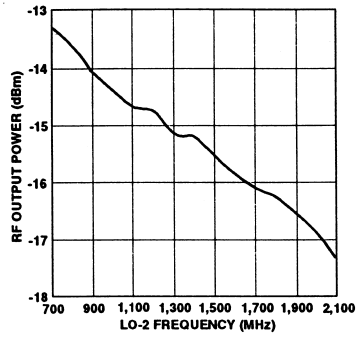


Figure 7. Typical RF Output Frequency Response; LO-1 = -14 dBm at 100 MHz: LO-2 = -3dBm: I/Q = 70 kHz, 1.2 V P-P; Test Circuit #1

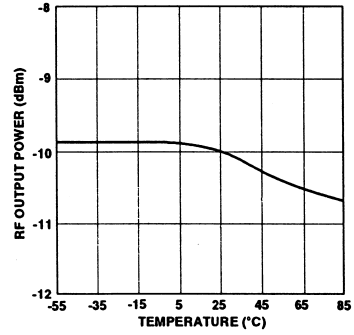


Figure 8. Typical Output Power at 800.07 MHz vs. Temperature; LO-1 = -14 dBm at 100 MHz; LO-2 = -3dBm at 900 MHz; I/Q = 70 kHz, 1.2 V P-P; Test Circuit #2

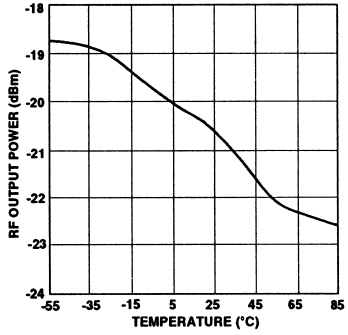


Figure 9. Typical Output Power at 800.07 MHz vs. Temperature; LO-1 = -28 dBm at 100 MHz; LO-2 = -3dBm at 900 MHz; I/Q = 70 kHz, 1.2 V P-P; Test Circuit #2

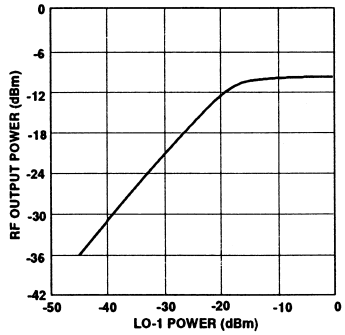


Figure 10. Typical Output Power at 800.07 MHz vs. LO-1 Power; LO-1 = 100 MHz; LO-2 = -3dBm at 900 MHz; I/Q = 70 kHz, 1.2 V P-P; Test Circuit #2

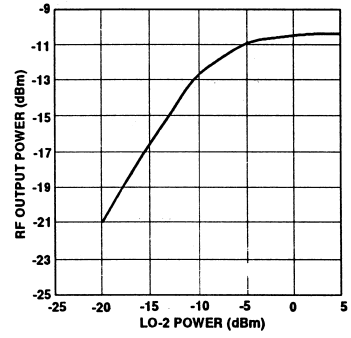


Figure 11. Typical Output Power at 800.07 MHz vs. LO-2 Power; LO-1 = -14 dBm at 100 MHz; LO-2 = 900 MHz; I/Q = 70 kHz, 1.2 V P-P; Test Circuit #2

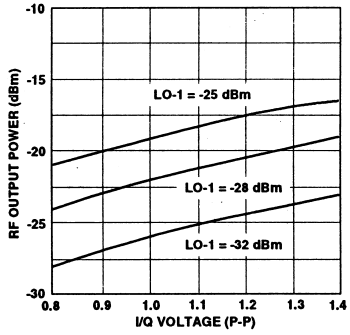


Figure 12. Typical Output Power vs. I/Q Voltage vs. LO-1 Power; LO-1 at 100 MHz; LO-2 = -3dBm at 900 MHz; Test Circuit #2

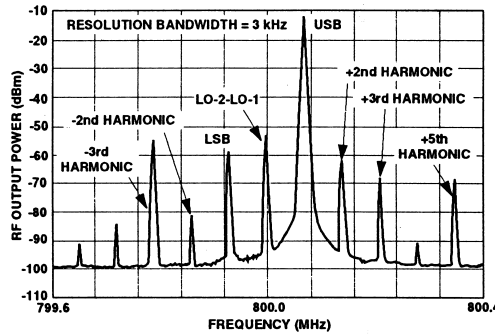


Figure 13. Typical Output Frequency Spectrum, LO-1 = -14 dBm at 100 MHz; LO-2 = -3dBm at 900 MHz; I/Q = 70 kHz, 1.2 V P-P; Test Circuit #1

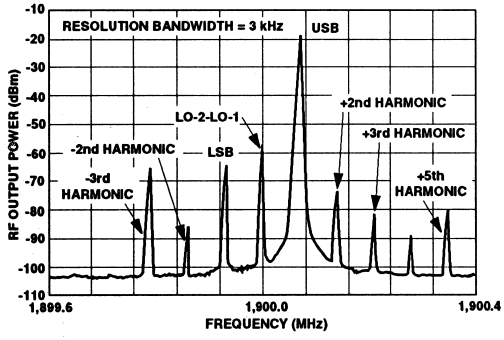


Figure 14. Typical Output Frequency Spectrum, LO-1 = -14 dBm at 100 MHz; LO-2 = -3dBm at 2,000 MHz; I/Q = 70 kHz, 1.2 V P-P; Test Circuit #1

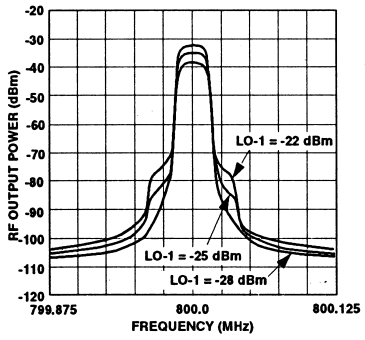


Figure 15. Typical Output Spectral Mask vs. LO-1 Power; LO-1 = 100 MHz; LO-2 = -3dBm at 900 MHz; I/Q = 1.2 Volts P-P; π/4 DQPSK, PRBS = 20; Symbol Clock = 24.3 kHz; Test Circuit #3

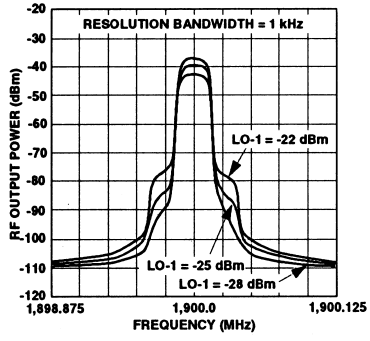


Figure 16. Typical Output Spectral Mask vs. LO-1 Power; LO-1 = 100 MHz; LO-2 = -3 dBm at 2,000 MHz; I/Q = 1.2 Volts P-P; π/4 DQPSK, PRBS = 20; Symbol Clock = 24.3 kHz, Test Circuit #3

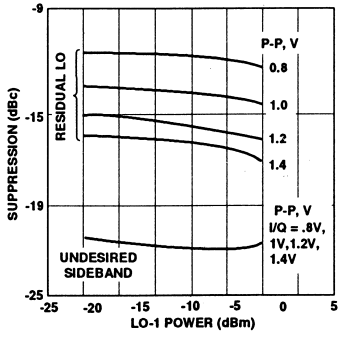


Figure 17. Typical Residual LO and Undesired Sideband Suppression at 800 MHz vs. LO-1 Power vs. I/Q Voltage; LO-1 = 100 MHz; LO-2 = -3 dBm; at 900 MHz, LO-2 = -3 dBm at 900 MHz, I/Q = 70 kHz, Test Circuit #2

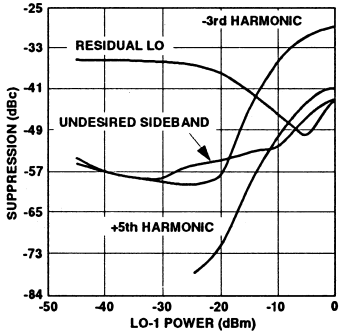


Figure 18. Typical Undesired Sideband, Residual LO, and Harmonic Suppression at 800 MHz vs. LO-1 Power; LO-1 = 100 MHz; LO-2 = -3dBm at 900 MHz, I/Q = 70 kHz, 1.2 Volts P-P; Test Circuit #2

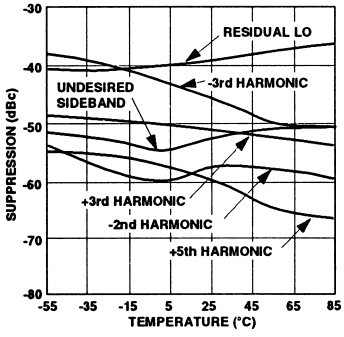


Figure 19. Typical Residual LO, Undesired Sideband and Harmonic Suppression at 800 MHz, LO-1 = -14 dBm at 100 MHz; LO-2 = -3 dBm at 900 MHz; I/Q = 1.2 Volts P-P, π/4 DQPSK; PRBS = 20, Symbol Clock = 24.3 kHz; Test Circuit #3

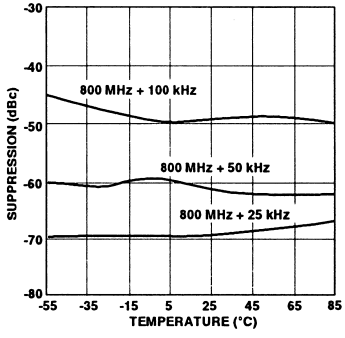
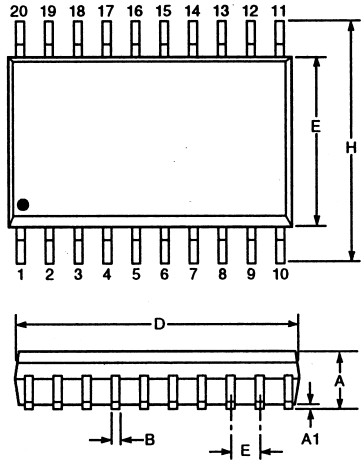


Figure 20. Typical Spectral Mask IMD/ Noise Suppression vs. Temperature; LO-1 = -28 dBm at 100 MHz; LO-2 = -3 dBm at 900 MHz; I/Q = 1.2 Volts P-P, π/4 DQPSK; PRBS = 20, Symbol Clock = 24.3 kHz; Test Circuit #3

Package Dimensions

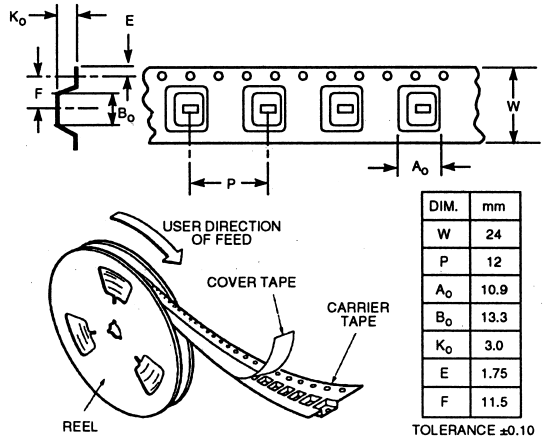
Plastic SO-20 Package



SYMBOL	DIMENSIONS MIN.	DIMENSIONS MAX.
A	2.35 (0.093)	2.65 (0.104)
A1	0.10 (0.004)	0.30 (0.012)
B	0.35 (0.014)	0.49 (0.019)
C	0.23 (0.009)	0.31 (0.012)
D	12.6 (0.496)	13.0 (0.512)
E	7.40 (0.291)	7.60 (0.299)
e	1.27 BSC (0.050)	
H	10.26 (0.404)	10.65 (0.419)
h	0.50 (0.020)	0.75 (0.030)
L	0.86 (0.034)	1.07 (0.042)
θ	0	8

MEETS JEDEC OUTLINE DIMENSIONS.
DIMENSIONS ARE IN MILLIMETERS (INCHES).

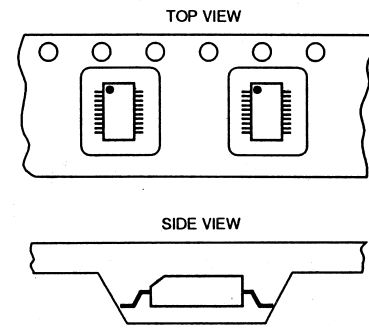
SOIC-20L Carrier Tape – HPMX-2002



DIM.	mm
W	24
P	12
A_o	10.9
B_o	13.3
K_o	3.0
E	1.75
F	11.5

TOLERANCE ±0.10

Device Orientation



HEWLETT PACKARD

Silicon Bipolar MMIC 900 MHz Vector Modulator

Technical Data

HPMX-2003

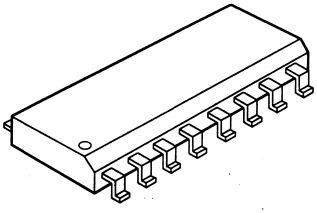
Features

- 800 - 1000 MHz Output Frequency Range
- +6 dBm Peak Output Power
- Single Ended 50 Ω Output
- Internal 90° Phase Shifter
- 5 Volt, 36 mA Bias
- SO-16 Surface Mount Package

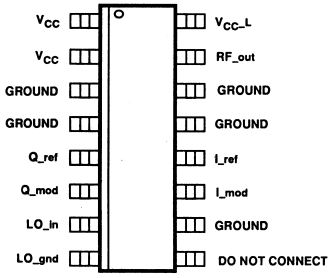
Applications

- Direct Modulator for 900 MHz Cellular Telephone Handsets, Including GSM, JDC, and NADC
- Direct Modulator for 900 MHz ISM Band Spread-Spectrum Transmitters and LANs

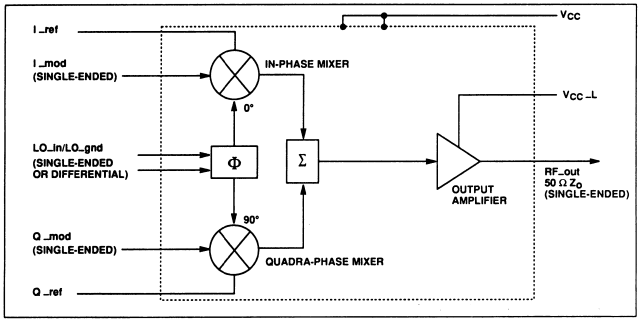
Plastic S0-16 Package



Pin Configuration



Functional Block Diagram



Description

Hewlett-Packard's HPMX-2003 is a Silicon RFIC direct conversion vector modulator designed for use at output frequencies between 800 MHz and 1 GHz. Housed in an SO-16 surface mount plastic package, the IC contains two matched Gilbert cell mixers, an RC phase shifter, a summer, and an output amplifier complete with 50 Ω impedance match and DC block.

The internal impedance match on the output pin (RF_out) results in high levels of linear output power and eliminates the need for output matching circuitry such as transformers or baluns -only a 50 Ω characteristic impedance transmission line is needed for interfacing to the load. This pin is configured for single-ended (unbalanced) use.

For drive from a single-ended LO, the LO_in pin is AC coupled to a -12 dBm source using 50 Ω transmission line, with the LO_gnd pin AC bypassed to ground. Alternatively, a differential (balanced) signal may be AC coupled across the LO_in and LO_gnd pins.

At the time this catalog was printed, this product was not yet released for sale. Please contact the local HP Field Sales Office for more information. All specifications are subject to change.

A DC reference voltage, typically 2.5 V ± 0.5 V, must be applied to both the in-phase (I) and Quadra-Phase (Q) reference pins, V_{I_ref} and V_{Q_ref}. These two pins may be shorted together for drive from a single reference source. The V_{I_mod} and V_{Q_mod} pins should be DC coupled to single-ended voltage inputs supplying the I and Q data. For the HPMX-2003 the I and Q data should swing ±1.25 V about the reference voltage.

Device power is provided by three V_{CC} pins. Two pins (V_{CC}) are directly coupled to the V_{CC} supply (5 V) with appropriate AC bypassing near the pins (1000 pF typ.). The third (V_{CC}_L) can be used with an optional external small inductor (1-2 nH) from the pin to the bypass point that will optimize the output matching at frequencies closer to 800 MHz.

This device is well suited for use in direct modulated portable and mobile telephone handsets for cellular systems such as GSM, North American Digital Cellular, and Japan Digital Cellular. It can also be used in digital transmitters operating in the 900 MHz ISM (Industrial-Scientific-Medical) band, including use in Local Area Networks (LANs).

The HPMX-2003 is fabricated with Hewlett-Packard's 25 GHz ISOSAT-II process, which combines stepper lithography, ion-implantation, self-alignment techniques, and gold metallization to produce RFICs with superior performance, uniformity, and reliability.

HPMX-2003 Absolute Maximum Ratings, T_A = 25°C*

Symbol	Parameter	Units	Absolute Maximum
P_{diss}	Power Dissipation[1,2]	mW	500
LO_{in}	LO Input Power	dBm	0
V_{CC}	Supply Voltage	V	8
Δ_I, Δ_Q	Swing of V_{I_mod} about V_{I_ref} or V_{Q_mod} about V_{Q_ref}	V V_{p-p}	2.5 5
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to +150

*Operation of this device above any one of these parameters may cause permanent damage.

Thermal Resistance: HPMX-2003 Thermal Resistance[2]: θ_{jc} =125°C/W

Notes:
1. T_{case} = 25°C (T_{case} is defined to be the temperature at the ends of pin 3 where it contacts the circuit board).
2. Derate at 8 mW/°C for T_C > 112°C.

At the time this catalog was printed, this product was not yet released for sale. Please contact the local HP Field Sales Office for more information. All specifications are subject to change.

HPMX-2003 Electrical Specifications, T_A = 25°C, Z_o = 50 Ω

V_{CC} = 5 V, LO = -12 dBm @ 900 MHz (single-ended input), I_ref = Q_ref = 2.5 V (unless otherwise noted).

Symbol	Parameters	Test Conditions	Units	Typical
P_{out}	Output Power	$V_{I_mod} = V_{Q_mod}$ = 3.75 V	dBm	6
P_{1dB}	Power at 1 dB Compression		dBm	7
VSWR	Output VSWR (50 Ω)			1.5:1
	Input LO VSWR (50 Ω)			1.5:1
LO_{leak}	LO Leakage at Output	$V_{I_mod} = V_{Q_mod}$ = 2.5 V	dBm	-30
	Unwanted Sideband Signal	$V_{I_mod} = V_{I_ref}$ +1.25 V sin(ω_nt) $V_{Q_mod} = V_{Q_ref}$ +1.25 V cos(ω_nt) ω_n = 30 kHz	dBm	-30
Noise	Output Noise Floor	$V_{I_mod} = V_{Q_mod}$ = 3.75 V	dBm/Hz	-134
R_{in}	Input Resistance (I_mod to I_ref or Q_mod to Q_ref)		Ω	10 k
A_i	RMS Amplitude Imbalance	$SQR(V_I^2 + V_Q^2)$ = 1.25 V[1]	dB	0.15
P_i	RMS Phase Imbalance	$SQR(V_I^2 + V_Q^2)$ = 1.25 V[1]	deg	1.25
I_d	Device Current		mA	36

Note:

1. $V_I = V_{I_mod} - V_{I_ref}$ and $V_Q = V_{Q_mod} - V_{Q_ref}$.

At the time this catalog was printed, this product was not yet released for sale. Please contact the local HP Field Sales Office for more information. All specifications are subject to change.

HEWLETT PACKARD

Silicon Bipolar Monolithic Dual Conversion Vector Modulator with Phase Shifter

Technical Data

HPMX-2004

Features

- **On Board Active Digital Phase Shifter**
- **I/Q Bandwidth > 10 MHz**
- **Wide Bandwidth:**
  1st LO, 40-240 MHz
  2nd LO, 250-2250 MHz
  RF Output, 250-2000 MHz
- **On Chip Mixer for Dual Conversion**
- **Low Power Dissipation:**
  Standby, 120 µW
  Operating, 150 mW
- **Low Cost Plastic Surface Mount Package**

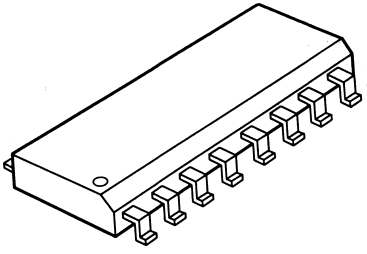
Applications

- **Digital Cellular and Cordless Telephones such as NADC, JDC, GSM, PCN, and PHP**
- **Wireless LANs**
- **RF Data Links**
- **Vector Generators**

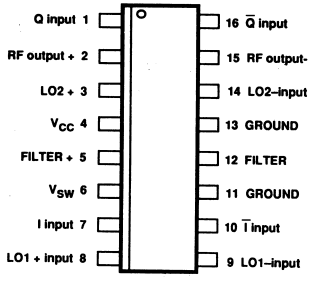
Description

The HPMX-2004 is a silicon monolithic, dual conversion, quadrature modulator in a plastic, surface mount SO- 16 package.

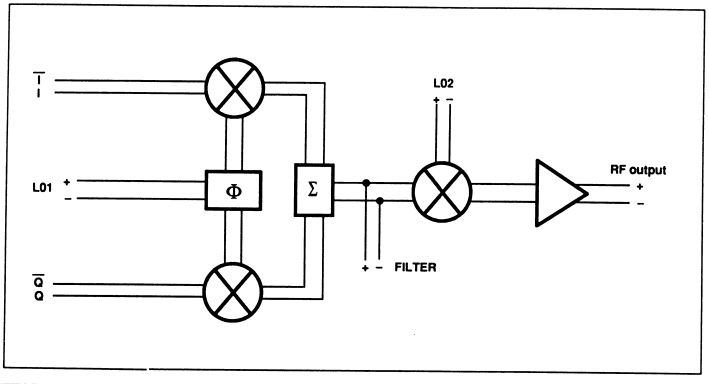
Plastic S0-16 Package



HPMX-2004 Pinout



Functional Block Diagram



At the time this catalog was printed, this product was not yet released for sale. Please contact the local HP Field Sales Office for more information. All specifications are subject to change.

The dual conversion architecture and wide band nature of the Gilbert cells allows operation over a broad range of frequencies with little change in performance. A low gain output stage is used to achieve a wide bandwidth with 50 Ω match.

All signal inputs and outputs except V_{SW} are differentially balanced with RF ports matched to 50 Ω, and can be used balanced or unbalanced in any combination. Double balanced mixers are used to improve port to port isolation and reduce harmonic content in the output signal.

I and Q inputs are internally biased and have high input impedances to allow them to be driven from high impedance sources. either AC or DC coupled.

All on-chip circuitry is biased by a set of current sources controlled by the standby circuit. When activated, the standby circuit turns all the current sources off, reducing current drain to only 25 μA, the current required by the standby circuit alone.

This device is manufactured using Hewlett-Packard's 13 GHz f_T, 25 GHz f_{MAX} silicon bipolar integrated circuit process.

HPMX-2004 Absolute Maximum Ratings, T_A = 25°C*

Symbol	Parameter	Units	HPMX-2004
V_{CC}	Device Voltage, T_{case} = 25°C	Volts	6
V_{in} I/Q	I/Q Input Voltage	V_{p-p}	4
P_{in} LO	Local Oscillator Input Power	dBm	+10
V_{sw}	Standby Mode Switch Voltage	Volts	6
T_{op}	Ambient Operating Temperature	°C	-55 to +85
T_{stg}	Storage Temperature	°C	-55 to +150

*Operation in excess of any one of these conditions may result in permanent damage to this device. Care should be taken to prevent electrostatic discharge (ESD) that could permanently damage the device. This device has a Class 1 ESD rating.

Thermal Resistance: HPMX-2004 Thermal Resistance, Junction to Ambient, Θ_{ja} = 160°C/W

Notes:
1. Junction temperature can be determined by $T_j = (P_d \times \Theta_{ja}) + T_a$.
2. Maximum soldering temperature is 260°C for 5 seconds.

At the time this catalog was printed, this product was not yet released for sale. Please contact the local HP Field Sales Office for more information. All specifications are subject to change.

Electrical Parameters, T_A = 25°C, V_{CC} = 5 V

Symbol	Parameters/Test Conditions: LO1 = - 7 dBm @ 100 MHz, LO2 = -3 dBm @ 900 MHz, I/Q = 1.2 V_{p-p} @ 70 kHz, Z_o = 50 Ω, Test Circuit #1 (unless otherwise noted)	Units	Typical
I_{cc}	Power Supply Current	mA	30
I_{cc}	Standby Current, V_{sw} = +3.0 V	mA	21
	I/Q Input Impedance (Internally Biased with High Impedance Source to ≈ 2.5 VDC)	Ohms pF	8,000 1.0
	LO1 Operating Frequency Range	MHz	40 to 240
	LO2 Operating Frequency Range	MHz	250 to 2,000
	I/Q Modulating Frequency Range	MHz	DC to 10
	RF Output Frequency Range	MHz	250 to 2,000
T_{on}	Turn-On Time, to ± 0.5 dB of Final Output Power (Test Circuit #4)	µS	1.2
T_{off}	Turn-Off Time, to Output Power Below Noise Floor (Test Circuit #4)	µS	0.4

800 MHz RF Electrical Parameters, T_A = 25°C, V_{CC} = 5 V

Symbol	Parameters/Test Conditions: LO1 = - 7 dBm @ 100 MHz, LO2 = -3 dBm @ 900 MHz, I/Q = 1.2 V_{p-p} differential @ 70 kHz, Z_o = 50 Ω, Test Circuit #2 (unless otherwise noted)		Units	Typical
P_{out}	RF Output Power @ 800 MHz		dBm	-13.0
	RF Output Power Flatness, 800-1000 MHz		dB	± 0.6
P_{1dB}	Power Output at 1 dB Compression Point (I/Q voltage swept)		dBm	-12.5
LO1 P_{in}	LO1 Power Input for Phase Shift of 90° ± 3°		dBm	-7
Noise	Output Noise Floor		dBm/Hz	-136
	Modulation Product Power Levels in dB Relative to the Desired Sideband Using Filter at 1st Carrier Output	Residual LO (800 MHz) Undesired Sideband (799.93 MHz) 2nd Harmonic (800 ± 0.140 MHz) 3rd Harmonic (800 ± 0.210 MHz) 5th Harmonic (800 ± 0.350 MHz)	dBc dBc dBc dBc dBc	-34 -41 -49 -53 -72
	LO1 Input SWR		VSWR	2.0:1
	LO2 Input SWR		VSWR	1.2:1
	RF Output SWR (operating)		VSWR	1.5:1
A_i	I/Q Amp. Imbalance (derived from undesired sideband data)		dB	± 0.15
P_i	I/Q Phase Imbalance (derived from undesired sideband data)		Deg.	± 0.97

At the time this catalog was printed, this product was not yet released for sale. Please contact the local HP Field Sales Office for more information. All specifications are subject to change.

HEWLETT PACKARD

Silicon Bipolar MMIC 100 MHz Vector Modulator

Technical Data

HPMX-2005

Features

- 50 - 200 MHz Output Frequency Range
- -6 dBm Peak Output Power
- Internal 90° Phase Shifter
- 5 Volt, 15 mA Bias
- SO-16 Surface Mount Package

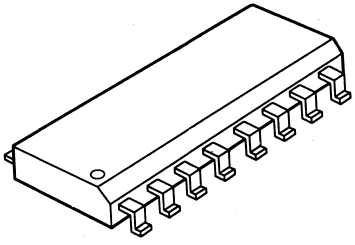
Applications

- Modulator for Dual Conversion Telephone Handsets, Including JDC, NADC, and PCS.
- Modulator for Dual Conversion ISM Band Spread-Spectrum Transmitters and LANs
- Direct Modulator for Digital Transmitters in the 50 - 200 MHz Frequency Range.

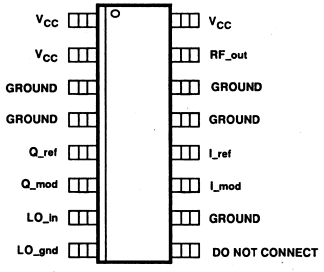
Description

Hewlett-Packard's HPMX-2005 is a Silicon RFIC Vector Modulator housed in an SO-16 surface mount plastic package. This IC can be used as a direct modulator with an output in the frequency range of 50 to 200 MHz, or, in combination with an up-converting mixer, as a dual

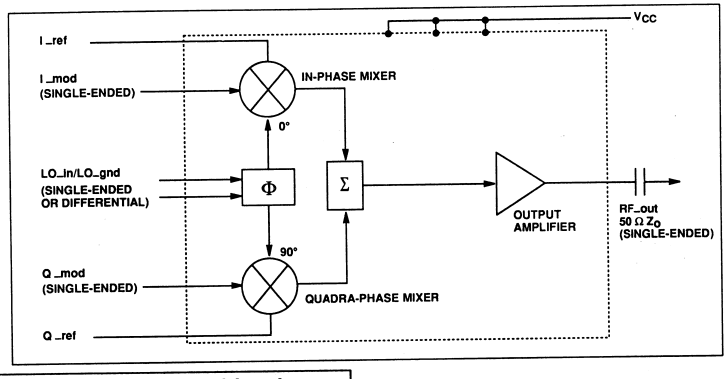
Plastic S0-16 Package



Pin Configuration



Functional Block Diagram



At the time this catalog was printed, this product was not yet released for sale. Please contact the local HP Field Sales Office for more information. All specifications are subject to change.

conversion modulator operating to higher frequencies. The IC contains two matched Gilbert cell mixers, an RC phase shifter, summer, and output amplifier.

The output (RF_out) is capable of directly driving a 50 Ω load, and requires only a 50 Ω characteristic impedance transmission line and DC blocking capacitor for interfacing. Output configuration is for single-ended (unbalanced) use.

For drive from a single-ended LO, the LO in pin is AC coupled to a -12 dBm source using 50 Ω transmission line, with the LO_gnd pin AC bypassed to ground. Alternatively, a differential (balanced) signal may be AC coupled across the LO_in and LO_gnd pins.

A DC reference voltage, typically 2.5 V ± 0.5 V, must be applied to both the in-phase (I) and quadra-phase (Q) reference pins, V_{I_ref} and V_{Q_ref}. These two pins may be shorted together for drive from a single reference source. The V_{I_mod} and V_{Q_mod} pins should be DC coupled to single-ended voltage inputs supplying the I and Q data. For the HPMX-2005, the I and Q data should swing ±0.75 V about the reference voltage.

Device power is provided by three V_{CC} pins, all of which should be directly coupled to the V_{CC} supply (5 V) with appropriate AC bypassing near the pins (1000 pF typ.).

This device is well suited for use in dual conversion portable and mobile telephone handsets for cellular systems such as North American Digital Cellular, GSM, and Japan Digital Cellular or Personal Communications Systems applications such as DCT-1800 and "handyphones". It can also be used in digital transmitters operating in the 900 and 2.4 GHz ISM (Industrial-Scientific-Medical) bands, including use in Local Area Networks (LANs).

The HPMX-2005 is fabricated with Hewlett-Packard's 25 GHz ISOSAT-II process, which combines stepper lithography, ion-implantation, self-alignment techniques, and gold metallization to produce RFICs with superior performance, uniformity, and reliability.

HPMX-2005 Absolute Maximum Ratings, T_A = 25°C*

Symbol	Parameter	Units	Absolute Maximum
P_{diss}	Power Dissipation[1,2]	mW	300
LO_{in}	LO Input Power	dBm	0
V_{CC}	Supply Voltage	V	8
Δ_I, Δ_Q	Swing of V_{I_mod} about V_{I_ref} or V_{Q_mod} about V_{Q_ref}	V V_{p-p}	2.5 5
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to +150

*Operation of this device above any one of these parameters may cause permanent damage.

Thermal Resistance: HPMX-2005 Thermal Resistance[1]:
Q_{jc} =125°C/W

Notes:
1. T_{case} = 25°C (T_{case} is defined to be the temperature at the ends of pin 3 where it contacts the circuit board).
2. Derate at 8 mW/°C for T_C > 112°C.

At the time this catalog was printed, this product was not yet released for sale. Please contact the local HP Field Sales Office for more information. All specifications are subject to change.

HPMX-2005 Electrical Specifications, T_A = 25°C, Z_o = 50 Ω

V_{CC} = 5 V, LO = -12 dBm @ 100 MHz, $V_{I_ref} = V_{Q_ref}$ = 2.5 V (unless otherwise noted).

Symbol	Parameters	Test Conditions	Units	Typical
P_{out}	Output Power	$V_{I_mod} = V_{Q_mod}$ = 3.25 V	dBm	-6
P_{1dB}	Power at 1 dB Compression		dBm	-5
VSWR	Output VSWR (50 Ω)			2.7:1
	Input LO VSWR (50 Ω)			1.3:1
LO_{leak}	LO Leakage at Output	$V_{I_mod} = V_{Q_mod}$ = 2.5 V	dBm	-45
	Unwanted Sideband Signal	$V_{I_mod} = V_{I_ref}$ +0.75 V sin(ω_nt) $V_{Q_mod} = V_{Q_ref}$ +0.75 V cos(ω_nt) ω_n = 30 kHz	dBm	-45
Noise	Output Noise Floor	$V_{I_mod} = V_{Q_mod}$ = 3.25 V	dBm/Hz	-132
R_{in}	Input Resistance (I_mod to I_ref or Q_mod to Q_ref)		Ω	10 k
A_i	RMS Amplitude Imbalance	SQR($V_I^2 + V_Q^2$) = 0.75 V[1]	dB	0.12
P_i	RMS Phase Imbalance	SQR($V_I^2 + V_Q^2$) = 0.75 V[1]	deg	0.8
I_d	Device Current		mA	15

Note:
1. $V_I = V_{I_mod} - V_{I_ref}$ and $V_Q = V_{Q_mod} - V_{Q_ref}$.

At the time this catalog was printed, this product was not yet released for sale. Please contact the local HP Field Sales Office for more information. All specifications are subject to change.

HEWLETT PACKARD

Silicon Bipolar MMIC 900 MHz Driver Amplifier

Technical Data

HPMX-3002

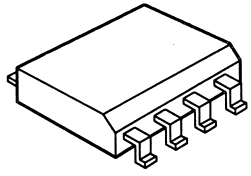
Features

- MMIC Power Amplifier for Cellular and Spread Spectrum Applications
- Frequency Range: 150 - 960 MHz
- Output Power: +22 dBm Typ. $P_{1\,dB}$
- Power Control Range: 50 dB Typ.
- 5 V, 170 mA Operation
- S-08 Surface Mount Package with Improved Heatsinking

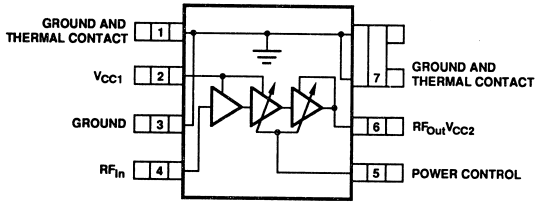
Applications

- Driver for Cellular Handsets, Including GSM, JDC, NADC, and AMPS
- Driver or Output Stage for 900 MHz ISM Band Transmitters

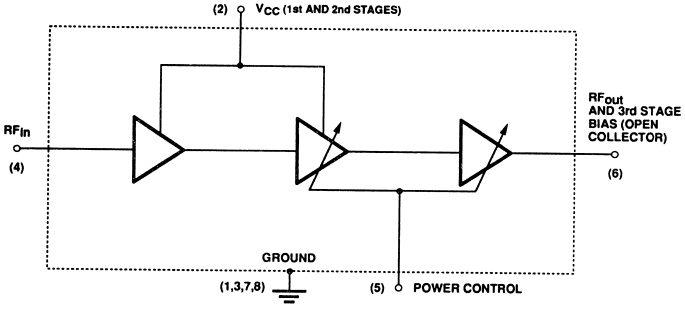
Plastic SO-8 Package



Pin Configuration



Functional Block Diagram



At the time this catalog was printed, this product was not yet released for sale. Please contact the local HP Field Sales Office for more information. All specifications are subject to change.

Description

Hewlett-Packard's HPMX-3002 is a silicon microwave monolithic integrated circuit driver amplifier housed in a SO-8 surface mount plastic package. It is designed for operation in the 150 - 960 MHz frequency range, and is capable of producing +23 dBm of output power, with 30 dB of gain and a 50 dB power control range. The amplifier has a well-matched input, and an open collector output which provides good linearity and efficiency and is easy to externally match to 50 Ω for optimal power output.

This device is well suited as a driver amplifier for low cost portable and mobile telephone systems such as AMPS, North American Digital Cellular, GSM (Global System for Mobile communications), Japan Digital Cellular, or as the output stage for other low cost applications such as 900 MHz ISM band spread-spectrum.

The HPMX-3002 is fabricated with Hewlett-Packard's 25 GHz ISOSAT-II process, which combines stepper lithography, ion-implantation, self-alignment techniques, and gold metallization to produce RFICs with superior performance, uniformity and reliability .

Absolute Maximum Ratings, HPMX-3002

Symbol	Parameter	Units	Absolute Maximum[1]
P_{diss}	Power Dissipation[2,3]	W	1.5
P_{in}	Input Power	dBm	+5
$V_{CC\,1}$	Supply Voltage	V	8
$V_{CC\,2}$	Supply Voltage, 3rd Stage	V	12
V_{cont}	Control Voltage	V	5
T_j	Junction Temperature	°C	200
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]: Θ_{jc} =60°C/W

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. $T_{pin\,7}$ = 25°C (T_{case} is defined to be the temperature at the ends of pin 7 where it contacts the circuit board).
3. Derate at 16.7 mW/°C for T_C > 110°C.

HPMX-3002 Electrical Specifications, $T_{A\,(temperature\ of\ leads\ 7,8)}$ = 35°C, Z_O = 50 Ω

V_{CC1} = 4.5 V, V_{CC2} = 6 V, P_{in} = -6 dBm @ 900 MHz, output matched for maximum power, I_{VCC1} = 60 mA nom., I_{VCC2} = 90 mA nom. set by $V_{control}$ (pin 5) = 2.2 V (unless otherwise noted).

Symbol	Parameters	Test Conditions	Units	Typical
P_{out}	Output Power	P_{in} = -6 dBm, f = 900 MHz	dBm	23
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	P_{in} set for $P_{out} = P_{1\,dB}$, f = 900 MHz	dBm	22
PCR	Power Control Range	f = 900 MHz, $V_{control}$ = 0 to 2.2 V	dBc	50
G_{ss}	Small Signal Gain	f = 900 MHz, P_{in} =-18 dBm	dB	32
IP_3	Third Order Intercept Point	f_1= 900 MHz, f_2 = 901 MHz P_{out}/tone = 12 dBm	dBm	29
IP_5	Fifth Order Intercept Point	f_1= 900 MHz, f_2 = 901 MHz P_{out}/tone = 12 dBm	dBm	26
NF	Noise Figure		dB	9.5
RL_{in}	Input Return Loss		dB	12
I_d	Supply Current (V_{CC1} + V_{CC2})	$V_{CC\,1}$=4.5 V, $V_{CC\,2}$ =6 V	mA	160
$I_{control}$	Control Current	$V_{control}$ = 0 to 2.2 V	mA	2.5

At the time this catalog was printed, this product was not yet released for sale. Please contact the local HP Field Sales Office for more information. All specifications are subject to change.

Typical Amplifier Performance

T_A = 25°C, Z_O = 50 Ω
P_{in} = -6 dBm @ 900 MHz
V_{CC1} = 4.5 V, V_{CC2} = 6 V,
$V_{control}$ = 2.2 V
I_{out} = 155 mA nom.
Output matched for max.
P_{out} (unless otherwise noted)

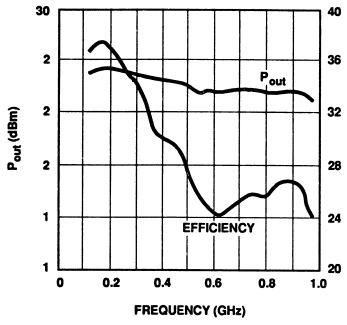


Figure 1. HPMX-3002 Wideband Output Power and Efficiency vs. Frequency, V_{CC1} = 4.5 V and V_{CC2} = 7.2 V.

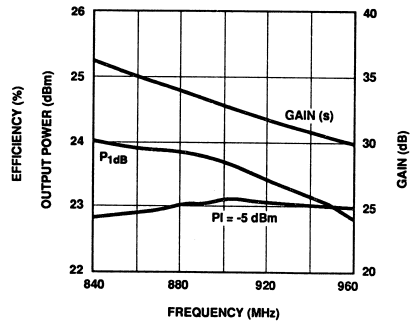


Figure 2. HPMX-3002 Output Power and Small Signal Gain vs. Frequency.

At the time this catalog was printed, this product was not yet released for sale. Please contact the local HP Field Sales Office for more information. All specifications are subject to change.

HEWLETT PACKARD

IAM-81000
MagIC™ Silicon Bipolar MMIC 5 GHz Active Double Balanced Mixer/IF Amplifer Chip

Features

- **8 dB RF-IF Conversion Gain From 0.05 to 5 GHz**
- **IF Output From DC to 1 GHz with Gain**
- **Low Power Dissipation: 60 mW at V_{CC} = 5 V typ.**
- **Single Polarity Bias Supply: V_{CC} = 4 to 8 V**
- **Load-insensitive Performance**
- **Conversion Gain Flat Over Temperature**
- **Low LO Power Requirements: -5 dBm typical**
- **Low RF to IF Feedthrough, Low LO Leakage**

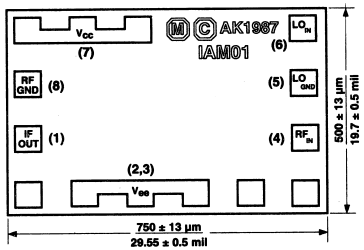
Description

The IAM-81000 is a complete low power consumption, double balanced active mixer chip. It is designed for narrow or wide bandwidth commercial, industrial, and military applications. It has RF inputs to 5 GHz and IF outputs to 1 GHz with conversion gain or above 1 GHz with conversion loss. Low frequency operation is determined by values of the external capacitors used. IAM-81000 mixers are particularly well suited for applications that require load insensitive conversion gain and good spurious signal suppression with minimum LO and bias power consumption. Typical applications include frequency down conversion, modulation, demodulation and frequency doubling, GPS satellite navigation, mobile radio, and battery powered communications receivers.

The IAM series of Gilbert multiplier based mixers is fabricated using HP's 10 GHz, f_T, 25 GHz f_{MAX} ISOSAT™-I silicon bipolar process. This process uses nitride self alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide inter metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

Recommended die attach procedure is either conductive epoxy or eutectic die attach with gold preform at 400°C. Wedge or ball bonding using 0.7 mil goldwire may be used.[1]

IAM-81000 Chip Outline



Electrical specifications and associated graphs provided in this data sheet are obtained by packaging and testing IAM-81000 dice in a 180 mil package with three internal 105 pF capacitors.

Operating Frequency Range

The lower frequency limit of the IAM-81000 mixer chip at which the RF and LO ports will work is set by the AC grounding provided to these ports external to the chip. MOS capacitors are used in packaged IAM mixers to provide these grounds; package dimensions limit the values of these capacitors from 50 to 200 pF, which sets a lower frequency of operation for the RF and LO ports of approximately 50 MHz. The low frequency limit of operation for the IF is set solely by the value of the DC blocking capacitor and the lead impedance (50 Ω) at this port. Low frequency cutoff can be decreased by using high value capacitors.

Differential Use

IAM-81000 can be driven in differential mode at the RF and/or LO port. This is done by using an external balun at the port and omitting AC bypassing capacitors. To maintain DC level across the port, input blocking capacitors are used. Differential operation of either RF or LO port improves mixer LO to IF isolation.

Electrical Specifications[2,3], T_A = 25°C

Symbol	Parameters and Test Conditions:[4] V_{cc} = 5 V, V_{ee} = 0 V, Z_L = 50 Ω		Units	Min.	Typ.	Max.
G_C	Conversion Gain	RF = 2 GHz, LO = 1.75 GHz	dB		8.5	
$F_{3\,dB}RF$	RF Bandwidth (G_C 3 dB Down)	IF = 250 MHz	GHz		4.5	
$F_{3\,dB}IF$	IF Bandwidth (G_C 3 dB Down)	LO = 2 GHz	GHz		0.6	
$P_{1\,dB}$	IF Output Power at 1 dB Gain Compression	RF=2 GHz, LO =1.75 GHz	dBm		-6	
IP_3	IF Output Third Order Intercept Point	RF = 2 GHz, LO = 1.75 GHz	dBm		3	
NF	SSB Noise Figure	RF = 2 GHz, LO = 1.75 GHz	dB		15	
VSWR	RF Port VSWR	f = 0.05 to 5 GHz			1.5:1	
	LO Port VSWR	f = 0.05 to 5 GHz			1.5:1	
	IF Port VSWR	f < 1 GHz			1.5:1	
RF_{if}	RF Feedthrough at IF Port	RF = 2 GHz, LO=1.75 GHz	dBc		-25	
LO_{if}	LO Leakage at IF Port	LO = 1.75 GHz	dBm		-25	
LO_{rf}	LO Leakage at RF Port	LO = 1.75 GHz	dBm		-35	
I_{CC}	Supply Current		mA	10	12.5	16

NOTES:
1. See Application Note, "AN-005: Transistor Chip Use" for additional information.
2. The recommended operating voltage range for this device is 4 to 8 V. Typical performance as function of voltage is on the following page.
3. Tested in a 180 mil package with three interal 150 pF capacitors.
4. RF performance of the chip is determined by packaging and testing 10 devices per wafer.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	10 V
Power Dissipation[2, 3]	300 mW
RF Input Power	+14 dBm
LO Input Power	+14 dBm
Junction Temperature	200°C
Storage Temperature	-65 to 200°C

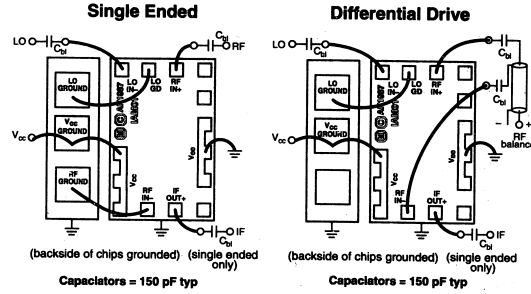
Thermal Resistance: θ_{jc} = 25°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{mounting\ surface}$ (T_{ms}) = 25°C
3. Derate at 40 mW/°C for T_{ms} > 182°C

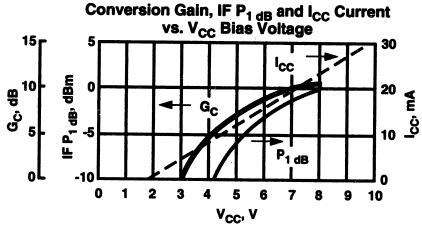
Part Number Ordering Information

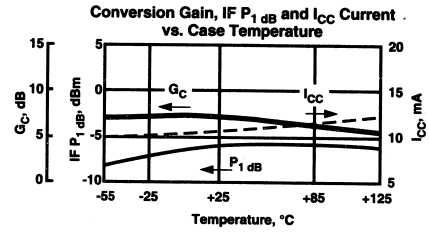
Part Number	Devices Per Tray
IAM-81000-GP2	10
IAM-81000-GP4	100
IAM-81000-GP6	up to 300

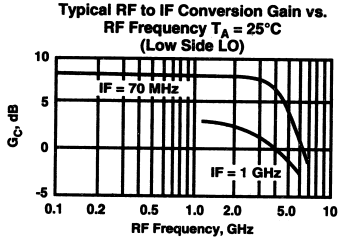
Bonding Diagrams

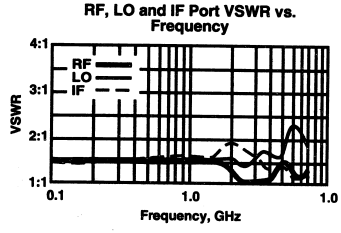


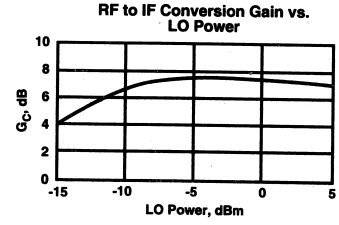
Typical Performance, T_A = 25°C, V_{CC} = 5 V
RF: -20 dBm at 2 GHz, LO: -5 dBm at 1.75 GHz
(Unless otherwise noted)

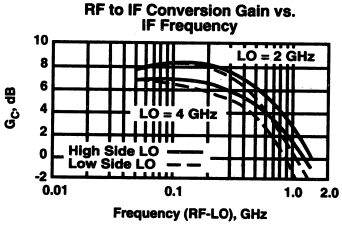


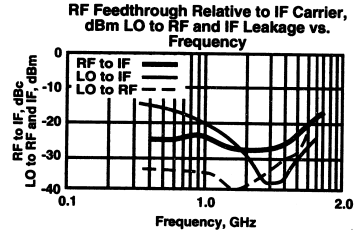












Harmonic Intermodulation Suppression (dB Below Desired Output)
RF at 1 GHz, LO at 0.752 GHz, IF at 0.248 GHz

Harmonic LO Order	0	1	2	3	4	5
0	—	21	35	>75	>75	>75
1	12	0	48	48	>75	>75
2	13	41	39	71	>75	>75
3	36	28	53	57	>75	>75
4	27	49	49	72	>75	>75
5	45	35	63	62	>75	>75

Harmonic RF Order
Xmn = Plf-P(m*rf-n*lo)

HEWLETT PACKARD

IAM-81008
MagIC™ Silicon Bipolar MMIC 5 GHz Active Double Balanced Mixer/IF Amp

Features

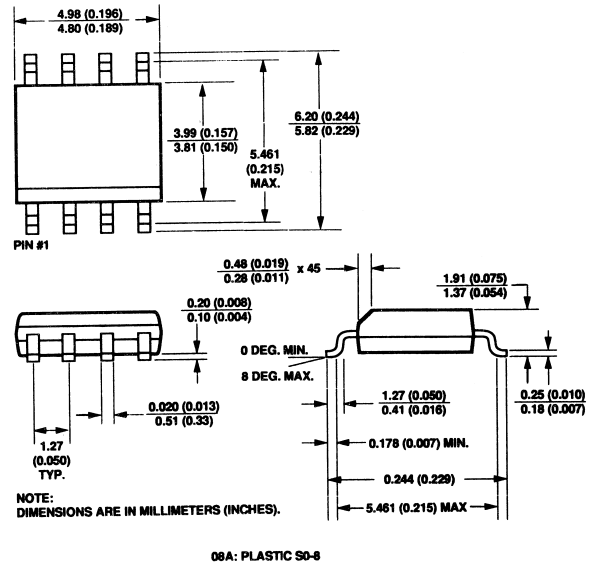
- **RF-IF Conversion Gain From 0.05 - 5 GHz**
- **IF Conversion Gain From DC to 1 GHz**
- **Low Power Dissipation: 65 mW at V_{CC} = 5 V typ.**
- **Single Polarity Bias Supply: V_{CC} = 4 to 8 V**
- **Load-insensitive Performance**
- **Conversion Gain Flat Over Temperature**
- **Low LO Power Requirements: -5 dBm typical**
- **Low Cost Plastic Surface Mount Package**

Description

The IAM-81008 is a complete low power-consumption double-balanced active mixer housed in a miniature low cost plastic surface mount package. It is designed for narrow or wide bandwidth commercial and industrial applications having RF inputs up to 5 GHz. Operation at RF and LO frequencies less than 50 MHz can be achieved using optional external capacitors to ground. The IAM-81008 is particularly well suited for applications that require load-insensitive conversion and good spurious signal suppression with minimum LO and bias power consumption. Typical applications include frequency down conversion, modulation, demodulation and phase detection. Markets include fiber-optics, GPS satellite navigation, mobile radio, and battery powered communications receivers.

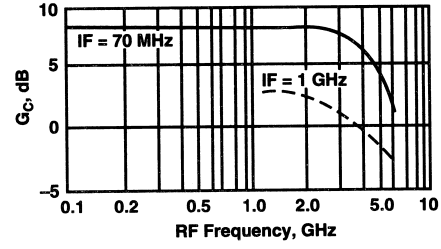
The IAM series of Gilbert multiplier-based frequency converters is fabricated using HP's 10 GHz, f_T, 25 GHz f_{MAX} ISOSAT™-I silicon bipolar process. This process uses nitride self alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

SO-8 Package



08A: PLASTIC SO-8

Typical RF to IF Conversion Gain vs. RF Frequency T_A = 25°C (Low Side LO)



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: V_{CC} = 5 V, Z_O = 50 Ω, LO = -5 dBm, RF = -20 dBm		Units	Min.	Typ.	Max.
G_C	Conversion Gain	RF = 2 GHz, LO = 1.75 GHz	dB	6.0	8.5	10
$f_{3\ dB}RF$	RF Bandwidth (G_C 3 dB Down)	IF = 250 MHz	GHz		3.5	
$f_{3\ dB}IF$	IF Bandwidth (G_C 3 dB Down)	LO = 2 GHz	GHz		0.6	
$P_{1\ dB}$	IF Output Power at 1 dB Gain Compression	RF = 2 GHz, LO = 1.75 GHz	dBm		-6	
IP_3	IF Output Third Order Intercept Point	RF = 2 GHz, LO = 1.75 GHz	dBm		3	
NF	SSB Noise Figure	RF = 2 GHz, LO = 1.75 GHz	dB		17	
VSWR	RF Port VSWR	f = 0.05 to 3.5 GHz			1.5:1	
	LO Port VSWR	f = 0.05 to 3.5 GHz			2.0:1	
	IF Port VSWR	f < 1 GHz			1.5:1	
RF_{if}	RF Feedthrough at IF Port	RF = 2 GHz, LO = 1.75 GHz	dBc		-25	
LO_{if}	LO Leakage at IF Port	LO = 1.75 GHz	dBm		-25	
LO_{rf}	LO Leakage at RF Port	LO = 1.75 GHz	dBm		-30	
I_{CC}	Supply Current		mA	10	13	16

NOTES: 1. The recommended operating voltage range for this device is 4 to 8 V. Typical performance as a function of voltage is on the following page.

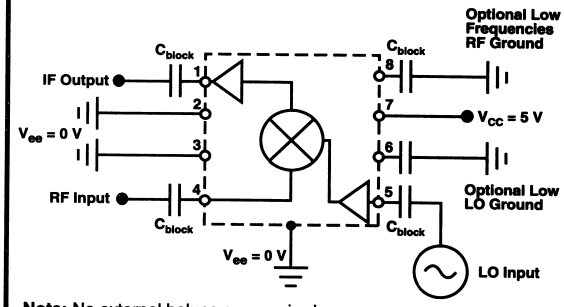
Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	10V
Power Dissipation[2, 3]	300 mW
RF Input Power	+14 dBm
LO Input Power	+14 dBm
Junction Temperature	150°C
Storage Temperature	-65 to 150°C

Thermal Resistance[2]: θ_{jc} = 225°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 4.4 mW/°C for T_c > 82°C.

Typical Biasing Configuration and Functional Block Diagram



Note: No external baluns are required.

Typical Performance, T_A = 25°C, V_{CC} = 5 V, RF: -20 dBm at 2 GHz, LO: -5 dBm at 1.75 GHz

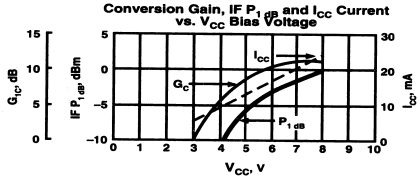
(Unless otherwise noted)

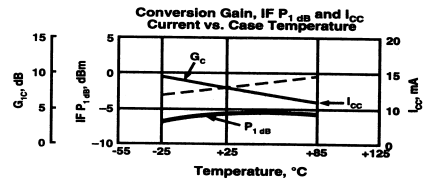
Small Graph Guide

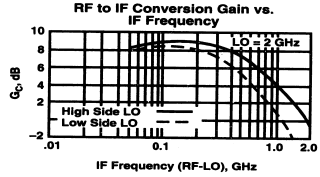
Part Number Ordering Information

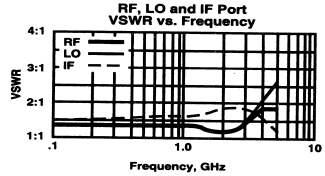
Part Number	Devices Per Reel	Reel Size
IAM-81008-TR1	1000	7"
IAM-81008-TR2	4000	13"

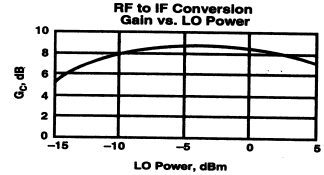
For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

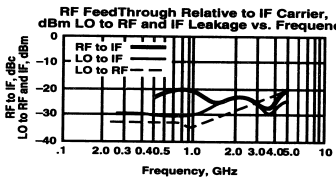












Harmonic Intermodulation Suppression (dB Below Desired Output)
RF at 1 GHz, LO at 0.752 GHz, IF at 0.248 GHz

Harmonic LO Order	0	1	2	3	4	5
0	–	21	35	74	>75	>75
1	18	0	45	48	>75	>75
2	16	35	42	72	>75	>75
3	42	20	44	59	>75	>75
4	29	44	52	64	>75	>75
5	45	36	57	64	>75	>75

Harmonic RF Order
Xmn = Pif-P(m*rf-n*lo)

HEWLETT PACKARD

IAM-81018
Silicon Bipolar MMIC 5 GHz Active Double Balanced Mixer/IF Amp

Features

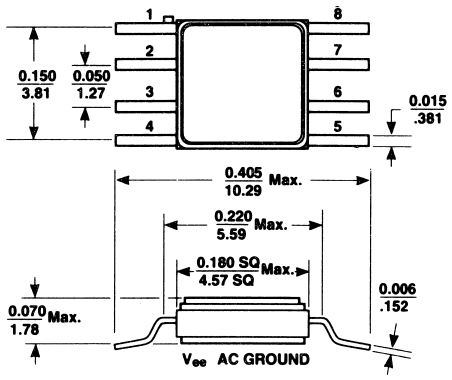
- 8 dB RF-IF Conversion Gain From 0.05 - 5 GHz
- IF Output From DC to 1 GHz
- Low Power Dissipation: 60 mW at V_{CC} = 5 V typ.
- Single Polarity Bias Supply: V_{CC} = 4 to 8 V
- Load-insensitive Performance
- Conversion Gain Flat Over Temperature
- Low LO Power Requirements: -5 dBm typical
- Low RF to IF Feedthrough, Low LO Leakage
- Hermetic Glass-Metal Surface Mount Package

Description

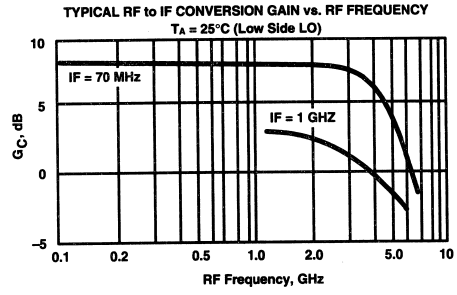
The IAM-81018 is a complete low-power-consumption double-balanced active mixer housed in a miniature glass-metal hermetic surface mount package. It is designed for narrow or wide bandwidth commercial, industrial and military applications having RF inputs up to 5 GHz and IF outputs from DC to 1 GHz. Operation at RF and LO frequencies less than 50 MHz can be achieved using optional external capacitors to ground. The IAM-81018 is particularly well suited for applications that require load-insensitive conversion gain and good spurious signal suppression with minimum LO and bias power consumption. Typical applications include frequency down conversion, modulation, demodulation and phase detection for fiber-optic, GPS satellite navigation, mobile radio, and battery powered communications receivers.

The IAM series of Gilbert multiplier-based frequency converters is fabricated using HP's 10 GHz, f_T, 25 GHz f_{MAX} ISOSAT™-I silicon bipolar process. This process uses nitride self alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

180 mil Package



Notes:
(unless otherwise specified)
1. Dimensions are $\frac{in}{mm}$
2. Tolerances
in .XXX = ± 0.005
mm .XX = ± 0.13



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: V_{CC} = 5 V, Z_O = 50 Ω, LO = -5 dBm, RF = -20 dBm		Units	Min.	Typ.	Max.
GC	Conversion Gain	RF = 2 GHz, LO = 1.75 GHz	dB	7.0	8.5	10
$f_{3\ dB}RF$	RF Bandwidth (GC 3 dB Down)	IF = 250 MHz	GHz		4.5	
$f_{3\ dB}IF$	IF Bandwidth (GC 3 dB Down)	LO = 2 GHz	GHz		0.6	
$P_{1\ dB}$	IF Output Power at 1 dB Gain Compression	RF = 2 GHz, LO = 1.75 GHz	dBm		-6	
IP_3	IF Output Third Order Intercept Point	RF = 2 GHz, LO = 1.75 GHz	dBm		3	
NF	SSB Noise Figure	RF = 2 GHz, LO = 1.75 GHz	dB		15	
VSWR	RF Port VSWR	f = 0.05 to 5 GHz			1.5:1	
	LO Port VSWR	f = 0.05 to 5 GHz			1.5:1	
	IF Port VSWR	f < 1 GHz			1.5:1	
RF_{if}	RF Feedthrough at IF Port	RF = 2 GHz, LO = 1.75 GHz	dBc		-25	
LO_{if}	LO Leakage at IF Port	LO = 1.75 GHz	dBm		-25	
LO_{rf}	LO Leakage at RF Port	LO = 1.75 GHz	dBm		-35	
I_{cc}	Supply Current		mA	10	12.5	16

Note: 1. The recommended operating voltage range for this device is 4 to 8 V. Typical performance as a function of voltage is on the following page.

IAM-81018 Silicon Bipolar MMIC 5 GHz Active Double Balanced Mixer/IF Amp

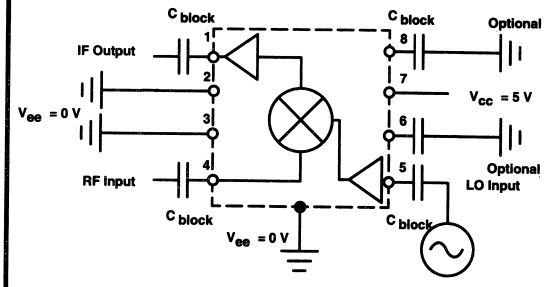
Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	10 V
Power Dissipation[2,3]	300 mW
RF Input Power	+14 dBm
LO Input Power	+14 dBm
Junction Temperature	200°C
Storage Temperature	−65°C to 200°C
Thermal Resistance[2,4]: θ_{jc} = 50°C/W	

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 20 mW/°C for T_C >185°C
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Typical Biasing Configuration and Functional Block Diagram

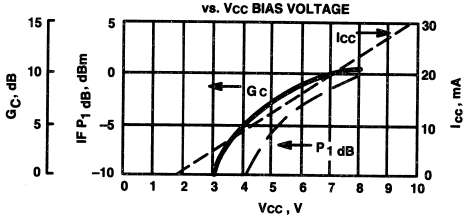


Note: No external BALUNs are required.

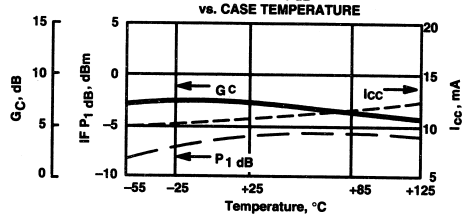
Typical Performance, T_A = 25°C, V_{CC} = 5 V RF: -20 dBm at 2 GHz, LO: -5 dBm at 1.75 GHz

(unless otherwise noted)

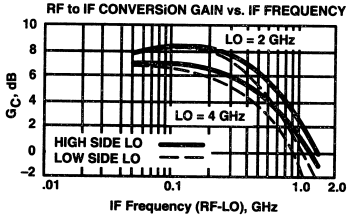
CONVERSION GAIN, IF $P_{1\ dB}$ and Icc CURRENT vs. Vcc BIAS VOLTAGE



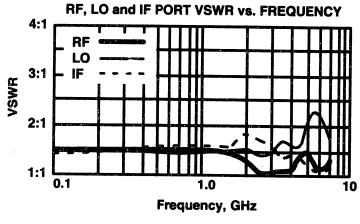
CONVERSION GAIN, IF $P_{1\ dB}$ and Icc CURRENT vs. CASE TEMPERATURE



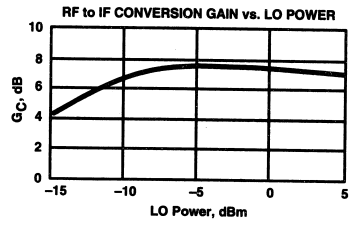
RF to IF CONVERSION GAIN vs. IF FREQUENCY



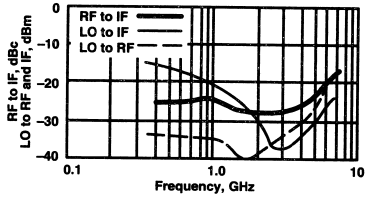
RF, LO and IF PORT VSWR vs. FREQUENCY



RF to IF CONVERSION GAIN vs. LO POWER



RF FEEDTHROUGH RELATIVE to IF CARRIER, dBm LO to RF and IF LEAKAGE vs. FREQUENCY



HARMONIC INTERMODULATION SUPPRESSION (dB BELOW DESIRED OUTPUT)
RF at 1 GHz, LO at 0.752 GHz, IF at 0.248 GHz

Harmonic LO Order	0	1	2	3	4	5
0	–	21	35	>75	>75	>75
1	12	0	48	48	>75	>75
2	13	41	39	71	>75	>75
3	36	28	53	57	>75	>75
4	27	49	49	72	>75	>75
5	45	35	63	62	>75	>75

Harmonic RF Order

Xmn = Pif-P(m*rf-n*lo)

HEWLETT PACKARD

Silicon Bipolar MMIC 5 GHz Active Double Balanced Mixer/IF Amp

Technical Data

IAM-82008

Features

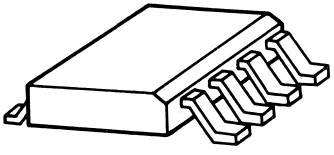
- **RF-IF Conversion Gain: 15 dB from 0.05-5 GHz**
- **IF Conversion Gain from DC to 2 GHz**
- **IF Output P_{1dB}: +8 dBm Typical**
- **Single Polarity Bias Supply: V_{CC} = 7 to 13 V**
- **Load Insensitive Performance**
- **Conversion Gain Flat over Temperature**

Description

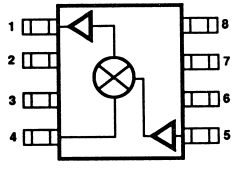
Hewlett-Packard's IAM-82008 is a complete moderate-power double-balanced active mixer housed in a miniature low cost surface mount package. It is designed for narrow or wide bandwidth commercial and industrial applications having RF inputs up to 5 GHz. Operation of RF and LO frequencies below 50 MHz can be achieved using optional external capacitors to ground. The IAM-82008 is particularly well suited for applications that require load-insensitive conversion gain and good spurious signal suppression and moderate dynamic range with low LO power. Typical applications include frequency down-conversion, up-conversion, modulation, demodulation, and phase detection. Markets include fiber-optics, GPS satellite navigation, mobile radio, and communications transmitters and receivers.

The IAM series of Gilbert multiplier-based frequency converters is fabricated using Hewlett Packard's 10 GHz f_T 25 GHz f_{MAX} ISOSAT™-1 silicon bipolar process. This process uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization, and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

Plastic SO-8 Package



Functional Block Diagram and Pin Configuration



Pin Description	
1 IF Output	8 RF Ground (optional)
2 V_{ee}, AC Ground	7 V_{CC}
3 V_{ee}, AC Ground Thermal Contact	6 LO Ground (optional)
4 RF Input	5 LO Input

Absolute Maximum Ratings[1] (T_A = 25°C)

Symbol	Parameter	Units	Value
V_d	Device Voltage	V	15
P_t	Total Device Dissipation[2]	mW	1200
$P_{in\ RF}$	RF Input Power	dBm	+14
$P_{in\ LO}$	LO Input Power	dBm	+14
T_j	Junction Temperature	°C	150
T_{stg}	Storage Temperature	°C	-65 to +150

Θ_{jc}	Thermal Resistance Junction to Case[3]	°C/W	92

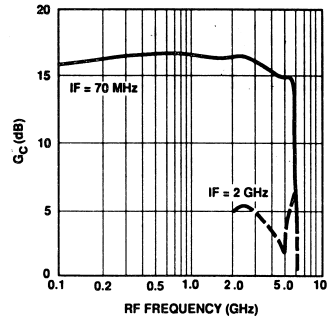


Figure 1. Typical RF to IF Conversion Gain vs. RF Frequency, T_A = 25°C, Low Side LO.

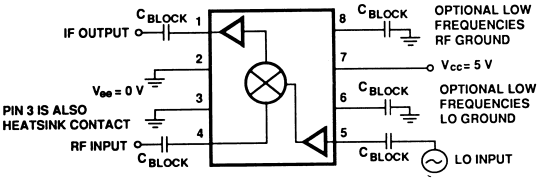
Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. Derate at 10.9 mW/°C for $T_{PIN\ 3}$ > 40°C.
3. T_j = 150°C.

Electrical Specifications

V_{CC} = 10 V, Z_O = 50 Ω, LO = 0 dBm, RF = -20 dBm, T_A = 25°C

Symbol	Parameter	Units	Minimum	Typical	Maximum
G_C	Conversion Gain, RF = 2 GHz, LO = 1.75 GHz	dB	13	15	17
$f_{3\ dB}$ RF	RF Bandwidth (G_C 3 dB down), IF = 250 MHz	GHz		5.5	
$f_{3\ dB}$ IF	IF Bandwidth (G_C 3 dB down), LO = 2 GHz	GHz		0.5	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression, RF = 2 GHz, LO = 1.75 GHz	dBm		8	
IP_3	Third Order Inpercept Point, RF = 2 GHz, LO = 1.75 GHz	dBm		18	
NF	SSB Noise Figure	dB		19	
VSWR	RF Port VSWR			1.5:1	
	LO Port VSWR			2.0:1	
	IF Port VSWR			2.5:1	
RF_{if}	RF Feedthrough at IF Port	dBc		-30	
LO_{if}	LO Leakage at IF Port	dBm		-15	
LO_{rf}	LO Leakage at RF Port	dBm		-22	
I_{CC}	Supply Current	mA	45	55	68

Notes:
1. The recommended operating voltage range for this device is 7 to 13 V. Typical performance as a function of voltage is shown on the following page.



Notes:
1. No external baluns are required.
2. Good heatsinking required on Pin 3 for specified performance.

Figure 2. IAM-82008 Typical Biasing Configuration.

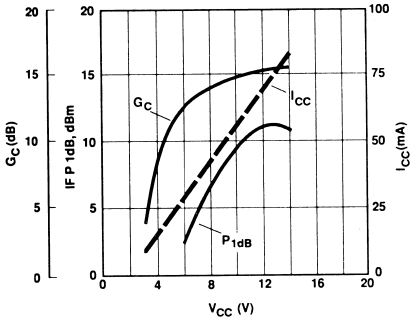


Figure 3. Typical Conversion Gain, IF $P_{1\,dB}$, and I_{CC} Current vs. V_{CC} Bias Voltage, T_A = 25°C, RF: -20 dBm at 2 GHz, LO: 0 dBm at 1.75 GHz.

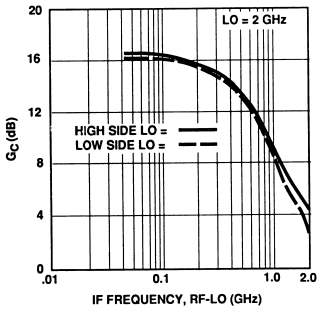


Figure 4. Typical RF to IF Conversion Gain vs. IF Frequency, T_A = 25°C, V_{CC} = 10 V, LO: 0 dBm at 2 GHz.

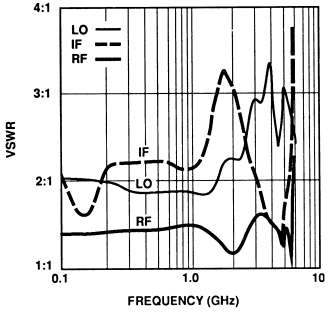


Figure 5. RF, LO, and IF Port VSWR vs. Frequency, T_A = 25°C, V_{CC} = 10 V.

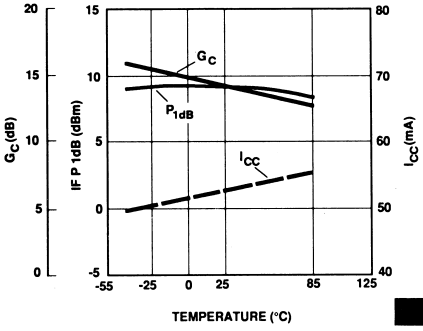


Figure 6. Typical Conversion Gain, IF $P_{1\,dB}$, and I_{CC} Current vs. Case Temperature, T_A = 25°C, V_{CC} = 10 V, RF: -20 dBm at 2 GHz, LO: 0 dBm at 1.75 GHz.

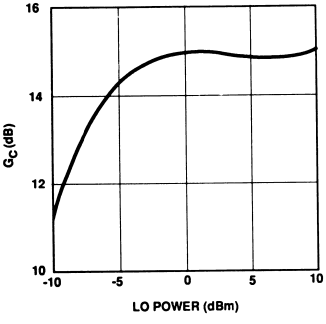


Figure 7. Typical RF to IF Conversion Gain vs. LO Power, T_A = 25°C, V_{CC} = 10 V, RF: -10 dBm at 2 GHz, LO: 0 dBm at 1.75 GHz.

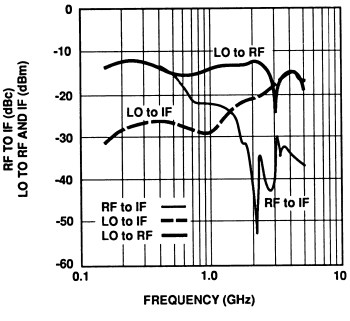


Figure 8. Typical RF Feedthrough Relative to IF Carrier, LO to RF and LO to IF Leakage vs. Frequency, T_A = 25°C, V_{CC} = 10 V, RF: -20 dBm at 2 GHz, LO: 0 dBm at 1.75 GHz.

HARMONIC LO ORDER

0	–	21	40	73	>75	>75
1	12	0	51	60	>75	>75
2	6	22	41	>75	>75	>75
3	24	18	40	74	>75	>75
4	22	33	52	75	>75	>75
5	41	36	55	>75	>75	>75
	0	1	2	3	4	5

HARMONIC RF ORDER

Xmn = Pif – P(m*rf-n*lo)

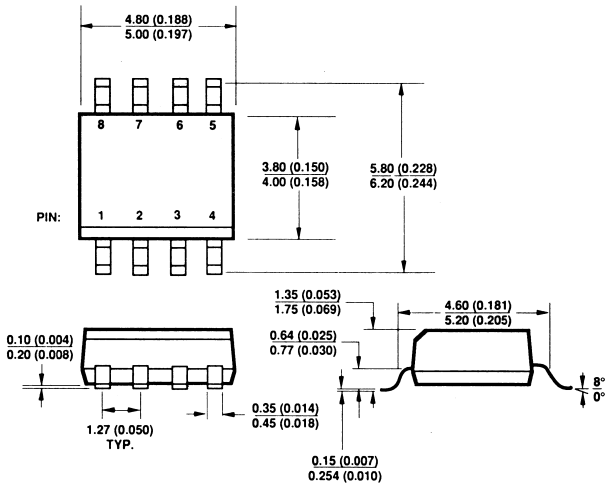
Figure 9. Harmonic Intermodulation Suppression (dB Below Desired Output) RF at 1 GHz, LO at 0.752 GHz, IF at 0.248 GHz.

Part Number Ordering Information

Part Number	Devices per Reel	Reel Size
IAM-82008-TR1	1000	7"
IAM-82008-TR2	4000	13"

Package Dimensions

SO-8 Plastic Package



DIMENSIONS IN MILLIMETERS AND (INCHES).

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

HEWLETT PACKARD

IAM-82018
Silicon Bipolar MMIC 5 GHz Active Double Balanced Mixer/IF Amp

Features

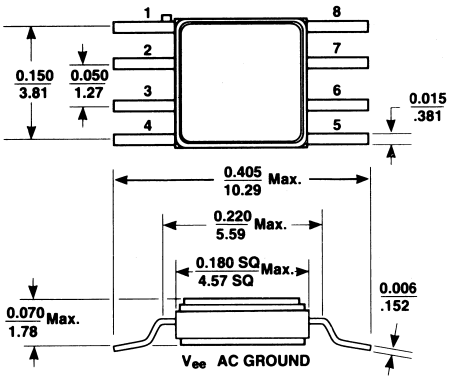
- **15 dB RF-IF Conversion Gain From 0.05 - 5 GHz**
- **IF Output From DC to 2 GHz**
- **IF Output P_{1dB} up to + 12 dBm**
- **Single Polarity Bias Supply: V_{cc} = 7 to 13 V**
- **Load-insensitive Performance**
- **Conversion Gain Flat Over Temperature**
- **Low LO Power Requirements: 0 dBm typical**
- **Low RF to IF Feedthrough, Low LO Leakage**
- **Hermetic Glass-Metal Surface Mount Package**

Description

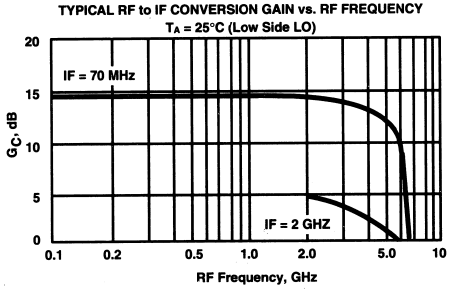
The IAM-82018 is a complete moderate-power double-balanced active mixer housed in a miniature glass-metal hermetic surface mount package. It is designed for narrow or wide bandwidth commercial, industrial and military applications having RF inputs up to 5 GHz and IF outputs from DC to 2 GHz. Operation at RF and LO frequencies less than 50 MHz can be achieved using optional external capacitors to ground. The IAM-82018 is particularly well suited for applications that require load-insensitive conversion gain and good spurious signal suppression and moderate dynamic range with minimum LO power. Typical applications include frequency downconversion, modulation, demodulation and phase detection for fiber-optic, GPS satellite navigation, mobile radio, and communications receivers.

The IAM series of Gilbert multiplier-based frequency converters is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX} ISOSAT™-I silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

180 mil Package



Notes:
(unless otherwise specified)
1. Dimensions are $\frac{in}{mm}$
2. Tolerances
in .XXX = ± 0.005
mm .XX = ± 0.13



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: V_{CC} = 10 V, Z_O = 50 Ω, LO = 0 dBm, RF = -20 dBm		Units	Min.	Typ.	Max.
G_C	Conversion Gain	RF = 2 GHz, LO = 1.75 GHz	dB	13.5	15	16.5
$f_{3\,dB}RF$	RF Bandwidth (G_C 3 dB Down)	IF = 250 MHz	GHz		5.5	
$f_{3\,dB}IF$	IF Bandwidth (G_C 3 dB Down)	LO = 2 GHz	GHz		0.6	
$P_{1\,dB}$	IF Output Power @ 1 dB Gain Compression	RF = 2 GHz, LO = 1.75 GHz	dBm		8	
IP_3	IF Output Third Order Intercept Point	RF = 2 GHz, LO = 1.75 GHz	dBm		18	
NF	SSB Noise Figure	RF = 2 GHz, LO = 1.75 GHz	dB		16	
VSWR	RF Port VSWR	f = 0.05 to 5 GHz			1.5:1	
	LO Port VSWR	f = 0.05 to 5 GHz			2:1	
	IF Port VSWR	f < 2 GHz			2.3:1	
RF_{if}	RF Feedthrough at IF Port	RF = 2 GHz, LO = 1.75 GHz	dBc		–30	
LO_{if}	LO Leakage at IF Port	LO = 1.75 GHz	dBm		–20	
LO_{rf}	LO Leakage at RF Port	LO = 1.75 GHz	dBm		–30	
I_{cc}	Supply Current		mA	40	55	65

Note: 1. The recommended operating voltage range for this device is 7 to 13 V. Typical performance as a function of voltage is on the following page.

Absolute Maximum Ratings

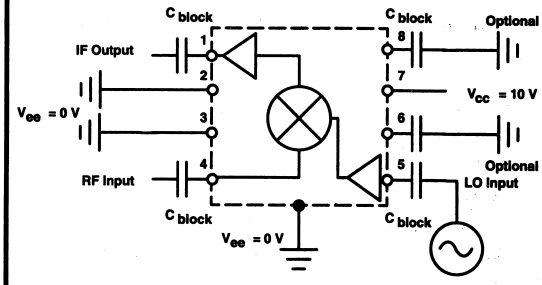
Parameter	Absolute Maximum[1]
Device Voltage	15 V
Power Dissipation[2,3]	1200 mW
RF Input Power	+14 dBm
LO Input Power	+14 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 45°C/W

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 22.2 mW/°C for T_C >146°C
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Typical Biasing Configuration and Functional Block Diagram

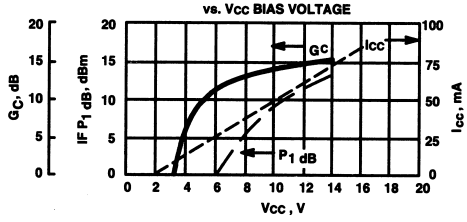


Note: No external BALUNs are required.

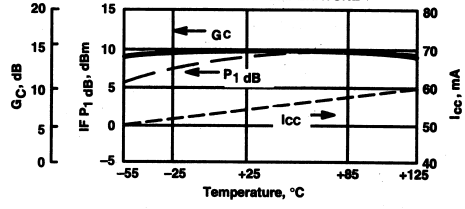
Typical Performance, T_A = 25°C, V_{CC} = 10 V
RF: -20 dBm at 2 GHz, LO: 0 dBm at 1.75 GHz

(unless otherwise noted)

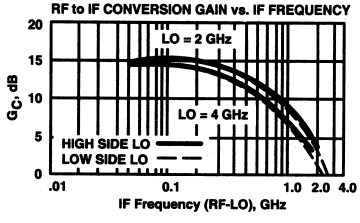
CONVERSION GAIN, IF $P_{1\ dB}$ and Icc CURRENT vs. V_{CC} BIAS VOLTAGE



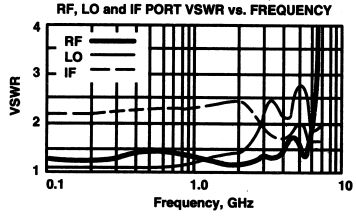
CONVERSION GAIN, IF $P_{1\ dB}$ and Icc CURRENT vs. CASE TEMPERATURE



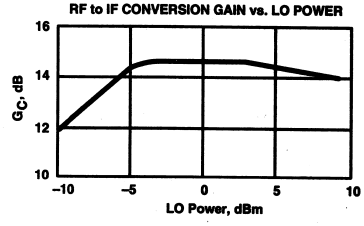
RF to IF CONVERSION GAIN vs. IF FREQUENCY



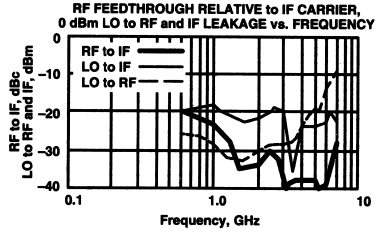
RF, LO and IF PORT VSWR vs. FREQUENCY



RF to IF CONVERSION GAIN vs. LO POWER



RF FEEDTHROUGH RELATIVE to IF CARRIER, 0 dBm LO to RF and IF LEAKAGE vs. FREQUENCY



HARMONIC INTERMODULATION SUPRESSION (dB BELOW DESIRED OUTPUT)
RF at 1 GHz, LO at 0.752 GHz, IF at 0.248 GHz

Harmonic LO Order	0	1	2	3	4	5
0	–	23	40	>75	>75	>75
1	12	0	52	60	>75	>75
2	6	35	43	>75	>75	>75
3	27	18	59	74	>75	>75
4	22	38	52	>75	>75	>75
5	41	36	73	74	>75	>75

Harmonic RF Order
Xmn = P/f-P(m*rf-n*lo)

HEWLETT PACKARD

Silicon Bipolar MMIC 3.5 and 5.5 GHz Divide-by-4 Static Prescalers

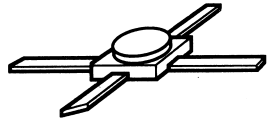
Technical Data

IFD-53010
IFD-53110

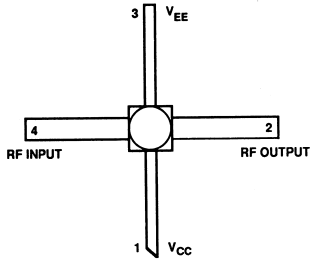
Features

- **Wide Operating Frequency Range:**
  IFD-53010: 0.15 to 5.5 GHz
  IFD-53110: 0.15 to 3.5 GHz
- **Low Phase Noise:**
  -143 dBc/Hz @ 1 kHz Offset
- **Output Power: -5 dBm typ.**
- **Single Supply Voltage**
  V_{cc} = 5 V or V_{ee} = -5 V
- **On-Chip Terminations Provide Good Input and Output VSWRs**
- **Hermetic Gold-Ceramic Surface Mount Package**

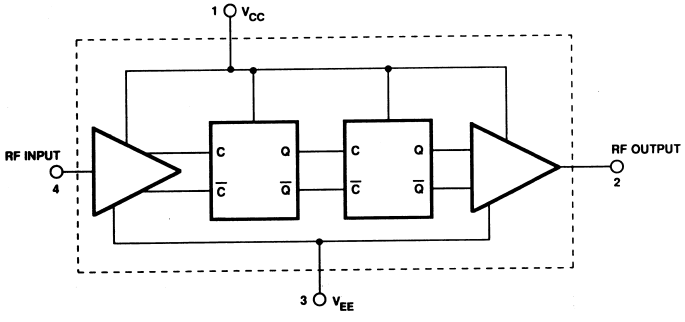
100 mil Stripline Package



Pin Configuration



Functional Block Diagram



Description

Hewlett-Packard's IFD-53010 and IFD-53110 are low phase noise silicon bipolar static digital frequency dividers using two scaled Emitter-Coupled-Logic (ECL) master-slave D flip-flops and buffer amplifiers. They are housed in hermetic high reliability surface mount packages suitable for commercial, industrial, and military applications. Typical applications include stabilized or digitally controlled local oscillators for GPS, SATCOM or military receivers, and frequency synthesizers and counters in instrumentation systems. The IFD-53110 is a lower cost selected version of the IFD-53010, and is distinguished by a reduced operating frequency range.

The IFD series of frequency dividers is fabricated using Hewlett-Packard's 18 GHz, f_t, ISOSAT™-2 silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion-implantation, gold metallization and polyimide intermetal dielectric and scratch protection to achieve excellent device uniformity, performance, and reliability.

Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{cc} - V_{ee}	Device Voltage	V	8
P_{diss}	Power Dissipation[2,3]	mW	650
P_{in}	RF Input Power	dBm	+15
T_j	Junction Temperature	°C	200
T_{STG}	Storage Temperature	°C	-65 to +200

Thermal Resistance[2]: Θ_{jc} = 107°C/W

Notes:
1, Operation of this device above any one of these parameters may cause permanent damage.
2. T_{case} = 25°C.
3. Derate at 9.3 mW/°C for $T_C \geq 130$°C.

Guaranteed Electrical Specifications, IFD-53010 and IFD-53110

T_A = 25°C, Z_O = 50 Ω, V_{cc} - V_{ee} = 5.0 V

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
F_{MAX}	IFD-53010: Maximum Clock Frequency P_{in} = -10 dBm (200 mVpp)	GHz	5.5	6.0	
F_{MAX}	IFD-53110: Maximum Clock Frequency P_{in} = -10 dBm (200 mVpp)	GHz	3.5	5.0	
I_{CC}	IFD-53010 and IFD-53110: Supply Current	mA	35	43	50

Typical Design Information, T_A = 25°C, Z_0 = 50 Ω, V_{cc} - V_{ee} = 5.0 V, P_{in} = -10 dBm.

All values apply to both IFD-53010 and IFD-53110. f_{test} is 5 GHz for IFD-53010 and 3 GHz for IFD-53110 (unless otherwise noted).

Symbol	Parameters and Test Conditions		Units	Value
F_{MIN}	Minimum Clock Frequency[1]		MHz	150
P_{in}	Input Sensitivity	$f = f_{test}$	dBm mVpp	-22 50
P_{out}	Output Power	f = 0.15 to f_{test}	dBm mVpp	-5 355
VSWR	Input VSWR Output VSWR	f = 0.15 to f_{test} f = 0.15 to f_{test}		2.0:1 2.5:1
PN	SSB Phase Noise	f = 3 GHz, 1 kHz offset f = 5 GHz, 1 kHz offset (IFD-53010 only)	dBc/Hz	-143 -138
T_r	Output Rise Time, 20% - 80%	$f = f_{test}$	psec	145
T_f	Output Fall Time, 20% - 80%	$f = f_{test}$	psec	85

Note:
1. Minimum clock frequency when driven from a sinusoidal input. Operation to lower frequencies is possible when using input signals with faster rise times, such as occurs in the case of a cascade of two or more IFDs.

Typical Performance, T_A = 25°C, Z_O = 50 Ω, V_{cc} - V_{ee} = 5.0 V

Graphs apply to both IFD-53010 and IFD-53110 (unless otherwise noted).

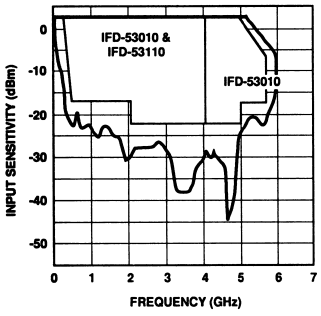


Figure 1. Input Sensitivity vs. Input Frequency and Recommended Operating Ranges for Nominal Operating Conditions (T = 25°C, V_{cc} - V_{ee} = 5 V).

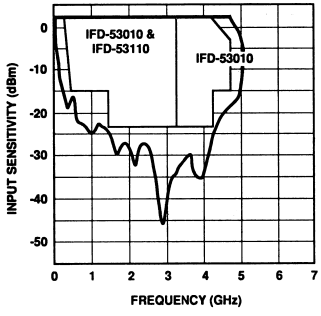


Figure 2. Input Sensitivity vs. Input Frequency and Recommended Operating Ranges for Worst Case Operating Conditions (-55°C < T < 125°C and 4.5 V < V_{cc} - V_{ee} < 5.5 V.

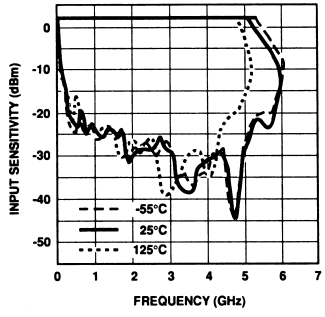


Figure 3. Input Sensitivity vs. Input Frequency and Temperature (V_{cc} - V_{ee} = 5 V).

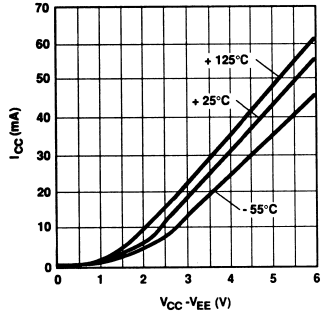


Figure 4. Device Current vs. Voltage and Temperature.

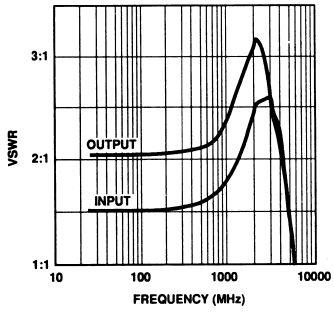


Figure 5. Input and Output VSWR vs. Frequency.

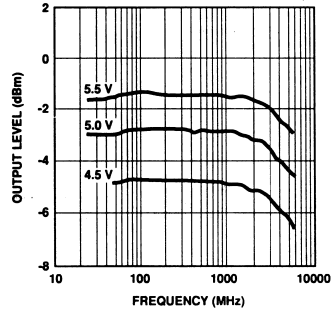


Figure 6. Output Power Level vs. Input Frequency and V_{cc} - V_{ee}.

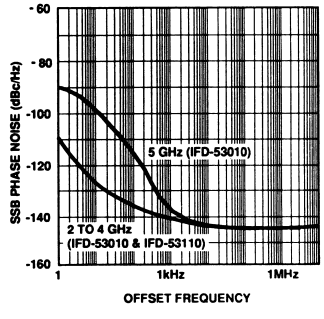


Figure 7. SSB Phase Noise vs. Offset Frequency, and Input Frequency.

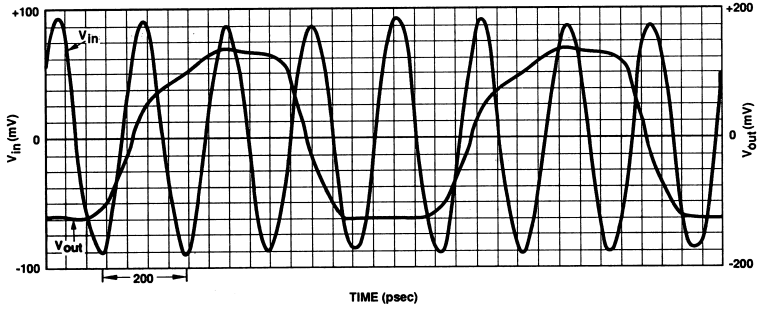


Figure 8. IFD-53010 Typical Output Response with 5 GHz Input.

BLOCKING CAPACITORS ARE 1000 pF TYP.
BYPASS CAPACITORS ARE 47 nF min.

BLOCKING CAPACITORS MAY BE OMITTED
IF GENERATOR AND LOAD ARE AT V_{CC} LEVEL.

TRANSMISSION LINES ARE 50 Ω.

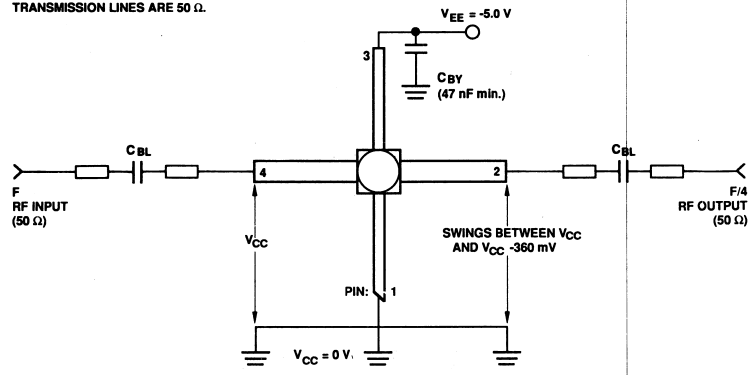


Figure 9. Typical ECL Biasing Configuration, IFD-53010 and IFD-53110.

BLOCKING CAPACITORS ARE 1000 pF TYP.

BYPASS CAPACITOR SHOULD BE 47 nF min.
TO ENSURE GOOD SENSITIVITY PERFORMANCE.

TRANSMISSION LINES ARE 50 Ω.

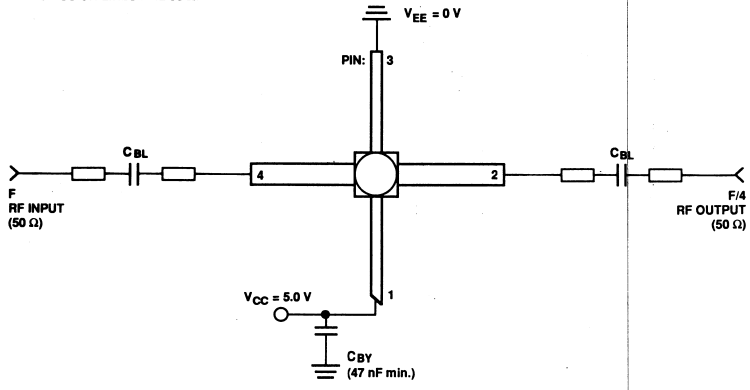


Figure 10. Typical RF Biasing Configuration, IFD-53010 and IFD-53110.

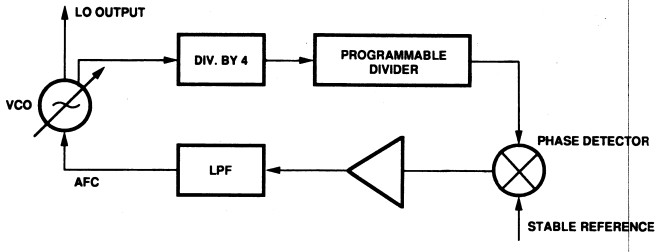


Figure 11. Typical Stabilized LO Configuration, IFD-53010 and IFD-53110.

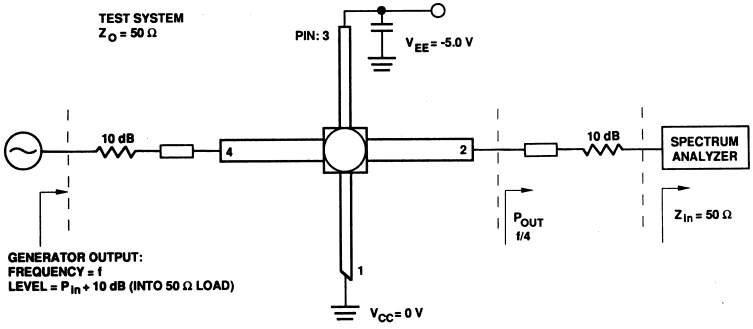
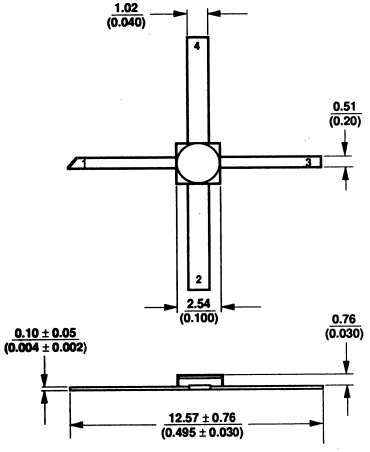


Figure 12. Sensitivity Test Configuration, IFD-53010 and IFD-53110.

Package Dimensions

100 mil Stripline Package



NOTES: (unless otherwise specified)
1. DIMENSIONS ARE IN mm (INCHES)
2. TOLERANCES: in .xxx = ± .005
mm .xx = ± .13

HEWLETT PACKARD

INA-01100
MagIC™ Low Noise, Cascadable Silicon Bipolar MMIC Amplifier

Features

- **Cascadable 50 Ω Gain Block**
- **Low Noise Figure: 1.7 dB typical at 100 MHz**
- **High Gain: 32.5 dB typical at 100 MHz**
- **3 dB Bandwidth: DC to 500 MHz**
- **Unconditionally Stable (k>1)**

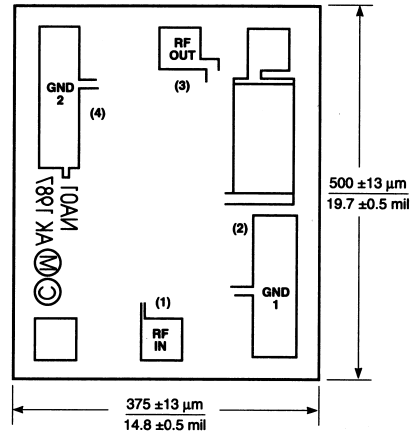
Description

The INA-01100 is a low noise silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) feedback amplifier chip. It is designed for narrow or wide bandwidth industrial and military applications that require high gain and low noise IF or RF amplification.

The INA series of MMICs is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, ISOSAT™-I silicon bipolar process which uses nitride self-alignment submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide intermetal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

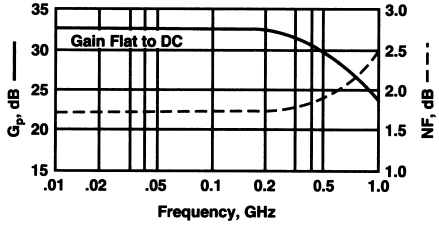
The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire.[1]

Chip Outline[1]

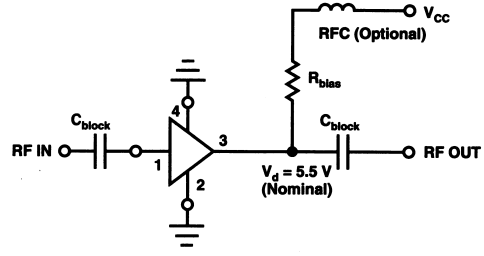


Chip thickness is 140 µm/5.5 mil Bond Pads are 41 µm/1.6 mil typical on each side.
Note: Ground Bonding is Critical[5].

Typical Gain and Noise Figure vs. Frequency[4]
T_A = 25°C, I_d = 35 mA



Typical Biasing Configuration



Electrical Specifications[2, 4], T_A = 25°C

Symbol	Parameters and Test Conditions[3]: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 100 MHz	dB		32.5	
ΔG_P	Gain Flatness	f = 10 to 250 MHz	dB		±0.5	
$f_{3\,dB}$	3 dB Bandwidth		MHz		500	
ISO	Reverse Isolation ($\|S_{12}\|^2$)	f = 10 to 250 MHz	dB		39	
VSWR	Input VSWR	f = 10 to 250 MHz			1.6:1	
	Output VSWR	f = 10 to 250 MHz			1.5:1	
NF	50 Ω Noise Figure	f = 100 MHz	dB		1.7	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 100 MHz	dBm		11	
IP_3	Third Order Intercept Point	f = 100 MHz	dBm		23	
t_D	Group Delay	f = 100 MHz	psec		200	
V_d	Device Voltage		V	4.0	5.5	7.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		+10	

NOTES:
1. See Application Note, "AN-A005: Transistor Chip Use" for additional information.
2. The recommended operating current range for this device is 30 to 40 mA. Typical performance as a function of current is on the following page.
3. RF performance of the chip is determined by packaging and testing 10 devices per wafer.
4. The values are the achievable performance for the INA-01100 mounted in a 70 mil stripline package.
5. Refer to Application Bulletin, "AB-0007: INA Bonding Configuration".

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2, 3]	400 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	-65 to 200°C

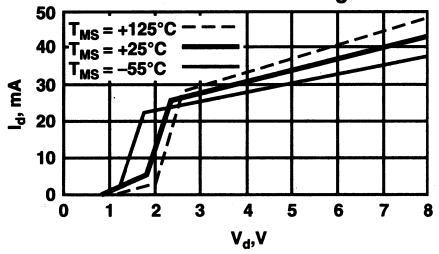
Thermal Resistance[2]: θ_{jc} = 60°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{MOUNTING\ SURFACE}$ (T_{MS}) = 25°C.
3. Derate at 16.7 mW/°C for T_{MS} > 176°C.

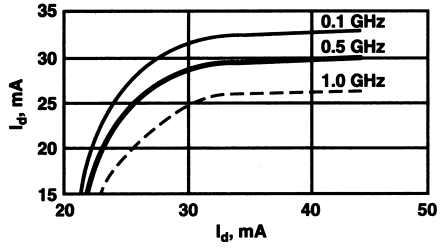
Typical Performance, T_A = 25°C

Unless otherwise noted: The values are the achievable performance for the INA-01100 mounted in a 70 mil stripline package.

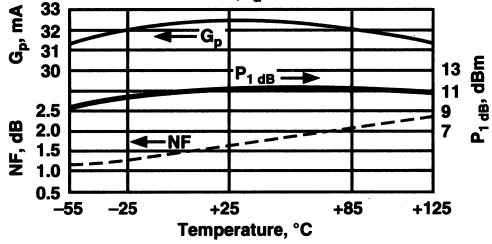
Device Current vs. Voltage



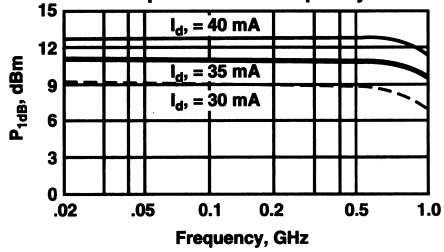
Power Gain vs. Current



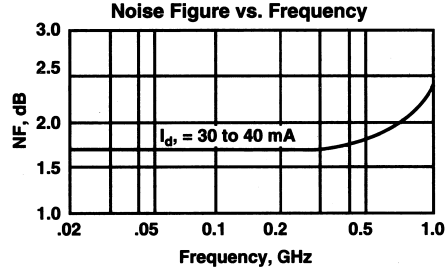
Output Power and 1 dB Gain Compression, NF and Power Gain vs. Case Temperature f = 0.1 GHz, I_d = 35 mA



Output Power at 1 dB Gain Compression vs. Frequency



Noise Figure vs. Frequency



Typical Scattering Parameters[5]: Z_O = 50 Ω

T_A = 25°C, Vcc = 35 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
MHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.01	0.09	-16	32.7	43.4	-1	-38.5	.012	-1	.18	1	1.17
0.05	0.10	-27	32.7	43.1	-10	-38.6	.012	15	.19	5	1.18
0.10	0.11	-5	32.4	41.9	-20	-38.4	.012	-8	.20	10	1.17
0.20	0.14	-80	31.6	38.0	-37	-38.6	.012	4	.24	14	1.22
0.30	0.18	-98	30.5	33.7	-52	-38.8	.011	-10	.27	15	1.31
0.40	0.20	-110	29.4	29.6	-65	-39.6	.011	2	.30	10	1.51
0.50	0.22	-115	28.4	26.2	-75	-38.6	.012	-12	.32	6	1.48
0.60	0.24	-120	27.4	23.4	-84	-39.1	.011	-7	.34	1	1.67
0.80	0.27	-124	25.7	19.3	-100	-38.3	.012	-6	.36	-11	1.76
1.00	0.30	-127	24.3	16.3	-115	-36.1	.016	-5	.36	-22	1.58
1500	0.44	165	21.8	12.37	-179	-33.6	.020	42	.19	-69	1.75
2000	0.44	154	17.9	7.88	146	-33.0	.022	42	.13	-106	2.42
2500	0.46	148	14.6	5.36	121	-30.6	.029	36	.12	-151	2.63
3000	0.48	139	11.4	3.71	96	-30.0	.032	45	.10	159	3.31

Note: 5. S-parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section of the *Avantek Microwave Semiconductors* databook

INA-01170
Low Noise, Cascadable Silicon Bipolar MMIC Amplifier

Features

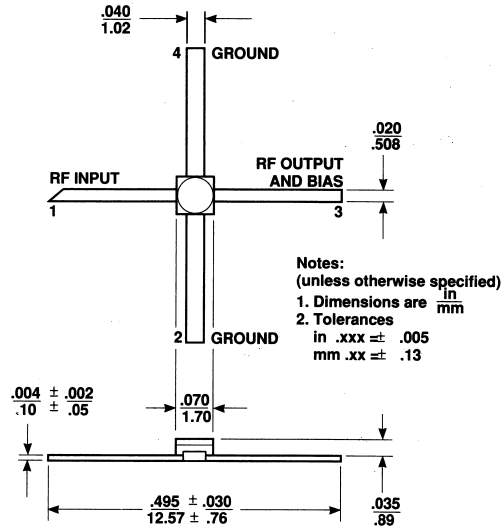
- **Cascadable 50 Ω Gain Block**
- **Low Noise Figure: 1.7 dB typical at 100 MHz**
- **High Gain: 32.5 dB typical at 100 MHz**
- **3 dB Bandwidth: DC to 500 MHz**
- **Unconditionally Stable (k>1)**
- **Hermetic Gold-Ceramic Surface Mount Package**

Description

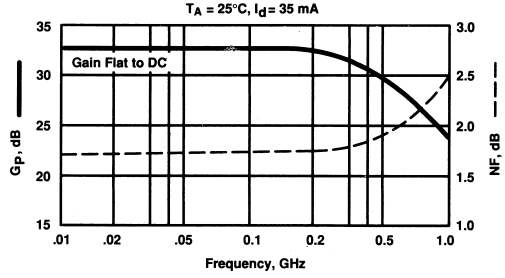
The INA-01170 is a low-noise silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) feedback amplifier housed in a hermetic, high reliability package. It is designed for narrow or wide bandwidth industrial and military applications that require high gain and low noise IF or RF amplification.

The INA series of MMICs is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX} ISOSAT™-I silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide intermetal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

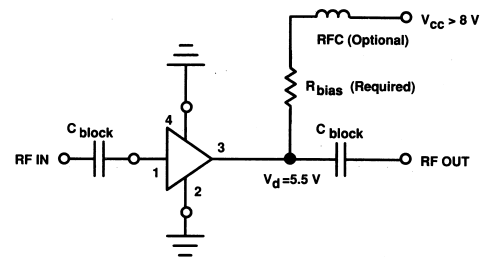
70 mil Package



TYPICAL GAIN AND NOISE FIGURE vs. FREQUENCY



Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 100 MHz	dB	30	32.5	35
ΔG_P	Gain Flatness	f = 10 to 250 MHz	dB		±0.5	
$f_{3\,dB}$	3 dB Bandwidth[2]		MHz		500	
ISO	Reverse Isolation ($\|S_{12}\|^2$)	f = 10 to 250 MHz	dB		39	
VSWR	Input VSWR	f = 10 to 250 MHz			1.6:1	
	Output VSWR	f = 10 to 250 MHz			1.5:1	
NF	50 Ω Noise Figure	f = 100 MHz	dB		2.0	2.5
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 100 MHz	dBm		11	
IP_3	Third Order Intercept Point	f = 100 MHz	dBm		23	
t_D	Group Delay	f = 100 MHz	psec		200	
V_d	Device Voltage		V	4.0	5.5	7.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		+10	

Notes: 1. The recommended operating current range for this device is 30 to 40 mA. Typical performance as a function of current is on the following page.
2. Referenced from 10 MHz Gain (G_P).

Absolute Maximum Ratings

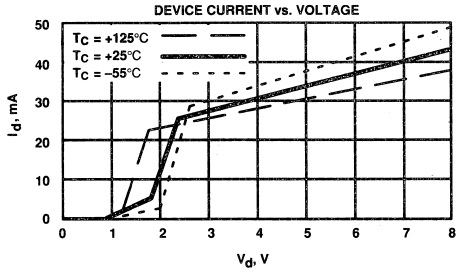
Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2,3]	400 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

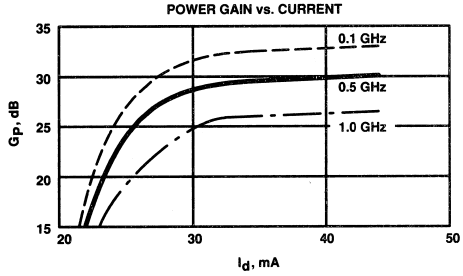
Thermal Resistance[2,4]: θ_{jc} = 140°C/W

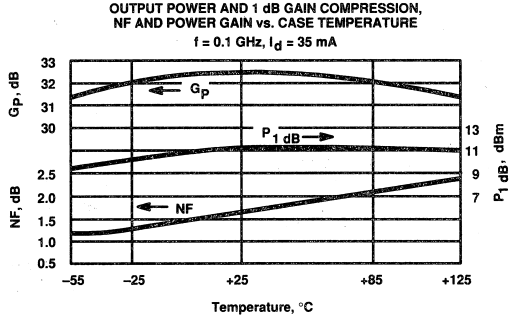
Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 7.1 mW/°C for T_C >144°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

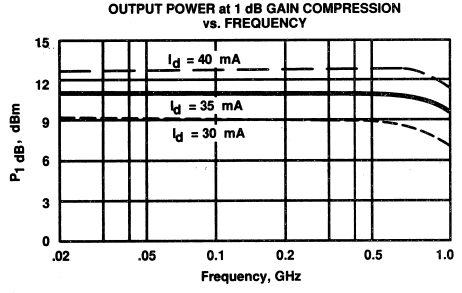
Typical Performance, T_A = 25°C

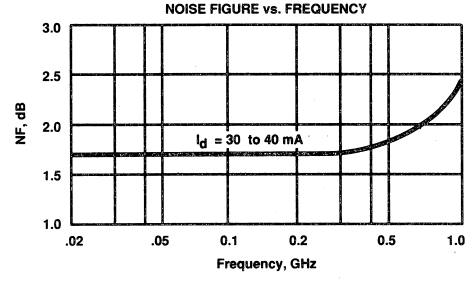
(unless otherwise noted)











Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 35 mA

Freq. MHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang	k
10	.09	–20	32.8	43.65	–2	–38.4	.012	–5	.17	–1	1.17
50	.10	–39	32.8	43.51	–9	–38.3	.012	17	.18	0	1.17
100	.13	–65	32.6	42.82	–18	–38.3	.012	–4	.18	1	1.17
150	.17	–83	32.4	41.71	–26	–38.4	.012	17	.19	2	1.18
200	.21	–96	32.1	40.41	–35	–38.6	.012	12	.19	3	1.18
250	.25	–107	31.8	38.93	–43	–39.0	.011	26	.19	4	1.26
300	.28	–115	31.5	37.38	–50	–39.0	.011	3	.20	5	1.26
400	.33	–130	30.7	34.19	–65	–39.3	.011	21	.21	3	1.31
500	.37	–140	29.9	31.13	–78	–39.2	.011	11	.22	0	1.35
600	.40	–150	29.0	28.30	–90	–38.9	.011	22	.23	–5	1.43
800	.43	–164	27.4	23.48	–112	–38.5	.012	30	.24	–19	1.52
1000	.44	–176	25.8	19.45	–132	–36.5	.015	32	.23	–32	1.49
1500	.44	165	21.8	12.37	–179	–33.6	.020	42	.19	–69	1.75
2000	.44	154	17.9	7.88	146	–33.0	.022	42	.13	–106	2.42
2500	.46	148	14.6	5.36	121	–30.6	.029	36	.12	–151	2.63
3000	.48	139	11.4	3.71	96	–30.0	.032	45	.10	159	3.31

HEWLETT PACKARD

INA-02100
MagIC™ Low Noise, Cascadable Silicon Bipolar MMIC Amplifier

Features

- **Cascadable 50 Ω Gain Block**
- **Low Noise Figure: 2.0 dB typical at 0.5 GHz**
- **High Gain: 31.5 dB typical at 0.5 GHz**
  25.0 dB typical at 1.5 GHz
- **3 dB Bandwidth: DC to 1.0 GHz**
- **Unconditionally Stable (k>1)**

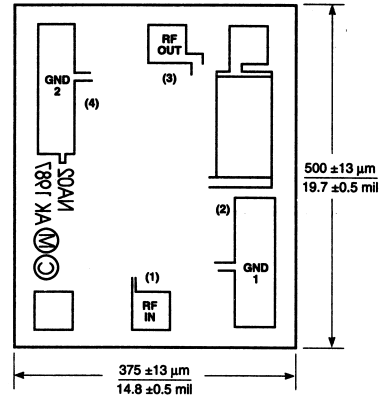
Description

The INA-02100 is a low-noise silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) feedback amplifier chip. It is designed for narrow or wide bandwidth industrial and military applications that require high gain and low noise IF or RF amplification.

The INA series of MMICs is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, ISOSAT™-I silicon bipolar process which uses nitride self-alignment submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide intermetal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

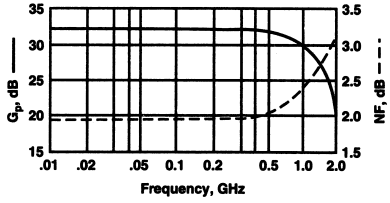
The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire[1].

Chip Outline[1]

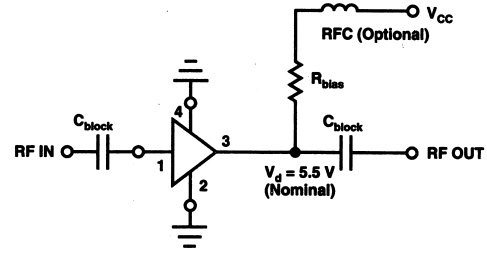


Chip thickness is 140 µm/5.5 mil Bond Pads are 41 µm/1.6 mil typical on each side.
Note: Ground Bonding is Critical[5].

Typical Gain and Noise Figure vs. Frequency[4]
T_A = 25°C, I_d = 35 mA



Typical Biasing Configuration



Electrical Specifications[2, 4], T_A = 25°C

Symbol	Parameters and Test Conditions[3]: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.5 GHz	dB		31.5	
ΔG_P	Gain Flatness	f = 0.01 to 1.0 GHz	dB		±1.5	
$f_{3\,dB}$	3 dB Bandwidth		GHz		1.0	
ISO	Reverse Isolation ($\|S_{12}\|^2$)	f = 0.01 to 1.0 GHz	dB		39	
VSWR	Input VSWR	f = 0.01 to 1.0 GHz			1.4:1	
	Output VSWR	f = 0.01 to 1.0 GHz			1.5:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		2.0	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		11	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		23	
t_D	Group Delay	f = 0.5 GHz	psec		350	
V_d	Device Voltage		V	4.0	5.5	7.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		+10	

NOTES:
1. See Application Note, "AN-A005: Transistor Chip Use" for additional information.
2. The recommended operating current range for this device is 30 to 40 mA. Typical performance as a function of current is on the following page.
3. RF performance of the chip is determined by packaging and testing 10 devices per wafer.
4. The values are the achievable performance for the INA-02100 mounted in a 70 mil stripline package.
5. Refer to Application Bulletin, "AB-0007: INA Bonding Configuration".

Absolute Maximum Ratings

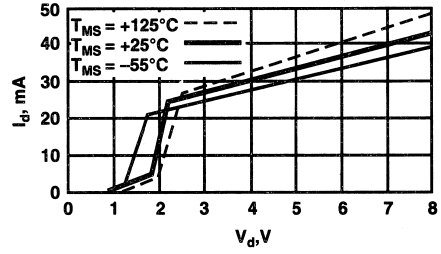
Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2, 3]	400 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	-65 to 200°C
Thermal Resistance[2]: θ_{jc} = 60°C/W	

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{MOUNTING\ SURFACE}$ (T_{MS}) = 25°C.
3. Derate at 16.7 mW/°C for T_{MS} > 176°C.

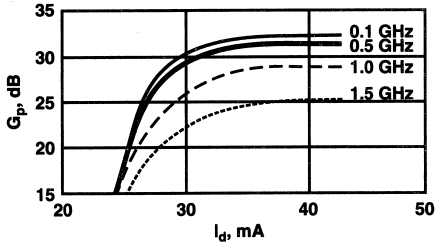
Typical Performance, T_A = 25°C

Unless otherwise noted: The values are the achievable performance for the INA-02100 mounted in a 70 mil stripline package.

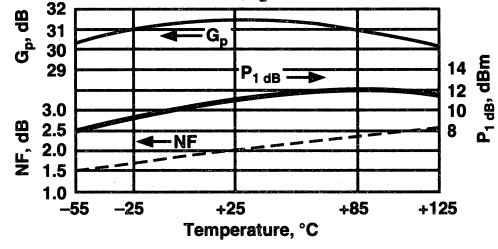
Device Current vs. Voltage



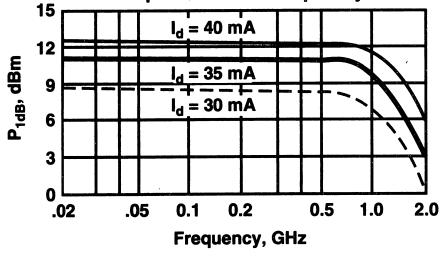
Power Gain vs. Current



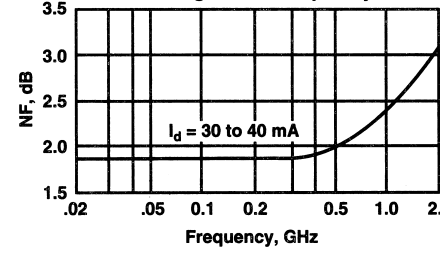
Output Power and 1 dB Gain Compression, NF and Power Gain vs. Case Temperature f = 0.1 GHz, I_d = 35 mA



Output Power at 1 dB Gain Compression vs. Frequency



Noise Figure vs. Frequency



Typical Scattering Parameters[5]: Z_O = 50 Ω

T_A = 25 °C, I_d = 5 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.01	0.06	-4	32.5	42.1	-2	-39.3	.011	14	.20	-1	1.27
0.05	0.05	-8	32.5	42.0	-8	-39.4	.011	12	.20	1	1.28
0.10	0.03	-46	32.3	41.3	-16	-37.9	.013	6	.20	-1	1.17
0.20	0.02	-52	31.8	39.0	-30	-39.2	.011	-4	.21	3	1.33
0.30	0.01	-46	31.1	36.2	-43	-38.8	.011	-12	.22	4	1.36
0.40	0.02	-44	30.4	33.3	-55	-40.4	.010	-2	.24	2	1.63
0.50	0.03	-35	29.7	30.7	-65	-39.3	.011	-17	.26	-1	1.56
0.60	0.06	-29	29.0	28.4	-74	-39.5	.011	-5	.28	-4	1.67
0.80	0.10	-41	27.9	24.8	-92	-38.1	.012	-9	.32	-14	1.58
1.00	0.17	-60	26.9	22.0	-108	-36.4	.015	-19	.34	-26	1.41
1.20	0.24	-73	26.0	19.9	-124	-35.5	.017	-16	.36	-40	1.32
1.40	0.30	-89	25.1	18.0	-141	-34.1	.020	-16	.38	-60	1.17
1.60	0.37	-103	24.1	16.0	-157	-32.6	.023	-30	.32	-91	1.19
1.80	0.42	-116	22.9	14.0	-174	-33.1	.022	-28	.26	-111	1.29
2.00	0.46	-128	21.5	12.0	171	-31.4	.027	-31	.22	-122	1.25
2.50	0.50	-146	18.3	8.2	142	-29.3	.034	-44	.19	-148	1.34
3.00	0.51	-162	14.6	5.4	116	-28.5	.038	-47	.15	-178	1.83

NOTE: 5. S parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section

INA-02170
Low Noise, Cascadable Silicon Bipolar MMIC Amplifier

Features

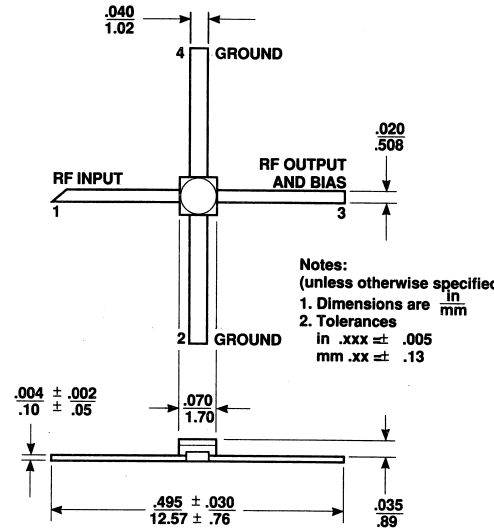
- **Cascadable 50 Ω Gain Block**
- **Low Noise Figure: 2.0 dB typical at 0.5 GHz**
- **High Gain: 31.5 dB typical at 0.5 GHz**
  25.0 dB typical at 1.5 GHz
- **3 dB Bandwidth: DC to 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Hermetic Gold-Ceramic Surface Mount Package**

Description

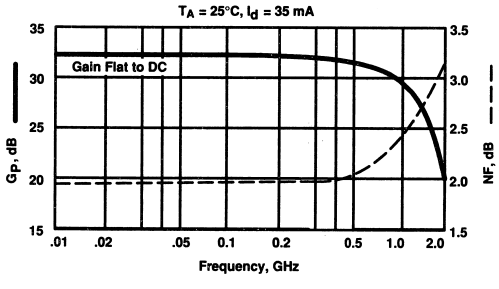
The INA-02170 is a low-noise silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) feedback amplifier housed in a hermetic, high reliability package. It is designed for narrow or wide bandwidth industrial and military applications that require high gain and low noise IF or RF amplification.

The INA series of MMICs is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX} ISOSAT™-I silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide intermetal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

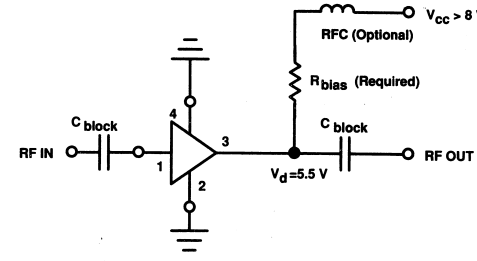
70 mil Package



TYPICAL GAIN AND NOISE FIGURE vs. FREQUENCY



Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.5 GHz	dB	29.0	31.5	34.0
ΔG_P	Gain Flatness	f = 0.01 to 1.0 GHz	dB		±1.5	
$f_{3\,dB}$	3 dB Bandwidth[2]		GHz		1.0	
ISO	Reverse Isolation ($\|S_{12}\|^2$)	f = 0.01 to 1.0 GHz	dB		39	
VSWR	Input VSWR	f = 0.01 to 1.0 GHz			1.4:1	
	Output VSWR	f = 0.01 to 1.0 GHz			1.5:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		2.0	2.5
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		11	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		23	
t_D	Group Delay	f = 0.5 GHz	psec		350	
V_d	Device Voltage		V	4.0	5.5	7.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		+10	

Notes: 1. The recommended operating current range for this device is 30 to 40 mA. Typical performance as a function of current is on the following page.
2. Referenced from 10 MHz Gain (G_P).

Absolute Maximum Ratings

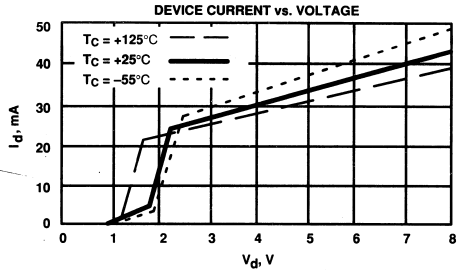
Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2,3]	400 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

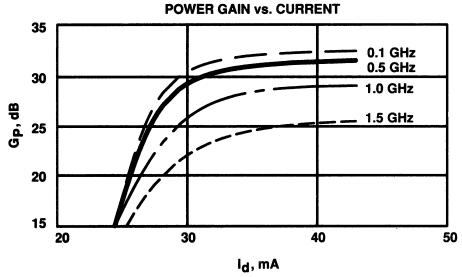
Thermal Resistance[2,4]: θ_{jc} = 140°C/W

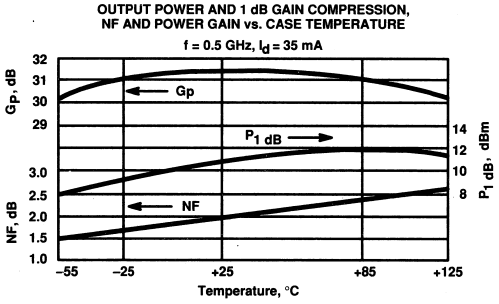
Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 7.1 mW/°C for T_C >144°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

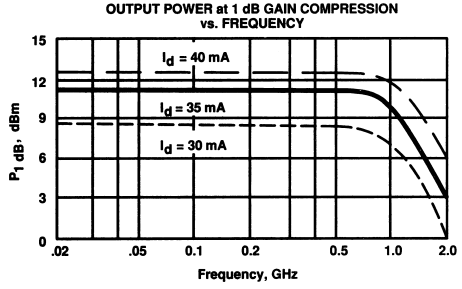
Typical Performance, T_A = 25°C

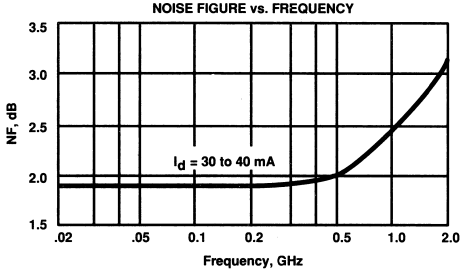
(unless otherwise noted)











Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 35 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang	k
0.01	.05	–8	32.5	42.32	–2	–39.2	.011	14	.19	–1	1.26
0.05	.05	–31	32.5	42.32	–7	–38.9	.011	14	.19	–5	1.26
0.10	.06	–85	32.5	42.05	–14	–38.0	.013	10	.19	–10	1.15
0.20	.09	–110	32.3	41.06	–27	–38.8	.011	5	.18	–16	1.29
0.30	.12	–129	32.0	39.82	–40	–38.8	.011	1	.17	–21	1.32
0.40	.15	–140	31.7	38.43	–53	–40.2	.010	19	.16	–25	1.45
0.50	.17	–151	31.4	37.08	–65	–40.0	.010	8	.16	–27	1.48
0.60	.17	–159	31.0	35.49	–77	–39.6	.011	23	.16	–30	1.43
0.80	.18	–174	30.2	32.45	–101	–38.2	.012	23	.16	–40	1.43
1.00	.19	179	29.2	28.70	–126	–38.2	.012	17	.16	–53	1.55
1.20	.19	173	27.8	24.51	–149	–37.5	.013	27	.15	–71	1.66
1.40	.20	166	26.1	20.18	–171	–36.2	.015	35	.14	–102	1.73
1.60	.21	162	24.2	16.26	170	–36.3	.015	34	.12	–172	2.07
1.80	.22	159	22.3	13.02	153	–34.1	.020	46	.10	144	1.94
2.00	.23	155	20.4	10.45	139	–33.0	.022	37	.07	117	2.17
2.50	.25	150	16.7	6.82	112	–33.3	.022	32	.05	95	3.19
3.00	.29	144	13.1	4.51	87	–31.8	.026	32	.04	78	3.96

HEWLETT PACKARD

INA-02184, INA-02186
MagIC™ Low Noise, Cascadable Silicon Bipolar MMIC Amplifier

Features

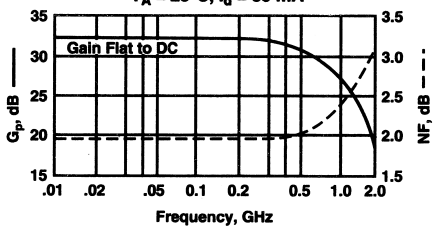
- **Cascadable 50 Ω Gain Block**
- **Low Noise Figure: 2.0 dB Typical at 0.5 GHz**
- **High Gain: 31 dB Typical at 0.5 GHz**
  26 dB Typical at 1.5 GHz
- **3 dB Bandwidth: DC to 0.8 GHz**
- **Unconditionally Stable (k>1)**
- **Low Cost Plastic Package**

Description

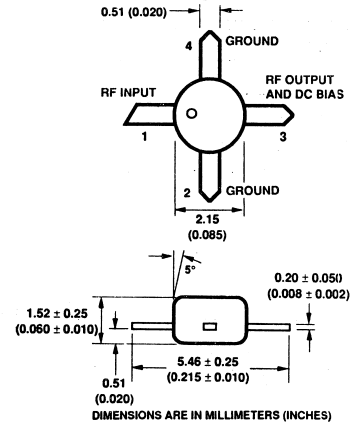
The INA-02184 and INA-02186 is a low-noise silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) feedback amplifier housed in low cost plastic packages. They are designed for narrow or wide bandwidth commercial applications that require high gain and low noise IF or RF amplification.

The INA series of MMICs is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, ISOSAT™-I silicon bipolar process which uses nitride self-alignment submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide intermetal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

Typical Gain and Noise Figure vs. Frequency
T_A = 25°C, I_d = 35 mA

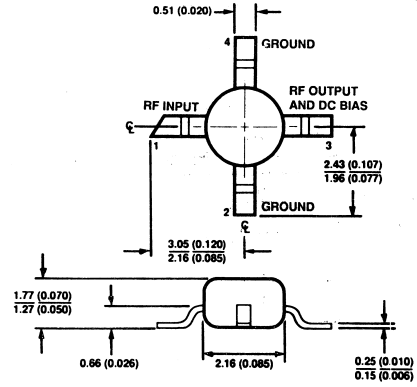


Package 84



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Package 86



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 35 mA, Z_O = 50 Ω		Units	INA-02184 Min.	INA-02184 Typ.	INA-02184 Max.	INA-02186 Min.	INA-02186 Typ.	INA-02186 Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.5 GHz	dB	29.0	31.0		29.0	31.0	
ΔG_P	Gain Flatness	f = 0.01 to 1.0 GHz	dB		±2.0			±2.0	
$f_{3\,dB}$	3 dB Bandwidth[2]		GHz		0.8			0.8	
ISO	Reverse Isolation ($\|S_{12}\|^2$)	f = 0.01 to 1.0 GHz	dB		39			39	
VSWR	Input VSWR (Max over Freq. Range)	f = 0.01 to 1.0 GHz			1.5			2.0	
	Output VSWR (Max over Freq. Range)	f = 0.01 to 1.0 GHz			1.7			1.7	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		2.0			2.0	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		11			11	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		23			23	
t_D	Group Delay	f = 0.5 GHz	psec		330			350	
V_d	Device Voltage		V	4.0	5.5	7.0	4.0	5.5	7.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		+10			+10	

NOTES: 1. The recommended operating current range for this device is 30 to 40 mA. Typical performance as a function of current is on the following page.
2. Referenced from 10 MHz Gain (G_P).

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2,3,4]	400 mW
RF Input Power	+13 dBm
Junction Temperature	+150°C
Storage Temperature	–65 to +150°C

Thermal Resistance[2]: θ_{jc} = 90°C/W — INA-02184
θ_{jc} = 100°C/W — INA-02186

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
2. Derate at 11.1 mW/°C for T_C > 114°C for INA-02184
4. Derate at 10 mW/°C for T_C > 110°C for INA-02186

Part Number Ordering Information

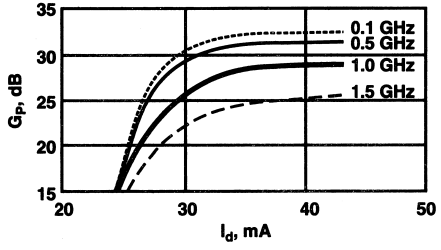
Part Number	Devices Per Reel	Reel Size
INA-02184-TR1	1000	7"
INA-02184-TR2	4000	13"
INA-02186-TR1	1000	7"
INA-02186-TR2	4000	13"

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

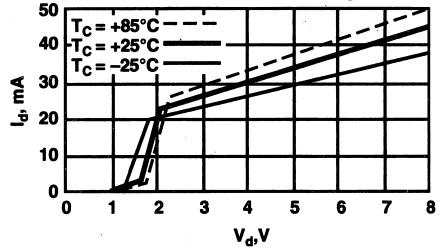
Typical Performance, INA-02184 and INA-02186, T_A = 25°C

(Unless otherwise noted)

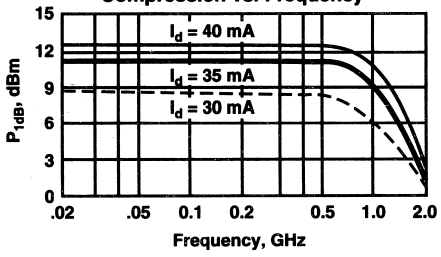
Power Gain vs. Current



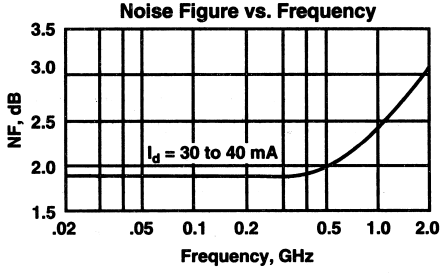
Device Current vs. Voltage



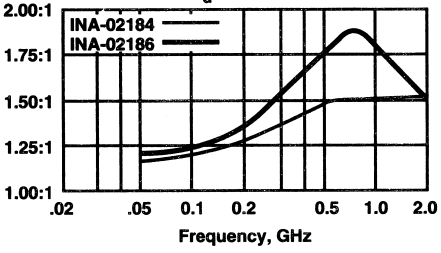
Output Power at 1 dB Gain Compression vs. Frequency



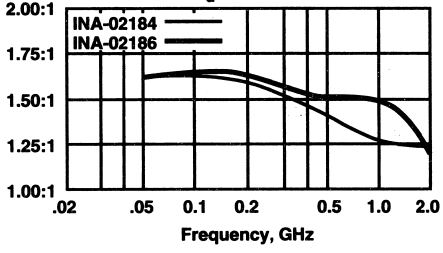
Noise Figure vs. Frequency



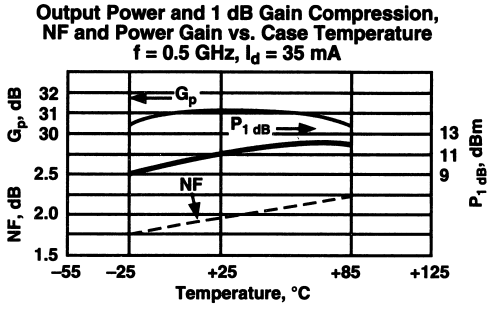
Input VSWR vs. Frequency
I_d = 35 mA



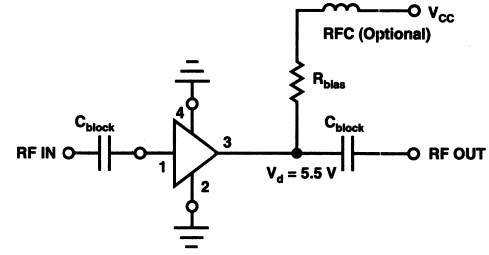
Output VSWR vs. Frequency
I_d = 35 mA



Typical Performance, INA-02184 and INA-02186,
$T_A = 25°C$ (Unless otherwise noted)



Typical Biasing Configuration



Typical INA-02184 Scattering Parameters: $Z_O = 50\ \Omega$ — $T_A = 25°C$, $I_d = 35$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
MHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.01	.09	-176	31.9	39.33	-1	-40.0	.010	1	.25	-1	1.40
0.05	.09	-171	31.9	39.24	-6	-41.9	.008	-12	.25	-4	1.66
0.10	10	-163	31.8	39.07	-13	-40.9	.009	1	.25	-8	1.52
0.20	.13	-159	31.7	38.30	-26	-40.0	.010	15	.23	-13	1.44
0.30	.15	-161	31.4	37.30	-39	-38.4	.012	16	.22	-17	1.29
0.40	.18	-168	31.2	36.42	-51	-39.2	.011	32	.21	-15	1.39
0.50	.19	-175	31.0	35.40	-63	-40.0	.010	34	.21	-16	1.52
0.60	.20	179	30.7	34.20	-75	-37.1	.014	35	.21	-17	1.24
0.80	.19	166	29.9	31.21	-101	-38.4	.012	38	.24	-26	1.44
1.00	.17	159	28.4	26.36	-126	-36.5	.015	53	.24	-41	1.40
1.20	.15	159	26.8	21.89	-149	-34.0	.020	56	.22	-60	1.31
1.40	.15	163	24.8	17.36	-169	-33.2	.022	62	.18	-78	1.50
1.60	.16	168	22.6	13.59	175	-31.4	.027	67	.14	-93	1.50
1.80	.18	168	20.7	10.86	161	-31.1	.028	61	.11	-108	1.74
2.00	.19	165	18.8	8.71	149	-30.2	.031	64	.08	-125	1.92
2.50	.23	159	14.9	5.56	127	-29.1	.035	56	.05	-167	2.54
3.00	.27	150	11.5	3.76	106	-27.1	.044	65	.04	155	2.89
3.50	.30	143	8.8	2.74	89	-26.0	.050	57	.04	137	3.39
4.00	.33	133	6.6	2.14	73	-25.0	.056	62	.05	137	3.78

Typical INA-02186 Scattering Parameters: $Z_O = 50\ \Omega$ — $T_A = 25°C$, $I_d = 35$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
MHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.01	.09	-178	31.5	37.38	-1	-40.0	.010	1	.24	-1	1.46
0.05	.09	-172	31.5	37.55	-6	-37.7	.013	11	.24	-5	1.22
0.10	.11	-160	31.5	37.46	-13	-39.2	.011	8	.23	-9	1.37
0.20	.14	-153	31.4	37.04	-25	-40.9	.009	15	.22	-17	1.60
0.30	.18	-156	31.3	36.62	-37	-38.4	.012	1	.21	-25	1.30
0.40	.22	-161	31.2	36.20	-49	-37.7	.013	28	.19	-30	1.25
0.50	.25	-169	31.1	35.70	-61	-39.2	.011	42	.18	-35	1.40
0.60	.28	-177	30.9	34.94	-74	-38.4	.012	44	.16	-39	1.33
0.80	.31	165	30.2	32.34	-101	-36.5	.015	52	.15	-47	1.20
1.00	.30	148	28.8	27.64	-129	-34.4	.019	57	.12	-59	1.15
1.20	.27	135	27.0	22.26	-153	-32.4	.024	62	.09	-70	1.15
1.40	.24	129	24.7	17.22	-173	-31.1	.028	61	.07	-80	1.23
1.60	.21	128	22.5	13.27	170	-31.4	.027	62	.04	-82	1.52
1.80	.20	129	20.4	10.42	156	-29.1	.035	61	.02	-83	1.50
2.00	.20	131	18.4	8.34	144	-29.1	.035	63	.01	-20	1.79
2.50	.23	133	14.5	5.29	123	-27.1	.044	59	.02	30	2.15
3.00	.27	130	11.2	3.61	103	-25.7	.052	63	.02	27	2.56
3.50	.31	124	8.3	2.60	86	-24.4	.060	64	.02	34	2.97
4.00	.34	118	6.1	2.02	70	-23.4	.068	58	.01	30	3.28

Emitter Inductance and Performance

As a direct result of their circuit topology, the performance of INA MMICs is extremely sensitive to groundpath ("emitter") inductance. The two stage design creates the possibility of a feedback loop being formed through the ground returns of the stages. If the path to ground provided by the external circuit is "long" (high in impedance) compared to the path back through the ground return of the other stage, then instability can occur (see Fig. 1). This phenomena can show up as a "peaking" in the gain versus frequency response (perhaps creating a negative gain slope amplifier), an increase in input VSWR, or even as return gain (a reflection coefficient greater than unity) at the input of the MMIC.

The "bottomline" is that ***excellent grounding is critical*** when using INA MMICs. The use of plated through holes or equivalent minimal path ground returns ***right at the device*** is essential. An appropriate layout is shown in Figure 2. A corollary is that designs should be done on the thinnest practical substrate. The parasitic inductance of a pair of via holes passing through .032" thick pc board is approximately 0.1 nH, while that of a pair of via holes passing through 0.062" thick board is close to 0.5 nH. HP does not recommend using INA family MMICs on boards thicker than 32 mils.

These stability effects are entirely predictable. A circuit simulation using the data sheet S-parameters and including a description of the ground return path (via model or equivalent "emitter" inductance) will give an accurate picture of the performance that can be expected. Device characterizations are made with the ground leads of the MMIC directly contacting a solid copper block (system ground) at a distance of 2 to 4 mils from the body of the package. Thus the information in the data sheet is a true description of the performance capability of the MMIC, and contains minimal contributions from fixturing.

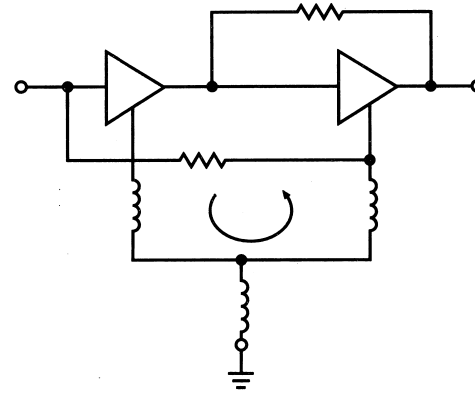


Figure 1. INA Potential Ground Loop

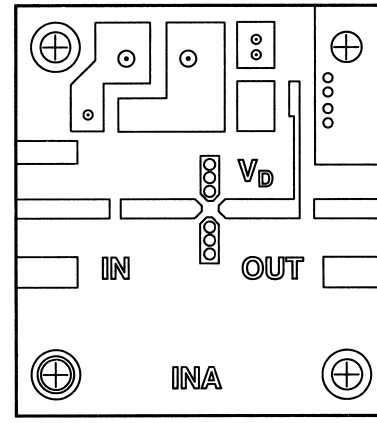


Figure 2. INA Circuit Board 2x Actual Size

HEWLETT PACKARD

INA-03100
MagIC™ Low Noise, Cascadable Silicon Bipolar MMIC Amplifier

Features

- **Cascadable 50 Ω Gain Block**
- **Low Noise Figure: 2.5 dB typical at 1.5 GHz**
- **High Gain: 26.0 dB typical at 1.5 GHz**
- **3 dB Bandwidth: DC to 2.8 GHz**
- **Unconditionally Stable (k>1)**
- **Low Power Consumption**

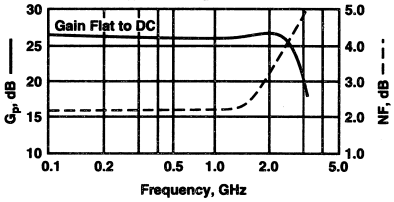
Description

The INA-03100 is a low-noise silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) feedback amplifier chip. It is designed for narrow or wide bandwidth commercial, industrial and military applications that require high gain and low noise IF or RF amplification with minimum power consumption.

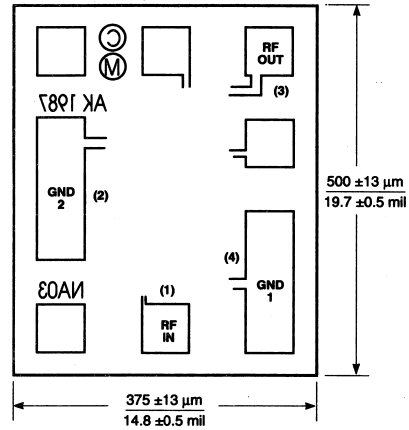
The INA series of MMICs is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, ISOSAT™-I silicon bipolar process which uses nitride self-alignment submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide intermetal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire.[1]

Typical Gain and Noise Figure vs. Frequency[4]
T_A = 25°C, I_d = 12 mA

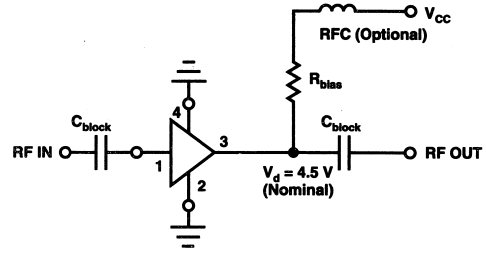


Chip Outline[1]



Chip thickness is 140 µm/5.5 mil Bond Pads are 41 µm/1.6 mil typical on each side.
Note: Ground Bonding is Critical[6].

Typical Biasing Configuration



Electrical Specifications[2, 4], T_A = 25°C

Symbol	Parameters and Test Conditions[3]: I_d = 12 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 1.5 GHz	dB		26.0	
ΔG_P	Gain Flatness	f = 0.01 to 2.0 GHz	dB		±0.5	
$f_{3\ dB}$	3 dB Bandwidth		GHz		2.8	
ISO	Reverse Isolation ($\|S_{12}\|^2$)	f = 0.01 to 2.0 GHz	dB		37	
VSWR	Input VSWR	f = 0.01 to 2.0 GHz			2.0[5]	
	Output VSWR	f = 0.01 to 2.0 GHz			3.0[5]	
NF	50 Ω Noise Figure	f = 1.5 GHz	dB		2.5	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 1.5 GHz	dBm		1.0	
IP_3	Third Order Intercept Point	f = 1.5 GHz	dBm		10	
t_D	Group Delay	f = 1.5 GHz	psec		200	
V_d	Device Voltage	f = 1.5 GHz	V	3.5	4.5	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		+5	

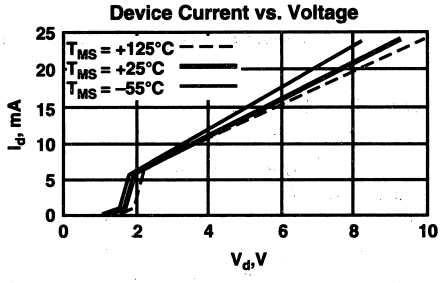
Notes:
1. See Application Note, "AN-A005: Transistor Chip Use" for additional information.
2. The recommended operating current range for this device is 8 to 20 mA. Typical performance as a function of current is on the following page.
3. RF performance of the chip is determined by packaging and testing 10 devices per wafer.
4. The values are the achievable performance for the INA-03100 mounted in a 70 mil stripline package.
5. VSWR can be improved by bypassing a 100 Ω bias resistor directly to ground.
6. Refer to Application Bulletin, "AB-0007: INA Bonding Configuration".

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	25 mA
Power Dissipation[2, 3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	-65 to 200°C

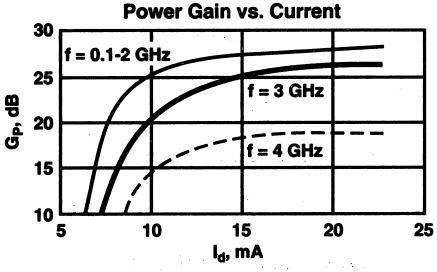
Thermal Resistance[2]: θ_{jc} = 70°C/W

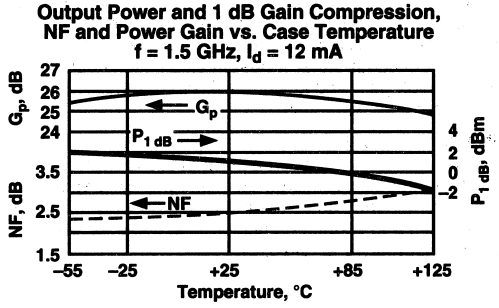
Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{MOUNTING\ SURFACE}$ (T_{MS}) = 25°C.
3. Derate at 14.3 mW/°C for T_{MS} > 186°C.

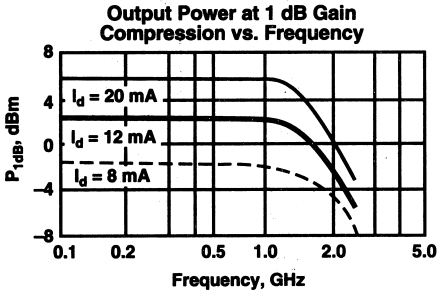


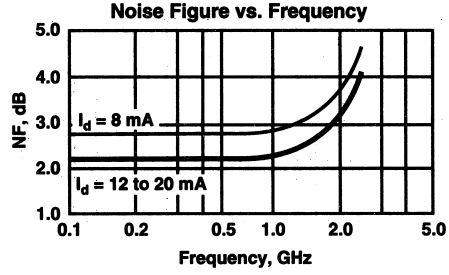
Typical Performance, T_A = 25°C

Unless otherwise noted: The values are the achievable performance for the INA-03100 mounted in a 70 mil stripline package.









Typical INA-03100 Scattering Parameters[5]: Z_O = 50 Ω

T_A = 25°C, I_d = 12 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.05	0.35	176	26.6	21.4	-4	-36.0	.016	8	.56	-1	1.25
0.10	0.35	172	26.6	21.3	-8	-36.5	.015	-4	.56	-3	1.30
0.20	0.33	165	26.4	21.0	-15	-36.4	.015	-5	.56	-4	1.30
0.40	0.31	150	26.1	20.1	-29	-36.0	.016	-13	.54	-7	1.33
0.60	0.27	137	25.6	19.0	-42	-37.6	.013	-14	.54	-8	1.58
0.80	0.23	125	25.0	17.8	-53	-36.1	.016	-13	.53	-9	1.49
1.00	0.19	113	24.5	16.7	-63	-35.1	.018	-16	.53	-10	1.43
1.20	0.16	99	24.0	15.9	-72	-36.9	.014	-21	.54	-12	1.72
1.40	0.13	76	23.8	15.4	-81	-36.4	.015	-12	.55	-15	1.65
1.60	0.12	51	23.6	15.2	-88	-35.6	.017	-11	.56	-17	1.54
1.80	0.13	21	23.6	15.5	-97	-34.1	.020	-5	.58	-20	1.24
2.00	0.18	-5	23.8	15.5	-106	-34.3	.019	-13	.60	-25	1.18
2.50	0.40	-52	24.7	17.2	-132	-30.2	.031	-9	.67	-38	0.53
3.00	0.81	-86	25.6	19.1	-167	-27.0	.045	-12	.70	-64	0.03

Note: 5. S parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section of the *Avantek Microwave Semiconductors* databook

INA-03170
Low Noise, Cascadable Silicon Bipolar MMIC Amplifier

Features

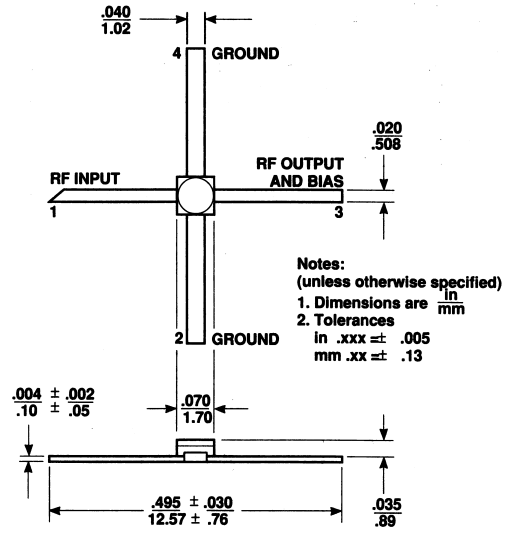
- **Cascadable 50 Ω Gain Block**
- **Low Noise Figure: 2.5 dB typical at 1.5 GHz**
- **High Gain: 26.0 dB typical at 1.5 GHz**
- **3 dB Bandwidth: DC to 2.8 GHz**
- **Unconditionally Stable (k>1)**
- **Low Power Dissipation**
- **Hermetic Gold-Ceramic Surface Mount Package**

Description

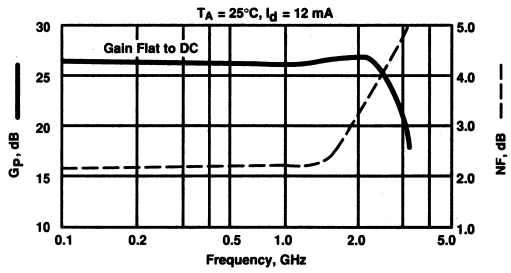
The INA-03170 is a low-noise silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) feedback amplifier housed in a hermetic, high reliability package. It is designed for narrow or wide bandwidth commercial, industrial and military applications that require high gain and low noise IF or RF amplification with minimum power consumption.

The INA series of MMICs is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX} ISOSAT™-I silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion-implantation, gold metallization and polyimide intermetal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

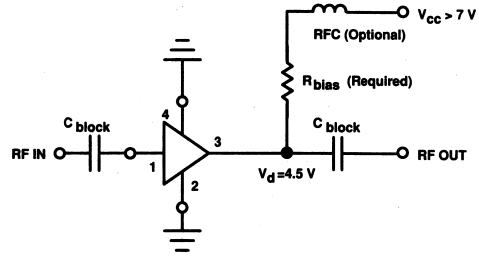
70 mil Package



TYPICAL GAIN AND NOISE FIGURE vs. FREQUENCY



Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 12 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 1.5 GHz	dB	24.5	28.0	30.0
ΔG_P	Gain Flatness	f = 0.01 to 2.0 GHz	dB		±0.5	
$f_{3\,dB}$	3 dB Bandwidth[2]		GHz		2.8	
ISO	Reverse Isolation ($\|S_{12}\|^2$)	f = 0.01 to 2.0 GHz	dB		37	
VSWR	Input VSWR	f = 0.01 to 2.0 GHz			2.0[3]	
	Output VSWR	f = 0.01 to 2.0 GHz			3.0[3]	
NF	50 Ω Noise Figure	f = 1.5 GHz	dB		2.5	3.0
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.5 GHz	dBm		1.0	
IP_3	Third Order Intercept Point	f = 1.5 GHz	dBm		10	
t_D	Group Delay	f = 1.5 GHz	psec		200	
V_d	Device Voltage	f = 1.5 GHz	V	3.5	4.5	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		+5	

Notes: 1. The recommended operating current range for this device is 8 to 20 mA. Typical performance as a function of current is on the following page.
2. Referenced from 10 MHz Gain (G_P).
3. VSWR can be improved by bypassing the bias directly to ground.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	25 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

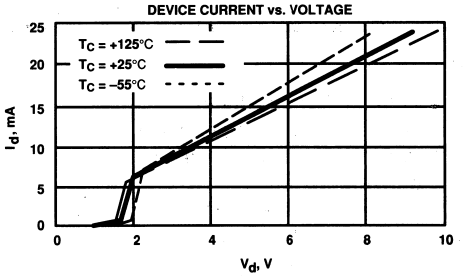
Thermal Resistance[2,4]: θ_{jc} = 150°C/W

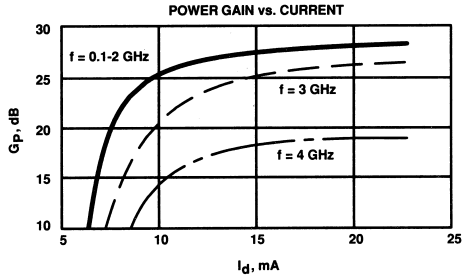
Notes:

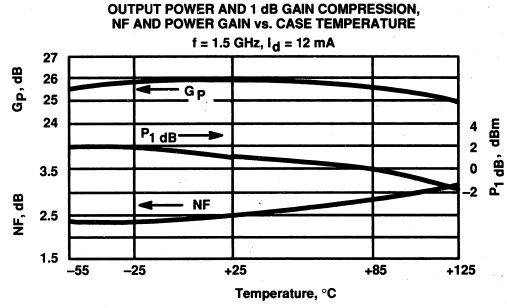
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 6.7 mW/°C for T_C >170°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

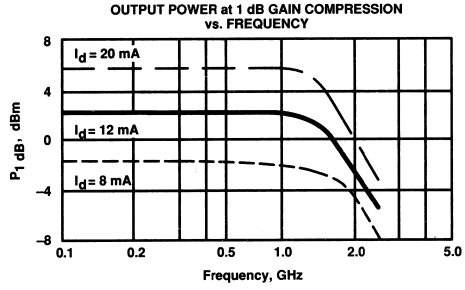
Typical Performance, T_A = 25°C

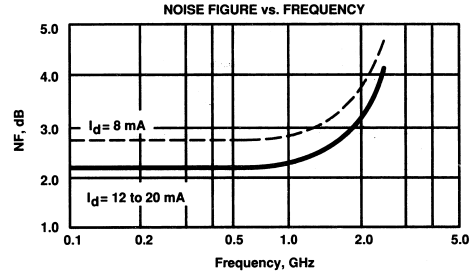
(unless otherwise noted)











Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 12 mA

Freq. GHz	S11 Mag	S11 Ang	S21 dB	S21 Mag	S21 Ang	S12 dB	S12 Mag	S12 Ang	S22 Mag	S22 Ang	k
0.05	.35	178	26.6	21.48	–4	–35.9	.016	9	.56	–1	1.24
0.10	.35	176	26.6	21.42	–7	–36.5	.015	6	.56	–4	1.29
0.20	.34	172	26.6	21.37	–14	–36.5	.015	–1	..56	–7	1.30
0.40	.34	164	26.5	21.19	–28	–36.5	.015	–5	.54	–13	1.33
0.60	.33	158	26.4	20.91	–41	–38.4	.012	2	.53	–18	1.58
0.80	.32	152	26.3	20.69	–54	–37.1	.014	5	.51	–22	1.46
1.00	.32	147	26.2	20.48	–67	–36.5	.015	4	.50	–27	1.41
1.20	.32	141	26.2	20.40	–80	–39.2	.011	13	.49	–32	1.79
1.40	.31	133	26.3	20.73	–93	–37.7	.013	25	.48	–38	1.57
1.60	.31	125	26.5	21.15	–106	–37.1	.014	28	.47	–45	1.47
1.80	.30	117	26.8	21.84	–121	–35.4	.017	30	.46	–52	1.28
2.00	.27	106	26.9	22.20	–138	–37.1	.014	33	.42	–62	1.48
2.50	.15	94	26.6	21.48	–177	–35.4	.017	23	.31	–79	1.44
3.00	.16	159	23.7	15.32	133	–34.4	.019	42	.16	–72	1.78
3.50	.28	150	19.8	9.81	99	–35.4	.017	28	.19	–60	2.71

HEWLETT PACKARD

INA-03184
Low Noise, Cascadable Silicon Bipolar MMIC Amplifier

Features

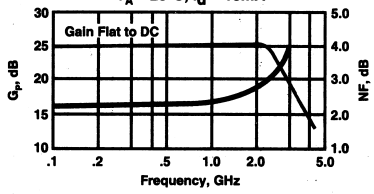
- **Cascadable 50 Ω Gain Block**
- **Low Noise Figure: 2.6 dB typical at 1.5 GHz**
- **High Gain: 25 dB typical at 1.5 GHz**
- **3 dB Bandwidth: DC to 2.5 GHz**
- **Unconditionally Stable (k>1)**
- **Low Power Dissipation: 10 mA Bias**
- **Low Cost Plastic Package**

Description

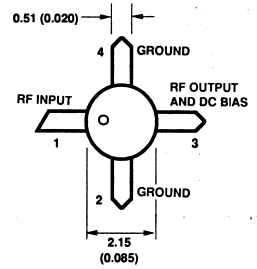
The INA-03184 is a low-noise silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) feedback amplifier housed in a low cost surface mount plastic package. It is designed for narrow or wide bandwidth commercial and industrial applications that require high gain and low noise IF or RF amplification with minimum power consumption.

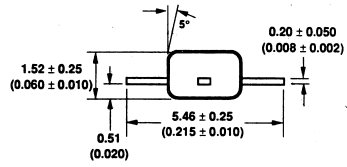
The INA series of MMICs is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, ISOSAT™-I silicon bipolar process which uses nitride self-alignment submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide intermetal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

Typical Gain and NF vs. Frequency
T_A = 25°C, I_d = 10mA



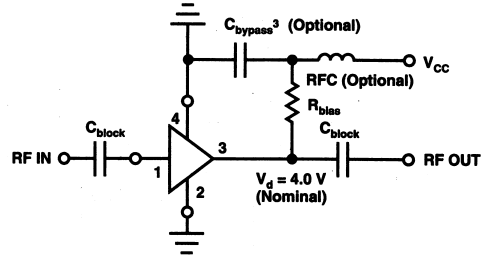
84 Plastic Package





DIMENSIONS ARE IN MILLIMETERS (INCHES)

Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 10 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 1.5 GHz	dB	23.0	25.0	
ΔG_P	Gain Flatness	f = 0.1 to 2 GHz	dB		±0.8	
$f_{3\,dB}$	3 dB Bandwidth[2]		GHz		2.5	
ISO	Reverse Isolation ($\|S_{12}\|^2$)	f = 1.5 GHz	dB		35	
VSWR	Input VSWR	f = 0.01 to 2 GHz			2.0:1	
	Output VSWR	f = 0.01 to 2 GHz			3.0:1[3]	
NF	50 Ω Noise Figure	f = 1.5 GHz	dB		2.6	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.5 GHz	dBm		–2.0	
IP_3	Third Order Intercept Point	f = 1.5 GHz	dBm		7	
t_D	Group Delay	f = 1.5 GHz	psec		210	
V_d	Device Voltage		V	3.0	4.0	5.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		+4	

Notes:
1. The recommended operating current range for this device is 8 to 16 mA. Typical performance as a function of current is on the following page.
2. Reference from 10 MHz gain (Gp).
3. VSWR can be improved by bypassing a 100-200 Ω bias resistor directly to ground. See AN-S012: MagIC Low Noise Amplifiers

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	25 mA
Power Dissipation[2]	200 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	-65 to 150°C

Thermal Resistance: θ_{jc} = 100°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. Derate at 10 mW/°C for T_C > 130°C.

Part Number Ordering Information

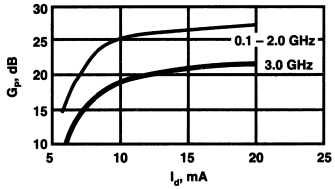
Part Number	Devices Per Reel	Reel Size
INA-03184-TR1	1000	7"
INA-03184-TR2	4000	13"

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

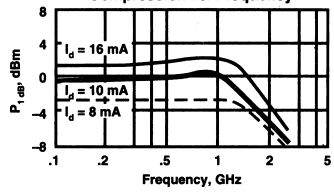
Typical Performance, T_A = 25°C

(Unless otherwise noted)

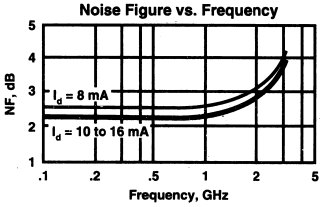
Power Gain vs. Current



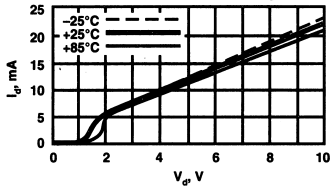
Output Power @ 1 dB Gain Compression vs. Frequency



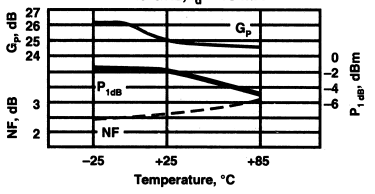
Noise Figure vs. Frequency



Device Current vs. Voltage



Output Power @ 1 dB Gain Compression, NF and Power Gain vs. Case Temperature
f = 1.5 GHz, I_d = 10 mA



Typical INA-03184 Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 10 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
MHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.05	.32	179	25.6	19.14	-3	-37.1	.014	3	.55	0	1.48
0.10	.32	176	25.6	19.05	-7	-37.1	.014	4	.57	-3	1.45
0.20	.32	172	25.6	19.05	-14	-37.1	.014	6	.55	-5	1.48
0.40	.32	165	25.5	18.78	-29	-37.1	.014	10	.53	-11	1.53
0.60	.32	158	25.4	18.71	-43	-36.5	.015	11	.51	-14	1.49
0.80	.32	151	25.4	18.53	-57	-36.5	.015	13	.51	-17	1.50
1.00	.32	144	25.2	18.18	-72	-35.9	.016	21	.50	-20	1.46
1.20	.30	135	25.2	18.27	-86	-35.9	.016	25	.50	-23	1.46
1.40	.31	126	25.2	18.10	-102	-35.4	.017	30	.49	-29	1.42
1.60	.30	117	25.1	17.92	-117	-34.9	.018	38	.48	-34	1.38
1.80	.26	102	24.9	17.49	-135	-34.4	.019	44	.45	-41	1.39
2.00	.22	92	24.4	16.62	-153	-34.0	.020	49	.40	-50	1.44
2.50	.09	91	22.2	12.88	168	-33.6	.021	57	.26	-48	1.87
3.00	.14	160	18.9	8.79	134	-32.8	.023	65	.22	-33	2.40
3.50	.24	151	15.4	5.92	108	-32.0	.025	69	.26	-33	3.01
4.00	.29	139	12.4	4.18	87	-30.8	.029	81	.28	-43	3.52

Note: 5. S-parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section

HEWLETT PACKARD

INA-10386
Low Noise, Cascadable Silicon Bipolar MMIC Amplifier

Features

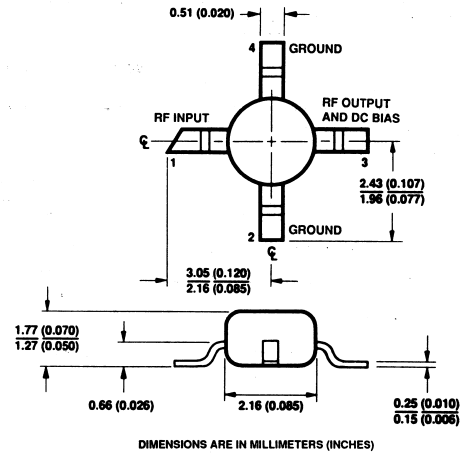
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 1.8 GHz**
- **26 dB typical Gain at 1.5 GHz**
- **10 dBm typical P_{1dB} at 1.5 GHz**
- **Unconditionally Stable (k>1)**
- **Surface Mount Plastic Package**

Description

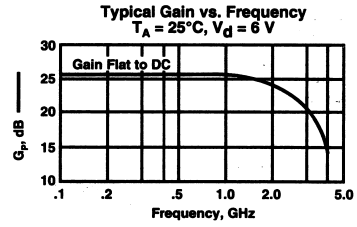
The INA-10386 is a low-noise silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) feedback amplifier housed in a low cost surface mount plastic package. It is designed for narrow or wide bandwidth commercial and industrial applications that require high gain and moderate power.

The INA series of MMICs is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, ISOSAT™-I silicon bipolar process which uses nitride self-alignment submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide intermetal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

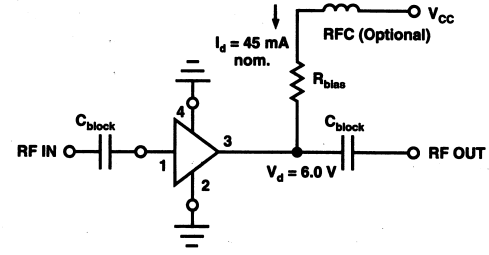
86 Plastic Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)



Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: V_d = 6V, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 1.5 GHz	dB	23.0	26.0	
ΔG_P	Gain Flatness	f = 0.1 to 1.5 GHz	dB		±1.0	
$f_{3\,dB}$	3 dB Bandwidth		GHz		1.8	
ISO	Reverse Isolation ($\|S_{12}\|^2$)	f = 2 GHz	dB		30	
VSWR	Input VSWR	f = 0.1 to 2 GHz			1.5:1	
	Output VSWR	f = 0.1 to 2 GHz			1.5:1	
NF	50 Ω Noise Figure	f = 1.5 GHz	dB		3.8	
$P_{1\,dB}$	Output Power at 1 dB Gain Compression	f = 1.5 GHz	dBm		10	
IP_3	Third Order Intercept Point	f = 1.5 GHz	dBm		23	
t_D	Group Delay	f = 1.5 GHz	psec		250	
V_d	Device Voltage		mA	35	45	55
dV/dT	Device Voltage Temperature Coefficient		mV/°C		+10	

Notes: 1. The recommended operating current range for this device is 40 to 60 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	750 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	-65 to 150°C

Thermal Resistance: θ_{jc} = 100°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
2. Derate at 10 mW/°C for T_C > 75°C.

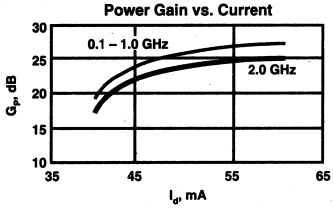
Part Number Ordering Information

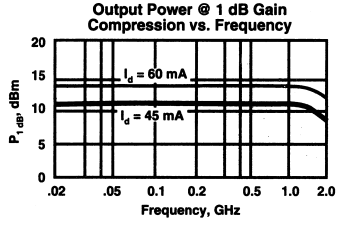
Part Number	Devices Per Reel	Reel Size
INA-10386-TR1	1000	7"
INA-10386-TR2	4000	13"

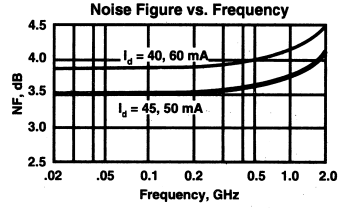
For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

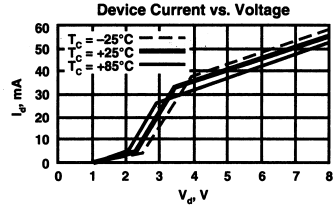
Typical Performance, T_A = 25°C

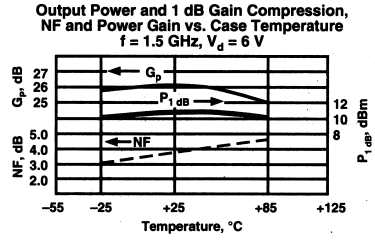
(Unless otherwise noted)











Typical INA-10386 Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, V_d = 6 V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
MHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.05	.12	-9	26.6	21.4	-4	-35.2	.017	1	.11	-3	1.51
0.10	.11	-17	26.7	21.6	-8	-35.6	.017	3	.12	-10	1.50
0.50	.13	-79	26.7	21.6	-38	-35.7	.016	10	.07	-40	1.59
1.00	.17	-137	26.8	21.9	-80	-34.1	.020	43	.03	18	1.33
1.50	.21	171	26.0	20.0	-126	-33.1	.023	53	.07	32	1.26
2.00	.21	127	23.6	15.1	-168	-29.9	.032	55	.07	9	1.23
2.50	.19	106	21.7	12.2	159	-28.4	.038	58	.04	42	1.27
3.00	.14	86	19.2	9.1	127	-26.7	.046	55	.05	56	1.37
3.50	.07	85	16.8	6.9	97	-24.8	.058	50	.06	47	1.44
4.00	.08	148	14.2	5.1	70	-24.7	.058	51	.04	40	1.82

HEWLETT PACKARD

MSA-0100
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 1.3 GHz**
- **High Gain: 18.5 dB typical at 0.5 GHz**
- **Unconditionally Stable (k>1)**

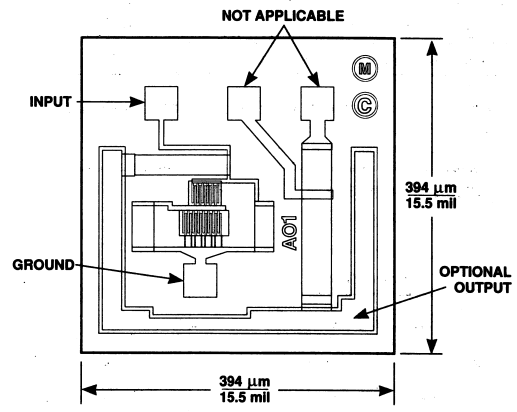
Description

The MSA-0100 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial, industrial and military applications.

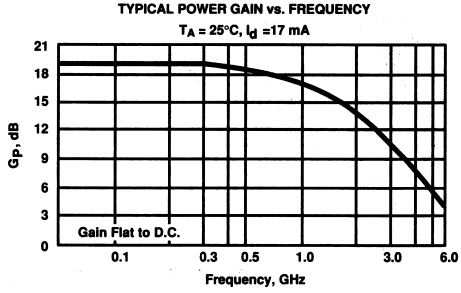
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire. See APPLICATIONS section, "Chip Use".

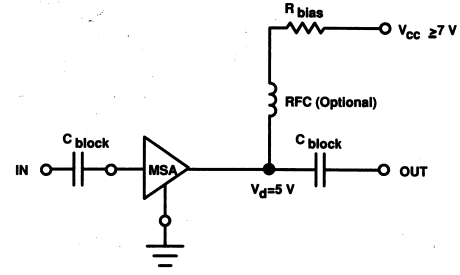
Chip Outline[1]



Unless otherwise specified, tolerances are ±13 µm / ±0.5 mils.
Chip thickness is 114 µm / 4.5 mil. Bond pads are 41 µm / 1.6 mil typical on each side.
*** Output contact is made by die attaching the backside of the die.**



Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions[3]: I_d = 17 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		19.0	
ΔG_P	Gain Flatness	f = 0.1 to 0.7 GHz	dB		±0.6	
$f_{3\,dB}$	3 dB Bandwidth		GHz		1.3	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.3:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.3:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 0.5 GHz	dBm		1.5	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		5.5	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.0	
t_D	Group Delay	f = 0.5 GHz	psec.		150	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–9.0	

Notes: 1. This chip contains additional biasing options. The performance specified applies only to the bias option whose bond pads are indicated on the chip outline. Refer to the APPLICATIONS section "MODAMP™ Silicon MMIC Chip Use" for additional information.
2. The recommended operating current range for this device is 13 mA to 25 mA. Typical performance as a function of current is on the following page.
3. RF performance of the chip is determined by packaging and testing 10 devices per wafer in a dual ground configuration.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	40 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+20 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 45°C/W

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{MOUNTING\ SURFACE}$ = 25°C
3. Derate at 22.2 mW/°C for $T_{MOUNTING\ SURFACE}$ > 191°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

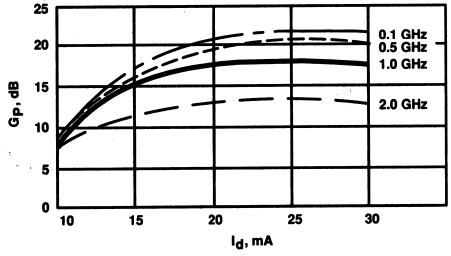
Part Number Ordering Information

Part Number	Devices Per Tray
MSA-0100-GP2	10
MSA-0100-GP4	100
MSA-0100-GP6	up to 300

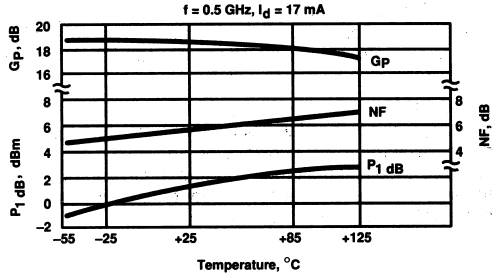
Typical Performance, T_A = 25°C

(unless otherwise noted)

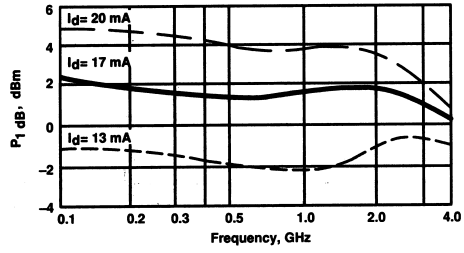
POWER GAIN vs. CURRENT



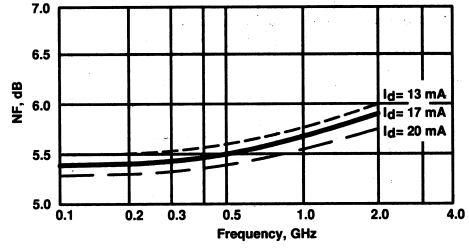
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. MOUNTING
SURFACE TEMPERATURE
f = 0.5 GHz, I_d = 17 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters[4]: Z_O = 50 Ω

T_A = 25°C, I_d = 17 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.08	171	19.0	8.91	174	–22.7	.073	2	.10	–11
0.2	.07	161	18.9	8.82	169	–22.5	.075	6	.11	–24
0.3	.07	152	18.8	8.72	163	–22.3	.077	9	.10	–35
0.4	.06	143	18.6	8.56	156	–22.4	.076	12	.11	–44
0.5	.06	133	18.5	8.37	151	–22.1	.079	14	.11	–53
0.6	.05	115	18.2	8.15	146	–21.9	.080	19	.12	–60
0.8	.04	84	17.7	7.68	136	–21.3	.086	22	.12	–75
1.0	.04	3	17.1	7.17	126	–20.3	.096	26	.12	–88
1.5	.08	–39	15.5	5.95	106	–19.3	.109	32	.10	–107
2.0	.12	–76	13.7	4.86	90	–17.9	.127	32	.08	–128
2.5	.15	–102	12.2	4.09	82	–16.9	.142	36	.06	–130
3.0	.19	–122	10.8	3.47	71	–16.4	.151	36	.06	–125
3.5	.25	–137	9.4	2.96	60	–15.6	.165	34	.07	–107
4.0	.27	–147	8.2	2.56	51	–15.2	.173	32	.10	–86
4.5	.28	–157	7.0	2.24	42	–14.8	.182	29	.13	–80
5.0	.28	–171	6.0	2.00	35	–14.4	.190	28	.16	–77

Note: 4. S-parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0104
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

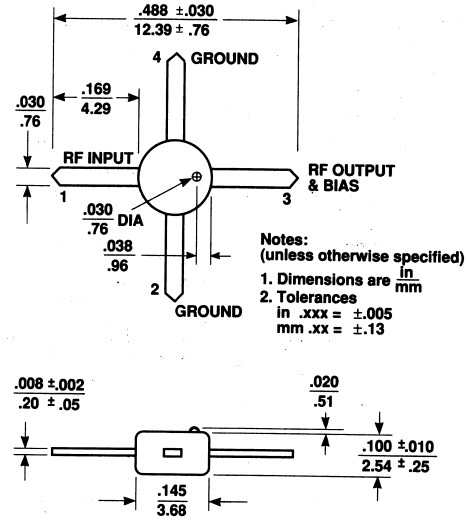
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 0.8 GHz**
- **High Gain: 17.0 dB typical at 0.5 GHz**
- **Unconditionally Stable (k>1)**
- **Low Cost Plastic Package**

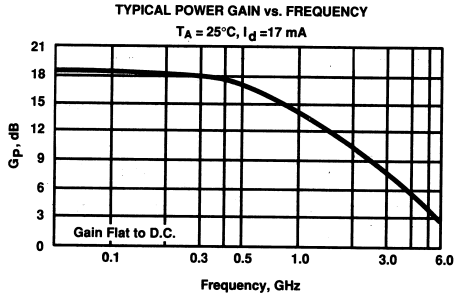
Description

The MSA-0104 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

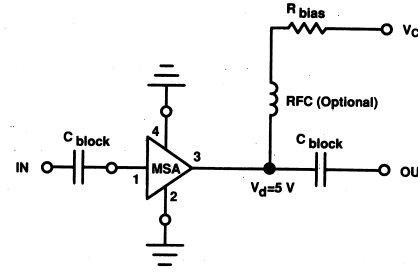
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

04A Plastic Package





Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 17 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 0.5 GHz	dB	17.0	18.5 17.0	
ΔG_P	Gain Flatness	f = 0.1 to 0.6 GHz	dB		±1.0	
$f_{3\ dB}$	3 dB Bandwidth		GHz		0.8	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.4:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.3:1	
$P_{1\ dB}$	Output Power @ 1 dB Gain Compression	f = 0.5 GHz	dBm		1.5	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		5.5	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.0	
t_D	Group Delay	f = 0.5 GHz	psec.		180	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–9.0	

Note: 1. The recommended operating current range for this device is 13 mA to 25 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	40 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

Thermal Resistance[2,4]: θ_{jc} = 100°C/W

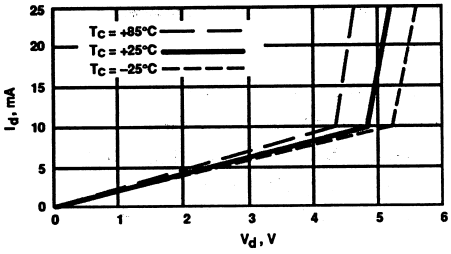
Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 10 mW/°C for T_C > 130°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

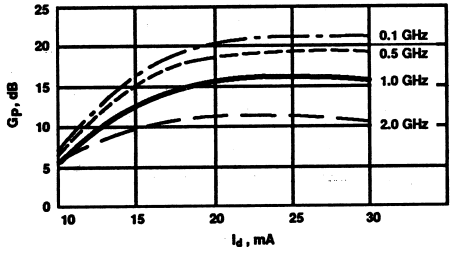
Typical Performance, T_A = 25°C

(unless otherwise noted)

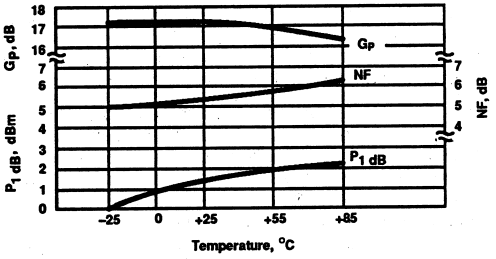
DEVICE CURRENT vs. VOLTAGE



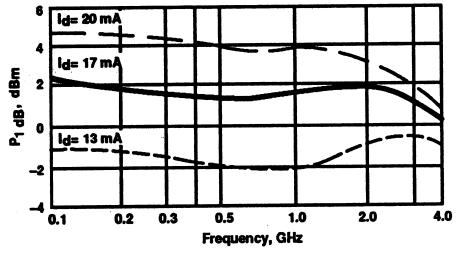
POWER GAIN vs. CURRENT



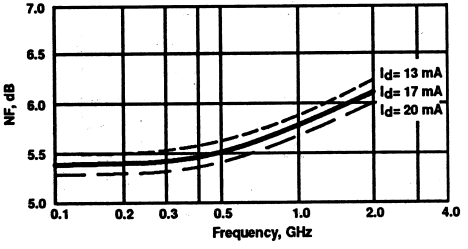
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. CASE TEMPERATURE
f = 0.5 GHz, I_d = 17 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 17 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	.06	141	18.4	8.31	170	–22.3	.077	5	.07	–9
0.2	.08	112	18.1	8.07	160	–22.3	.077	9	.07	–15
0.3	.10	94	17.8	7.75	151	–22.0	.079	15	.07	–22
0.4	.12	77	17.4	7.38	142	–21.6	.083	16	.07	–32
0.5	.13	70	16.9	7.01	134	–21.0	.089	19	.07	–37
0.6	.14	56	16.4	6.60	127	–20.7	.092	21	.08	–44
0.8	.16	41	15.4	5.87	114	–19.5	.106	27	.08	–53
1.0	.17	28	14.3	5.21	102	–18.9	.114	29	.08	–61
1.5	.17	5	12.1	4.02	78	–16.6	.148	30	.08	–73
2.0	.13	–12	10.2	3.25	59	–14.9	.179	25	.07	–90
2.5	.08	–20	8.9	2.77	46	–13.6	.209	25	.05	–112
3.0	.02	–37	7.7	2.42	31	–12.7	.232	18	.05	–134
3.5	.05	128	6.7	2.15	15	–11.9	.253	10	.06	–160
4.0	.12	113	5.7	1.92	–1	–11.3	.272	2	.06	–175
4.5	.19	97	4.8	1.73	–15	–10.8	.289	–7	.07	173
5.0	.27	80	3.9	1.56	–30	–10.6	.294	–15	.07	150

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0135, -0136
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 1.2 GHz**
- **High Gain: 18.5 dB typical at 0.5 GHz**
- **Unconditionally Stable (k>1)**
- **Cost Effective Ceramic Microstrip Package**

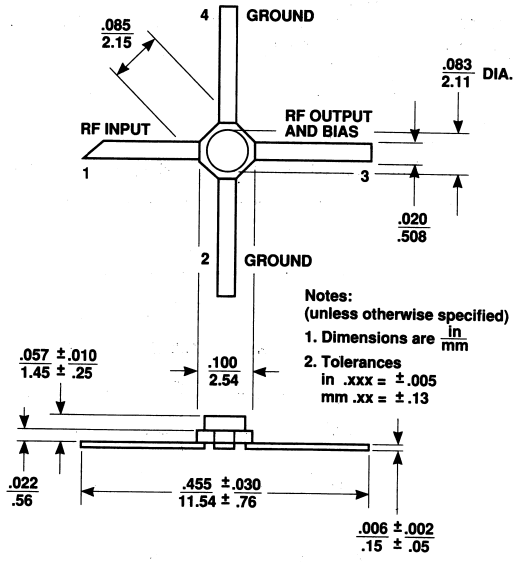
Description

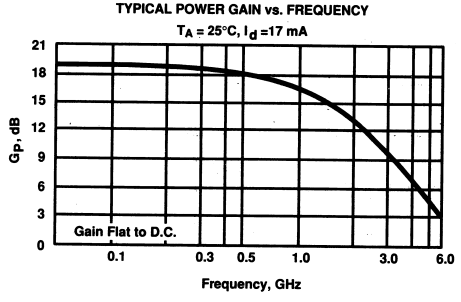
The MSA-0135 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a cost effective, microstrip package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

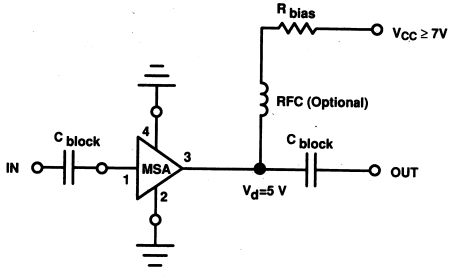
Available in cut lead version (package 36) as MSA-0136.

35 micro-X Package[1]





Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 17 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	18.0	19.0	20.0
ΔG_P	Gain Flatness	f = 0.1 to 0.6 GHz	dB		±0.6	±1.0
$f_{3\,dB}$	3 dB Bandwidth		GHz		1.2	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.3:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.3:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 0.5 GHz	dBm		1.5	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		5.5	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.0	
t_D	Group Delay	f = 0.5 GHz	psec.		160	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–9.0	

Notes: 1. Short leaded 36 package available upon request.
2. The recommended operating current range for this device is 13 mA to 25 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	40 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature[4]	–65°C to 200°C

Thermal Resistance[2,5]: θ_{jc} = 150°C/W

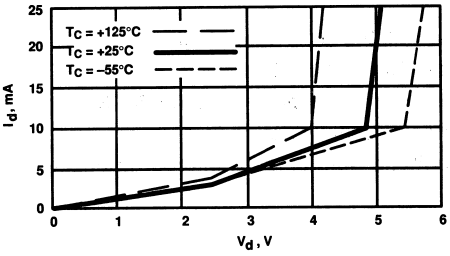
Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 6.7 mW/°C for T_C > 170°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

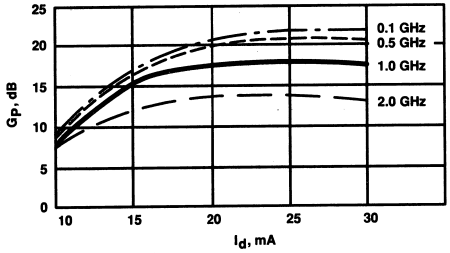
Typical Performance, T_A = 25°C

(unless otherwise noted)

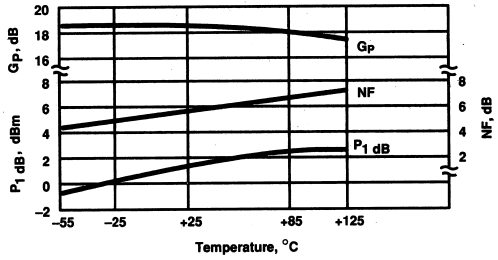
DEVICE CURRENT vs. VOLTAGE



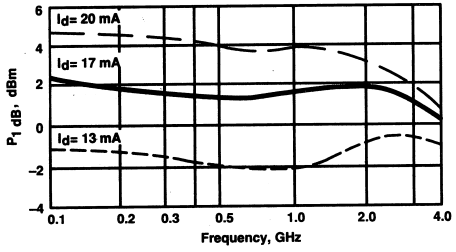
POWER GAIN vs. CURRENT



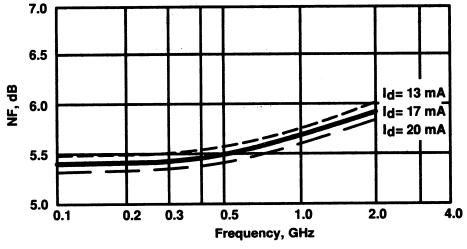
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. CASE TEMPERATURE
f = 0.5 GHz, I_d = 17 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 17 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	.08	158	19.1	9.01	172	–23.0	.071	3	.07	–2
0.2	.08	134	18.9	8.84	165	–22.4	.076	6	.07	–10
0.3	.08	116	18.7	8.65	157	–22.5	.075	12	.07	–10
0.4	.08	97	18.5	8.40	150	–22.2	.078	13	.07	–15
0.5	.09	83	18.2	8.13	143	–21.7	.082	16	.07	–17
0.6	.09	68	17.9	7.84	136	–21.6	.083	17	.07	–21
0.8	.11	47	17.2	7.25	125	–20.7	.092	22	.07	–30
1.0	.11	27	16.5	6.64	113	–19.9	.101	23	.07	–34
1.5	.11	–18	14.6	5.37	90	–18.3	.122	27	.06	–34
2.0	.09	–62	12.8	4.38	70	–16.8	.144	24	.05	–39
2.5	.08	–114	11.3	3.67	58	–16.1	.157	24	.03	–61
3.0	.12	–158	10.0	3.15	43	–15.0	.177	20	.03	–67
3.5	.18	178	8.7	2.72	28	–14.5	.189	14	.05	–88
4.0	.21	163	7.5	2.37	15	–14.0	.200	9	.10	–92
4.5	.23	145	6.4	2.10	2	–13.4	.213	4	.14	–99
5.0	.27	125	5.5	1.88	–10	–13.2	.220	–2	.15	–102

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0170
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

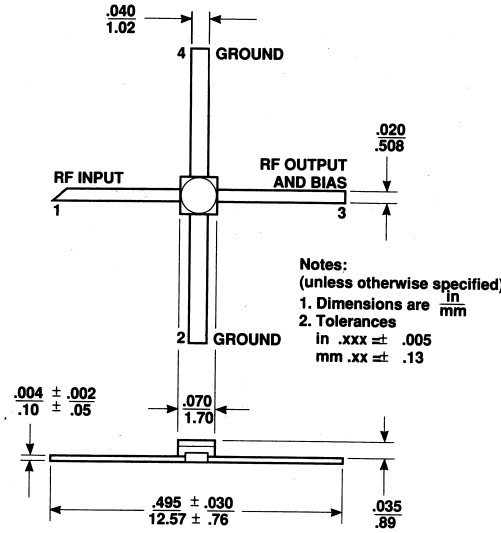
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 1.3 GHz**
- **High Gain: 18.5 dB typical at 0.5 GHz**
- **Unconditionally Stable (k>1)**
- **Hermetic Gold-ceramic Microstrip Package**

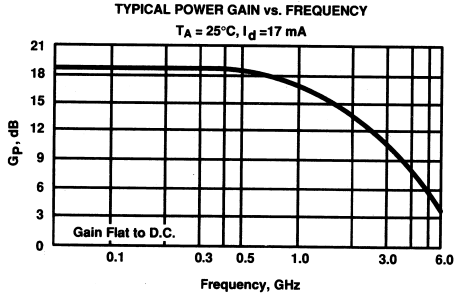
Description

The MSA-0170 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic high reliability package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

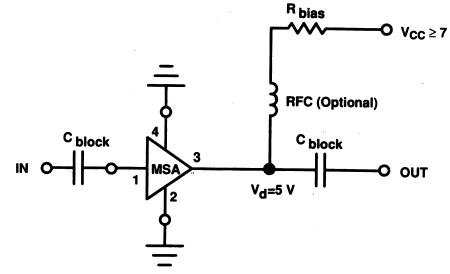
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

70 mil Package





Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 17 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	18.0	19.0	20.0
ΔG_P	Gain Flatness	f = 0.1 to 0.7 GHz	dB		±0.6	±1.0
$f_{3\ dB}$	3 dB Bandwidth		GHz		1.3	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.3:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.3:1	
$P_{1\ dB}$	Output Power @ 1 dB Gain Compression	f = 0.5 GHz	dBm		1.5	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		5.5	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.0	
t_D	Group Delay	f = 0.5 GHz	psec.		150	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–9.0	

Note: 1. The recommended operating current range for this device is 13 mA to 25 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	40 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

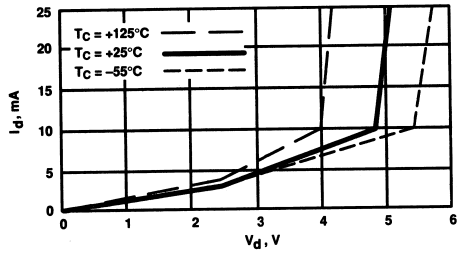
Thermal Resistance[2,4]: θ_{jc} = 125°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 8 mW/°C for T_C > 175°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

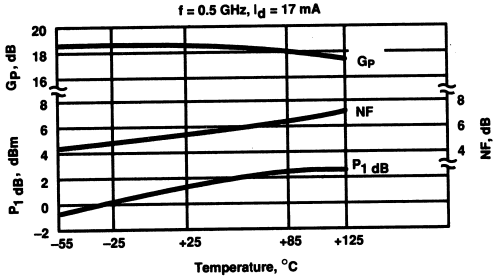
Typical Performance, T_A = 25°C

(unless otherwise noted)

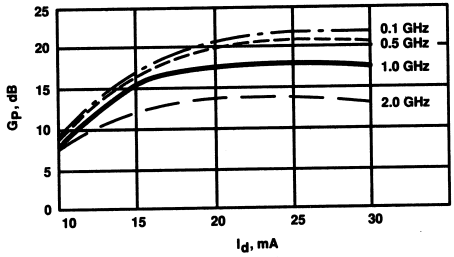
DEVICE CURRENT vs. VOLTAGE



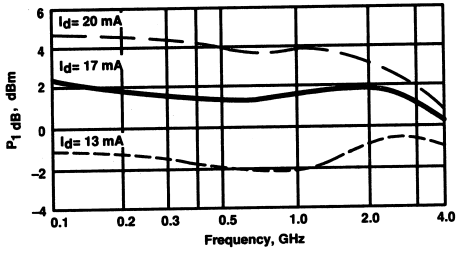
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. CASE TEMPERATURE
f = 0.5 GHz, I_d = 17 mA



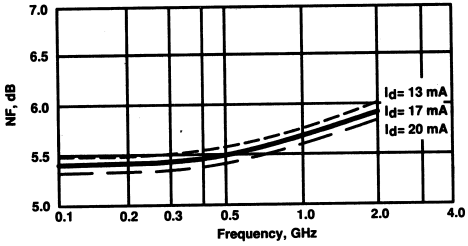
POWER GAIN vs. CURRENT



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 17 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	.08	171	19.0	8.88	173	–22.7	.073	2	.10	–13
0.2	.07	161	18.9	8.77	167	–22.5	.075	6	.11	–27
0.3	.07	152	18.7	8.64	160	–22.3	.077	8	.10	–39
0.4	.06	143	18.5	8.45	153	–22.4	.076	11	.11	–49
0.5	.05	133	18.3	8.23	147	–22.0	.079	13	.11	–59
0.6	.04	115	18.0	7.98	141	–21.8	.081	17	.12	–67
0.8	.03	79	17.5	7.46	130	–21.2	.087	20	.12	–83
1.0	.04	–14	16.8	6.90	119	–20.2	.098	23	.12	–96
1.5	.08	–52	15.0	5.64	96	–19.0	.112	26	.10	–116
2.0	.12	–87	13.2	4.58	78	–17.7	.131	24	.08	–134
2.5	.15	–112	11.7	3.85	67	–16.7	.147	25	.07	–135
3.0	.19	–132	10.3	3.27	54	–16.1	.156	22	.07	–129
3.5	.24	–148	8.9	2.80	41	–15.4	.170	18	.09	–117
4.0	.26	–159	7.7	2.43	29	–15.0	.177	13	.13	–106
4.5	.27	–170	6.6	2.14	18	–14.7	.184	8	.17	–105
5.0	.27	175	5.7	1.92	8	–14.3	.192	5	.20	–106

A model for this device is available in the DEVICE MODELS section.

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MSA-0185
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

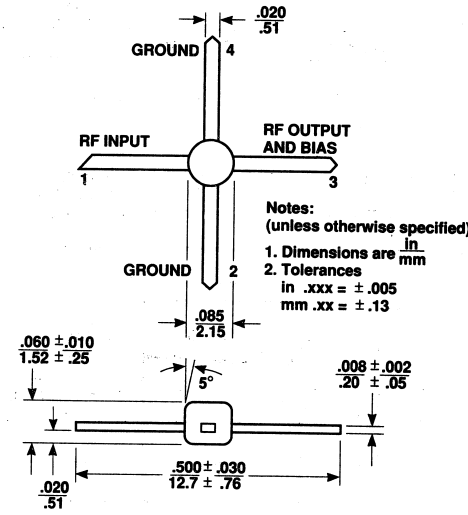
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 1.0 GHz**
- **High Gain: 17.5 dB typical at 0.5 GHz**
- **Unconditionally Stable (k>1)**
- **Low Cost Plastic Package**

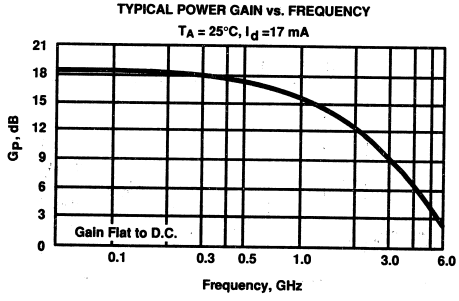
Description

The MSA-0185 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

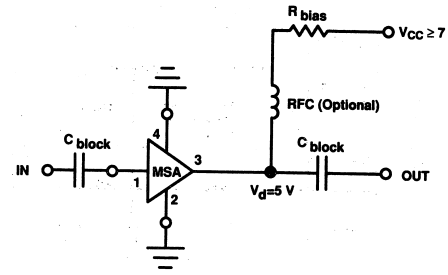
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

85 Plastic Package





Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 17 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 0.5 GHz	dB	 16.0	18.5 17.5	
ΔG_P	Gain Flatness	f = 0.1 to 0.6 GHz	dB		±0.6	
$f_{3\,dB}$	3 dB Bandwidth		GHz		1.0	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.3:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.3:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 0.5 GHz	dBm		1.5	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		5.5	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.0	
t_D	Group Delay	f = 0.5 GHz	psec.		150	
V_d	Device Voltage		V	4.0	5.0	6.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–9.0	

Note: 1. The recommended operating current range for this device is 13 mA to 25 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	40 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

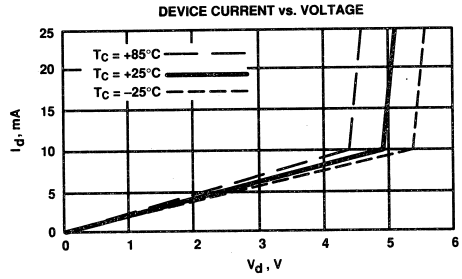
Thermal Resistance[2,4]: θ_{jc} = 105°C/W

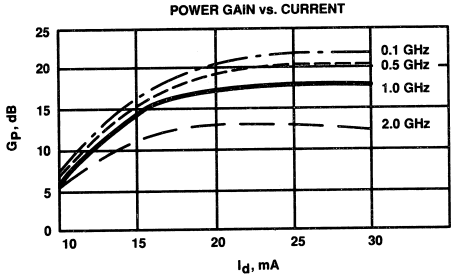
Notes:

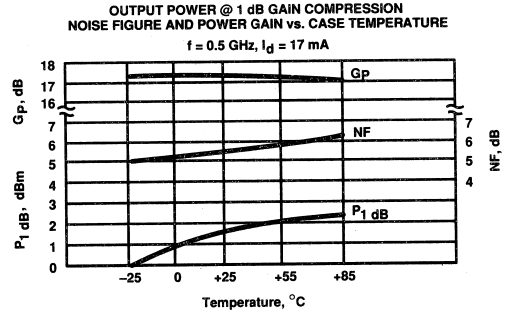
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 9.5 mW/°C for T_C > 129°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

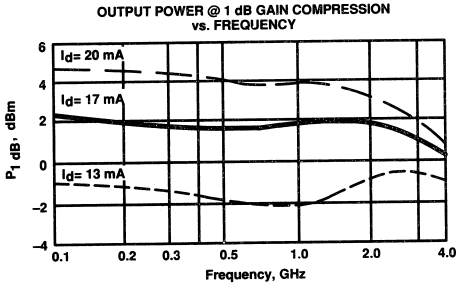
Typical Performance, T_A = 25°C

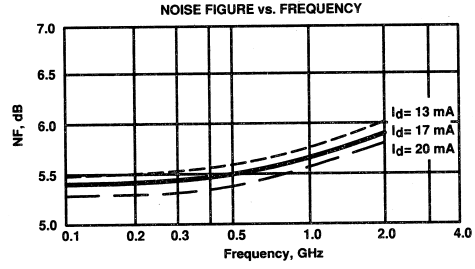
(unless otherwise noted)











Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 17 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	.06	166	18.4	8.36	172	–22.6	.074	3	.07	–17
0.2	.06	149	18.3	8.20	165	–22.0	.079	8	.07	–28
0.3	.06	133	18.1	8.01	158	–22.2	.078	11	.08	–43
0.4	.06	120	17.8	7.78	151	–21.9	.080	14	.09	–56
0.5	.06	105	17.5	7.53	144	–21.4	.085	18	.09	–68
0.6	.06	94	17.2	7.23	138	–21.4	.085	19	.09	–75
0.8	.07	72	16.5	6.66	127	–20.7	.092	24	.10	–89
1.0	.07	49	15.7	6.09	116	–19.7	.104	27	.10	–100
1.5	.07	12	13.8	4.89	94	–18.0	.126	32	.11	–120
2.0	.04	–13	12.0	3.98	76	–16.2	.154	31	.11	–134
2.5	.03	–84	10.6	3.38	65	–15.1	.175	33	.11	–138
3.0	.07	–159	9.2	2.88	52	–14.2	.194	29	.09	–146
3.5	.12	–174	8.0	2.50	38	–13.3	.216	24	.08	–135
4.0	.16	170	6.8	2.19	26	–12.8	.229	19	.08	–120
4.5	.21	150	5.7	1.93	14	–12.3	.242	13	.08	–107
5.0	.25	126	4.7	1.72	3	–12.2	.245	–6	.07	–110

A model for this device is available in the DEVICE MODELS section.

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MSA-0186
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

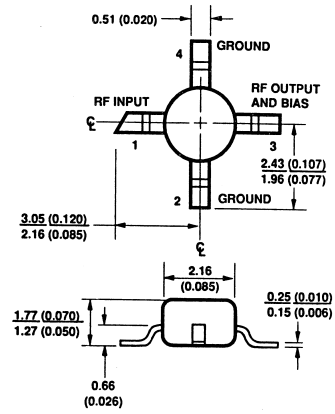
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 0.9 GHz**
- **High Gain: 17.5 dB typical at 0.5 GHz**
- **Unconditionally Stable (k>1)**
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Description

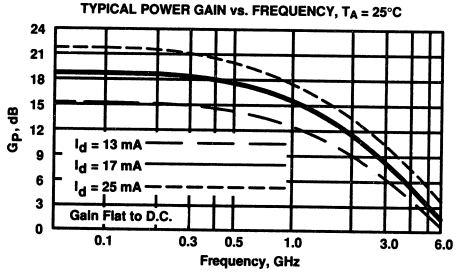
The MSA-0186 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost, surface mount plastic package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

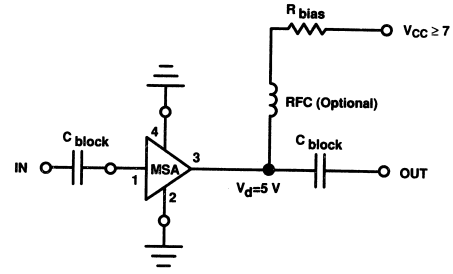
86 Plastic Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)



Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 17 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 0.5 GHz	dB	15.5	18.5 17.5	
ΔG_P	Gain Flatness	f = 0.1 to 0.6 GHz	dB		±0.7	
$f_{3\,dB}$	3 dB Bandwidth		GHz		0.9	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.3:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.2:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 0.5 GHz	dBm		1.5	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		5.5	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.0	
t_D	Group Delay	f = 0.5 GHz	psec.		200	
V_d	Device Voltage		V	4.0	5.0	6.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–9.0	

Notes: 1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices".
2. The recommended operating current range for this device is 13 mA to 25 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	40 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

Thermal Resistance[2,4]: θ_{jc} = 115°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 8.7 mW/°C for T_C > 127°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Part Number Ordering Information

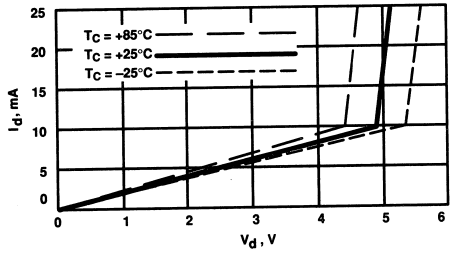
Part Number	Devices Per Reel	Reel Size
MSA-0186-TR1	1000	7"
MSA-0186-TR2	4000	13"

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

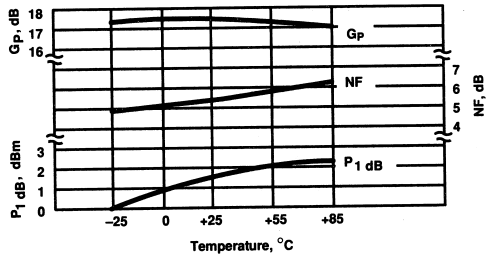
Typical Performance, T_A = 25°C

(unless otherwise noted)

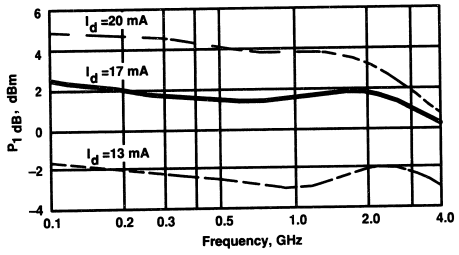
DEVICE CURRENT vs. VOLTAGE



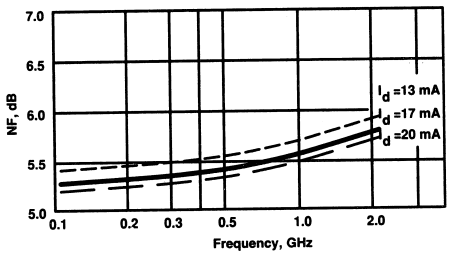
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. CASE TEMPERATURE
f = 0.5 GHz, I_d= 17 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 17 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.05	148	18.5	8.39	171	–23.0	.071	4	.08	–7
0.2	.06	124	18.3	8.22	162	–22.8	.073	9	.08	–14
0.3	.07	103	18.1	8.03	154	–22.6	.074	13	.07	–24
0.4	.08	89	17.7	7.67	146	–22.2	.078	14	.07	–31
0.5	.08	76	17.4	7.42	139	–21.9	.081	17	.06	–39
0.6	.09	66	17.0	7.06	131	–21.4	.085	21	.06	–47
0.8	.10	50	16.2	6.47	119	–20.5	.094	25	.07	–67
1.0	.10	35	15.3	5.83	107	–19.6	.105	29	.07	–89
1.5	.07	12	13.2	4.57	83	–17.7	.131	30	.08	–165
2.0	.02	–12	11.3	3.67	64	–16.1	.157	27	.08	156
2.5	.06	165	9.8	3.09	50	–14.8	.182	24	.08	134
3.0	.14	150	8.3	2.60	34	–13.9	.202	19	.09	124
3.5	.23	137	7.0	2.24	20	–13.4	.213	12	.09	117
4.0	.31	125	5.7	1.93	6	–13.0	.223	5	.09	114
5.0	.45	105	3.3	1.46	–17	–12.7	.231	–5	.09	132

A model for this device is available in the DEVICE MODELS section.

MSA-0200
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 2.8 GHz**
- **12.0 dB typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**

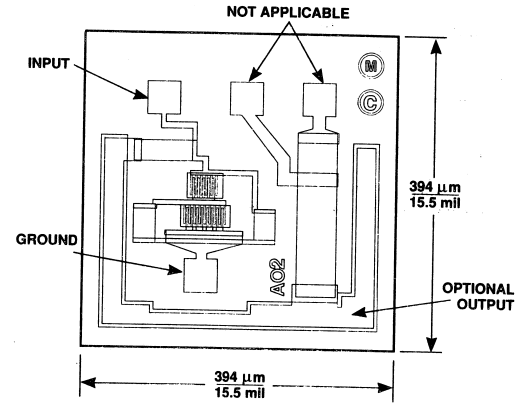
Description

The MSA-0200 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial, industrial and military applications.

The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

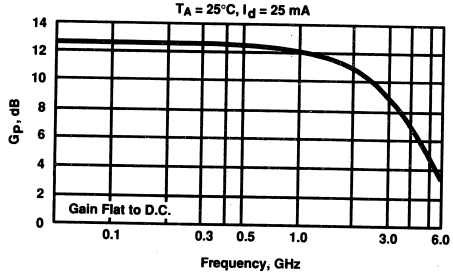
The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire. See APPLICATIONS section, "Chip Use".

Chip Outline[1]

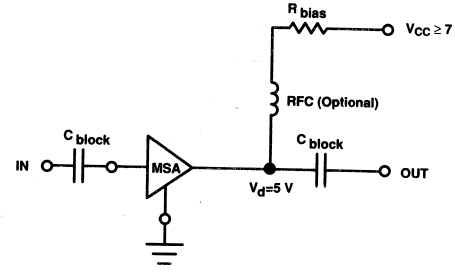


Unless otherwise specified, tolerances are ±13 µm / ±0.5 mils.
Chip thickness is 114 µm / 4.5 mil. Bond pads are 41 µm / 1.6 mil typical on each side.
*** Output contact is made by die attaching the backside of the die.**

TYPICAL POWER GAIN vs. FREQUENCY
T_A = 25°C, I_d = 25 mA



Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions[3]: I_d = 25 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		12.5	
ΔG_P	Gain Flatness	f = 0.1 to 1.8 GHz	dB		±0.6	
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.8	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.4:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.4:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		4.5	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		17.0	
t_D	Group Delay	f = 1.0 GHz	psec.		125	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		−8.0	

Notes: 1. This chip contains additional biasing options. The performance specified applies only to the bias option whose bond pads are indicated on the chip outline. Refer to the APPLICATIONS section "MODAMP™ Silicon MMIC Chip Use" for additional information.
2. The recommended operating current range for this device is 18 mA to 40 mA. Typical performance as a function of current is on the following page.
3. RF performance of the chip is determined by packaging and testing 10 devices per wafer in a dual ground configuration.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	325 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 35°C/W

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{MOUNTING\ SURFACE}$ = 25°C
3. Derate at 28.6 mW/°C for $T_{MOUNTING\ SURFACE}$ > 189°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

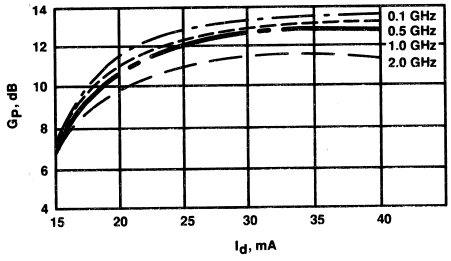
Part Number Ordering Information

Part Number	Devices Per Tray
MSA-0200-GP2	10
MSA-0200-GP4	100
MSA-0200-GP6	up to 300

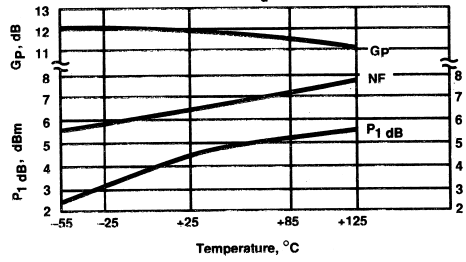
Typical Performance, T_A = 25°C

(unless otherwise noted)

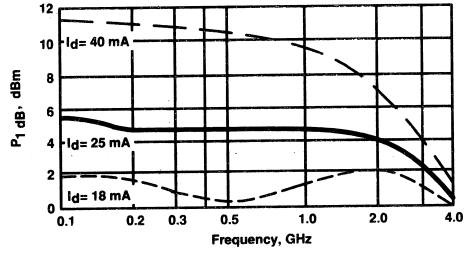
POWER GAIN vs. CURRENT



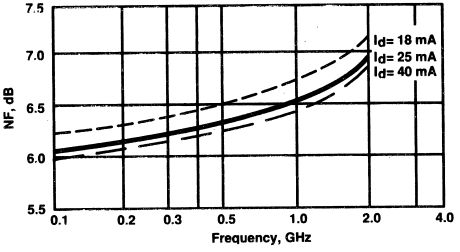
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. MOUNTING
SURFACE TEMPERATURE
f = 1.0 GHz, Id = 25 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters[4]: Z_O = 50 Ω

T_A = 25°C, I_d = 25 mA

Freq. GHz	S11 Mag	S11 Ang	S21 dB	S21 Mag	S21 Ang	S12 dB	S12 Mag	S12 Ang	S22 Mag	S22 Ang
0.1	.11	179	12.6	4.27	177	–18.4	.120	1	.11	–7
0.2	.11	174	12.6	4.26	172	–18.6	.117	4	.11	–12
0.4	.10	170	12.5	4.24	165	–18.4	.120	5	.12	–25
0.6	.09	166	12.5	4.22	158	–18.2	.123	7	.13	–38
0.8	.08	162	12.4	4.17	152	–18.2	.123	10	.13	–47
1.0	.06	161	12.3	4.13	144	–18.0	.126	13	.14	–55
1.5	.02	–170	12.0	3.99	126	–17.3	.137	17	.15	–72
2.0	.05	–105	11.5	3.74	109	–16.4	.152	20	.15	–89
2.5	.10	–103	10.8	3.46	97	–15.8	.163	25	.13	–91
3.0	.17	–124	9.8	3.10	83	–15.3	.172	26	.11	–100
3.5	.22	–137	8.7	2.71	68	–14.7	.184	22	.13	–94
4.0	.26	–144	7.4	2.35	55	–14.3	.192	22	.16	–85
5.0	.29	–165	5.1	1.80	35	–13.8	.203	17	.22	–76
6.0	.33	162	3.3	1.46	20	–13.5	.211	14	.23	–82

Note: 4. S-parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0204
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

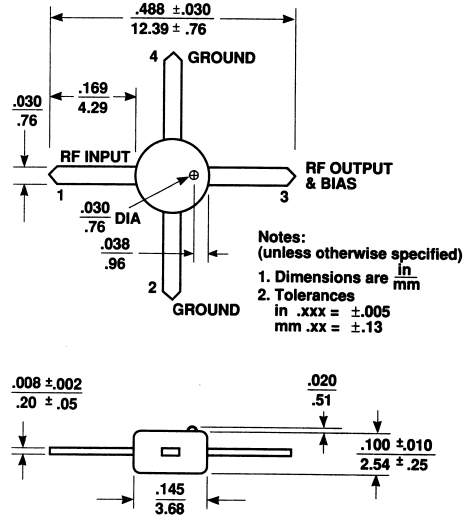
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 1.8 GHz**
- **11.0 dB typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Low Cost Plastic Package**

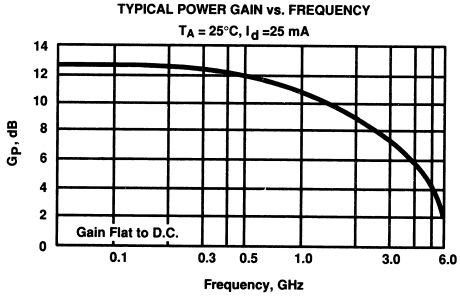
Description

The MSA-0204 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

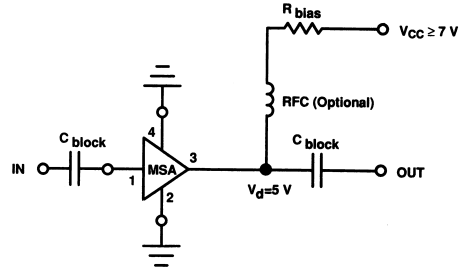
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

04A Plastic Package





Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 25 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 0.5 GHz f = 1.0 GHz	dB	10.0	12.5 12.0 11.0	
ΔG_P	Gain Flatness	f = 0.1 to 1.4 GHz	dB		±1.0	
$f_{3\ dB}$	3 dB Bandwidth		GHz		1.8	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.3:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.3:1	
$P_{1\ dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		4.5	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		17.0	
t_D	Group Delay	f = 1.0 GHz	psec.		150	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note: 1. The recommended operating current range for this device is 18 mA to 40 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	325 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

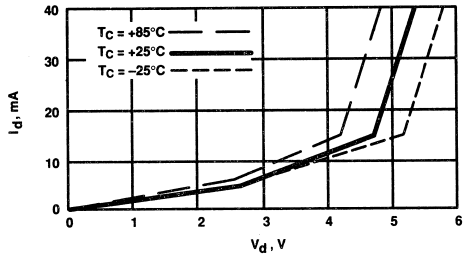
Thermal Resistance[2,4]: θ_{jc} = 90°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 11.1 mW/°C for T_C > 121°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

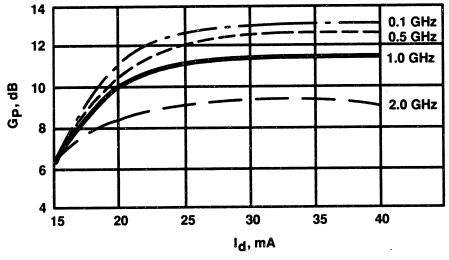
Typical Performance, T_A = 25°C

(unless otherwise noted)

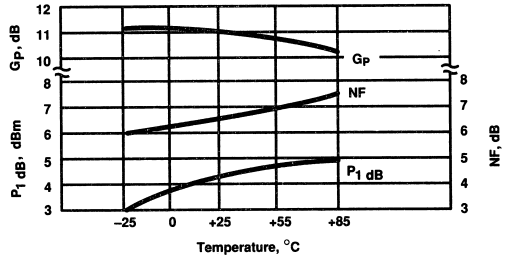
DEVICE CURRENT vs. VOLTAGE



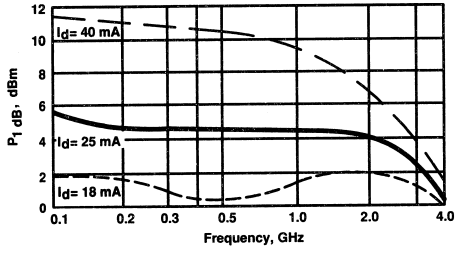
POWER GAIN vs. CURRENT



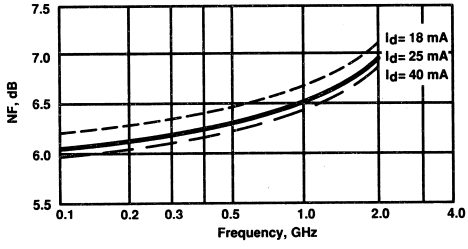
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. CASE TEMPERATURE
f = 1.0 GHz, I_d = 25 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 25 mA

Freq. GHz	S11 Mag	S11 Ang	S21 dB	S21 Mag	S21 Ang	S12 dB	S12 Mag	S12 Ang	S22 Mag	S22 Ang
0.1	.12	170	12.5	4.20	174	–18.5	.119	2	.12	–7
0.2	.12	160	12.4	4.16	168	–18.5	.119	4	.12	–14
0.4	.11	140	12.2	4.05	156	–18.1	.124	6	.12	–29
0.6	.11	121	11.9	3.93	144	–17.9	.127	8	.12	–42
0.8	.10	104	11.6	3.78	134	–17.6	.132	12	.12	–52
1.0	.10	84	11.2	3.62	123	–17.0	.142	14	.13	–61
1.5	.09	42	10.2	3.22	99	–16.1	.157	16	.12	–79
2.0	.07	16	9.1	2.86	77	–14.8	.181	15	.11	–96
2.5	.05	17	8.2	2.57	63	–13.9	.202	16	.09	–115
3.0	.02	95	7.3	2.32	46	–13.2	.220	13	.08	–141
3.5	.08	112	6.5	2.12	29	–12.4	.239	7	.09	–167
4.0	.14	100	5.7	1.93	12	–11.8	.258	0	.11	171
5.0	.35	72	4.0	1.58	–22	–11.2	.276	–15	.17	120
6.0	.59	51	1.6	1.20	–54	–11.3	.272	–33	.32	80

A model for this device is available in the DEVICE MODELS section.

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MSA-0235, -0236
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 2.7 GHz**
- **12.0 dB typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Cost Effective Ceramic Microstrip Package**

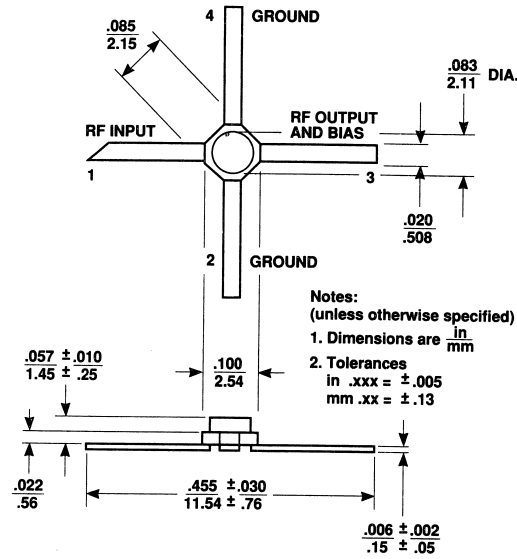
Description

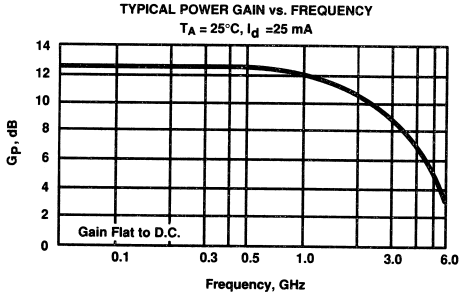
The MSA-0235 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a cost effective, microstrip package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

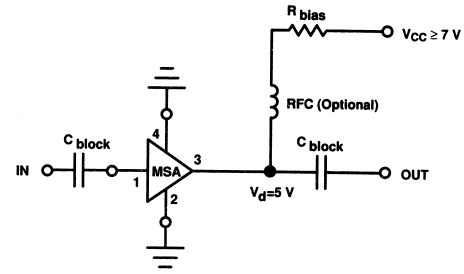
Available in cut lead version (package 36) as MSA-0236.

35 micro-X Package[1]





Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 25 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	11.5	12.5	13.5
ΔG_P	Gain Flatness	f = 0.1 to 1.6 GHz	dB		±0.6	±1.0
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.7	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.2:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.4:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		4.5	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		17.0	
t_D	Group Delay	f = 1.0 GHz	psec.		125	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes: 1. Short leaded 36 package available upon request.
2. The recommended operating current range for this device is 18 mA to 40 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	325 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature[4]	–65°C to 200°C

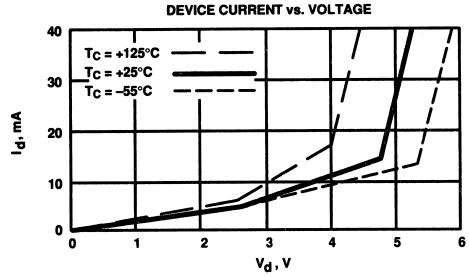
Thermal Resistance[2,5]: θ_{jc} = 145°C/W

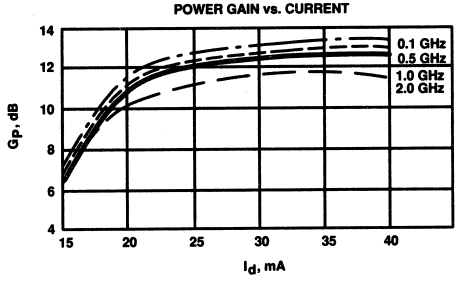
Notes:

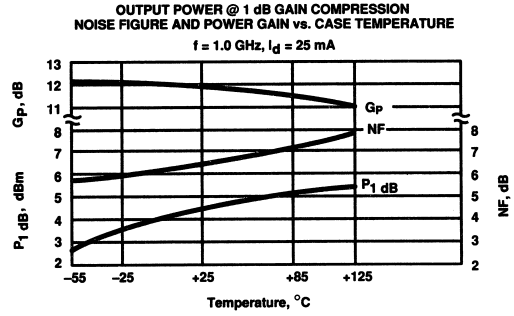
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 6.9 mW/°C for T_C > 153°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

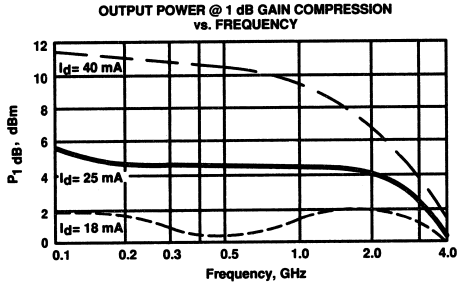
Typical Performance, T_A = 25°C

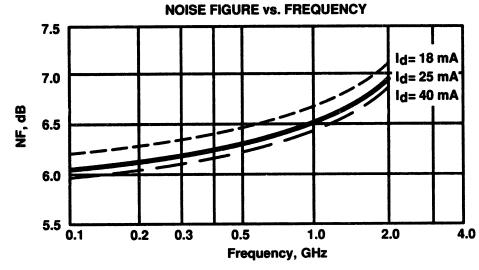
(unless otherwise noted)











Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 25 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.08	170	12.6	4.25	176	–18.6	.118	2	.16	–6
0.2	.08	163	12.5	4.23	171	–18.5	.119	2	.15	–10
0.4	.08	147	12.5	4.19	161	–18.4	.120	4	.15	–21
0.6	.08	130	12.4	4.14	152	–18.3	.121	4	.15	–30
0.8	.07	112	12.2	4.09	143	–18.1	.125	7	.15	–39
1.0	.07	91	12.1	4.02	134	–18.0	.126	10	.15	–46
1.5	.06	47	11.6	3.80	112	–17.3	.137	11	.13	–66
2.0	.03	–1	11.0	3.53	91	–16.3	.153	10	.11	–89
2.5	.03	–115	10.2	3.24	75	–15.4	.169	12	.09	–111
3.0	.09	–157	9.3	2.92	57	–15.1	.176	8	.08	–127
3.5	.16	–175	8.3	2.60	39	–14.4	.190	3	.09	–129
4.0	.20	173	7.2	2.29	23	–14.1	.198	–2	.11	–118
5.0	.27	136	5.2	1.81	–6	–13.5	.211	–11	.15	–117
6.0	.41	94	3.2	1.44	–33	–13.5	.212	–24	.11	–148

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0270
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

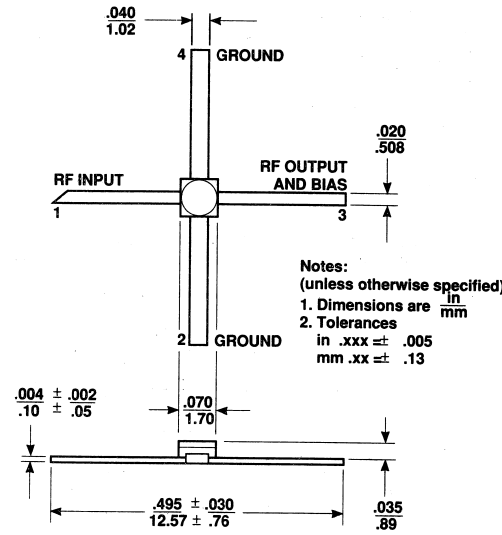
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 2.8 GHz**
- **12.0 dB typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Hermetic Gold-ceramic Microstrip Package**

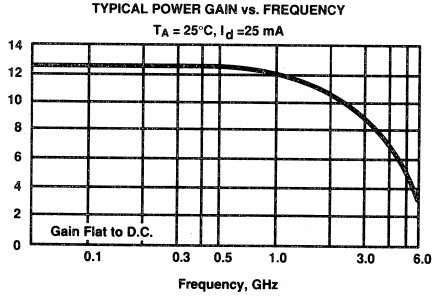
Description

The MSA-0270 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic, high reliability package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

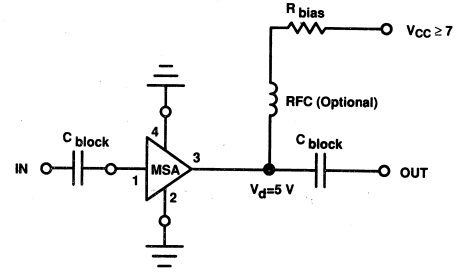
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

70 mil Package





Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 25 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	11.5	12.5	13.5
ΔG_P	Gain Flatness	f = 0.1 to 1.8 GHz	dB		±0.6	±1.0
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.8	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.4:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.4:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		4.5	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		17.0	
t_D	Group Delay	f = 1.0 GHz	psec.		125	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note: 1. The recommended operating current range for this device is 18 mA to 40 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	325 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

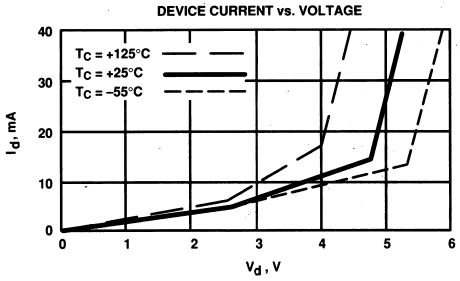
Thermal Resistance[2,4]: θ_{jc} = 120°C/W

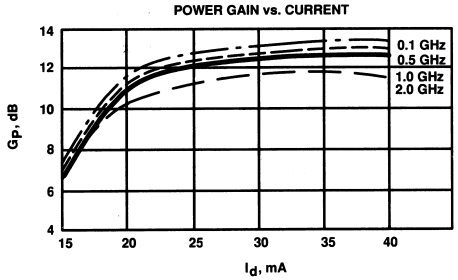
Notes:

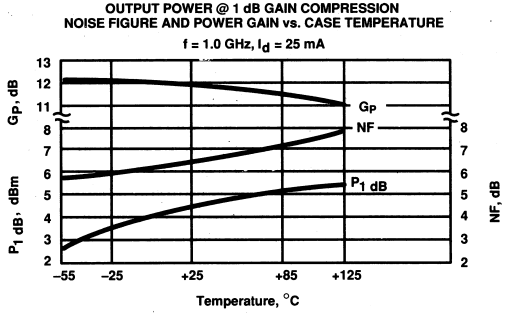
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 8.3 mW/°C for T_C > 161°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

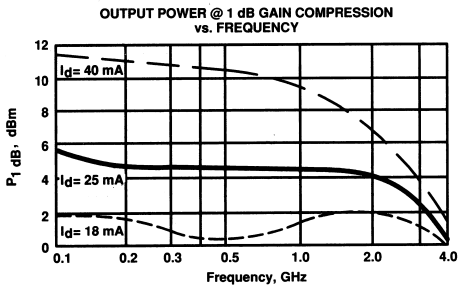
Typical Performance, T_A = 25°C

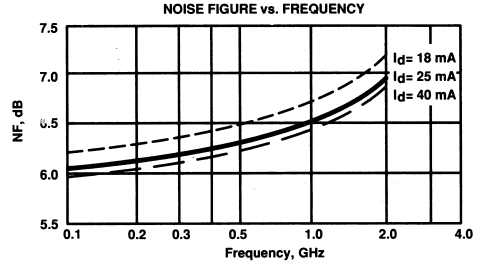
(unless otherwise noted)











Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 25 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.11	179	12.6	4.26	176	–18.4	.120	1	.12	–8
0.2	.11	174	12.6	4.24	171	–18.6	.117	3	.12	–15
0.4	.10	169	12.5	4.21	162	–18.4	.120	4	.13	–30
0.6	.09	165	12.4	4.17	154	–18.2	.123	5	.14	–44
0.8	.08	161	12.3	4.11	146	–18.2	.123	7	.14	–55
1.0	.06	161	12.2	4.05	137	–18.0	.126	9	.15	–64
1.5	.02	–150	11.7	3.85	116	–17.2	.138	11	.16	–84
2.0	.06	–110	11.1	3.57	96	–16.3	.153	11	.16	–102
2.5	.11	–112	10.3	3.27	82	–15.7	.165	14	.14	–106
3.0	.17	–134	9.3	2.92	65	–15.2	.174	12	.13	–114
3.5	.22	–147	8.2	2.56	48	–14.7	.185	6	.15	–111
4.0	.26	–156	7.0	2.23	33	–14.3	.192	3	.19	–107
5.0	.28	–179	4.7	1.72	8	–14.0	.199	–6	.27	–107
6.0	.30	143	3.0	1.41	–13	–13.8	.204	–14	.29	–119

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0285
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

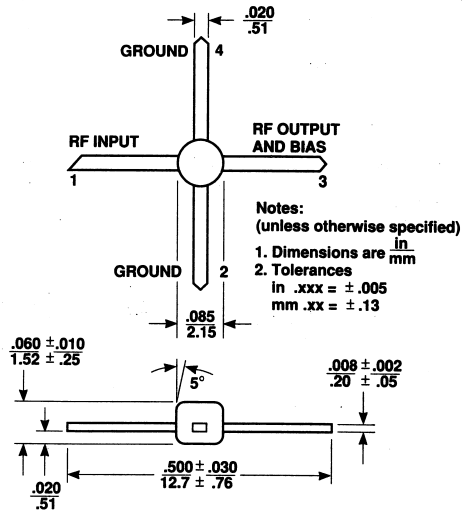
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 2.6 GHz**
- **12.0 dB typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Low Cost Plastic Package**

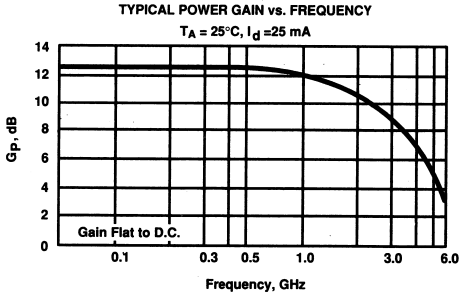
Description

The MSA-0285 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

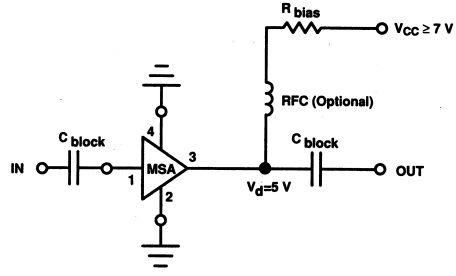
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

85 Plastic Package





Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 25 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz	dB	 10.0	12.5 12.0	
ΔG_P	Gain Flatness	f = 0.1 to 1.6 GHz	dB		±0.6	
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.6	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.3:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.4:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		4.5	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		17.0	
t_D	Group Delay	f = 1.0 GHz	psec.		125	
V_d	Device Voltage		V	4.0	5.0	6.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note: 1. The recommended operating current range for this device is 18 mA to 40 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

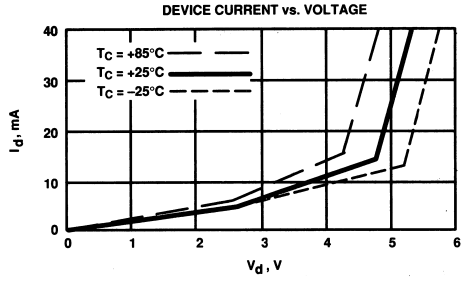
Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	325 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

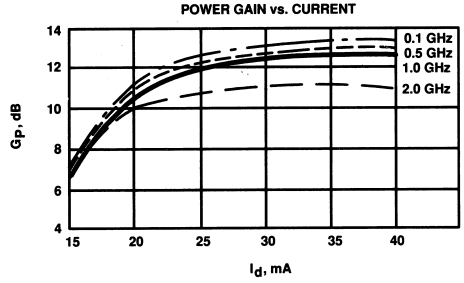
Thermal Resistance[2,4]: θ_{jc} = 95°C/W

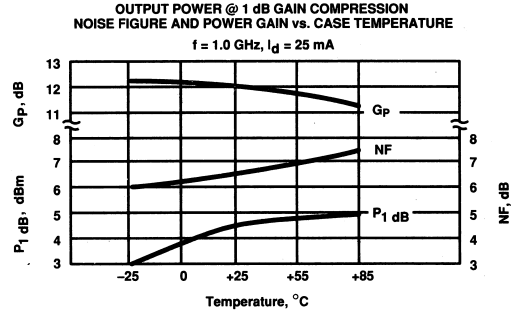
Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 10.5 mW/°C for T_C > 119°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

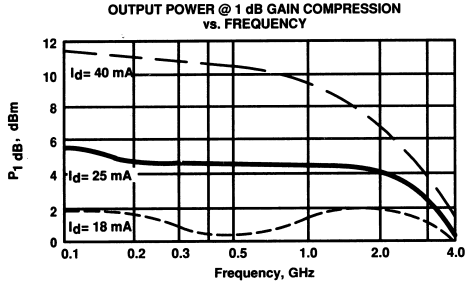
Typical Performance, T_A = 25°C

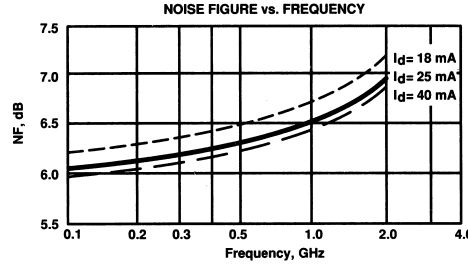
(unless otherwise noted)











Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 25 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.10	174	12.6	4.25	175	–18.6	.118	2	.14	–7
0.2	.10	168	12.5	4.22	171	–18.5	.119	3	.13	–12
0.4	.10	157	12.4	4.17	161	–18.3	.122	6	.14	–26
0.6	.09	143	12.3	4.10	153	–18.3	.121	7	.14	–38
0.8	.08	132	12.1	4.03	144	–18.0	.126	11	.14	–48
1.0	.08	122	11.9	3.95	135	–17.5	.133	12	.14	–60
1.5	.04	95	11.4	3.70	115	–17.0	.142	16	.13	–85
2.0	.02	117	10.6	3.40	95	–16.0	.158	17	.12	–110
2.5	.05	–173	9.9	3.11	82	–15.0	.177	20	.12	–128
3.0	.12	–175	8.9	2.78	65	–14.7	.185	19	.11	–148
3.5	.16	179	7.9	2.49	49	–14.0	.199	14	.10	–145
4.0	.21	169	6.9	2.22	35	–13.7	.207	11	.10	–134
5.0	.28	139	5.0	1.77	9	–13.0	.224	4	.12	–118
6.0	.41	100	3.0	1.42	–16	–12.9	.226	–5	.09	–154

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0286
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

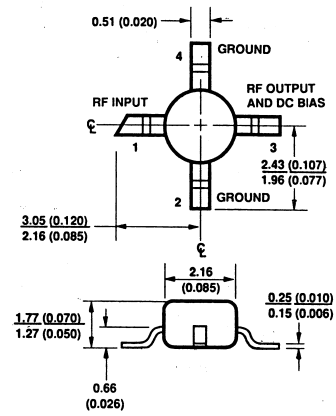
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 2.5 GHz**
- **12.0 dB typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Description

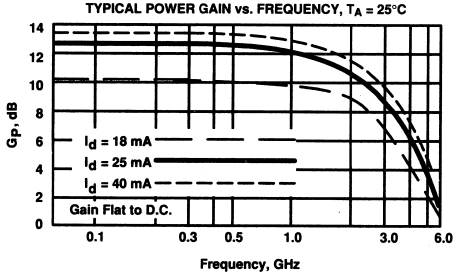
The MSA-0286 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost, surface mount plastic package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

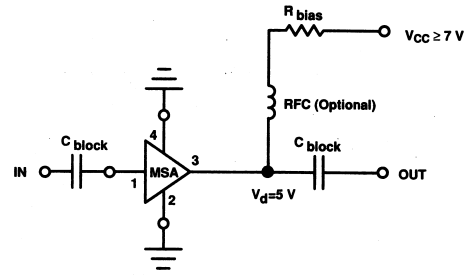
86 Plastic Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)



Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 25 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz	dB	 10.0	12.5 12.0	
ΔG_P	Gain Flatness	f = 0.1 to 1.6 GHz	dB		±0.6	
$f_{3\ dB}$	3 dB Bandwidth		GHz		2.5	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.5:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.4:1	
$P_{1\ dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		4.5	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		17.0	
t_D	Group Delay	f = 1.0 GHz	psec.		140	
V_d	Device Voltage		V	4.0	5.0	6.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes: 1. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors".
2. The recommended operating current range for this device is 18 mA to 40 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	325 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

Thermal Resistance[2,4]: θ_{jc} = 105°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 9.5 mW/°C for T_C > 116°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Part Number Ordering Information

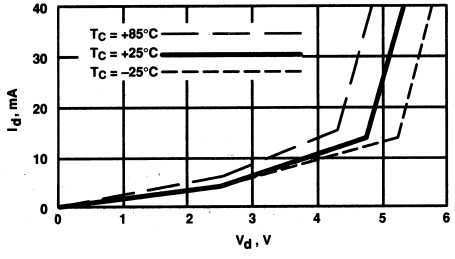
Part Number	Devices Per Reel	Reel Size
MSA-0286-TR1	1000	7"
MSA-0286-TR2	4000	13"

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

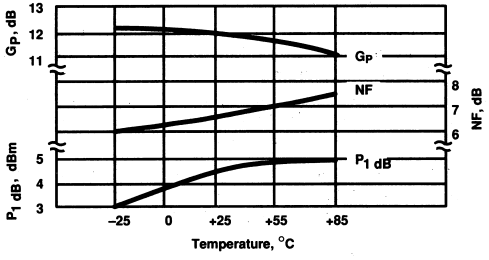
Typical Performance, T_A = 25°C

(unless otherwise noted)

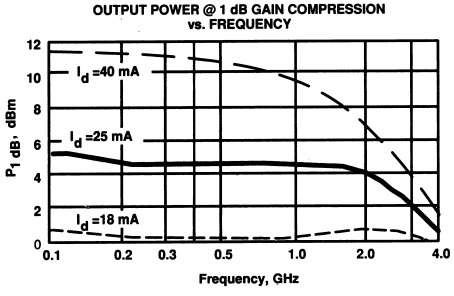
DEVICE CURRENT vs. VOLTAGE



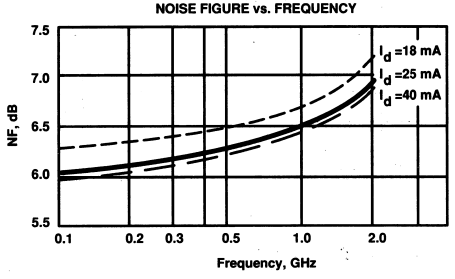
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. CASE TEMPERATURE
f = 1.0 GHz, I_d = 25 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 25 mA

Freq. GHz	S11		S21			S12			S22	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.10	171	12.5	4.22	175	–18.5	.119	1	.16	–5
0.2	.10	161	12.5	4.20	170	–18.3	.121	3	.16	–11
0.4	.10	144	12.4	4.16	159	–18.2	.122	6	.15	–24
0.6	.09	129	12.2	4.09	149	–18.0	.126	6	.15	–36
0.8	.08	119	12.1	4.01	139	–18.0	.127	9	.14	–48
1.0	.08	108	11.9	3.91	129	–17.4	.135	8	.14	–62
1.5	.06	111	11.3	3.67	106	–16.5	.149	12	.11	–99
2.0	.08	141	10.5	3.35	84	–15.7	.164	11	.11	–141
2.5	.14	150	9.6	3.01	67	–14.8	.182	9	.12	–176
3.0	.21	142	8.6	2.68	48	–14.3	.194	5	.13	155
3.5	.29	132	7.5	2.37	30	–14.0	.200	1	.14	140
4.0	.36	121	6.4	2.09	15	–13.5	.211	–3	.16	134
5.0	.50	101	4.1	1.61	–12	–13.3	.216	–12	.20	132

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0300
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 2.8 GHz**
- **12.0 dB typical Gain at 1.0 GHz**
- **10.0 dBm typical $P_{1\,dB}$ at 1.0 GHz**

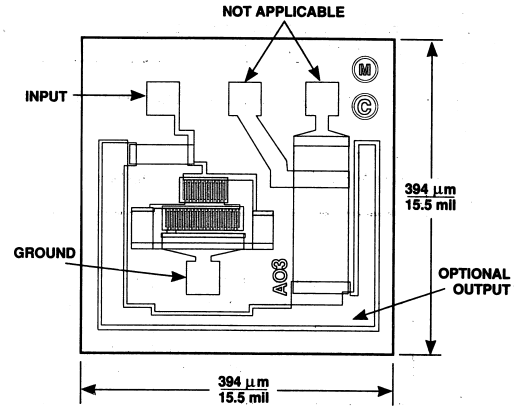
Description

The MSA-0300 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial, industrial and military applications.

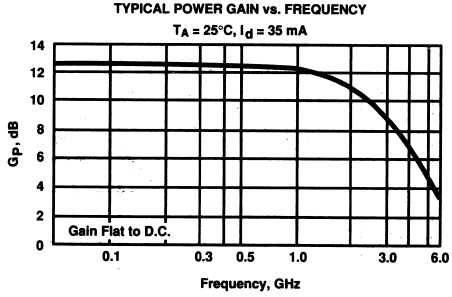
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire. See APPLICATIONS section, "Chip Use".

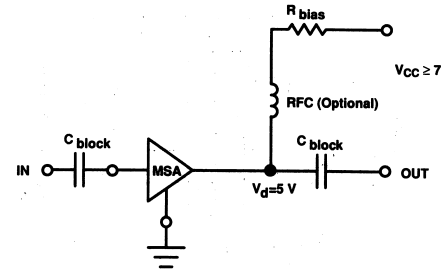
Chip Outline[1]



Unless otherwise specified, tolerances are ±13 µm / ±0.5 mils.
Chip thickness is 114 µm / 4.5 mil. Bond pads are 41 µm / 1.6 mil typical on each side.
*** Output contact is made by die attaching the backside of the die.**



Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions[3]: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		12.5	
ΔG_P	Gain Flatness	f = 0.1 to 1.8 GHz	dB		±0.6	
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.8	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.8:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.8:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		10.0	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		23.0	
t_D	Group Delay	f = 1.0 GHz	psec.		125	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes: 1. This chip contains additional biasing options. The performance specified applies only to the bias option whose bond pads are indicated on the chip outline. Refer to the APPLICATIONS section "MODAMP™ Silicon MMIC Chip Use" for additional information.
2. The recommended operating current range for this device is 20 mA to 50 mA. Typical performance as a function of current is on the following page.
3. RF performance of the chip is determined by packaging and testing 10 devices per wafer in a dual ground configuration.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	425 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 45°C/W

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 22.2 mW/°C for T_C > 181°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

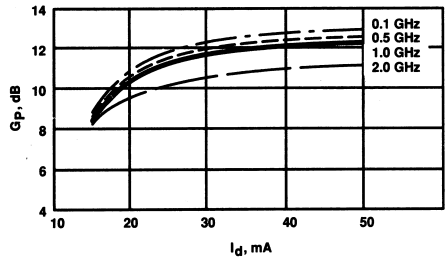
Part Number Ordering Information

Part Number	Devices Per Tray
MSA-0300-GP2	10
MSA-0300-GP4	100
MSA-0300-GP6	up to 300

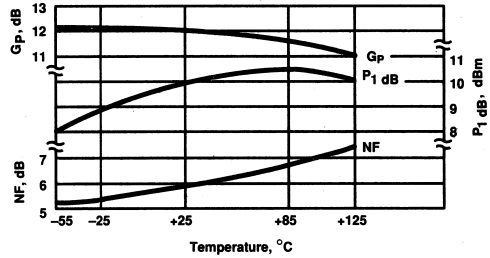
Typical Performance, T_A = 25°C

(unless otherwise noted)

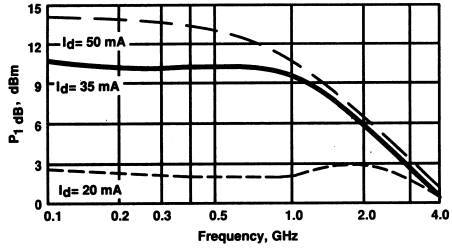
POWER GAIN vs. CURRENT



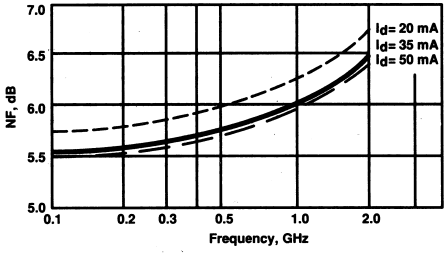
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. MOUNTING
SURFACE TEMPERATURE
f = 1.0 GHz, I_d = 35 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters[4]: Z_O = 50 Ω

T_A = 25°C, I_d = 35 mA

Freq. GHz	S11 Mag	S11 Ang	S21 dB	S21 Mag	S21 Ang	S12 dB	S12 Mag	S12 Ang	S22 Mag	S22 Ang	k
0.1	.13	–179	12.6	4.28	177	–18.6	.118	2	.09	–13	1.21
0.2	.13	–179	12.6	4.27	172	–18.3	.121	3	.10	–27	1.19
0.4	.12	–179	12.5	4.24	165	–18.3	.121	5	.12	–48	1.19
0.6	.11	–177	12.5	4.22	158	–18.2	.123	8	.14	–65	1.18
0.8	.11	–172	12.4	4.19	152	–17.8	.129	11	.17	–76	1.15
1.0	.10	–166	12.4	4.15	144	–17.7	.130	12	.20	–85	1.14
1.5	.11	–145	12.0	4.00	126	–17.1	.139	17	.24	–104	1.09
2.0	.16	–140	11.5	3.76	109	–16.2	.154	20	.27	–122	1.03
2.5	.23	–141	10.8	3.47	97	–15.6	.166	25	.28	–133	0.99
3.0	.29	–149	9.8	3.10	82	–15.2	.173	24	.28	–145	0.99
3.5	.35	–157	8.7	2.72	67	–14.5	.188	22	.27	–148	0.97
4.0	.38	–164	7.6	2.40	55	–14.3	.193	21	.25	–146	1.00
5.0	.41	179	5.5	1.88	35	–13.7	.206	17	.21	–134	1.14
6.0	.43	153	3.6	1.51	18	–13.3	.217	14	.21	–137	1.27

Note: 4. S-parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section.

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MSA-0304
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

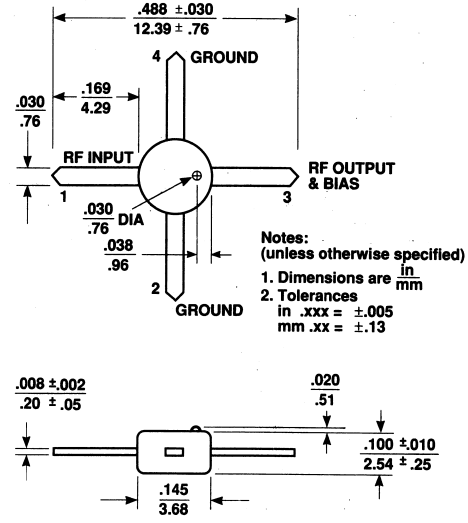
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 1.6 GHz**
- **11.0 dB typical Gain at 1.0 GHz**
- **10.0 dBm typical $P_{1\,dB}$ at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Low Cost Plastic Package**

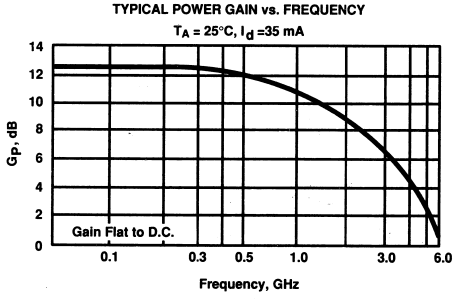
Description

The MSA-0304 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

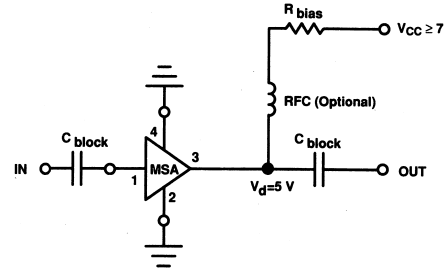
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

04A Plastic Package





Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 0.5 GHz f = 1.0 GHz	dB	10.0	12.5 12.0 11.0	
ΔG_P	Gain Flatness	f = 0.1 to 1.3 GHz	dB		±1.0	
$f_{3\,dB}$	3 dB Bandwidth		GHz		1.6	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.3:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.6:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		10.0	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		23.0	
t_D	Group Delay	f = 1.0 GHz	psec.		150	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note: 1. The recommended operating current range for this device is 20 mA to 50 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	70 mA
Power Dissipation[2,3]	400 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

Thermal Resistance[2,4]: θ_{jc} = 100°C/W

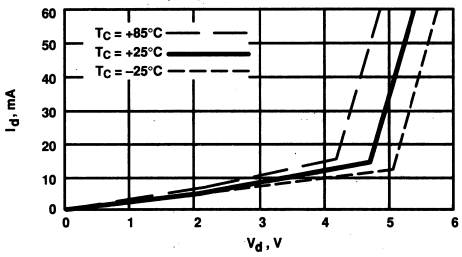
Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 10 mW/°C for T_C > 110°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

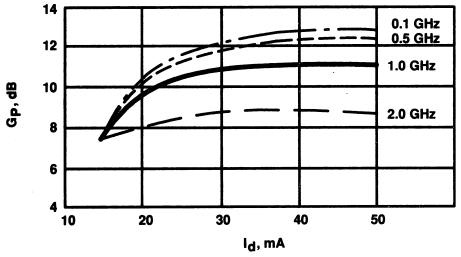
Typical Performance, T_A = 25°C

(unless otherwise noted)

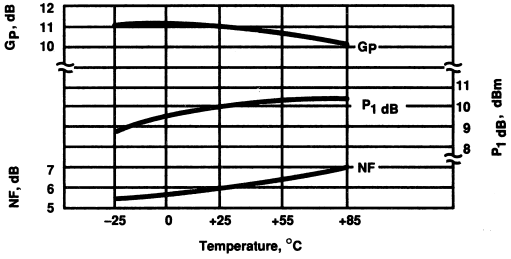
DEVICE CURRENT vs. VOLTAGE



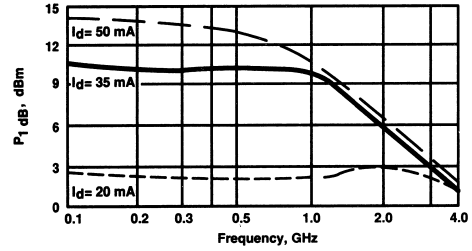
POWER GAIN vs. CURRENT



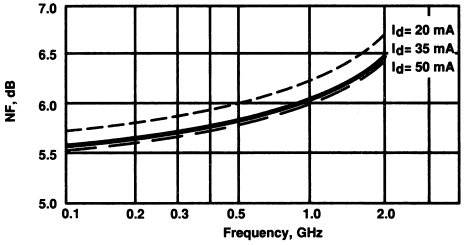
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. CASE TEMPERATURE
f = 1.0 GHz, I_d = 35 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 35 mA

Freq. GHz	S11 Mag	S11 Ang	S21 dB	S21 Mag	S21 Ang	S12 dB	S12 Mag	S12 Ang	S22 Mag	S22 Ang
0.1	.10	173	12.5	4.24	173	–18.5	.120	3	.12	–13
0.2	.10	162	12.5	4.21	167	–18.2	.123	4	.12	–24
0.4	.09	142	12.2	4.08	153	–18.0	.125	7	.13	–46
0.6	.08	127	11.9	3.93	141	–17.8	.128	10	.15	–64
0.8	.07	110	11.5	3.76	130	–17.3	.136	14	.16	–78
1.0	.06	92	11.1	3.58	118	–16.8	.144	16	.17	–91
1.5	.03	58	10.0	3.15	93	–15.5	.169	19	.19	–117
2.0	.03	175	8.8	2.76	71	–14.1	.197	18	.20	–139
2.5	.05	163	7.8	2.46	55	–13.2	.218	18	.21	–158
3.0	.12	148	6.8	2.20	38	–12.2	.246	15	.22	–174
3.5	.19	129	5.9	1.98	20	–11.2	.275	7	.24	171
4.0	.26	110	5.0	1.77	3	–10.6	.296	1	.26	158
5.0	.44	77	3.0	1.41	–28	–9.9	.319	–15	.29	128
6.0	.63	52	0.4	1.05	–56	–10.2	.310	–31	.37	94

A model for this device is available in the DEVICE MODELS section.

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MSA-0311
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

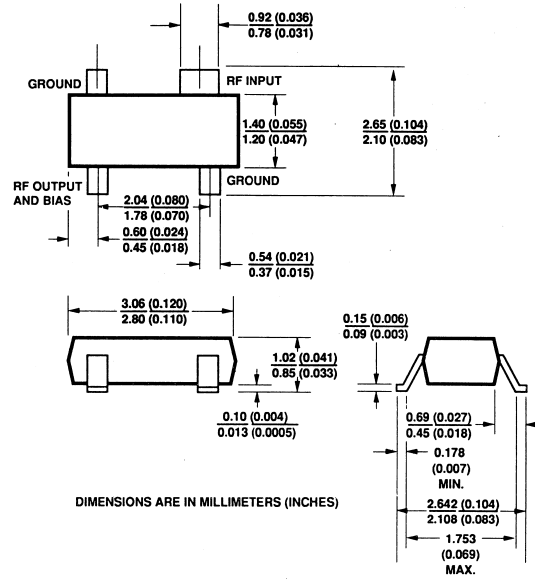
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 2.3 GHz**
- **11.0 dB typical Gain at 1.0 GHz**
- **9.0 dBm typical $P_{1\,dB}$ at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Low Cost Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Description

The MSA-0311 is a low cost silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in the surface mount plastic SOT-143 package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

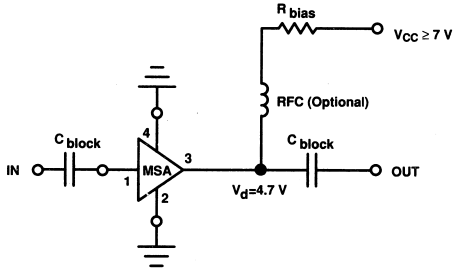
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

SOT-143 Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz	dB	 9.0	11.5 11.0	
ΔG_P	Gain Flatness	f = 0.1 to 1.6 GHz	dB		±0.7	
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.3	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.5:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.7:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		9.0	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		22.0	
t_D	Group Delay	f = 1.0 GHz	psec.		140	
V_d	Device Voltage	T_C = 25°C	V	3.8	4.7	5.6
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes: 1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices."
2. The recommended operating current range for this device is 20 mA to 40 mA. Typical gain performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	240 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

Thermal Resistance[2,4]: θ_{jc} = 500°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 2.0 mW/°C for T_C > 30°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

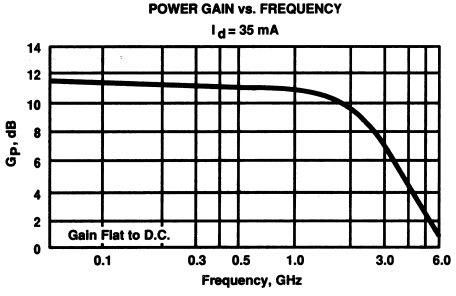
Part Number Ordering Information

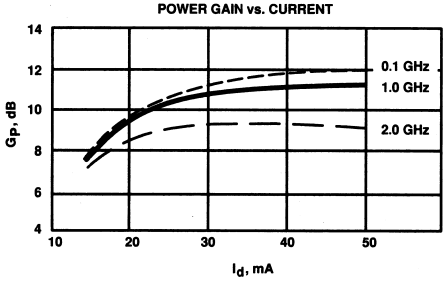
Part Number	Devices Per Reel	Reel Size
MSA-0311-TR1	3000	7"
MSA-0311-TR2	10000	13"

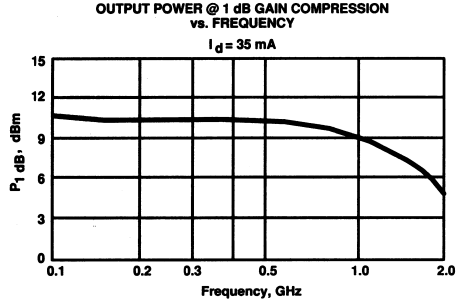
For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

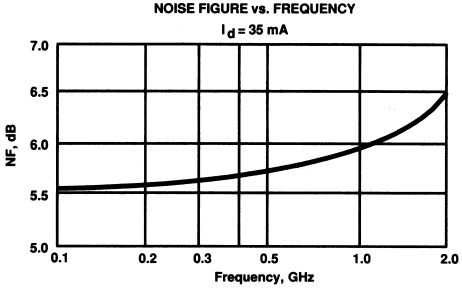
Typical Performance, T_A = 25°C

(unless otherwise noted)









Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 35 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	.06	25	11.7	3.84	175	–17.9	.127	2	.24	–7
0.2	.07	31	11.7	3.83	170	–17.9	.128	3	.23	–13
0.4	.07	38	11.6	3.78	159	–17.8	.129	6	.24	–28
0.6	.07	30	11.4	3.72	149	–17.6	.132	8	.24	–40
0.8	.08	21	11.2	3.65	140	–17.3	.136	11	.24	–53
1.0	.08	10	11.0	3.56	130	–17.0	.141	13	.24	–65
1.5	.09	–32	10.4	3.31	106	–15.9	.160	17	.24	–91
2.0	.09	–105	9.5	2.99	84	–14.9	.179	16	.23	–115
2.5	.13	–151	8.5	2.66	70	–14.1	.197	19	.23	–133
3.0	.19	–176	7.4	2.35	51	–13.5	.212	15	.22	–145
3.5	.24	166	6.2	2.04	35	–13.0	.224	11	.23	–151
4.0	.27	152	5.1	1.80	20	–12.7	.232	6	.24	–151
5.0	.36	114	2.9	1.39	–6	–12.1	.250	–1	.25	–152
6.0	.50	88	0.8	1.10	–28	–11.8	.258	–8	.25	–166

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0335, -0336
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 2.7 GHz**
- **12.0 dB typical Gain at 1.0 GHz**
- **10.0 dBm typical $P_{1\,dB}$ at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Cost Effective Ceramic Microstrip Package**

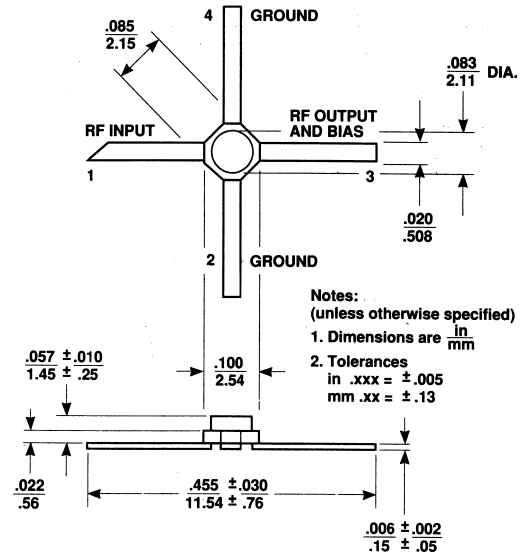
Description

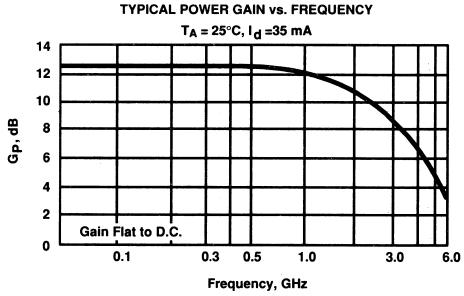
The MSA-0335 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a cost effective, microstrip package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

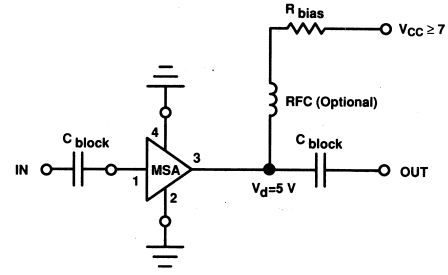
Available in cut lead version (package 36) as MSA-0336.

35 micro-X Package[1]





Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	11.5	12.5	13.5
ΔG_P	Gain Flatness	f = 0.1 to 1.6 GHz	dB		±0.6	±1.0
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.7	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.6:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.7:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		10.0	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		23.0	
t_D	Group Delay	f = 1.0 GHz	psec.		125	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes: 1. Short leaded 36 package available upon request.
2. The recommended operating current range for this device is 20 mA to 50 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	425 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature[4]	–65°C to 200°C

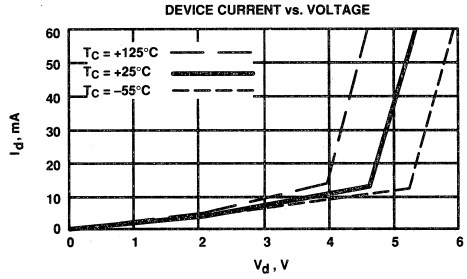
Thermal Resistance[2,5]: θ_{jc} = 150°C/W

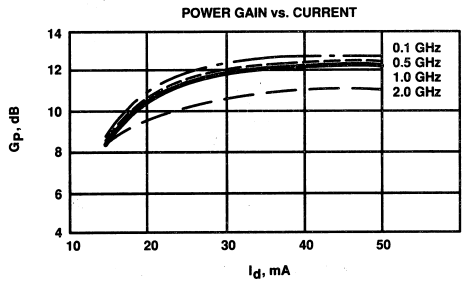
Notes:

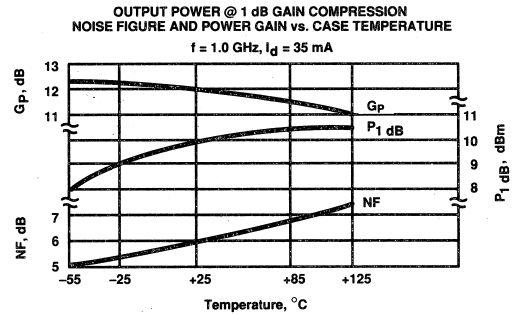
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 6.7 mW/°C for T_C > 136°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

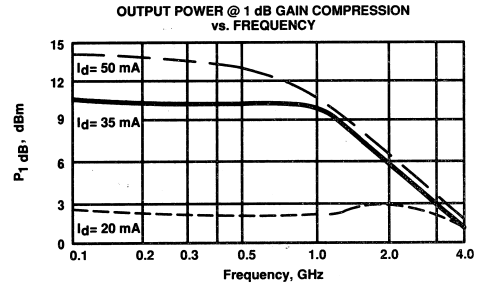
Typical Performance, T_A = 25°C

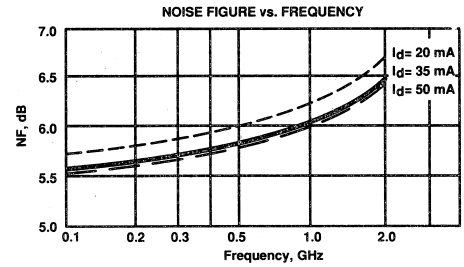
(unless otherwise noted)











Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 35 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.05	177	12.6	4.25	175	–18.6	.118	1	.17	–8
0.2	.05	170	12.5	4.24	170	–18.3	.121	2	.17	–17
0.4	.04	161	12.5	4.20	160	–18.3	.122	3	.17	–33
0.6	.04	156	12.4	4.15	151	–18.3	.121	5	.18	–47
0.8	.03	149	12.2	4.09	142	–17.9	.128	8	.19	–61
1.0	.02	154	12.1	4.02	132	–17.6	.131	9	.20	–73
1.5	.03	–104	11.6	3.79	109	–16.8	.145	13	.20	–102
2.0	.08	–136	10.9	3.49	87	–15.7	.164	11	.21	–133
2.5	.14	–157	10.0	3.16	71	–14.9	.180	13	.23	–155
3.0	.21	–176	9.0	2.81	53	–14.6	.187	8	.24	–173
3.5	.27	170	7.9	2.49	36	–13.9	.202	4	.25	178
4.0	.31	157	6.9	2.20	20	–13.6	.209	–1	.24	177
5.0	.37	125	4.9	1.76	–10	–12.9	.226	–12	.20	165
6.0	.51	87	2.8	1.38	–38	–12.8	.230	–25	.22	130

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0370
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

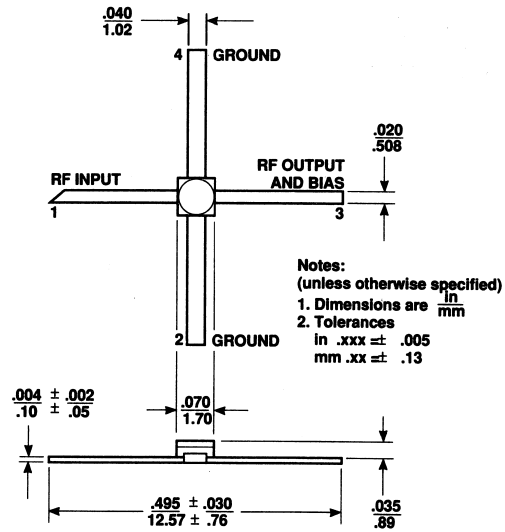
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 2.8 GHz**
- **12.0 dB typical Gain at 1.0 GHz**
- **10.0 dBm typical $P_{1\,dB}$ at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Hermetic Gold-ceramic Microstrip Package**

Description

The MSA-0370 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic, high reliability package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

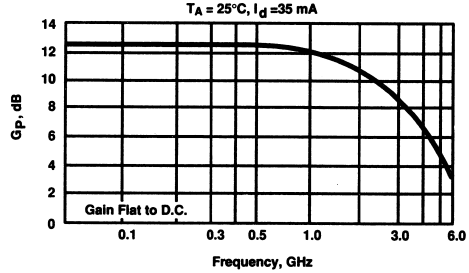
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

70 mil Package

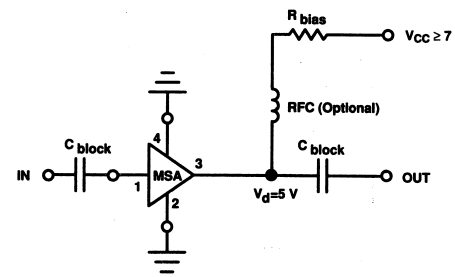


TYPICAL POWER GAIN vs. FREQUENCY

T_A = 25°C, I_d = 35 mA



Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	11.5	12.5	13.5
ΔG_P	Gain Flatness	f = 0.1 to 1.8 GHz	dB		±0.6	±1.0
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.8	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.8:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.8:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		10.0	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		23.0	
t_D	Group Delay	f = 1.0 GHz	psec.		125	
V_d	Device Voltage		V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		-8.0	

Note: 1. The recommended operating current range for this device is 20 mA to 50 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	425 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

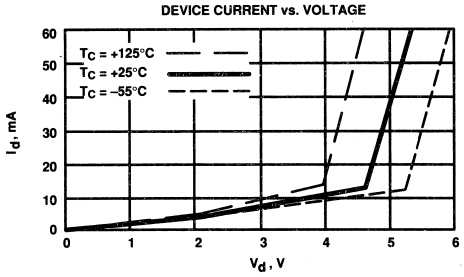
Thermal Resistance[2,4]: θ_{jc} = 125°C/W

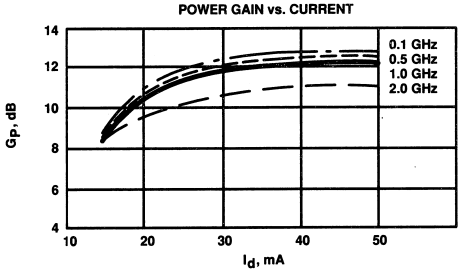
Notes:

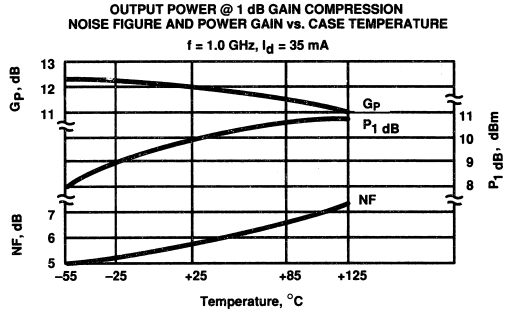
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 8 mW/°C for T_C > 147°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

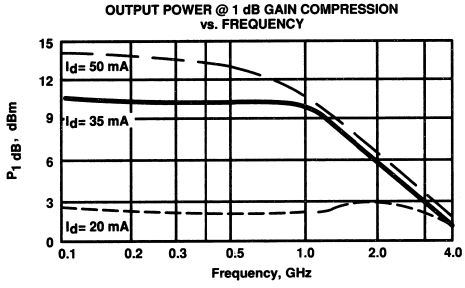
Typical Performance, T_A = 25°C

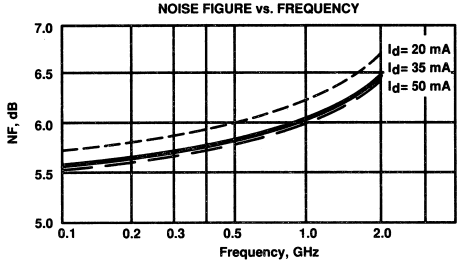
(unless otherwise noted)











Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 35 mA

Freq. GHz	S11 Mag	S11 Ang	S21 dB	S21 Mag	S21 Ang	S12 dB	S12 Mag	S12 Ang	S22 Mag	S22 Ang
0.1	.13	–179	12.6	4.27	176	–18.6	.118	2	.09	–14
0.2	.13	–180	12.6	4.25	171	–18.3	.121	2	.10	–29
0.4	.12	–180	12.5	4.21	162	–18.4	.121	4	.12	–52
0.6	.11	–178	12.4	4.17	154	–18.2	.123	6	.14	–70
0.8	.11	–174	12.3	4.11	146	–17.8	.129	8	.17	–82
1.0	.10	–168	12.2	4.06	137	–17.7	.130	8	.20	–92
1.5	.11	–149	11.7	3.85	116	–17.1	.140	11	.24	–114
2.0	.16	–147	11.1	3.57	96	–16.2	.155	11	.27	–134
2.5	.22	–151	10.3	3.27	82	–15.6	.167	14	.27	–146
3.0	.28	–160	9.3	2.91	65	–15.2	.174	11	.27	–159
3.5	.33	–169	8.2	2.58	48	–14.5	.188	7	.26	–163
4.0	.36	–177	7.1	2.27	34	–14.3	.192	3	.25	–162
5.0	.38	163	5.1	1.81	9	–13.8	.203	–5	.23	–153
6.0	.39	132	3.4	1.48	–14	–13.5	.213	–13	.24	–160

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0385
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

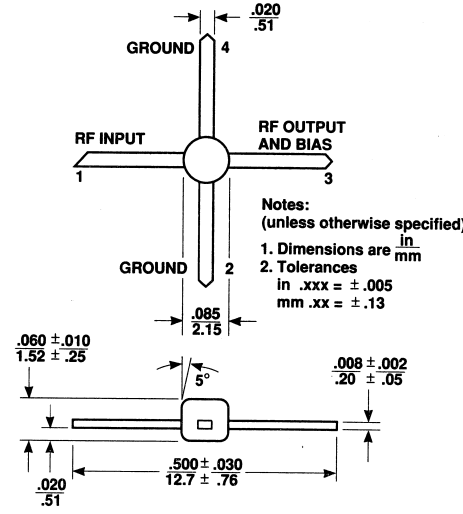
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 2.5 GHz**
- **12.0 dB typical Gain at 1.0 GHz**
- **10.0 dBm typical $P_{1\,dB}$ at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Low Cost Plastic Package**

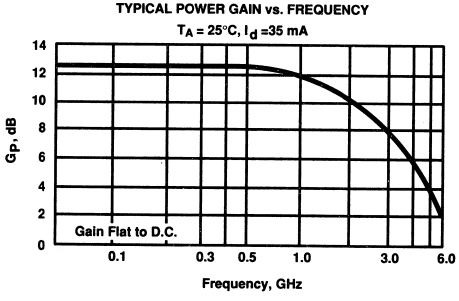
Description

The MSA-0385 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

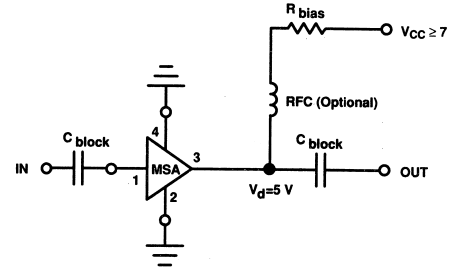
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

85 Plastic Package





Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz	dB	 10.0	12.5 12.0	
ΔG_P	Gain Flatness	f = 0.1 to 1.6 GHz	dB		±0.7	
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.5	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.5:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.7:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		10.0	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		23.0	
t_D	Group Delay	f = 1.0 GHz	psec.		125	
V_d	Device Voltage		V	4.0	5.0	6.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note: 1. The recommended operating current range for this device is 20 mA to 50 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	70 mA
Power Dissipation[2,3]	400 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

Thermal Resistance[2,4]: θ_{jC} = 105°C/W

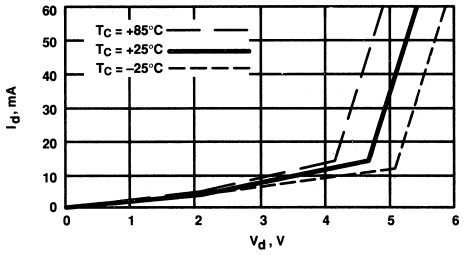
Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 9.5 mW/°C for T_C > 108°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

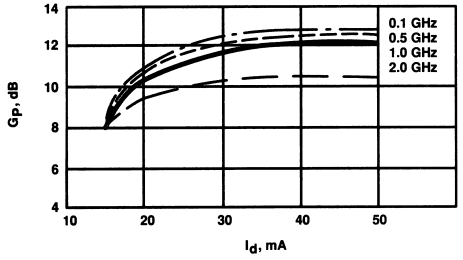
Typical Performance, T_A = 25°C

(unless otherwise noted)

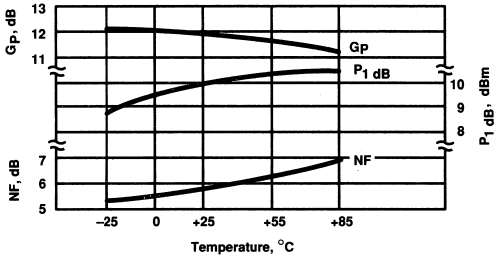
DEVICE CURRENT vs. VOLTAGE



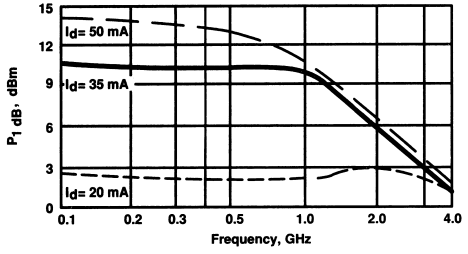
POWER GAIN vs. CURRENT



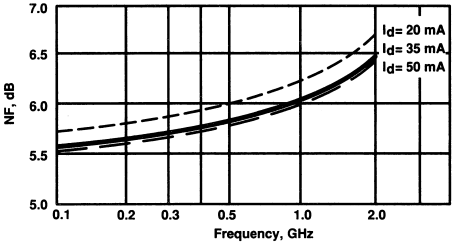
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. CASE TEMPERATURE
f = 1.0 GHz, I_d = 35 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 35 mA

Freq. GHz	S11 Mag	S11 Ang	S21 dB	S21 Mag	S21 Ang	S12 dB	S12 Mag	S12 Ang	S22 Mag	S22 Ang
0.1	.09	178	12.6	4.26	175	–18.1	.124	2	.13	–10
0.2	.09	171	12.5	4.24	170	–18.4	.120	3	.13	–20
0.4	.08	166	12.4	4.17	161	–18.4	.121	6	.14	–41
0.6	.07	160	12.3	4.10	151	–18.0	.126	8	.15	–57
0.8	.07	155	12.1	4.01	142	–17.9	.127	12	.16	–71
1.0	.06	152	11.9	3.92	133	–17.6	.132	12	.18	–84
1.5	.05	–169	11.2	3.63	112	–16.5	.149	18	.21	–112
2.0	.08	–174	10.4	3.29	92	–15.6	.167	19	.23	–136
2.5	.12	–173	9.5	2.98	79	–14.6	.186	22	.25	–150
3.0	.20	178	8.4	2.64	63	–14.1	.198	20	.26	–166
3.5	.25	170	7.5	2.36	47	–13.5	.211	17	.25	–174
4.0	.28	160	6.5	2.12	33	–13.0	.224	13	.24	–180
5.0	.42	134	4.7	1.71	7	–12.2	.247	4	.20	168
6.0	.50	99	2.7	1.37	–18	–12.0	.252	–7	.23	133

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0386
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

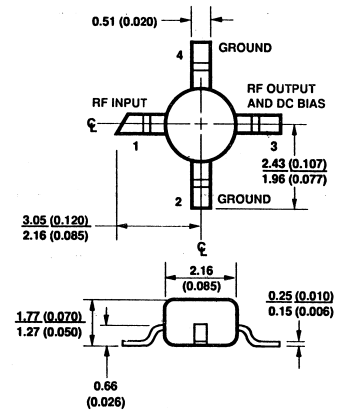
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 2.4 GHz**
- **12.0 dB typical Gain at 1.0 GHz**
- **10.0 dBm typical $P_{1\,dB}$ at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Description

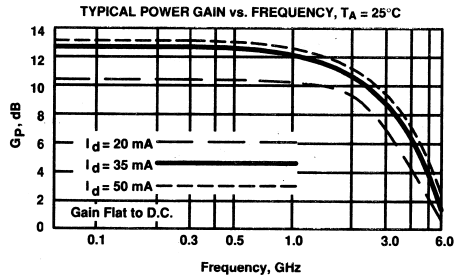
The MSA-0386 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost, surface mount plastic package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

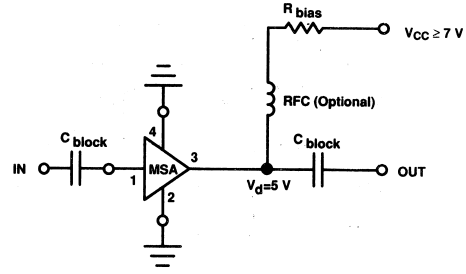
86 Plastic Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)



Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz	dB	 10.0	12.5 12.0	
ΔG_P	Gain Flatness	f = 0.1 to 1.6 GHz	dB		±0.7	
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.4	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.5:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.7:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		10.0	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		23.0	
t_D	Group Delay	f = 1.0 GHz	psec.		140	
V_d	Device Voltage		V	4.0	5.0	6.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes: 1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices."
2. The recommended operating current range for this device is 20 mA to 40 mA. Typical gain performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	70 mA
Power Dissipation[2,3]	400 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

Thermal Resistance[2,4]: θ_{jc} = 115°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 8.7 mW/°C for T_C > 104°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Part Number Ordering Information

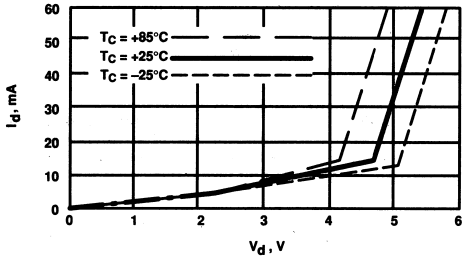
Part Number	Devices Per Reel	Reel Size
MSA-0386-TR1	1000	7"
MSA-0386-TR2	4000	13"

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

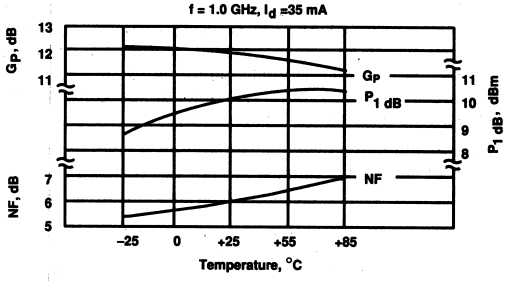
Typical Performance, T_A = 25°C

(unless otherwise noted)

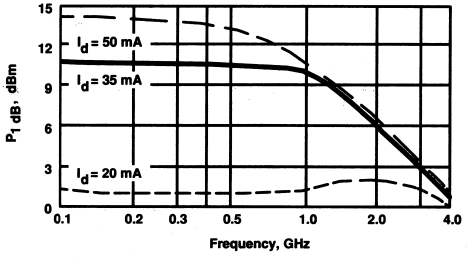
DEVICE CURRENT vs. VOLTAGE



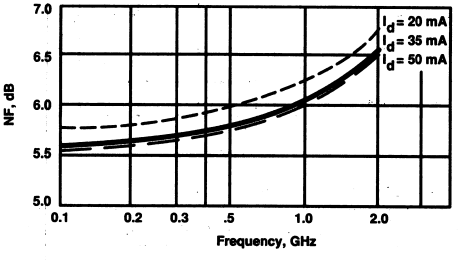
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. CASE TEMPERATURE
f = 1.0 GHz, I_d =35 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 35 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.11	174	12.5	4.22	175	–18.3	.122	1	.13	–11
0.2	.11	169	12.5	4.20	170	–18.2	.124	2	.13	–20
0.4	.11	159	12.4	4.16	159	–18.1	.124	5	.14	–41
0.6	.10	149	12.2	4.09	149	–17.9	.128	8	.15	–60
0.8	.10	142	12.1	4.00	139	–17.6	.131	9	.16	–78
1.0	.09	137	11.9	3.93	129	–17.4	.136	11	.18	–93
1.5	.09	139	11.2	3.61	106	–16.6	.149	14	.20	–129
2.0	.12	149	10.3	3.28	83	–15.3	.171	13	.23	–157
2.5	.18	150	9.4	2.95	66	–14.4	.190	12	.26	–176
3.0	.25	142	8.3	2.60	48	–13.7	.207	9	.29	167
3.5	.32	133	7.2	2.29	31	–13.2	.219	3	.30	152
4.0	.40	124	6.0	2.01	15	–13.0	.224	–1	.31	142
5.0	.53	106	3.7	1.53	–13	–12.8	.228	–11	.32	128

A model for this device is available in the DEVICE MODELS section.

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MSA-0400
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 4.0 GHz**
- **16.0 dBm typical $P_{1\ dB}$ at 1.0 GHz**
- **8.5 dB typical Gain at 1.0 GHz**

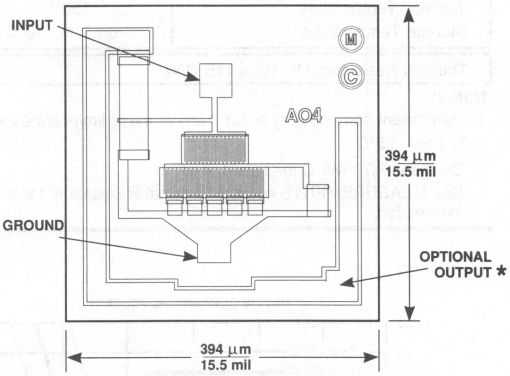
Description

The MSA-0400 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial, industrial and military applications.

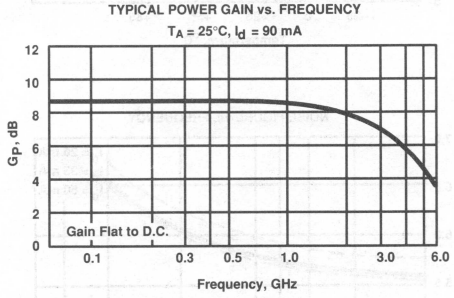
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire. See APPLICATIONS section, "Chip Use".

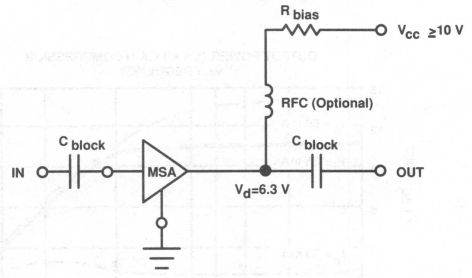
Chip Outline[1]



Unless otherwise specified, tolerances are ±13 µm / ±0.5 mils.
Chip thickness is 114 µm / 4.5 mil. Bond pads are 41 µm / 1.6 mil typical on each side.
★ Output contact is made by die attaching the backside of the die.



Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions[3]: I_d = 90 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		8.5	
ΔG_P	Gain Flatness	f = 0.1 to 2.5 GHz	dB		±0.6	
$f_{3\ dB}$	3 dB Bandwidth		GHz		4.3	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			1.7:1	
	Output VSWR	f = 0.1 to 2.5 GHz			1.8:1	
$P_{1\ dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz, I_d = 50 mA	dBm		12.5	
	Output Power @ 1 dB Gain Compression	f = 1.0 GHz, I_d = 90 mA	dBm		16.0	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		30.0	
t_D	Group Delay	f = 1.0 GHz	psec.		140	
V_d	Device Voltage		V	5.7	6.3	6.9
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes: 1. Refer to the APPLICATIONS section "MODAMP™ Silicon MMIC Chip Use" for additional information.
2. The recommended operating current range for this device is 40 mA to 110 mA. Typical performance as a function of current is on the following page.
3. RF performance of the chip is determined by packaging and testing 10 devices per wafer in a dual ground configuration.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	120 mA
Power Dissipation[2,3]	850 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 35°C/W

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{MOUNTING\ SURFACE}$ = 25°C
3. Derate at 28.6 mW/°C for $T_{MOUNTING\ SURFACE}$ > 170°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

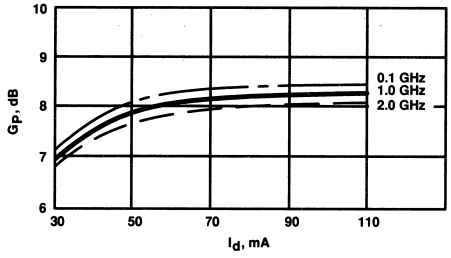
Part Number Ordering Information

Part Number	Devices Per Tray
MSA-0400-GP2	10
MSA-0400-GP4	100
MSA-0400-GP6	up to 300

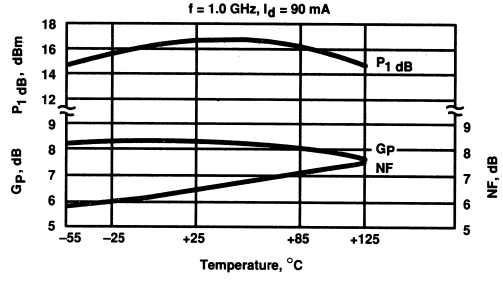
Typical Performance, T_A = 25°C

(unless otherwise noted)

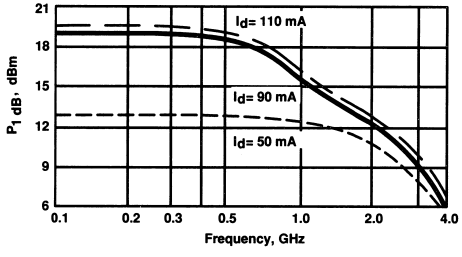
POWER GAIN vs. CURRENT



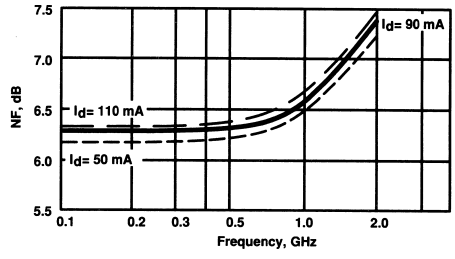
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. MOUNTING
SURFACE TEMPERATURE
f = 1.0 GHz, I_d = 90 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters: $Z_O = 50\ \Omega$

$T_A = 25°C$, $I_d = 50$ mA[4]

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.1	.18	179	8.6	2.68	177	−16.4	.151	1	.10	−13	1.37
0.5	.18	−179	8.6	2.68	163	−16.3	.153	7	.16	−54	1.34
1.0	.16	−171	8.5	2.65	145	−15.8	.161	10	.22	−83	1.28
1.5	.16	−161	8.4	2.63	127	−15.4	.169	16	.29	−101	1.19
2.0	.21	−156	8.2	2.56	109	−14.6	.187	18	.33	−119	1.07
2.5	.27	−152	7.8	2.45	98	−13.8	.205	24	.37	−128	0.98
3.0	.33	−159	7.0	2.23	82	−13.4	.213	24	.42	−140	0.91
4.0	.42	−171	5.2	1.81	54	−12.5	.237	21	.42	−151	0.86
5.0	.45	172	3.4	1.49	33	−11.7	.259	17	.38	−153	0.94

Typical Scattering Parameters: $Z_O = 50\ \Omega$

$T_A = 25°C$, $I_d = 90$ mA[5]

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.1	.25	179	8.7	2.73	177	−16.4	.152	2	.03	−36	1.33
0.5	.24	173	8.8	2.76	164	−16.3	.153	5	.10	−83	1.31
1.0	.22	166	8.8	2.74	148	−15.9	.160	10	.19	−91	1.26
1.5	.16	164	8.8	2.74	132	−15.3	.172	16	.27	−94	1.18
2.0	.13	173	8.7	2.73	116	−14.5	.189	22	.32	−98	1.10
2.5	.12	−162	8.3	2.60	106	−13.9	.203	31	.36	−95	1.04
3.0	.14	−147	8.0	2.50	90	−13.1	.222	33	.40	−95	0.97
4.0	.17	−154	6.7	2.17	64	−10.9	.286	36	.43	−93	0.87
5.0	.20	146	5.2	1.83	41	−9.2	.346	36	.40	−94	0.89

Notes: 4. S-parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section.
5. S-parameters are de-embedded from 200 mil BeO package measured data using the package model found in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0404
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

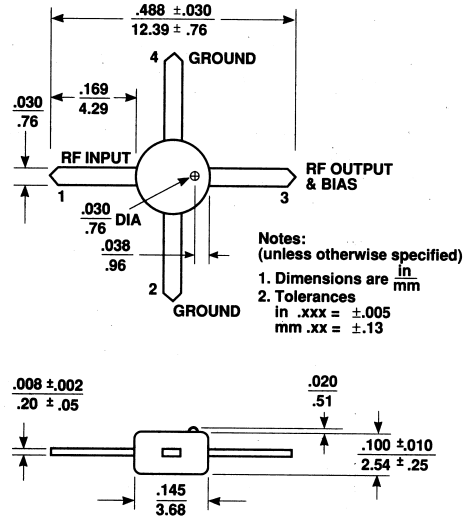
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 2.5 GHz**
- **11.5 dBm typical $P_{1\,dB}$ at 1.0 GHz**
- **7.5 dB typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Low Cost Plastic Package**

Description

The MSA-0404 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

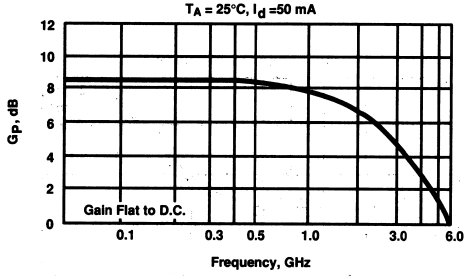
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

04A Plastic Package

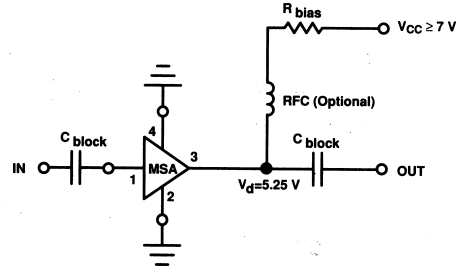


TYPICAL POWER GAIN vs. FREQUENCY

T_A = 25°C, I_d = 50 mA



Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 50 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 0.5 GHz f = 1.0 GHz	dB	7.0	8.3 8.0 7.5	
ΔG_P	Gain Flatness	f = 0.1 to 2.0 GHz	dB		±1.0	
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.5	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			1.4:1	
	Output VSWR	f = 0.1 to 2.5 GHz			1.8:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		11.5	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		7.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		24.5	
t_D	Group Delay	f = 1.0 GHz	psec.		150	
V_d	Device Voltage		V	4.75	5.25	5.75
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note: 1. The recommended operating current range for this device is 30 mA to 70 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

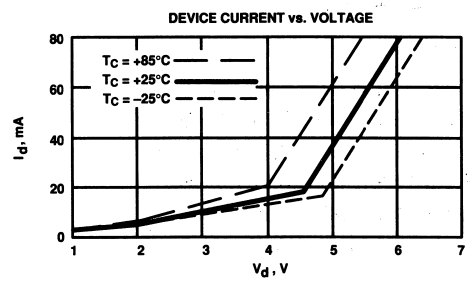
Parameter	Absolute Maximum[1]
Device Current	85 mA
Power Dissipation[2,3]	500 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

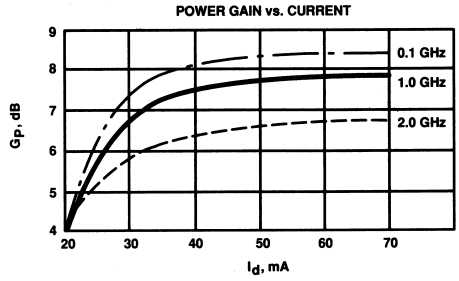
Thermal Resistance[2,4]: θ_{jc} = 85°C/W

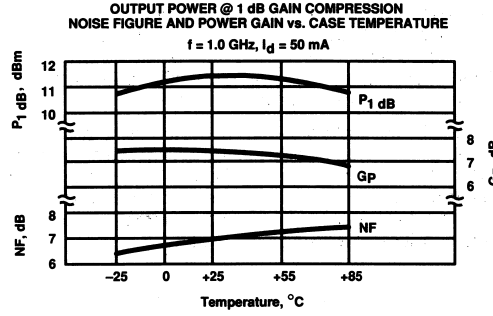
Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 11.8 mW/°C for T_C > 108°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

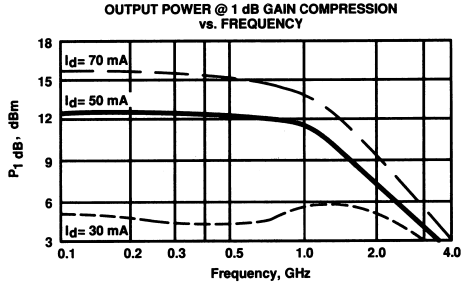
Typical Performance, T_A = 25°C

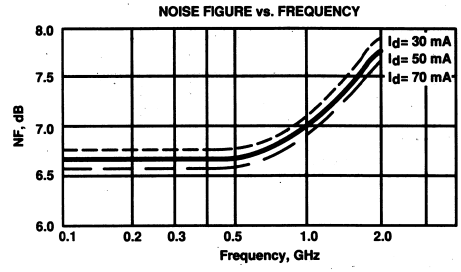
(unless otherwise noted)











Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 50 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	.16	175	8.3	2.59	174	–16.2	.156	0	.13	–13
0.2	.16	170	8.2	2.58	168	–16.2	.155	2	.13	–25
0.4	.15	161	8.1	2.54	156	–16.0	.158	4	.14	–47
0.6	.14	152	8.0	2.51	145	–16.0	.158	6	.16	–64
0.8	.12	145	7.8	2.46	133	–15.8	.163	8	.19	–79
1.0	.11	141	7.7	2.41	122	–15.4	.169	9	.21	–91
1.5	.07	141	7.2	2.29	96	–14.6	.186	13	.24	–118
2.0	.09	161	6.6	2.14	71	–13.3	.215	12	.26	–140
2.5	.14	159	5.9	1.98	53	–12.4	.240	13	.28	–157
3.0	.22	146	5.1	1.80	33	–11.7	.260	7	.29	–176
3.5	.30	128	4.3	1.64	13	–10.9	.286	0	.32	167
4.0	.38	109	3.2	1.45	–6	–10.4	.301	–7	.33	153
5.0	.47	91	2.1	1.27	–23	–10.2	.310	–15	.35	137
6.0	.55	75	1.0	1.09	–39	–10.1	.312	–24	.37	120

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0420
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

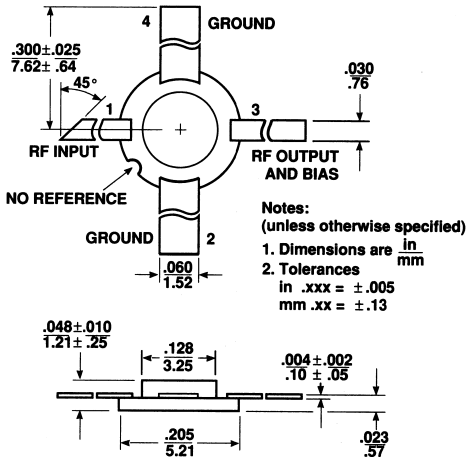
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 4.0 GHz**
- **16.0 dBm typical $P_{1\,dB}$ at 1.0 GHz**
- **8.5 dB typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Hermetic Metal/Beryllia Microstrip Package**

Description

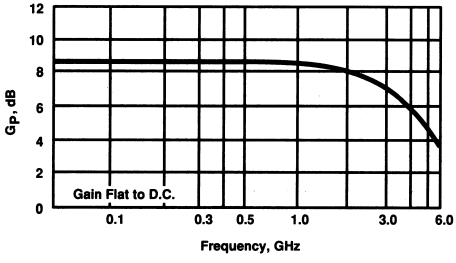
The MSA-0420 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic, high reliability package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

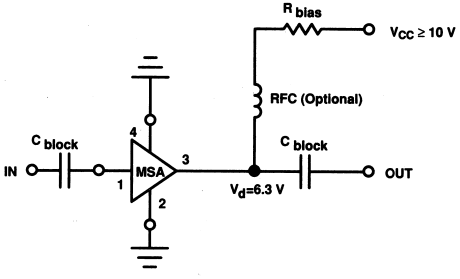
200 mil BeO Package



TYPICAL POWER GAIN vs. FREQUENCY
T_A = 25°C, I_d =90 mA



Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 90 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	7.5	8.5	9.5
ΔG_P	Gain Flatness	f = 0.1 to 2.5 GHz	dB		±0.6	±1.0
$f_{3\,dB}$	3 dB Bandwidth		GHz		4.3	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			1.7:1	
	Output VSWR	f = 0.1 to 2.5 GHz			1.8:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm	14.0	16.0	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		30.0	
t_D	Group Delay	f = 1.0 GHz	psec.		140	
V_d	Device Voltage		V	5.7	6.3	6.9
dV/dT	Device Voltage Temperature Coefficient		mV/°C		-8.0	

Note: 1. The recommended operating current range for this device is 40 mA to 110 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	120 mA
Power Dissipation[2,3]	850 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

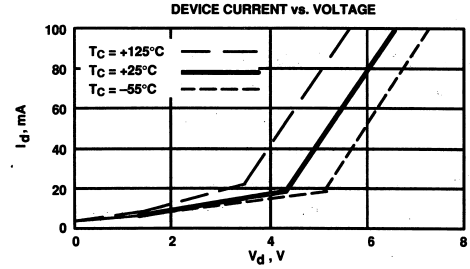
Thermal Resistance[2,4]: θ_{jc} = 40°C/W

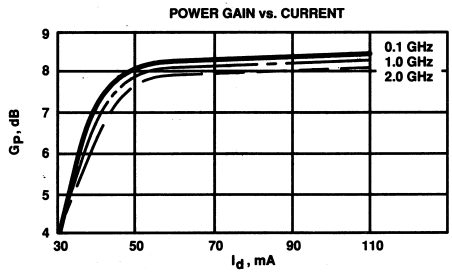
Notes:

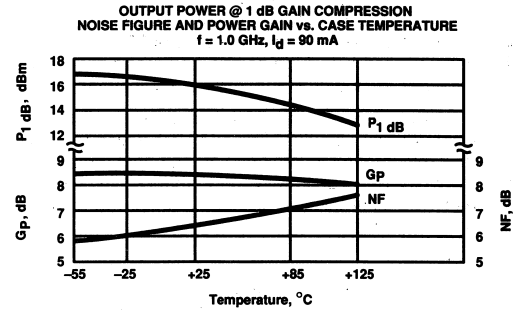
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 25 mW/°C for T_C > 166°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

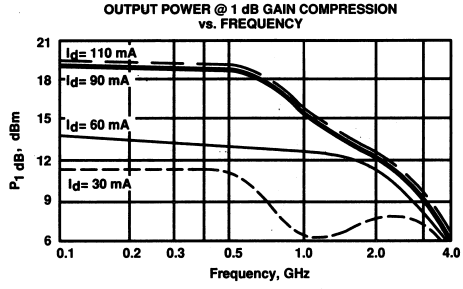
Typical Performance, T_A = 25°C

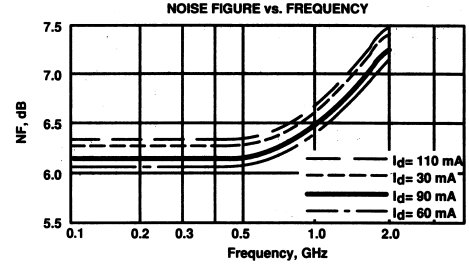
(unless otherwise noted)











Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 90 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	.25	177	8.6	2.70	175	–16.4	.151	1	.03	–30
0.2	.25	173	8.6	2.69	170	–16.5	.150	1	.04	–59
0.4	.24	167	8.6	2.69	159	–16.5	.150	–1	.07	–79
0.6	.22	160	8.5	2.67	149	–16.4	.152	–2	.10	–92
0.8	.21	154	8.5	2.66	139	–16.3	.154	–2	.13	–99
1.0	.20	148	8.3	2.60	129	–16.1	.156	–3	.16	–109
1.5	.14	136	8.1	2.54	104	–15.6	.166	–4	.22	–124
2.0	.10	136	7.9	2.48	80	–14.8	.181	–6	.25	–139
2.5	.08	161	7.4	2.34	62	–14.3	.193	–5	.28	–147
3.0	.10	178	7.0	2.24	39	–13.7	.206	–11	.31	–157
3.5	.13	176	6.6	2.13	18	–12.6	.233	–18	.34	–167
4.0	.14	163	5.9	1.97	–3	–11.9	.253	–25	.36	–176
4.5	.14	133	5.3	1.83	–23	–11.3	.273	–33	.37	174
5.0	.16	91	4.5	1.69	–43	–10.5	.299	–43	.37	162

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0435, -0436
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 3.8 GHz**
- **12.5 dBm typical $P_{1\,dB}$ at 1.0 GHz**
- **8.5 dB typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Cost Effective Ceramic Microstrip Package**

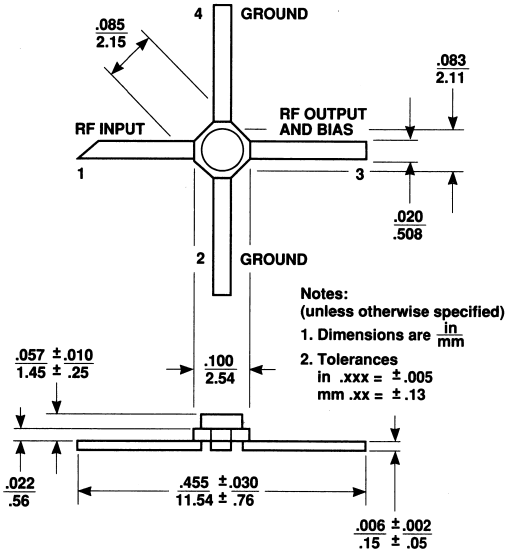
Description

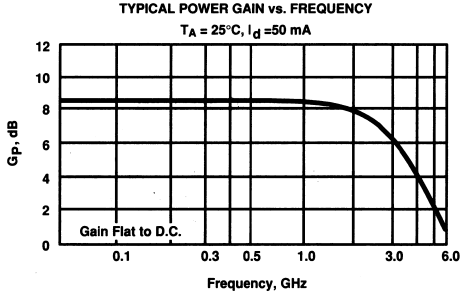
The MSA-0435 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a cost effective, microstrip package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

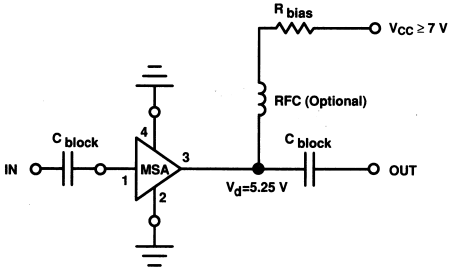
Available in cut lead version (package 36) as MSA-0436.

35 micro-X Package[1]





Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 50 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	7.5	8.5	9.5
ΔG_P	Gain Flatness	f = 0.1 to 2.5 GHz	dB		±0.6	±1.0
$f_{3\,dB}$	3 dB Bandwidth		GHz		3.8	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			1.4:1	
	Output VSWR	f = 0.1 to 2.5 GHz			1.9:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		12.5	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		25.5	
t_D	Group Delay	f = 1.0 GHz	psec.		125	
V_d	Device Voltage		V	4.75	5.25	5.75
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes: 1. Short leaded 36 package available upon request.
2. The recommended operating current range for this device is 30 mA to 70 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	100 mA
Power Dissipation[2,3]	650 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature[4]	–65°C to 200°C

Thermal Resistance[2,5]: θ_{jc} = 140°C/W

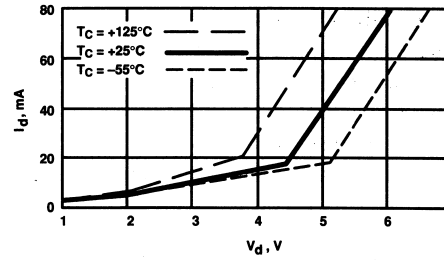
Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 7.1 mW/°C for T_C > 109°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

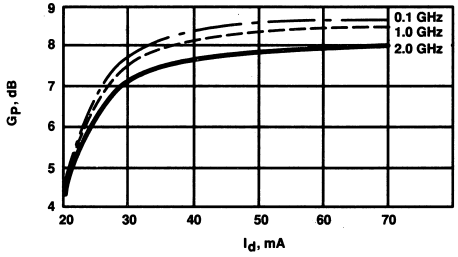
Typical Performance, T_A = 25°C

(unless otherwise noted)

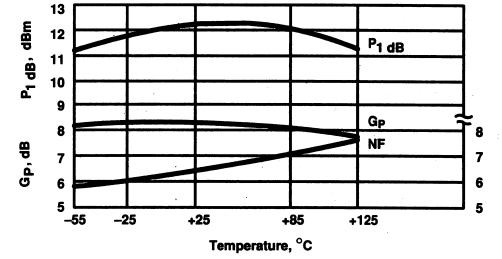
DEVICE CURRENT vs. VOLTAGE



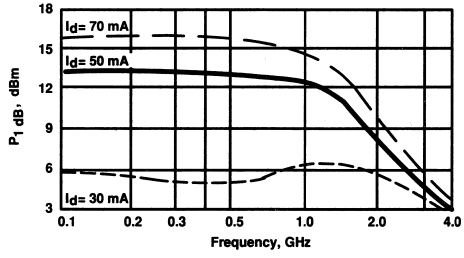
POWER GAIN vs. CURRENT



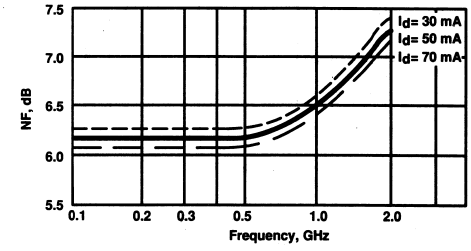
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. CASE TEMPERATURE
f = 1.0 GHz, I_d = 50 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 50 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	.08	175	8.5	2.67	175	–16.4	.151	1	.20	–10
0.2	.08	172	8.5	2.68	170	–16.3	.153	2	.20	–16
0.4	.07	171	8.5	2.67	161	–16.4	.151	3	.20	–33
0.6	.07	166	8.5	2.66	151	–16.2	.155	6	.21	–45
0.8	.05	169	8.4	2.64	142	–16.1	.156	8	.22	–57
1.0	.05	175	8.3	2.61	136	–16.0	.159	10	.24	–68
1.5	.04	–142	8.1	2.55	109	–15.0	.178	13	.26	–96
2.0	.09	–145	7.8	2.46	87	–14.2	.196	15	.28	–123
2.5	.14	–154	7.3	2.33	71	–13.1	.221	18	.31	–140
3.0	.22	–175	6.6	2.14	50	–12.5	.238	14	.33	–160
3.5	.28	170	5.8	1.94	32	–11.7	.260	9	.35	–173
4.0	.34	156	4.8	1.74	15	–11.3	.271	4	.34	–179
4.5	.37	140	3.9	1.57	–1	–10.7	.291	–2	.33	–171
5.0	.42	120	3.0	1.41	–16	–10.4	.302	–8	.32	–160

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0470
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

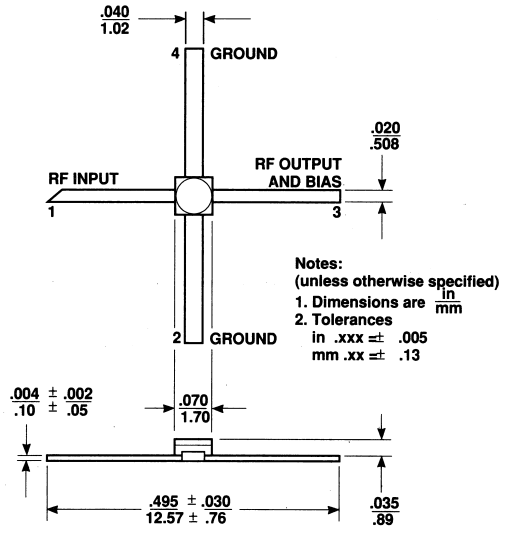
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 4.0 GHz**
- **12.5 dBm typical $P_{1\,dB}$ at 1.0 GHz**
- **8.5 dB typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Hermetic Gold-ceramic Microstrip Package**

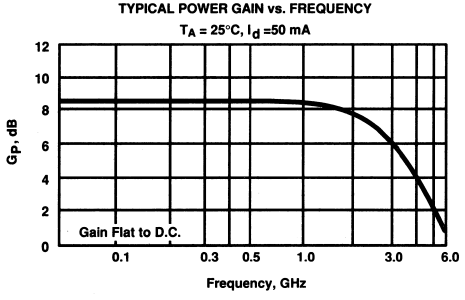
Description

The MSA-0470 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic high reliability package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

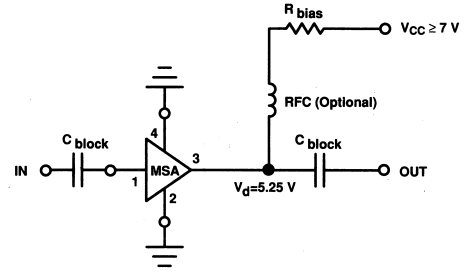
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

70 mil Package





Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 50 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	7.5	8.5	9.5
ΔG_P	Gain Flatness	f = 0.1 to 2.5 GHz	dB		±0.6	±1.0
$f_{3\,dB}$	3 dB Bandwidth		GHz		4.0	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			1.7:1	
	Output VSWR	f = 0.1 to 2.5 GHz			2.0:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		12.5	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		25.5	
t_D	Group Delay	f = 1.0 GHz	psec.		125	
V_d	Device Voltage		V	4.75	5.25	5.75
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note: 1. The recommended operating current range for this device is 30 mA to 70 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	100 mA
Power Dissipation[2,3]	650 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

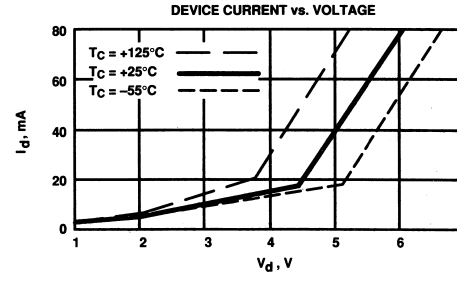
Thermal Resistance[2,4]: θ_{jc} = 115°C/W

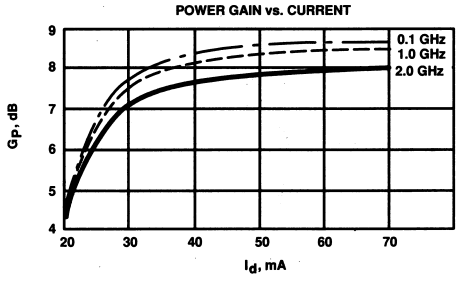
Notes:

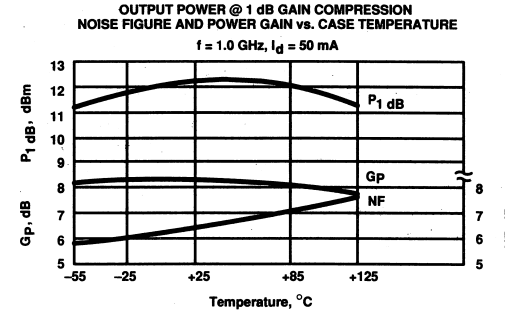
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 8.7 mW/°C for T_C > 125°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

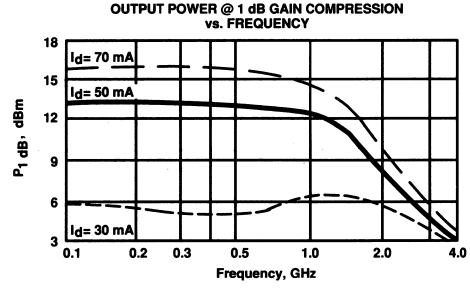
Typical Performance, T_A = 25°C

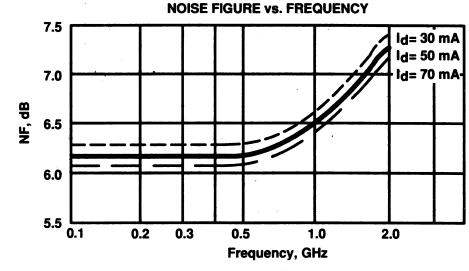
(unless otherwise noted)











Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 50 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.18	179	8.5	2.67	176	–16.4	.151	1	.10	–14
0.2	.18	179	8.5	2.67	172	–16.4	.151	2	.10	–30
0.4	.18	179	8.5	2.67	163	–16.4	.152	3	.13	–50
0.6	.17	–179	8.5	2.65	155	–16.2	.155	5	.16	–67
0.8	.16	–176	8.4	2.64	147	–16.1	.158	6	.19	–79
1.0	.16	–174	8.3	2.61	138	–15.9	.161	6	.22	–90
1.5	.16	–166	8.2	2.56	117	–15.5	.169	9	.29	–111
2.0	.21	–163	7.8	2.46	97	–14.6	.186	9	.33	–131
2.5	.26	–162	7.3	2.33	83	–13.8	.204	12	.36	–142
3.0	.32	–170	6.5	2.12	65	–13.5	.212	10	.40	–156
3.5	.37	–177	5.7	1.93	38	–13.2	.220	7	.40	–164
4.0	.40	175	4.7	1.73	33	–12.6	.234	3	.40	–170
4.5	.41	166	3.9	1.57	20	–12.4	.239	–1	.39	–173
5.0	.42	155	3.1	1.44	7	–11.9	.255	–6	.37	–176

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0485
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

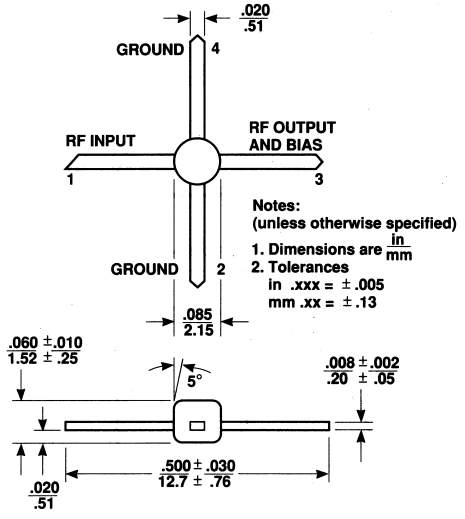
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 3.6 GHz**
- **12.5 dBm typical $P_{1\,dB}$ at 1.0 GHz**
- **8 dB typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Low Cost Plastic Package**

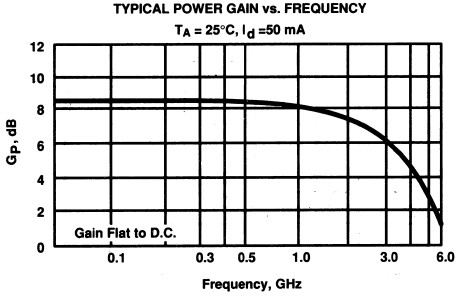
Description

The MSA-0485 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

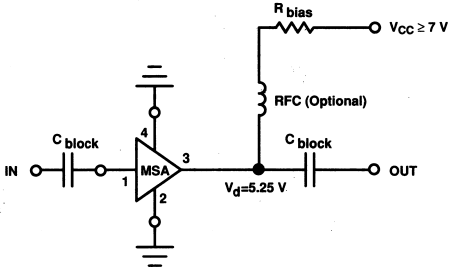
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

85 Plastic Package





Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 50 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz	dB	 7.0	8.3 8.0	
ΔG_P	Gain Flatness	f = 0.1 to 2.5 GHz	dB		±0.7	
$f_{3\,dB}$	3 dB Bandwidth		GHz		3.6	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			1.6:1	
	Output VSWR	f = 0.1 to 2.5 GHz			2.0:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		12.5	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		7.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		25.5	
t_D	Group Delay	f = 1.0 GHz	psec.		125	
V_d	Device Voltage		V	4.2	5.25	6.3
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note: 1. The recommended operating current range for this device is 30 mA to 70 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	85 mA
Power Dissipation[2,3]	500 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

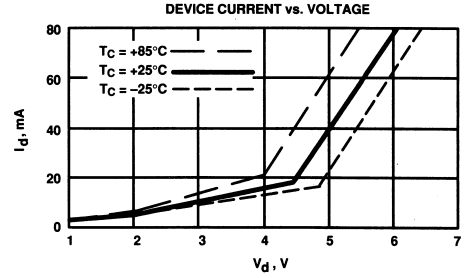
Thermal Resistance[2,4]: θ_{jc} = 90°C/W

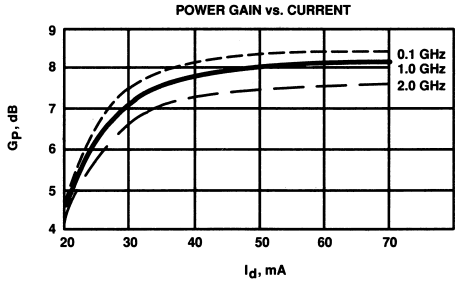
Notes:

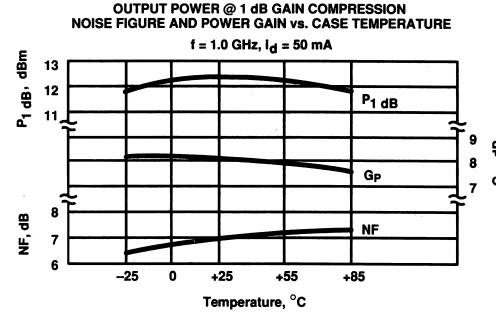
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 11.1 mW/°C for T_C > 105°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

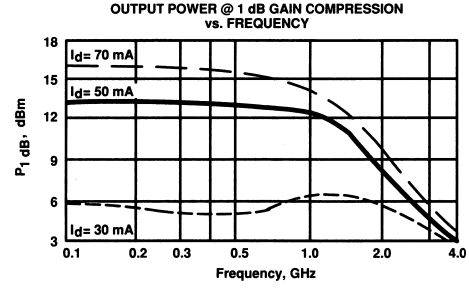
Typical Performance, T_A = 25°C

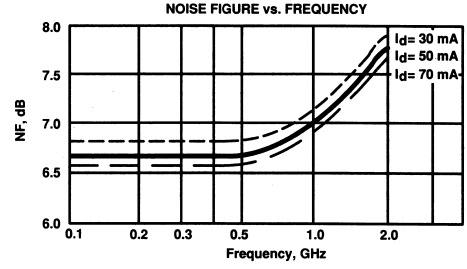
(unless otherwise noted)











Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 50 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.21	177	8.4	2.63	175	–16.1	.156	2	.08	–16
0.2	.20	176	8.3	2.60	171	–16.2	.155	2	.08	–30
0.4	.20	172	8.2	2.57	163	–16.1	.156	3	.10	–54
0.6	.19	171	8.1	2.55	155	–16.2	.155	5	.13	–71
0.8	.19	168	8.1	2.54	146	–16.0	.158	6	.16	–83
1.0	.18	166	8.0	2.52	138	–15.7	.164	9	.18	–93
1.5	.16	167	7.8	2.46	117	–15.3	.171	11	.25	–116
2.0	.18	168	7.4	2.34	97	–14.6	.187	12	.29	–135
2.5	.21	173	6.9	2.21	83	–13.8	.204	16	.34	–150
3.0	.27	169	6.3	2.07	65	–13.4	.213	13	.38	–161
3.5	.33	161	5.7	1.92	48	–12.6	.234	9	.39	–172
4.0	.38	154	4.8	1.74	33	–12.3	.242	6	.37	–179
4.5	.42	145	4.1	1.59	18	–12.1	.249	3	.36	–174
5.0	.44	131	3.3	1.46	4	–11.7	.259	–3	.34	–165

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0486
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

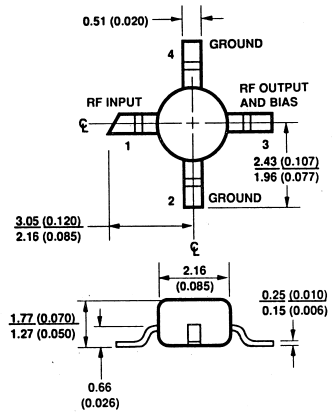
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 3.2 GHz**
- **12.5 dBm typical $P_{1\,dB}$ at 1.0 GHz**
- **8 dB typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Description

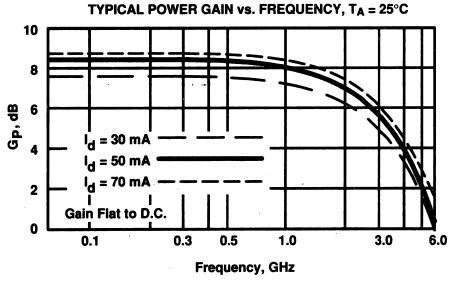
The MSA-0486 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost, surface mount plastic package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

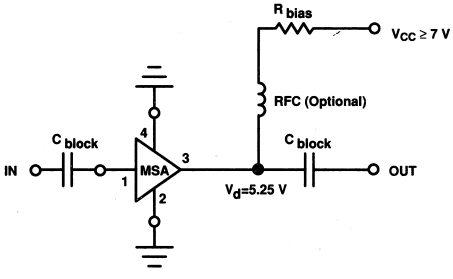
86 Plastic Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)



Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 50 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz	dB	 7.0	8.3 8.0	
ΔG_P	Gain Flatness	f = 0.1 to 2.0 GHz	dB		±0.6	
$f_{3\,dB}$	3 dB Bandwidth		GHz		3.2	
VSWR	Input VSWR	f = 0.1 to 2.0 GHz			1.5:1	
	Output VSWR	f = 0.1 to 2.0 GHz			1.9:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		12.5	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		7.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		25.5	
t_D	Group Delay	f = 1.0 GHz	psec.		140	
V_d	Device Voltage		V	4.2	5.25	6.3
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes: 1. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors".
2. The recommended operating current range for this device is 30 mA to 70 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	85 mA
Power Dissipation[2,3]	500 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

Thermal Resistance[2,4]: θ_{jc} = 100°C/W

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 10 mW/°C for T_C > 100°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Part Number Ordering Information

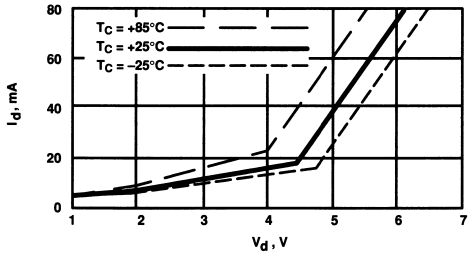
Part Number	Devices Per Reel	Reel Size
MSA-0486-TR1	1000	7"
MSA-0486-TR2	4000	13"

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

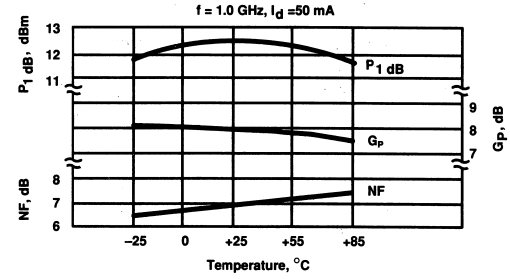
Typical Performance, T_A = 25°C

(unless otherwise noted)

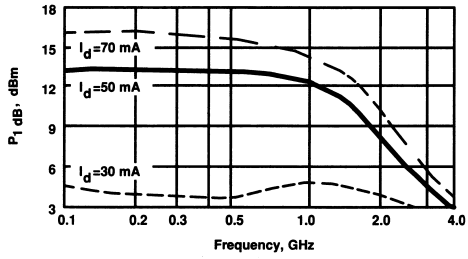
DEVICE CURRENT vs. VOLTAGE



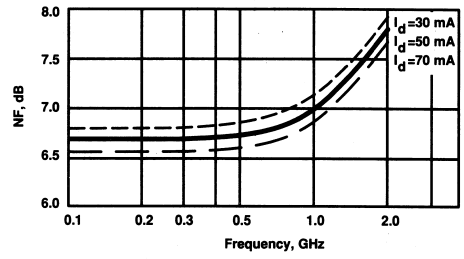
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. CASE TEMPERATURE
f = 1.0 GHz, I_d =50 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 50 mA

Freq.	S11		S21			S12			S22	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.14	178	8.4	2.62	175	–16.2	.154	1	.16	–10
0.2	.14	175	8.3	2.61	170	–16.3	.153	2	.16	–20
0.4	.14	171	8.2	2.57	161	–16.3	.154	3	.17	–39
0.6	.13	168	8.1	2.54	151	–16.0	.158	4	.18	–57
0.8	.13	166	8.0	2.52	141	–15.9	.161	5	.20	–74
1.0	.13	165	7.9	2.48	131	–15.7	.165	6	.21	–88
1.5	.15	168	7.7	2.42	108	–14.8	.182	8	.27	–121
2.0	.21	168	7.3	2.32	84	–14.0	.199	7	.32	–149
2.5	.29	165	6.8	2.18	65	–13.1	.222	4	.38	–168
3.0	.37	153	5.9	1.97	43	–12.7	.231	–1	.40	173
3.5	.44	142	4.8	1.74	24	–12.5	.238	–5	.41	157
4.0	.50	130	3.6	1.52	7	–12.5	.238	–10	.41	145
5.0	.61	109	1.3	1.16	–21	–12.7	.231	–17	.43	132

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0500
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

- **Cascadable 50 Ω Gain Block**
- **High Output Power: +23 dBm typical P_{1dB} at 1.0 GHz**
- **Low Distortion: 33 dBm typical IP_3 at 1.0 GHz**
- **8.5 dB typical Gain at 1.0 GHz**

Description

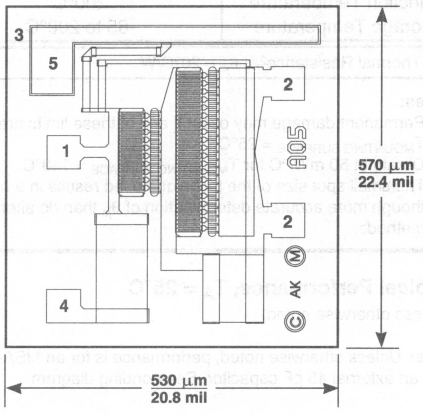
The MSA-0500 is a high performance, medium power silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broadband IF and RF amplifiers in industrial and military systems.

The MODAMP MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent uniformity, performance and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire.

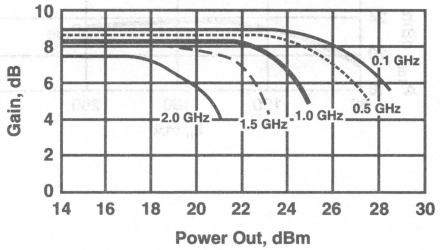
This chip is intended to be used with an external blocking capacitor completing the shunt feedback path (closed loop). Data sheet characterization is given for a 45 pF capacitor. Low frequency performance can be extended by using a larger valued capacitor[1].

Chip Outline[1]



Unless otherwise specified, tolerances are ±13 µm/±0.5 mils.
Chip thickness is 114 µm/4.5 mil Bond Pads are 41 µm/1.6 mil typical on each side.
*Output contact is normally made by die attaching the backside of the die.

Typical Gain vs. Power Out
T_A = 25°C, I_d = 165 mA



Electrical Specifications[2], T_A = 25°C

Unless otherwise noted, performance is for a MSA-0500 used with an external 45 pF capacitor. See bonding diagram.

Symbol	Parameters and Test Conditions[3]: I_d = 165 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
$P_{1\ dB}$	Output Power @1 dB Gain Compression	f = 1.0 GHz	dBm		23.0	
G_P	Power Gain ($\|S_{21}\|^2$)	f = 1.0 GHz	dB		9.0	
ΔG_P	Gain Flatness	f = 0.1 to 2.0 GHz	dB		±0.75	
$f_{3\ dB}$	3 dB Bandwidth[4]		GHz		2.8	
VSWR	Input VSWR	f = 0.1 to 2.0 GHz			2.0:1	
	Output VSWR	f = 0.1 to 2.0 GHz			2.5:1	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		33.0	
$NF_{50\ \Omega}$	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
t_D	Group Delay	f = 1.0 GHz	psec		125	
V_d	Device Voltage		V	10.5	12.0	13.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–16	

Notes:
1. See Application Note, AN-S009: MODAMP™ Silicon MMIC Chip Use for additional information.
2. The recommended operating current range for this device is 80 to 200 mA. Typical performance as a function of current is on the following page.
3. RF performance of the chip is determined by packaging and testing 10 devices per wafer.
4. Referenced from 0.1 GHz gain (G_P).

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	225 mA
Power Dissipation[2,3]	3.0 W
RF Input Power	+25 dBm
Junction Temperature	200°C
Storage Temperature	-65 to 200°C

Thermal Resistance[2,4]: θ_{jc} = 20°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{MOUNTING\ SURFACE}$ = 25°C.
3. Derate at 50 mW/°C for $T_{MOUNTING\ SURFACE}$ > 140°C.
4. The small spot size of the technique used results in a higher, though more accurate determination of θ_{jc} than do alternate methods.

Part Number Ordering Information

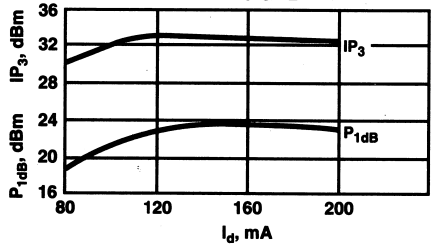
Part Number	Devices Per Tray
MSA-0500-GP2	10
MSA-0500-GP4	100
MSA-0500-GP6	Up to 300

Typical Performance, T_A = 25°C

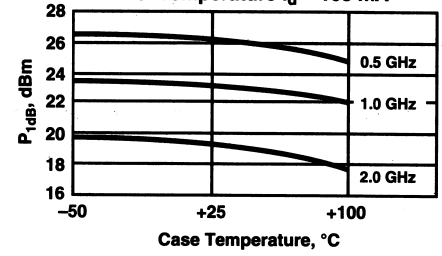
(Unless otherwise noted)

Note: Unless otherwise noted, performance is for an MSA-0500 used with an external 45 pF capacitor. See bonding diagram.

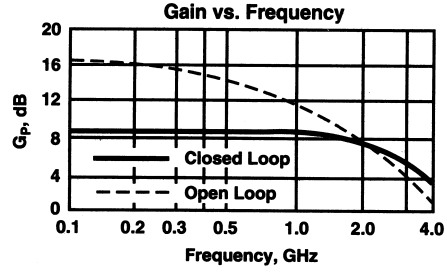
Output Power @ 1 dB Gain Compression, Third Order Intercept Point vs. Current f = 1.0 GHz



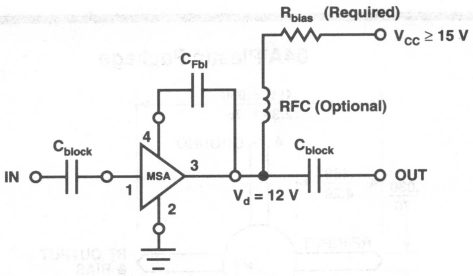
Output Power @ 1 dB Gain Compression vs. Temperature I_d = 165 mA



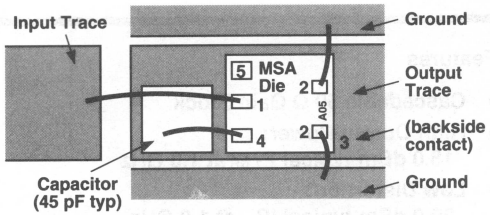
Gain vs. Frequency



Typical Biasing Configuration



Bonding Diagram



Numbers refer to pin contacts listed on the Chip Outline.

Typical Scattering Parameters[5,6]

$T_A = 25$ °C, $I_d = 165$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
.001	.68	-8	15.6	6.05	176	-26.2	.049	25	.79	-7	0.92
.005	.57	-38	14.6	5.37	166	-19.3	.108	38	.67	-35	0.56
.010	.43	-65	12.8	4.38	158	-15.7	.165	30	.50	-61	0.64
.050	.16	-111	9.8	3.08	164	-14.2	.194	10	.19	-101	1.06
.100	.12	-134	9.3	2.90	169	-14.0	.200	4	.13	-117	1.11
.200	.12	-141	9.1	2.86	168	-13.9	.202	4	.12	-125	1.13
.400	.13	-133	9.1	2.84	162	-13.8	.204	4	.17	-116	1.10
.600	.16	-124	9.1	2.84	155	-13.7	.207	4	.22	-109	1.05
.800	.21	-118	9.0	2.83	148	-13.6	.210	5	.28	-108	0.99
1.00	.25	-115	9.0	2.83	139	-13.4	.213	6	.34	-106	0.91
1.50	.36	-113	8.8	2.75	118	-12.7	.232	9	.44	-107	0.72
2.00	.45	-120	8.2	2.58	96	-11.6	.262	12	.66	-111	0.39
2.50	.51	-125	7.3	2.32	83	-11.0	.281	17	.58	-109	0.43
3.00	.52	-134	6.0	2.00	66	-10.5	.297	18	.58	-109	0.46
3.50	.51	-144	4.8	1.75	52	-9.6	.329	20	.58	-106	0.49
4.00	.46	-157	3.7	1.53	39	-9.2	.347	21	.54	-104	0.60

Notes: 5. S-parameters are de-embedded from 200 mil BeO package measured data using the package model found in the DEVICE MODELS section.

6. S-parameter data assumes an external 45 pF capacitor. Low frequency performance can be extended using a larger valued capacitor.

HEWLETT PACKARD

MSA-0504
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

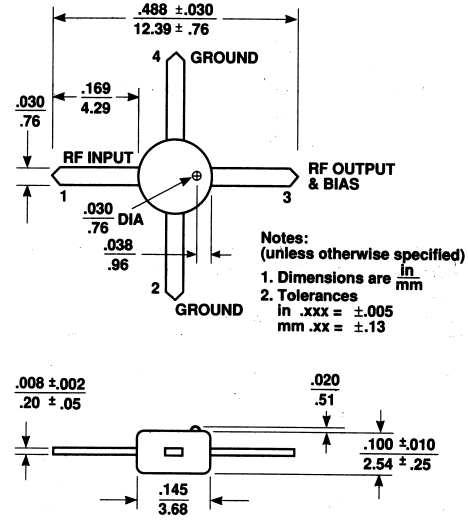
- **Cascadable 50 Ω Gain Block**
- **High Output Power:**
  18.0 dBm typical $P_{1\,dB}$ at 1.0 GHz
- **Low Distortion:**
  29.0 dBm typical IP_3 at 1.0 GHz
- **7.0 dB typical Gain at 1.0 GHz**
- **Low Cost Plastic Package**

Description

The MSA-0504 is a high performance medium power silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broadband IF and RF amplifiers in commercial systems.

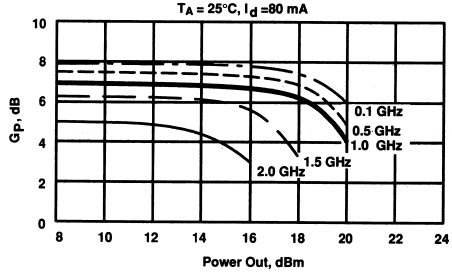
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent performance, uniformity, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

04A Plastic Package

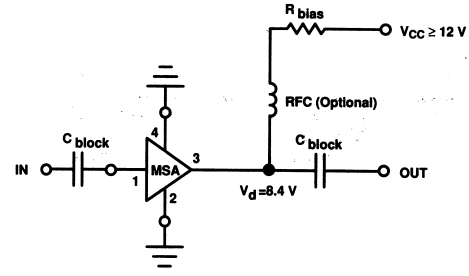


TYPICAL GAIN vs. POWER OUT

T_A = 25°C, I_d = 80 mA



Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 80 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
P_{1dB}	Output Power @ 1 dB Gain Compression	f = 0.5 GHz f = 1.0 GHz	dBm dBm	 16.0	19.0 18.0	
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.5 GHz f = 1.0 GHz	dB dB	 6.0	7.5 7.0	
ΔG_P	Gain Flatness	f = 0.1 to 1.5 GHz	dB		±0.75	
$f_{3\,dB}$	3 dB Bandwidth[2]		GHz		2.3	
VSWR	Input VSWR	f = 0.1 to 1.5 GHz			1.6:1	
	Output VSWR	f = 0.1 to 1.5 GHz			2.0:1	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		29.0	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
t_D	Group Delay	f = 1.0 GHz	psec.		180	
V_d	Device Voltage		V	6.7	8.4	10.1
dV/dT	Device Voltage Temperature Coefficient		mV/°C		−16.0	

Notes: 1. The recommended operating current range for this device is 60 mA to 100 mA. Typical performance as a function of current is on the following page.
2. Referenced from 0.1 GHz Gain (Gp).

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	135 mA
Power Dissipation[2,3]	1.5 W
RF Input Power	+25 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 150°C

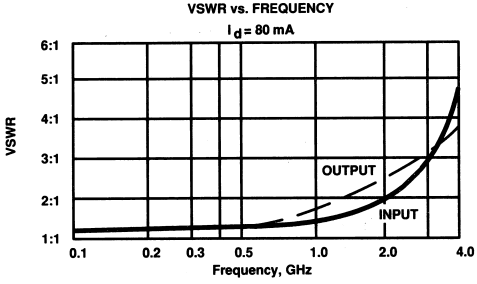
Thermal Resistance[2,4]: θ_{jc} = 75°C/W

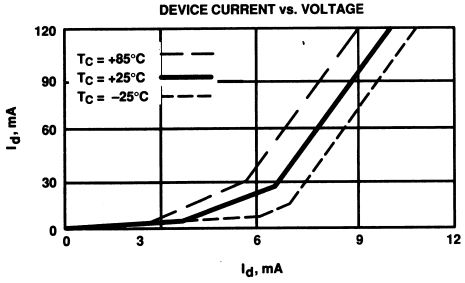
Notes:

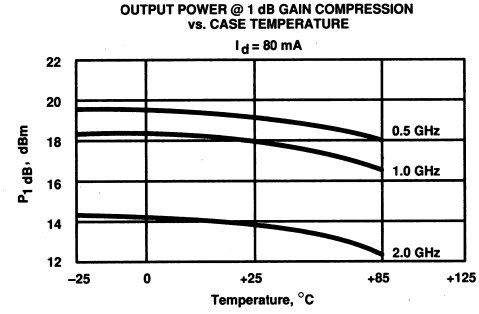
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 13.3 mW/°C for T_C > 88°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

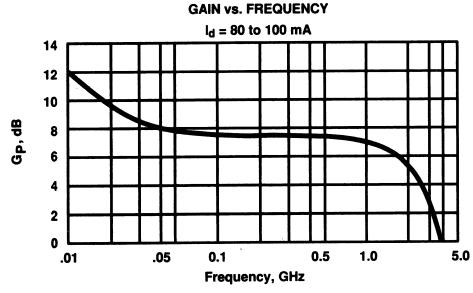
Typical Performance, T_A = 25°C

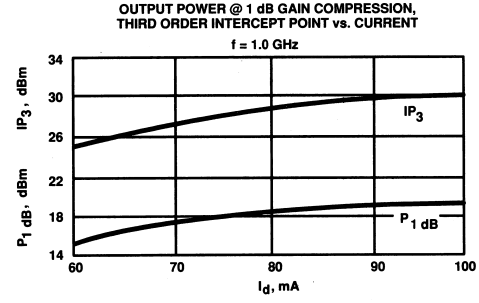
(unless otherwise noted)











Typical Scattering Parameters

T_A = 25°C, I_d = 80 mA

Freq. MHz	S11 Mag	S11 Ang	S21 dB	S21 Mag	S21 Ang	S12 dB	S12 Mag	S12 Ang	S22 Mag	S22 Ang	k
5	.54	–43	14.7	5.43	160	–18.4	.120	37	.63	–39	0.60
25	.24	–112	9.3	2.92	155	–13.8	.204	12	.24	–101	0.99
50	.18	–142	8.1	2.54	161	–13.7	.206	3	.16	–125	1.17
100	.14	–156	7.8	2.45	166	–13.7	.207	3	.13	–137	1.18
200	.14	–168	7.6	2.40	163	–13.7	.206	1	.13	–146	1.20
400	.14	–174	7.5	2.37	150	–13.7	.206	1	.16	–143	1.19
600	.14	–175	7.4	2.34	137	–13.6	.208	–1	.20	–144	1.18
800	.15	–174	7.2	2.29	124	–13.5	.211	–1	.25	–148	1.15
1000	.17	–174	7.0	2.24	111	–13.6	.209	–3	.29	–154	1.14
1500	.23	–179	6.4	2.09	80	–13.3	.216	–4	.37	–168	1.06
2000	.33	171	5.5	1.88	51	–12.8	.230	–10	.48	178	0.91
2500	.42	156	4.3	1.64	27	–13.0	.224	–12	.51	165	0.90
3000	.49	146	3.2	1.44	6	–12.8	.230	–11	.55	157	0.92

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0505
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

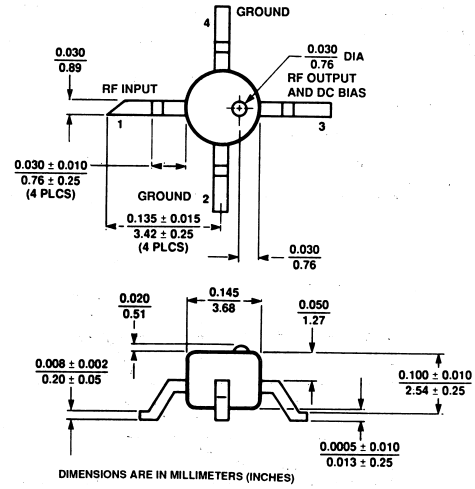
- **Cascadable 50 Ω Gain Block**
- **High Output Power:**
  18.0 dBm typical $P_{1\,dB}$ at 1.0 GHz
- **Low Distortion:**
  29.0 dBm typical IP_3 at 1.0 GHz
- **7.0 dB typical Gain at 1.0 GHz**
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Description

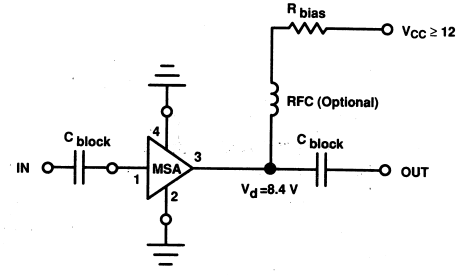
The MSA-0505 is a high performance medium power silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost, surface mount package.This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broadband IF and RF amplifiers in commercial systems.

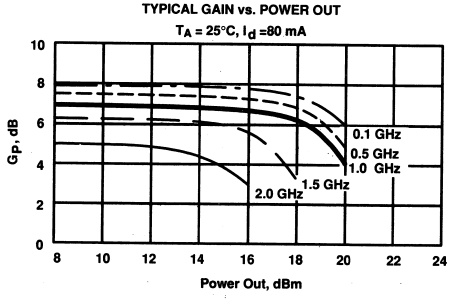
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent performance, uniformity, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

05 Plastic Package



Typical Biasing Configuration





Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 80 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
P_{1dB}	Output Power @ 1 dB Gain Compression	f = 0.5 GHz f = 1.0 GHz	dBm dBm	 16.0	19.0 18.0	
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.5 GHz f = 1.0 GHz	dB dB	 6.0	7.5 7.0	
ΔG_P	Gain Flatness	f = 0.1 to 1.5 GHz	dB		±0.75	
$f_{3\,dB}$	3 dB Bandwidth[3]		GHz		2.3	
VSWR	Input VSWR	f = 0.1 to 1.5 GHz			1.6:1	
	Output VSWR	f = 0.1 to 1.5 GHz			2.0:1	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		29.0	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
t_D	Group Delay	f = 1.0 GHz	psec.		190	
V_d	Device Voltage		V	6.7	8.4	10.1
dV/dT	Device Voltage Temperature Coefficient		mV/°C		−16.0	

Notes: 1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices."
2. The recommended operating current range for this device is 60 mA to 100 mA. Typical gain performance as a function of current is on the following page.
3. Referenced from 0.1 GHz Gain (Gp).

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	135 mA
Power Dissipation[2,3]	1.5 W
RF Input Power	+25 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 150°C

Thermal Resistance[2,4]: θ_{jc} = 85°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 11.8 mW/°C for T_C > 73°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Part Number Ordering Information

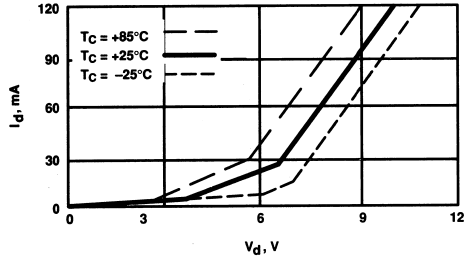
Part Number	Devices Per Reel	Reel Size
MSA-0505-TR1	500	7"
MSA-0505-TR2	1500	13"

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

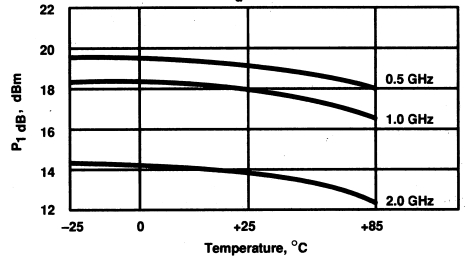
Typical Performance, T_A = 25°C

(unless otherwise noted)

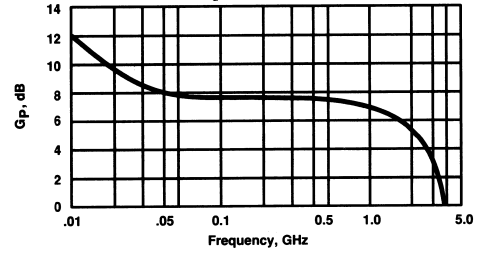
DEVICE CURRENT vs. VOLTAGE



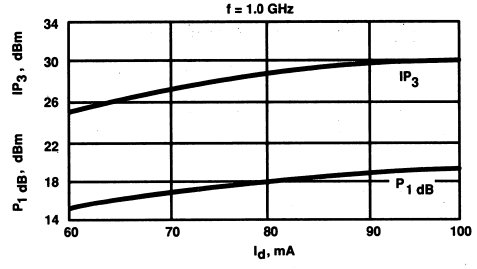
OUTPUT POWER @ 1 dB GAIN COMPRESSION vs. CASE TEMPERATURE
I_d = 80 mA



GAIN vs. FREQUENCY
I_d = 80 to 100 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION, THIRD ORDER INTERCEPT POINT vs. CURRENT
f = 1.0 GHz



Typical Scattering Parameters

T_A = 25°C, I_d = 80 mA

Freq. MHz	S11 Mag	S11 Ang	S21 dB	S21 Mag	S21 Ang	S12 dB	S12 Mag	S12 Ang	S22 Mag	S22 Ang	k
5	.56	–39	14.9	5.56	161	–18.5	.120	39	.65	–36	0.60
25	.24	–103	9.7	3.05	156	–13.9	.202	12	.25	–90	0.97
50	.15	–130	8.2	2.57	163	–13.7	.207	7	.15	–116	1.15
100	.13	–155	7.8	2.45	165	–13.7	.207	3	.11	–132	1.21
200	.12	–170	7.7	3.43	161	–13.5	.211	1	.11	–145	1.21
400	.12	178	7.5	2.37	148	–13.6	.209	–1	.14	–146	1.23
600	.13	172	7.4	2.34	134	–13.6	.209	–2	.17	–151	1.23
800	.13	168	7.2	2.29	119	–13.6	.209	–3	.21	–157	1.23
1000	.14	166	7.0	2.24	105	–13.4	.213	–4	.25	–164	1.21
1500	.21	159	6.4	2.09	72	–13.3	.217	–6	.34	176	1.16
2000	.30	148	5.2	1.82	42	–13.1	.222	–9	.42	159	1.12
2500	.40	136	4.1	1.60	17	–12.9	.227	–11	.48	146	1.05
3000	.52	121	2.7	1.36	–7	–12.6	.234	–16	.55	133	0.92

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0520
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

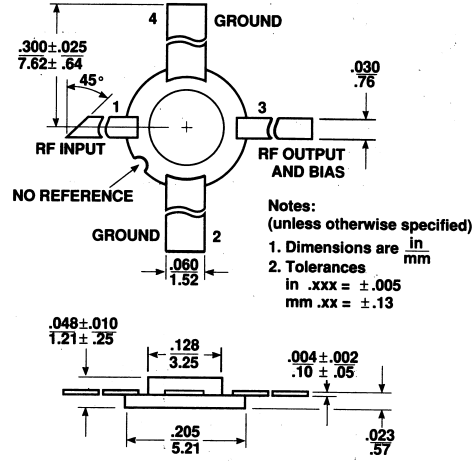
- **Cascadable 50 Ω Gain Block**
- **High Output Power:**
  +23 dBm typical $P_{1\,dB}$ at 1.0 GHz
- **Low Distortion:**
  33 dBm typical IP_3 at 1.0 GHz
- **8.5 dB typical Gain at 1.0 GHz**
- **Hermetic, Metal/Beryllia Microstrip Package**

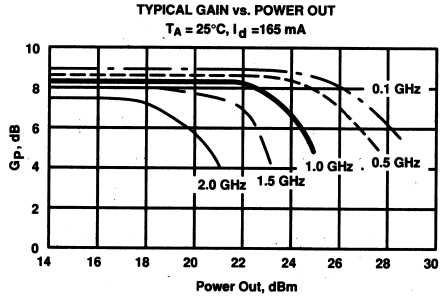
Description

The. MSA-0520 is a high performance, medium power silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic, BeO disk package for good thermal characteristics. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military systems.

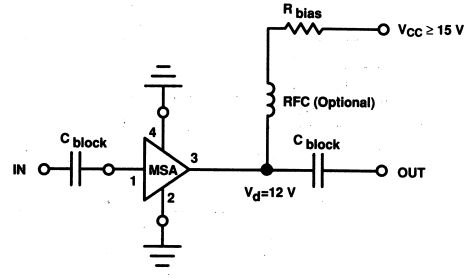
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

200 mil BeO Package





Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 165 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm	21.0	23.0	
G_P	Power Gain ($\|S_{21}\|^2$)	f = 1.0 GHz	dB	7.5	8.5	9.5
ΔG_P	Gain Flatness	f = 0.1 to 2.0 GHz	dB		±0.75	
$f_{3\,dB}$	3 dB Bandwidth[2]		GHz		2.8	
VSWR	Input VSWR	f = 0.1 to 2.0 GHz			2.0:1	
	Output VSWR	f = 0.1 to 2.0 GHz			2.5:1	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		33.0	
$NF_{50\,\Omega}$	50 Ω Noise Figure	f = 1.0 GHz	dB		6.5	
t_D	Group Delay	f = 1.0 GHz	psec.		170	
V_d	Device Voltage		V	10.5	12.0	13.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		−16.0	

Notes: 1. The recommended operating current range for this device is 80 mA to 200 mA. Typical performance as a function of current is on the following page.
2. Referenced from 0.1 GHz Gain (Gp).

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	225 mA
Power Dissipation[2,3]	3.0 W
RF Input Power	+25 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

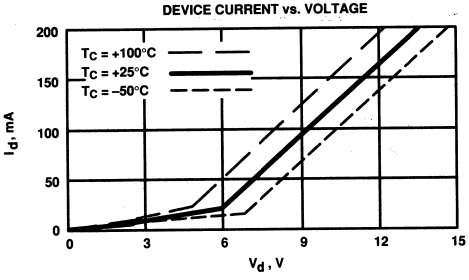
Thermal Resistance[2,4]: θ_{jc} = 25°C/W

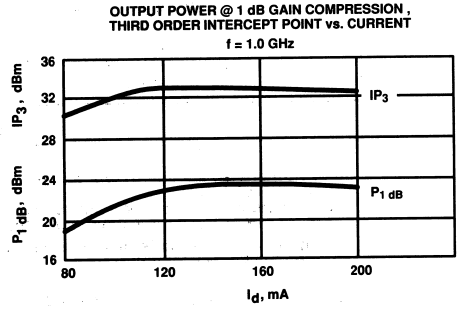
Notes:

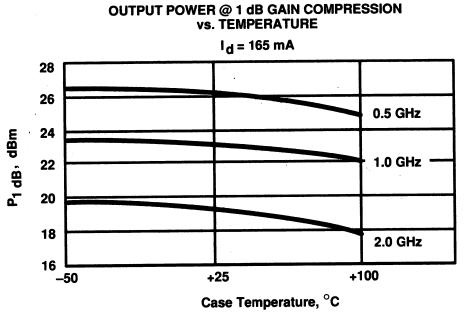
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 40 mW/°C for T_C > 125°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

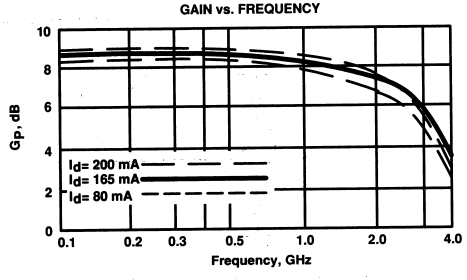
Typical Performance, T_A = 25°C

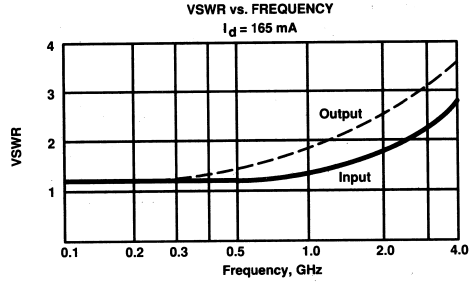
(unless otherwise noted)











Typical Scattering Parameters

T_A = 25°C, I_d = 165 mA

Freq. MHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang	k
5	.57	–38	14.4	5.25	165	–19.4	.107	38	.67	–35	0.57
25	.25	–90	10.7	3.42	160	–14.9	.180	17	.29	–81	.093
50	.15	–111	9.5	2.97	163	–14.4	.190	9	.18	–97	1.10
100	.11	–138	8.9	2.80	166	–14.2	.195	3	.11	–113	1.16
200	.10	–152	8.8	2.75	163	–14.1	.197	1	.10	–125	1.17
400	.10	–152	8.7	2.72	152	–14.1	.198	–2	.14	–123	1.16
600	.11	–147	8.6	2.70	140	–14.0	.199	–4	.18	–123	1.14
800	.13	–142	8.5	2.67	128	–14.1	.199	–6	.22	–127	1.12
1000	.15	–140	8.4	2.64	115	–14.1	.198	–8	.27	–131	1.09
1500	.22	–142	8.0	2.52	85	–13.7	.206	–12	.34	–143	0.98
2000	.30	–156	7.4	2.36	55	–13.3	.216	–16	.43	–158	0.85
2500	.37	–170	6.7	2.16	33	–12.9	.227	–18	.48	–166	0.75
3000	.41	170	5.6	1.91	8	–12.7	.232	–23	.51	–177	0.70
3500	.45	149	4.5	1.68	–16	–12.1	.249	–31	.55	173	0.63
4000	.46	124	3.3	1.45	–40	–11.7	.259	–39	.56	162	0.66

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0600
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

- **Cascadable 50 Ω Gain Block**
- **Low Operating Voltage (3.5 V typical V_d)**
- **3 dB Bandwidth: DC to 1.0 GHz**
- **High Gain: 19.5 dB typical at 0.5 GHz**
- **Low Noise Figure: 2.8 dB typical at 0.5 GHz**

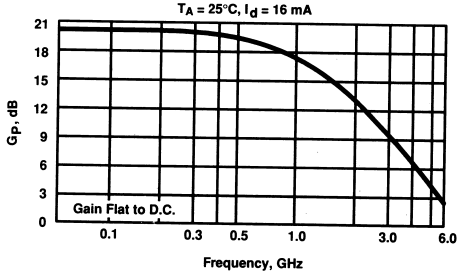
Description

The MSA-0600 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial, industrial and military applications.

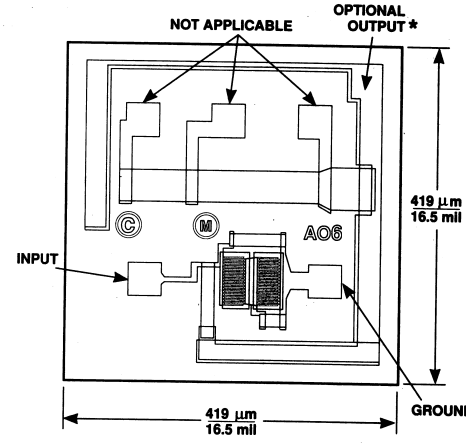
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire. See APPLICATIONS section, "Chip Use".

TYPICAL POWER GAIN vs. FREQUENCY
T_A = 25°C, I_d = 16 mA

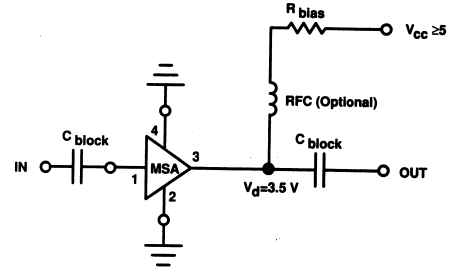


Chip Outline[1]



Unless otherwise specified, tolerances are ±13 µm / ±0.5 mils.
Chip thickness is 114 µm / 4.5 mil. Bond pads are 41 µm / 1.6 mil typical on each side.
*** Output contact is made by die attaching the backside of the die.**

Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions[3]: I_d = 16 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		20.5	
ΔG_P	Gain Flatness	f = 0.1 to 0.6 GHz	dB		±0.7	
$f_{3\,dB}$	3 dB Bandwidth		GHz		1.0	
VSWR	Input VSWR	f = 0.1 to 1.5 GHz			1.9:1	
	Output VSWR	f = 0.1 to 1.5 GHz			1.8:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression,	f = 0.5 GHz	dBm		2.0	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		2.8	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.5	
t_D	Group Delay	f = 0.5 GHz	psec.		200	
V_d	Device Voltage		V	3.1	3.5	3.9
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes: 1. This chip contains additional biasing options. The performance specified applies only to the bias option whose bond pads are indicated on the chip outline. Refer to the APPLICATIONS section "MODAMP™ Silicon MMIC Chip Use" for additional information.
2. The recommended operating current range for this device is 12 mA to 30 mA. Typical performance as a function of current is on the following page.
3. RF performance of the chip is determined by packaging and testing 10 devices per wafer in a dual ground configuration.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 50°C/W

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{MOUNTING\ SURFACE}$ = 25°C
3. Derate at 20 mW/°C for $T_{MOUNTING\ SURFACE}$ > 190°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

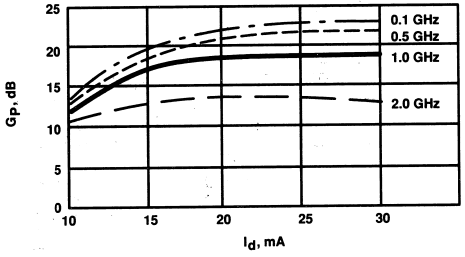
Part Number Ordering Information

Part Number	Devices Per Tray
MSA-0600-GP2	10
MSA-0600-GP4	100
MSA-0600-GP6	up to 300

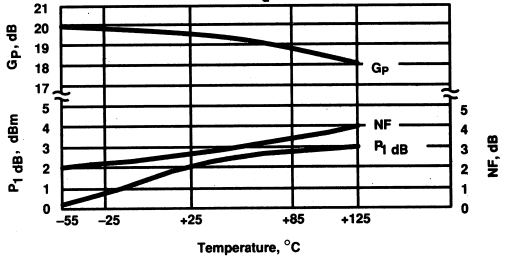
Typical Performance, T_A = 25°C

(unless otherwise noted)

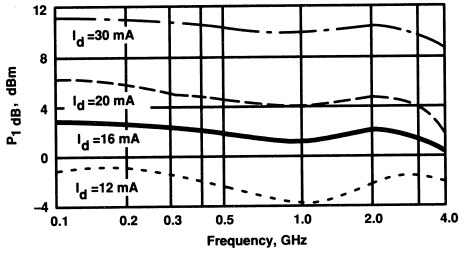
POWER GAIN vs. CURRENT



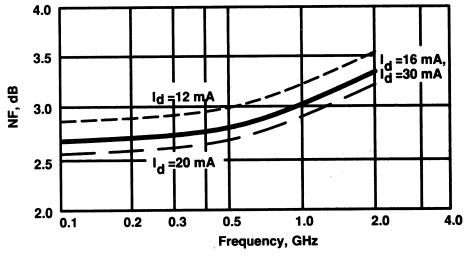
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. MOUNTING
SURFACE TEMPERATURE
f = 0.5 GHz, I_d = 16 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters[4]: Z_O = 50 Ω

T_A = 25°C, I_d = 16 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang	k
0.1	.05	–148	20.6	10.66	173	–23.3	.068	4	.05	–67	1.05
0.2	.07	–134	20.4	10.48	166	–23.1	.070	8	.09	–91	1.04
0.3	.09	–125	20.2	10.28	159	–22.6	.074	13	.13	–102	1.01
0.4	.11	–121	20.0	10.01	151	–22.4	.076	15	.16	–110	1.00
0.5	.13	–120	19.7	9.71	145	–22.1	.078	17	.20	–117	0.98
0.6	.15	–119	19.4	9.34	140	–21.8	.081	20	.22	–124	0.97
0.8	.19	–121	18.7	8.60	123	–20.7	.092	25	.25	–136	0.93
1.0	.25	–123	17.9	7.82	117	–19.8	.102	26	.28	–148	0.90
1.5	.32	–134	15.7	6.10	96	–18.3	.122	29	.29	–168	0.89
2.0	.40	–149	13.5	4.73	79	–17.4	.136	27	.26	175	0.91
2.5	.45	–157	11.6	3.79	70	–16.9	.142	30	.23	169	0.97
3.0	.49	–171	9.9	3.12	61	–16.6	.148	28	.19	168	1.03
3.5	.51	–174	8.3	2.60	51	–16.4	.152	25	.16	173	1.10
4.0	.51	179	6.9	2.21	43	–16.3	.153	26	.12	–170	1.22
4.5	.51	170	5.7	1.93	37	–16.0	.159	24	.10	–149	1.31
5.0	.51	162	4.7	1.71	29	–15.9	.161	24	.11	–126	1.41

Notes: 4. S-parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section.

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MSA-0611
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

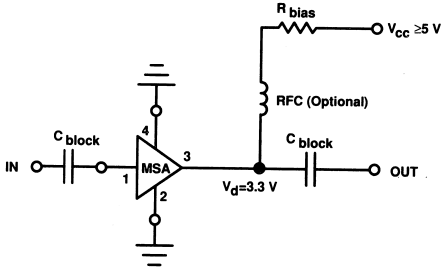
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 0.7 GHz**
- **High Gain: 18.0 dB typical at 0.5 GHz**
- **Low Noise Figure: 3.0 dB typical at 0.5 GHz**
- **Low Cost Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Description

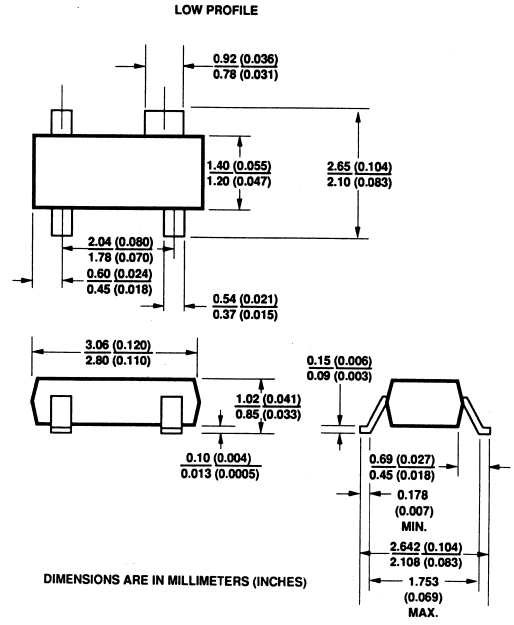
The MSA-0611 is a low cost silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in the surface mount plastic SOT-143 package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

Typical Biasing Configuration



SOT-143 Plastic Package



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 16 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 0.5 GHz	dB	 16.0	19.5 18.0	
ΔG_P	Gain Flatness	f = 0.1 to 0.5 GHz	dB		±0.8	
$f_{3\,dB}$	3 dB Bandwidth		GHz		0.7	
VSWR	Input VSWR	f = 0.1 to 1.5 GHz			1.6:1	
	Output VSWR	f = 0.1 to 1.5 GHz			1.5:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 0.5 GHz	dBm		2.0	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		3.0	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.0	
t_D	Group Delay	f = 0.5 GHz	psec.		225	
V_d	Device Voltage	T_C = 25°C	V	2.6	3.3	4.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes: 1. Refer to PACKAGING section "Tape-and-Reel Packaging for Surface Mount Semiconductors".
2. The recommended operating current range for this device is 12 mA to 20 mA. Gain performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	40 mA
Power Dissipation[2,3]	125 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

Thermal Resistance[2,4]: θ_{jc} = 505°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 2.0 mW/°C for T_C > 87°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Part Number Ordering Information

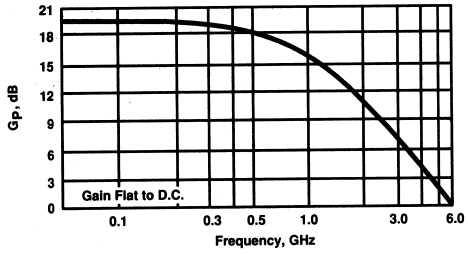
Part Number	Devices Per Reel	Reel Size
MSA-0611-TR1	3000	7"
MSA-0611-TR2	10000	13"

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

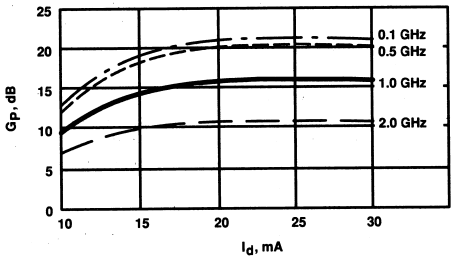
Typical Performance, T_A = 25°C

(unless otherwise noted)

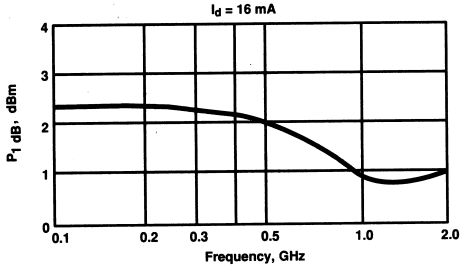
POWER GAIN vs. FREQUENCY
I_d = 16 mA



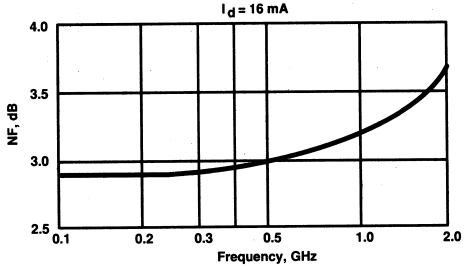
POWER GAIN vs. CURRENT



OUTPUT POWER @ 1 dB GAIN COMPRESSION vs. FREQUENCY
I_d = 16 mA



NOISE FIGURE vs. FREQUENCY
I_d = 16 mA



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 16 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang	k
0.1	.04	–176	19.6	9.53	170	–23.0	.071	6	.04	–57	1.07
0.2	.03	–163	19.3	9.25	160	–22.7	.073	10	.07	–82	1.07
0.3	.03	–149	18.9	8.79	150	–22.8	.072	14	.09	–97	1.10
0.4	.04	–132	18.5	8.38	141	–21.9	.080	17	.11	–111	1.07
0.5	.05	–127	18.0	7.96	133	–21.6	.083	21	.13	–122	1.07
0.6	.07	–123	17.3	7.33	125	–21.2	.087	23	.15	–131	1.07
0.8	.10	–129	16.2	6.46	111	–19.7	.103	25	.17	–147	1.04
1.0	.13	–139	15.0	5.64	98	–19.0	.112	28	.18	–160	1.06
1.5	.22	–164	12.5	4.22	73	–17.1	.139	25	.19	175	1.07
2.0	.31	171	10.1	3.20	53	–16.1	.157	21	.19	160	1.13
2.5	.39	158	8.1	2.55	42	–15.4	.169	22	.20	153	1.19
3.0	.45	144	6.3	2.07	28	–15.0	.178	18	.19	150	1.26
3.5	.50	132	4.7	1.72	16	–14.6	.185	15	.16	152	1.33
4.0	.52	121	3.4	1.48	4	–14.1	.197	11	.14	166	1.37

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0635, -0636
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

- **Cascadable 50 Ω Gain Block**
- **Low Operating Voltage (3.5 V typical V_d)**
- **3 dB Bandwidth: DC to 0.9 GHz**
- **High Gain: 19.0 dB typical at 0.5 GHz**
- **Low Noise Figure: 2.8 dB typical at 0.5 GHz**
- **Cost Effective Ceramic Microstrip Package**

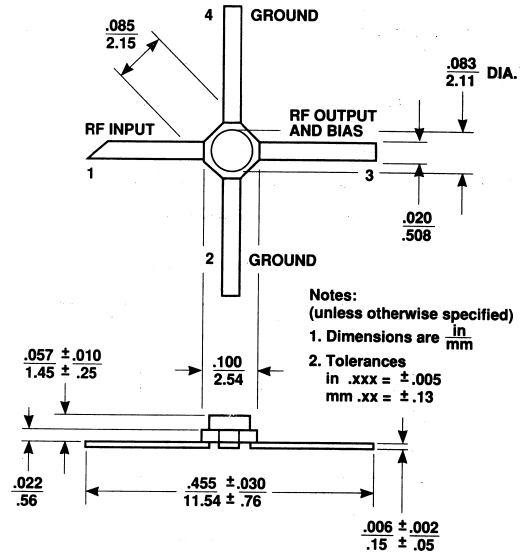
Description

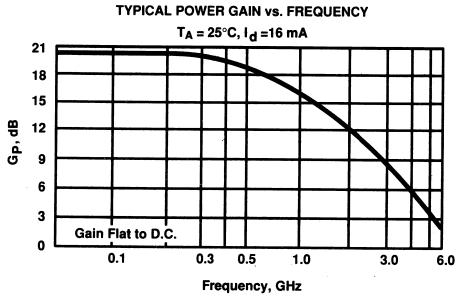
The MSA-0635 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a cost effective, microstrip package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

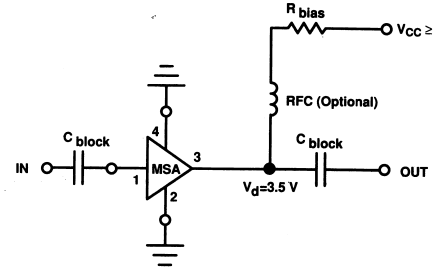
Available in cut lead version (package 36) as MSA-0636.

35 micro-X Package[1]





Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 16 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	19.0	20.5	22.0
ΔG_P	Gain Flatness	f = 0.1 to 2.5 GHz	dB		±0.7	±1.0
$f_{3\ dB}$	3 dB Bandwidth		GHz		0.9	
VSWR	Input VSWR	f = 0.1 to 1.5 GHz			1.4:1	
	Output VSWR	f = 0.1 to 1.5 GHz			1.3:1	
$P_{1\ dB}$	Output Power @ 1 dB Gain Compression	f = 0.5 GHz	dBm		2.0	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		2.8	4.0
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.5	
t_D	Group Delay	f = 0.5 GHz	psec.		200	
V_d	Device Voltage		V	3.1	3.5	3.9
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes: 1. Short leaded 36 package available upon request.
2. The recommended operating current range for this device is 12 mA to 30 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature[4]	–65°C to 200°C

Thermal Resistance[2,5]: θ_{jc} = 155°C/W

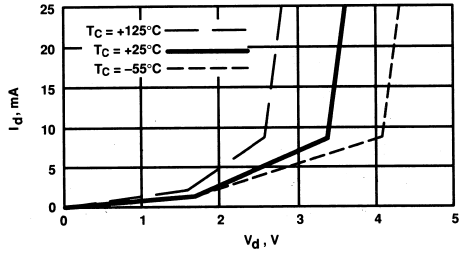
Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 6.5 mW/°C for T_C > 169°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

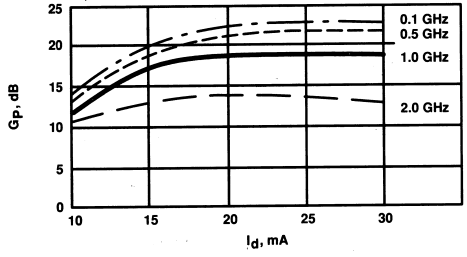
Typical Performance, T_A = 25°C

(unless otherwise noted)

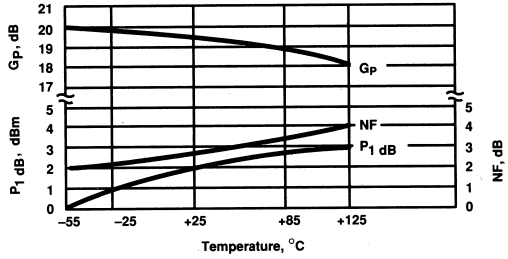
DEVICE CURRENT vs. VOLTAGE



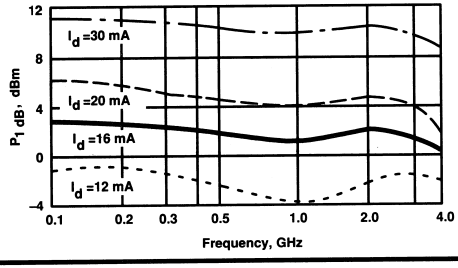
POWER GAIN vs. CURRENT



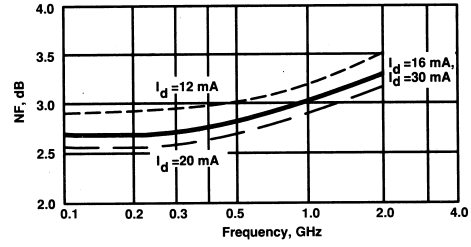
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. CASE TEMPERATURE
f = 0.5 GHz, I_d = 16 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 16 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang	k
0.1	.03	–178	20.5	10.59	171	–23.4	.068	5	.04	–44	1.05
0.2	.02	–177	20.3	10.31	161	–22.9	.071	8	.05	–68	1.04
0.3	.02	–164	20.0	9.96	152	–22.4	.076	14	.06	–87	1.04
0.4	.02	–116	19.6	9.55	144	–22.0	.079	19	.07	–104	1.03
0.5	.02	–100	19.2	9.08	136	–21.8	.081	21	.09	–114	1.04
0.6	.04	–89	18.7	8.59	128	–21.3	.086	24	.09	–123	1.04
0.8	.07	–96	17.7	7.66	115	–20.2	.098	29	.10	–140	1.03
1.0	.10	–108	16.6	6.79	103	–19.4	.107	31	.11	–156	1.02
1.5	.17	–134	14.2	5.13	79	–17.2	.138	30	.12	172	1.03
2.0	.24	–160	12.1	4.01	60	–15.8	.163	26	.12	148	1.04
2.5	.31	–178	10.3	3.26	48	–15.1	.175	27	.12	140	1.08
3.0	.37	166	8.7	2.72	34	–14.4	.190	24	.11	135	1.10
3.5	.42	151	7.4	2.33	21	–13.9	.203	19	.10	144	1.11
4.0	.46	139	6.2	2.04	9	–13.3	.216	16	.08	167	1.11
4.5	.48	126	5.1	1.81	–3	–12.8	.229	12	.08	–173	1.11
5.0	.52	110	4.2	1.62	–15	–12.2	.245	8	.09	–173	1.09

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0670
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

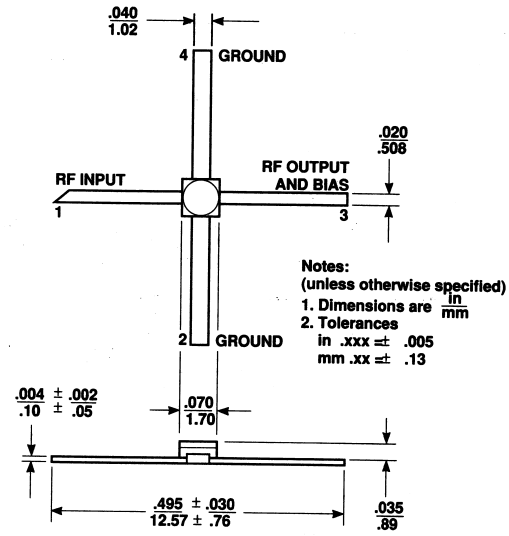
- **Cascadable 50 Ω Gain Block**
- **Low Operating Voltage (3.5 V typical V_d)**
- **3 dB Bandwidth: DC to 1.0 GHz**
- **High Gain: 19.5 dB typical at 0.5 GHz**
- **Low Noise Figure: 2.8 dB typical at 0.5 GHz**
- **Hermetic Gold-ceramic Microstrip Package**

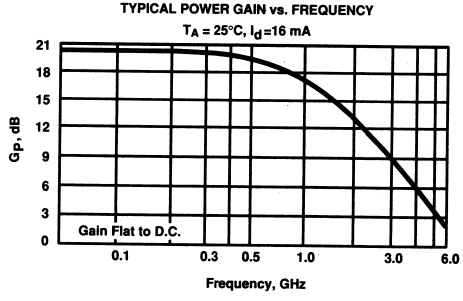
Description

The MSA-0670 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic, high reliability package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

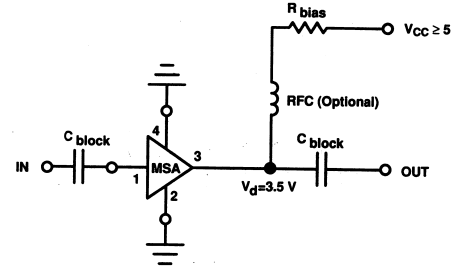
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

70 mil Package





Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 16 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	19.0	20.5	22.0
ΔG_P	Gain Flatness	f = 0.1 to 0.6 GHz	dB		±0.7	±1.0
$f_{3\,dB}$	3 dB Bandwidth		GHz		1.0	
VSWR	Input VSWR	f = 0.1 to 1.5 GHz			1.9:1	
	Output VSWR	f = 0.1 to 1.5 GHz			1.8:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 0.5 GHz	dBm		2.0	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		2.8	4.0
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.5	
t_D	Group Delay	f = 0.5 GHz	psec.		200	
V_d	Device Voltage		V	3.1	3.5	3.9
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note: 1. The recommended operating current range for this device is 12 mA to 30 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 130°C/W

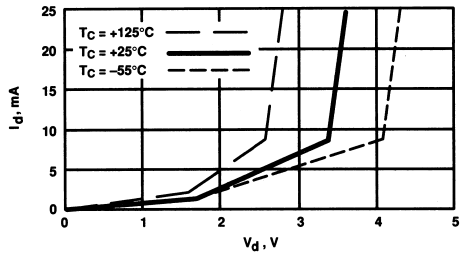
Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 7.7 mW/°C for T_C > 174°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

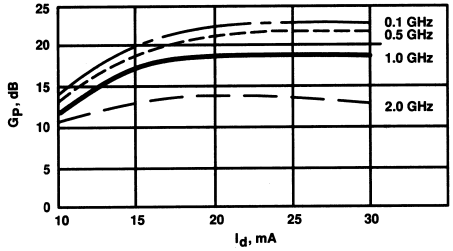
Typical Performance, T_A = 25°C

(unless otherwise noted)

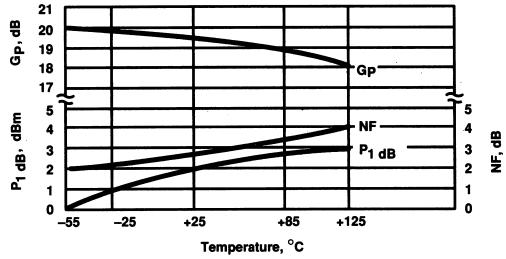
DEVICE CURRENT vs. VOLTAGE



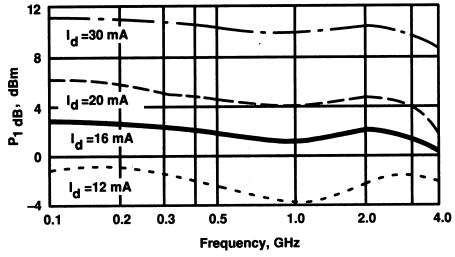
POWER GAIN vs. CURRENT



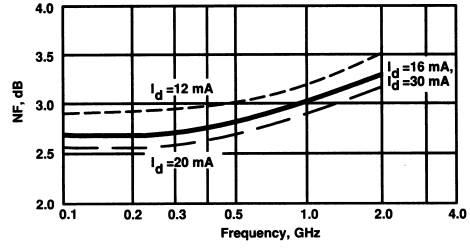
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. CASE TEMPERATURE
f = 0.5 GHz, I_d = 16 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 16 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang	k
0.1	.05	–147	20.5	10.62	172	–23.3	.068	4	.05	–69	1.05
0.2	.07	–134	20.4	10.41	164	–23.0	.070	8	.09	–92	1.04
0.3	.09	–126	20.1	10.16	156	–22.6	.074	12	.13	–104	1.02
0.4	.11	–123	19.9	9.85	148	–22.4	.076	14	.16	–113	1.00
0.5	.13	–123	19.6	9.50	141	–22.0	.079	16	.20	–121	0.99
0.6	.15	–123	19.2	9.09	135	–21.8	.082	18	.22	–128	0.97
0.8	.19	–126	18.4	8.28	122	–20.7	.093	22	.25	–141	0.94
1.0	.24	–129	17.5	7.46	110	–19.8	.103	22	.27	–154	0.92
1.5	.31	–141	15.2	5.76	87	–18.2	.124	23	.27	–176	0.91
2.0	.38	–157	13.0	4.47	68	–17.2	.138	19	.24	166	0.94
2.5	.42	–167	11.1	3.59	57	–16.7	.146	20	.21	158	1.01
3.0	.46	178	9.5	2.97	45	–16.4	.152	16	.17	156	1.07
3.5	.48	173	7.9	2.49	33	–16.2	.155	11	.14	163	1.15
4.0	.48	164	6.6	2.13	22	–16.1	.156	9	.11	–175	1.27
4.5	.48	155	5.5	1.87	13	–15.9	.161	5	.11	–154	1.35
5.0	.48	143	4.5	1.67	3	–15.8	.163	3	.14	–141	1.46

A model for this device is available in the DEVICE MODELS section.

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MSA-0685
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

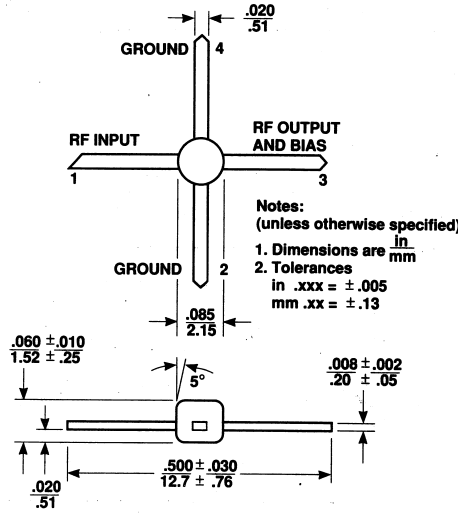
- **Cascadable 50 Ω Gain Block**
- **Low Operating Voltage (3.5 V typical V_d)**
- **3 dB Bandwidth: DC to 0.8 GHz**
- **High Gain: 18.5 dB typical at 0.5 GHz**
- **Low Noise Figure: 3.0 dB typical at 0.5 GHz**
- **Low Cost Plastic Package**

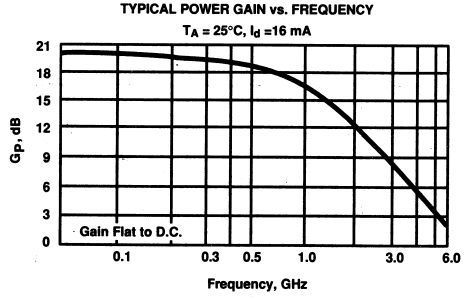
Description

The MSA-0685 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

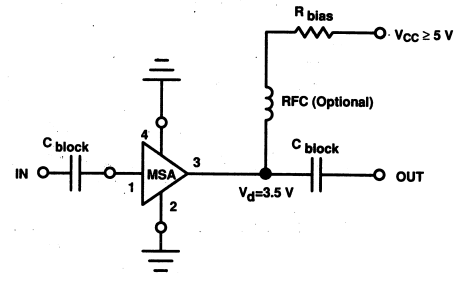
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

85 Plastic Package





Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 16 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 0.5 GHz	dB	 17.0	20.0 18.5	
ΔG_P	Gain Flatness	f = 0.1 to 0.5 GHz	dB		±0.7	
$f_{3\ dB}$	3 dB Bandwidth		GHz		0.8	
VSWR	Input VSWR	f = 0.1 to 1.5 GHz			1.5:1	
	Output VSWR	f = 0.1 to 1.5 GHz			1.4:1	
$P_{1\ dB}$	Output Power @ 1 dB Gain Compression	f = 0.5 GHz	dBm		2.0	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		3.0	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.5	
t_D	Group Delay	f = 0.5 GHz	psec.		200	
V_d	Device Voltage		V	2.8	3.5	4.2
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Note: 1. The recommended operating current range for this device is 12 mA to 25 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

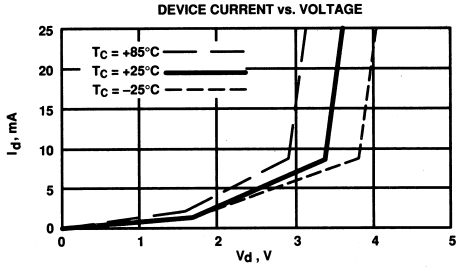
Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

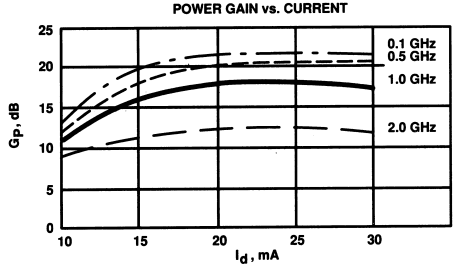
Thermal Resistance[2,4]: θ_{jc} = 110°C/W

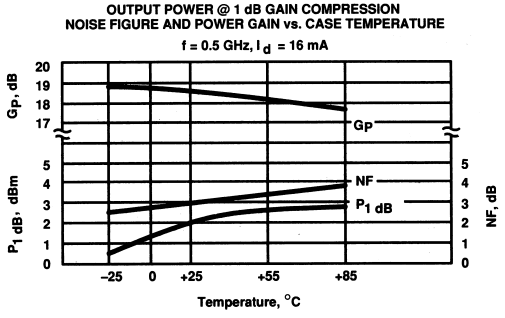
Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 9.1 mW/°C for T_C > 128°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

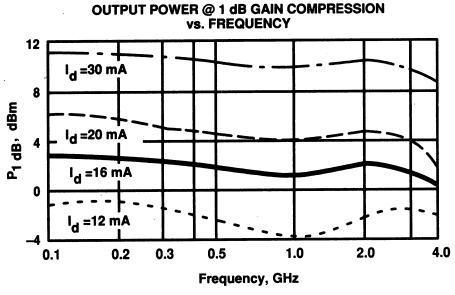
Typical Performance, T_A = 25°C

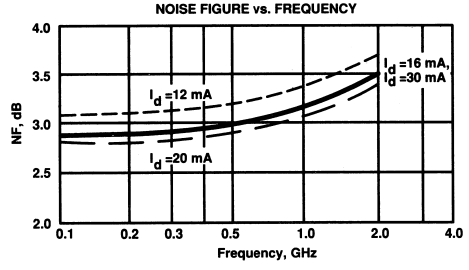
(unless otherwise noted)











Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 16 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.1	.04	171	20.1	10.09	171	–22.5	.075	5	.04	–30	1.04
0.2	.02	–180	19.8	9.75	161	–22.4	.076	10	.05	–56	1.04
0.3	.02	–143	19.4	9.38	153	–22.2	.077	15	.07	–76	1.05
0.4	.03	–113	19.1	8.99	145	–21.8	.081	17	.08	–91	1.04
0.5	.05	–105	18.7	8.57	138	–21.3	.086	21	.10	–104	1.04
0.6	.07	–101	18.2	8.14	131	–20.7	.092	25	.11	–116	1.03
0.8	.10	–111	17.3	7.32	119	–19.7	.103	28	.13	–134	1.01
1.0	.13	–118	16.4	6.57	107	–18.8	.115	28	.14	–150	0.99
1.5	.21	–140	14.1	5.06	84	–17.1	.140	28	.15	180	1.00
2.0	.29	–163	12.0	3.98	65	–15.8	.163	26	.16	157	1.02
2.5	.34	–176	10.3	3.26	55	–15.2	.174	28	.16	150	1.06
3.0	.41	169	8.7	2.71	42	–14.8	.181	25	.15	143	1.10
3.5	.46	157	7.2	2.31	30	–14.2	.194	22	.13	144	1.11
4.0	.49	146	6.1	2.01	18	–13.8	.203	20	.10	156	1.13
4.5	.52	135	5.0	1.77	7	–13.4	.215	17	.09	173	1.14
5.0	.54	123	4.1	1.60	–3	–12.9	.226	15	.09	–178	1.14

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0686
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

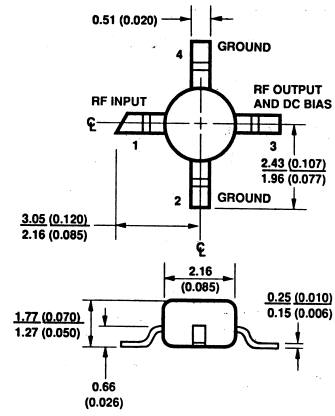
- **Cascadable 50 Ω Gain Block**
- **Low Operating Voltage (3.5 V typical V_d)**
- **3 dB Bandwidth: DC to 0.8 GHz**
- **High Gain: 18.5 dB typical at 0.5 GHz**
- **Low Noise Figure: 3.0 dB typical at 0.5 GHz**
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Description

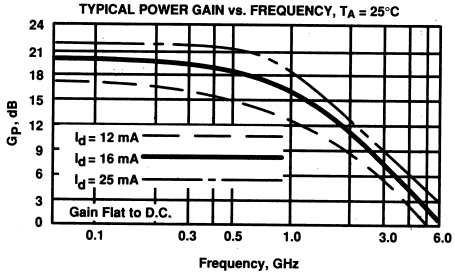
The MSA-0686 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost, surface mount plastic package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

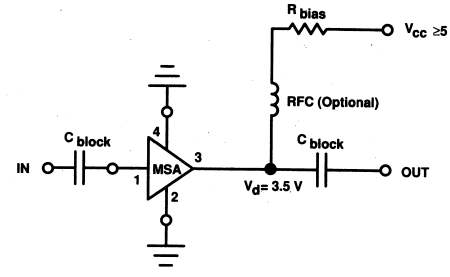
86 Plastic Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)



Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 16 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 0.5 GHz	dB	 16.5	20.0 18.5	
ΔG_P	Gain Flatness	f = 0.1 to 0.5 GHz	dB		±0.7	
$f_{3\,dB}$	3 dB Bandwidth		GHz		0.8	
VSWR	Input VSWR	f = 0.1 to 1.5 GHz			1.7:1	
	Output VSWR	f = 0.1 to 1.5 GHz			1.7:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 0.5 GHz	dBm		2.0	
NF	50Ω Noise Figure	f = 0.5 GHz	dB		3.0	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		14.5	
t_D	Group Delay	f = 0.5 GHz	psec.		225	
V_d	Device Voltage		V	2.8	3.5	4.2
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes: 1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices."
2. The recommended operating current range for this device is 12 mA to 20 mA. Typical gain performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2,3]	200 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

Thermal Resistance[2,4]: θ_{jc} = 120°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 8.3 mW/°C for T_C > 126°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Part Number Ordering Information

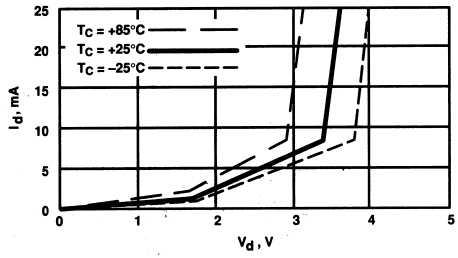
Part Number	Devices Per Reel	Reel Size
MSA-0686-TR1	1000	7"
MSA-0686-TR2	4000	13"

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

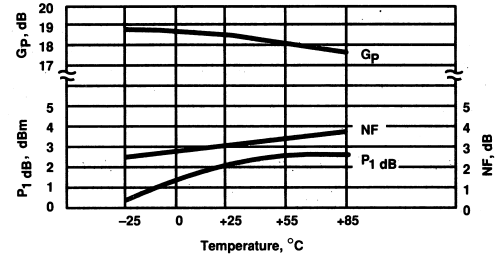
Typical Performance, T_A = 25°C

(unless otherwise noted)

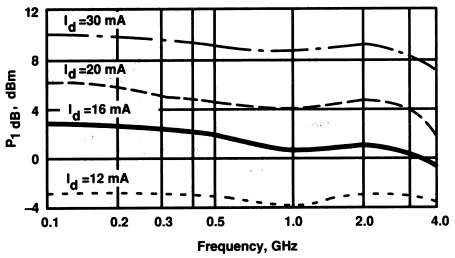
DEVICE CURRENT vs. VOLTAGE



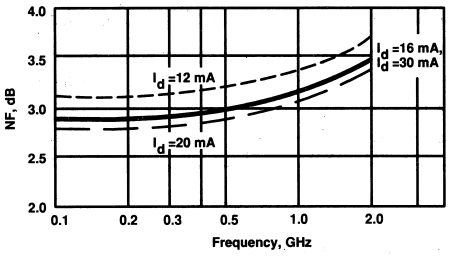
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. CASE TEMPERATURE
f = 1.0 GHz, I_d = 16 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 16 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang	k
0.1	.06	–175	20.1	10.08	170	–23.3	.069	4	.04	–84	1.05
0.2	.06	–169	19.8	9.77	161	–23.2	.069	8	.07	–103	1.05
0.3	.07	–164	19.4	9.35	152	–22.5	.075	13	.10	–113	1.03
0.4	.08	–158	19.1	8.98	144	–22.2	.078	16	.13	–123	1.02
0.5	.08	–154	18.7	8.58	135	–21.6	.083	18	.15	–131	1.01
0.6	.09	–152	18.0	7.94	128	–21.1	.088	21	.18	–140	1.01
0.8	.12	–152	17.2	7.25	114	–20.3	.097	25	.21	–155	1.00
1.0	.15	–154	16.3	6.51	102	–19.5	.106	25	.24	–168	0.99
1.5	.25	–171	14.0	5.01	76	–17.6	.133	22	.27	165	0.99
2.0	.34	171	11.9	3.94	56	–16.1	.157	19	.27	147	1.01
2.5	.43	155	9.8	3.09	42	–15.9	.161	16	.27	134	1.06
3.0	.49	140	8.0	2.51	28	–15.3	.171	11	.26	124	1.10
3.5	.56	128	6.4	2.09	15	–15.1	.175	6	.25	118	1.13
4.0	.61	118	5.0	1.78	3	–14.9	.180	3	.24	115	1.15
5.0	.70	99	2.4	1.32	–18	–14.7	.185	–2	.24	118	1.16

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0700
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

- **Cascadable 50 Ω Gain Block**
- **Low Operating Voltage (4.0 V typical V_d)**
- **3 dB Bandwidth: DC to 2.5 GHz**
- **13.0 dB typical Gain at 1.0 GHz**

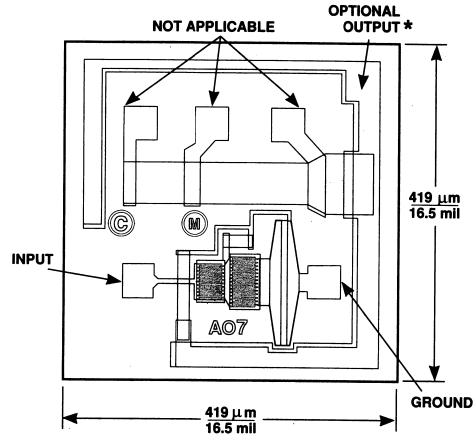
Description

The MSA-0700 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial, industrial and military applications.

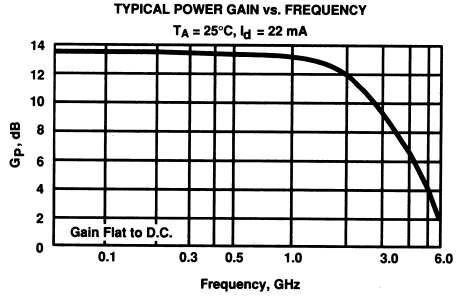
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire. See APPLICATIONS section, "Chip Use".

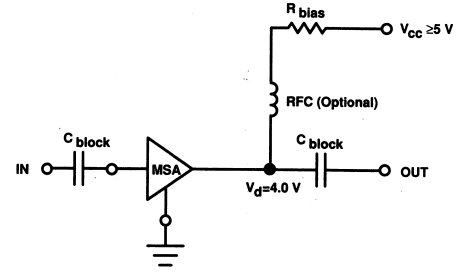
Chip Outline[1]



Unless otherwise specified, tolerances are ±13 µm / ±0.5 mils.
Chip thickness is 114 µm / 4.5 mil. Bond pads are 41 µm / 1.6 mil typical on each side.
*** Output contact is made by die attaching the backside of the die.**



Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions[3]: I_d = 22 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		13.5	
ΔG_P	Gain Flatness	f = 0.1 to 1.5 GHz	dB		±0.6	
$f_{3\ dB}$	3 dB Bandwidth		GHz		2.5	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			2.0:1	
	Output VSWR	f = 0.1 to 2.5 GHz			1.6:1	
$P_{1\ dB}$	Output Power @ 1 dB Gain Compression,	f = 1.0 GHz	dBm		5.5	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		4.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		19.0	
t_D	Group Delay	f = 1.0 GHz	psec.		130	
V_d	Device Voltage		V	3.6	4.0	4.4
dV/dT	Device Voltage Temperature Coefficient		mV/°C		−7.0	

Notes: 1. This chip contains additional biasing options. The performance specified applies only to the bias option whose bond pads are indicated on the chip outline. Refer to the APPLICATIONS section "MODAMP™ Silicon MMIC Chip Use" for additional information.
2. The recommended operating current range for this device is 15 mA to 40 mA. Typical performance as a function of current is on the following page.
3. RF performance of the chip is determined by packaging and testing 10 devices per wafer in a dual ground configuration.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	275 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 50°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{MOUNTING\ SURFACE}$ = 25°C
3. Derate at 20 mW/°C for $T_{MOUNTING\ SURFACE}$ > 186°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

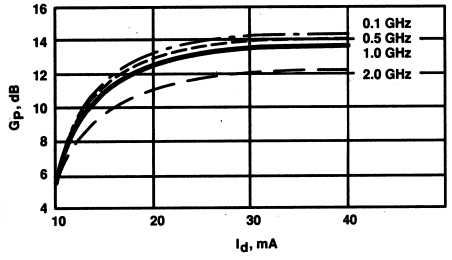
Part Number Ordering Information

Part Number	Devices Per Tray
MSA-0700-GP2	10
MSA-0700-GP4	up to 100
MSA-0700-GP6	up to 300

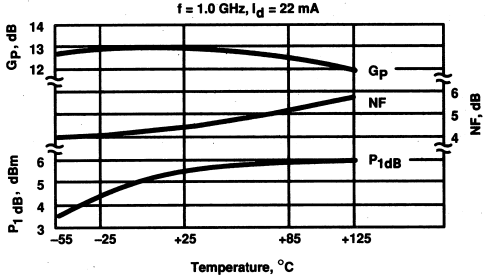
Typical Performance, T_A = 25°C

(unless otherwise noted)

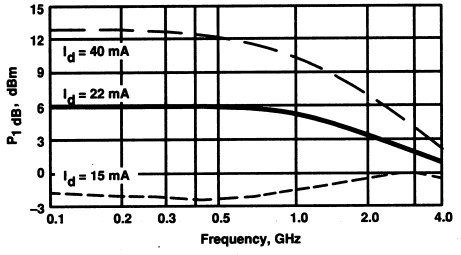
POWER GAIN vs. CURRENT



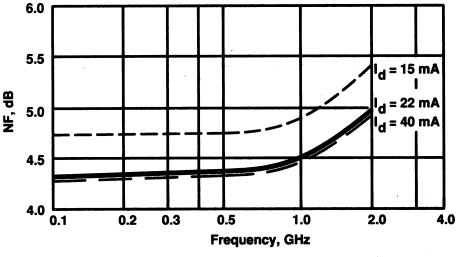
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. MOUNTING
SURFACE TEMPERATURE
f = 1.0 GHz, I_d = 22 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters[4]: Z_O = 50 Ω

T_A = 25°C, I_d = 22 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang	k
0.1	.04	–5	13.5	4.75	176	–18.6	.118	2	.20	–9	1.14
0.2	.05	–8	13.5	4.74	172	–18.4	.120	3	.19	–16	1.14
0.4	.06	–19	13.5	4.74	163	–18.3	.121	7	.20	–30	1.13
0.6	.08	–32	13.5	4.71	156	–18.1	.124	9	.21	–44	1.12
0.8	.10	–41	13.4	4.67	147	–17.5	.133	12	.23	–69	1.07
1.0	.12	–50	13.2	4.59	138	–17.6	.133	13	.23	–68	1.07
1.5	.20	–73	12.7	4.30	117	–16.6	.147	17	.23	–91	1.01
2.0	.31	–98	12.1	4.05	97	–15.8	.163	17	.22	–105	0.94
2.5	.38	–112	11.0	3.55	85	–15.3	.171	18	.18	–103	0.93
3.0	.43	–128	9.6	3.01	69	–15.3	.171	17	.19	–96	0.97
3.5	.48	–141	8.2	2.57	56	–15.3	.172	17	.21	–87	1.01
4.0	.48	–153	6.8	2.20	45	–15.2	.174	14	.26	–83	1.07
5.0	.49	–179	4.6	1.70	26	–15.2	.174	12	.31	–86	1.22
6.0	.54	154	2.5	1.34	9	–15.6	.166	13	.33	–98	1.38

Note: 4. S-parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section.

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MSA-0711
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

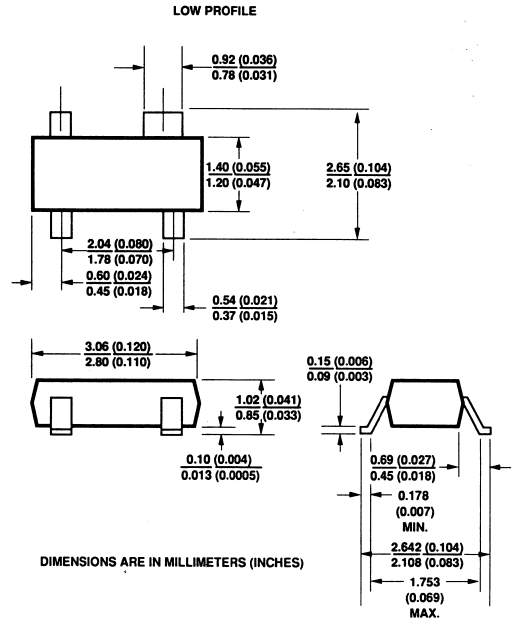
- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 1.9 GHz**
- **12.0 dB typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Low Cost Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Description

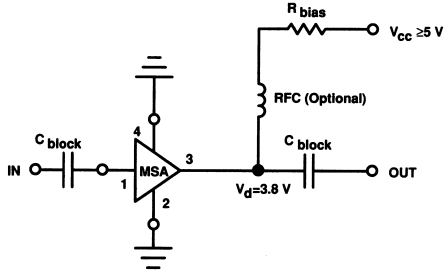
The MSA-0711 is a low cost silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in the surface mount plastic SOT-143 package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

SOT–143 Package



Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 22 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz	dB	 10.0	13.0 12.0	
ΔG_P	Gain Flatness	f = 0.1 to 1.3 GHz	dB		±0.8	
$f_{3\,dB}$	3 dB Bandwidth		GHz		1.9	
VSWR	Input VSWR	f = 0.1 to 2.0 GHz			1.5:1	
	Output VSWR	f = 0.1 to 2.0 GHz			1.5:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		5.5	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		5.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		18.0	
t_D	Group Delay	f = 1.0 GHz	psec.		145	
V_d	Device Voltage	T_C = 25°C	V	3.0	3.8	4.6
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–7.0	

Notes: 1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices."
2. The recommended operating current range for this device is 15 mA to 30 mA. Typical gain performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2,3]	175 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

Thermal Resistance[2,4]: θ_{jc} = 505°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 2.0 mW/°C for T_C > 62°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Part Number Ordering Information

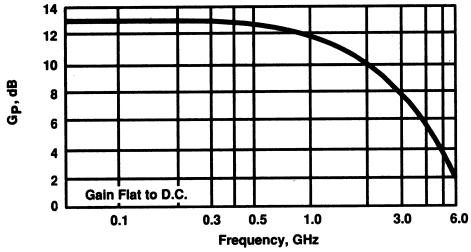
Part Number	Devices Per Reel	Reel Size
MSA-0711-TR1	3000	7"
MSA-0711-TR2	10000	13"

For more information, see "Tape and Reel Packaging for Surface Mount Devices, page

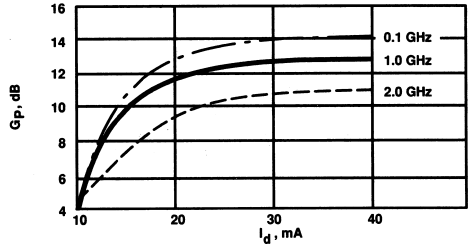
Typical Performance, T_A = 25°C

(unless otherwise noted)

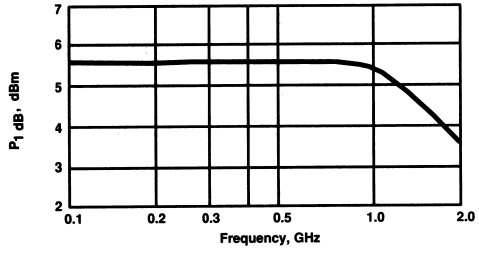
POWER GAIN vs. FREQUENCY
I_d = 22 mA



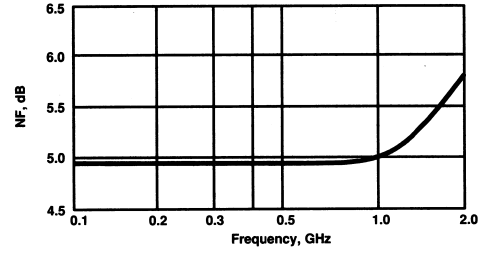
POWER GAIN vs. CURRENT



OUTPUT POWER @ 1 dB GAIN COMPRESSION vs. FREQUENCY
I_d = 22 mA



NOISE FIGURE vs. FREQUENCY
I_d = 22 mA



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 22 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	.03	1	13.0	4.47	174	–18.6	.118	1	.19	–8
0.2	.04	1	12.9	4.42	168	–18.5	.119	2	.19	–18
0.4	.04	–4	12.8	4.38	157	–18.4	.120	4	.19	–36
0.6	.05	–19	12.6	4.28	146	–18.1	.125	9	.19	–52
0.8	.07	–32	12.3	4.14	135	–17.7	.130	10	.20	–68
1.0	.08	–44	12.0	3.99	123	–17.4	.135	12	.19	–82
1.5	.13	–88	10.9	3.52	98	–16.1	.157	13	.19	–113
2.0	.18	–130	9.8	3.08	75	–15.2	.173	8	.18	–138
2.5	.25	–155	8.6	2.68	61	–14.7	.184	9	.18	–151
3.0	.32	–178	7.2	2.30	42	–14.7	.185	5	.17	–158
3.5	.38	165	5.8	1.96	26	–14.8	.181	3	.17	–150
4.0	.42	152	4.5	1.68	12	–14.7	.184	1	.20	–142

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0735, -0736
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

- **Cascadable 50 Ω Gain Block**
- **Low Operating Voltage (4.0 V typical V_d)**
- **3 dB Bandwidth: DC to 2.4 GHz**
- **13.0 dB typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Cost Effective Ceramic Microstrip Package**

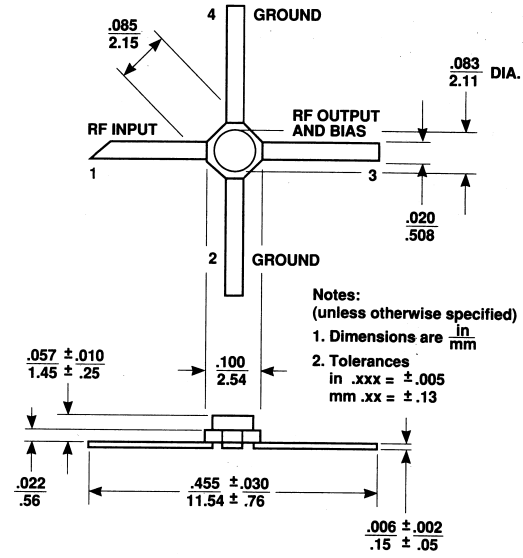
Description

The MSA-0735 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a cost effective, microstrip package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

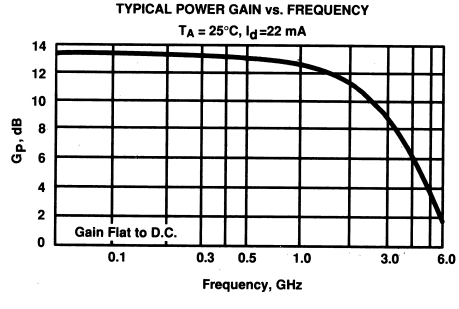
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

Available in cut lead version (package 36) as MSA-0736.

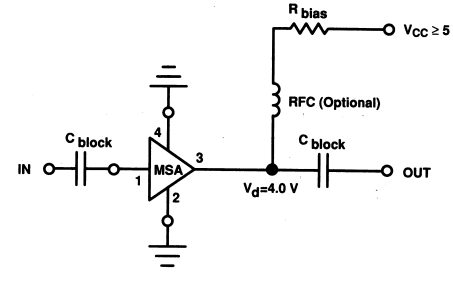
35 micro-X Package[1]



TYPICAL POWER GAIN vs. FREQUENCY



Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 22 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	12.5	13.5	14.5
ΔG_P	Gain Flatness	f = 0.1 to 1.3 GHz	dB		±0.6	±1.0
$f_{3\ dB}$	3 dB Bandwidth		GHz		2.4	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			2.0:1	
	Output VSWR	f = 0.1 to 2.5 GHz			1.8:1	
$P_{1\ dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		5.5	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		4.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		19.0	
t_D	Group Delay	f = 1.0 GHz	psec.		140	
V_d	Device Voltage		V	3.6	4.0	4.4
dV/dT	Device Voltage Temperature Coefficient		mV/°C		−7.0	

Notes: 1. Short leaded 36 package available upon request.
2. The recommended operating current range for this device is 15 mA to 40 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	275 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature[4]	–65°C to 200°C

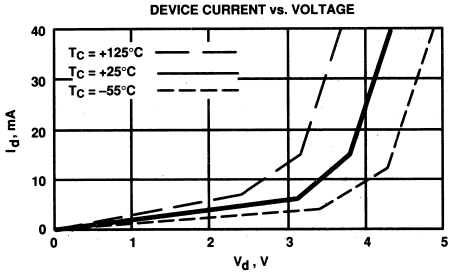
Thermal Resistance[2,5]: θ_{jc} = 155°C/W

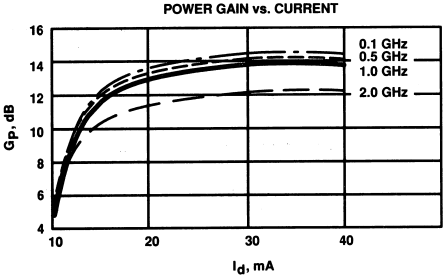
Notes:

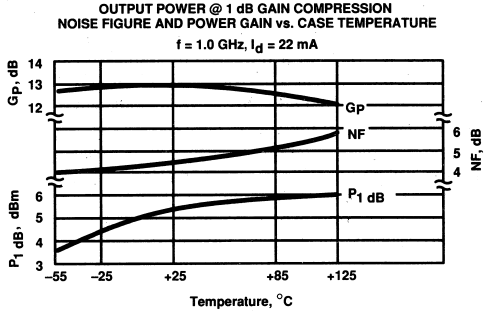
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 6.5 mW/°C for T_C > 157°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

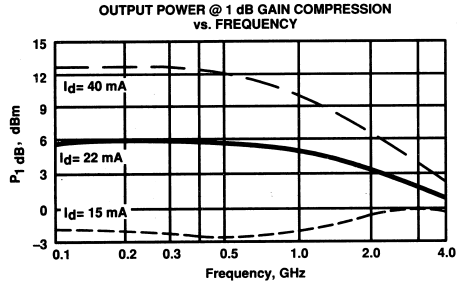
Typical Performance, T_A = 25°C

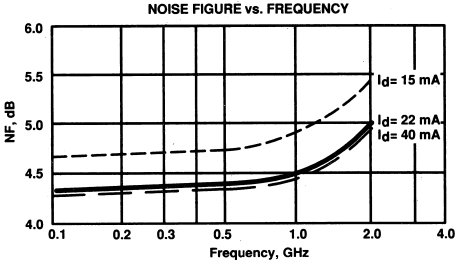
(unless otherwise noted)











Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 22 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.1	.13	–3	13.5	4.71	175	–19.0	.112	2	.29	–7
0.2	.13	–6	13.4	4.69	170	–18.5	.119	3	.29	–12
0.4	.14	–13	13.4	4.68	160	–18.6	.118	6	.29	–24
0.6	.16	–20	13.3	4.64	150	–18.4	.120	7	.28	–35
0.8	.19	–29	13.2	4.60	140	–18.1	.125	8	.28	–47
1.0	.21	–40	12.9	4.42	129	–17.6	.131	10	.27	–58
1.5	.27	–71	12.2	4.07	104	–16.5	.149	10	.24	–83
2.0	.32	–107	11.5	3.74	79	–15.6	.165	7	.19	–103
2.5	.37	–134	10.3	3.26	62	–15.3	.173	5	.15	–113
3.0	.43	–160	8.8	2.76	44	–15.4	.171	0	.14	–120
3.5	.47	–179	7.5	2.37	27	–15.3	.173	–4	.16	–120
4.0	.49	167	6.2	2.05	12	–15.2	.168	–6	.21	–121
5.0	.51	134	4.0	1.59	–15	–15.2	.173	–11	.28	–135
6.0	.60	96	2.1	1.27	–42	–14.6	.185	–16	.29	–167

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0770
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

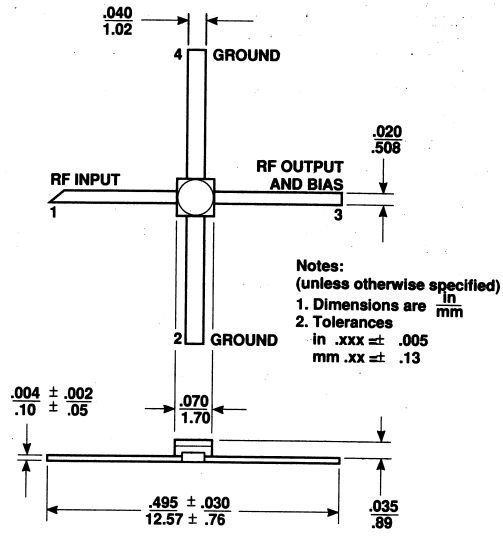
- **Cascadable 50 Ω Gain Block**
- **Low Operating Voltage (4.0 V typical V_d)**
- **3 dB Bandwidth: DC to 2.5 GHz**
- **13.0 dB typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Hermetic, Gold-ceramic Microstrip Package**

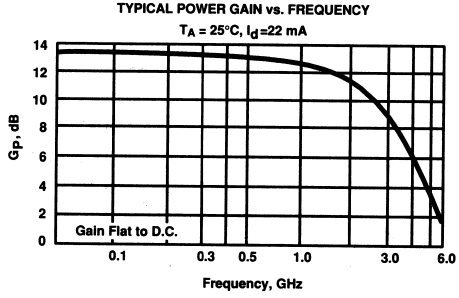
Description

The MSA-0770 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic, high reliability package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in industrial and military applications.

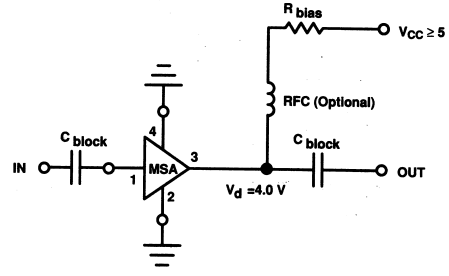
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

70 mil Package





Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 22 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	12.5	13.5	14.5
ΔG_P	Gain Flatness	f = 0.1 to 1.5 GHz	dB		±0.6	±1.0
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.5	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			2.0:1	
	Output VSWR	f = 0.1 to 2.5 GHz			1.6:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		5.5	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		4.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		19.0	
t_D	Group Delay	f = 1.0 GHz	psec.		130	
V_d	Device Voltage		V	3.6	4.0	4.4
dV/dT	Device Voltage Temperature Coefficient		mV/°C		-7.0	

Note: 1. The recommended operating current range for this device is 15 mA to 40 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	275 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 130°C/W

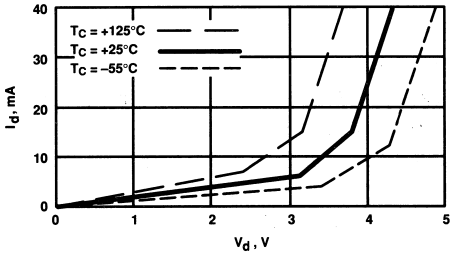
Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 7.7 mW/°C for T_C > 164°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

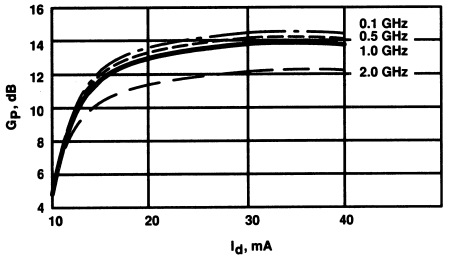
Typical Performance, T_A = 25°C

(unless otherwise noted)

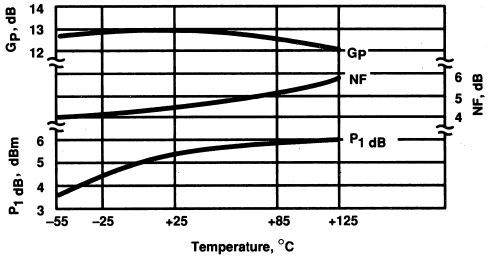
DEVICE CURRENT vs. VOLTAGE



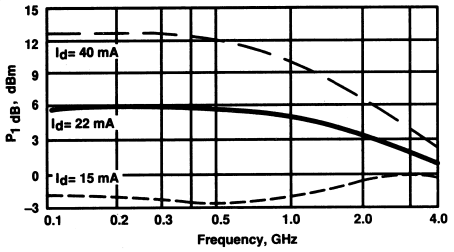
POWER GAIN vs. CURRENT



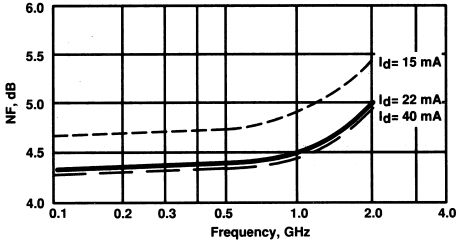
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. CASE TEMPERATURE
f = 1.0 GHz, I_d = 22 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 22 mA

Freq. GHz	S11 Mag	S11 Ang	S21 dB	S21 Mag	S21 Ang	S12 dB	S12 Mag	S12 Ang	S22 Mag	S22 Ang
0.1	.04	–7	13.5	4.74	175	–18.6	.118	2	.20	–10
0.2	.05	–11	13.5	4.72	170	–18.4	.120	2	.19	–18
0.4	.06	–24	13.4	4.70	160	–18.4	.121	6	.20	–34
0.6	.08	–38	13.4	4.65	151	–18.1	.124	7	.21	–50
0.8	.10	–48	13.2	4.58	141	–17.8	.133	9	.23	–76
1.0	.12	–58	13.0	4.47	131	–17.5	.133	9	.23	–76
1.5	.20	–82	12.3	4.12	107	–16.6	.148	10	.23	–101
2.0	.30	–107	11.6	3.82	85	–15.7	.163	8	.22	–116
2.5	.37	–123	10.4	3.33	70	–15.3	.171	7	.19	–116
3.0	.42	–140	9.0	2.83	52	–15.4	.170	3	.20	–111
3.5	.46	–154	7.7	2.42	37	–15.4	.170	1	.23	–107
4.0	.47	–167	6.4	2.08	23	–15.5	.169	–4	.29	–107
5.0	.47	163	4.2	1.63	–1	–15.5	.167	–9	.35	–116
6.0	.51	131	2.3	1.30	–23	–15.9	.160	–11	.38	–133

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0785
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

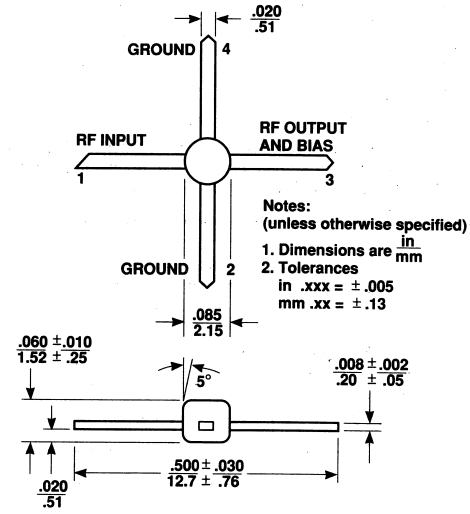
- **Cascadable 50 Ω Gain Block**
- **Low Operating Voltage (4.0 V typical V_d)**
- **3 dB Bandwidth: DC to 2.0 GHz**
- **12.5 dB typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Low Cost Plastic Package**

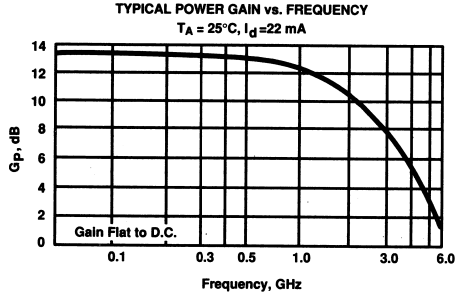
Description

The MSA-0785 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

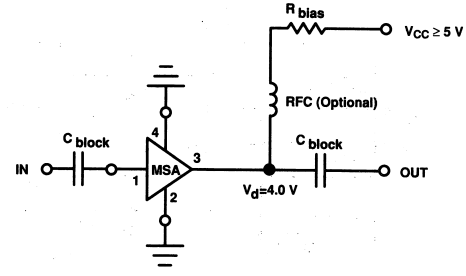
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

85 Plastic Package





Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 22 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz	dB	 10.5	13.5 12.5	
ΔG_P	Gain Flatness	f = 0.1 to 1.3 GHz	dB		±0.7	
$f_{3\,dB}$	3 dB Bandwidth		GHz		2.0	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			1.4:1	
	Output VSWR	f = 0.1 to 2.5 GHz			1.5:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		5.5	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		5.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		19.0	
t_D	Group Delay	f = 1.0 GHz	psec.		140	
V_d	Device Voltage		V	3.2	4.0	4.8
dV/dT	Device Voltage Temperature Coefficient		mV/°C		−7.0	

Note: 1. The recommended operating current range for this device is 15 mA to 40 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

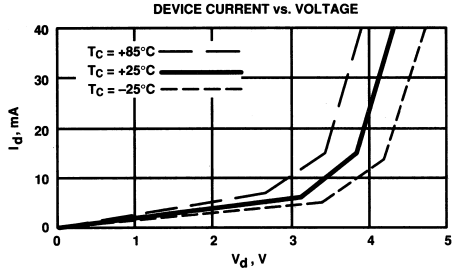
Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	275 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

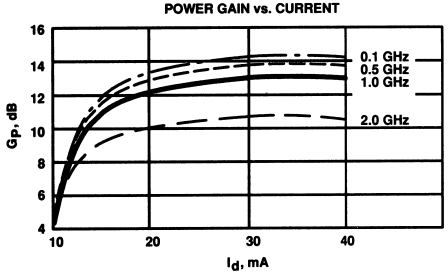
Thermal Resistance[2,4]: θ_{jc} = 110°C/W

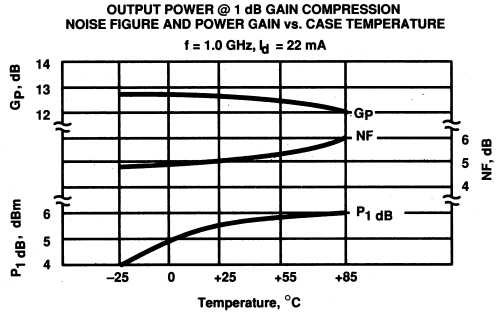
Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 9.1 mW/°C for T_C > 120°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

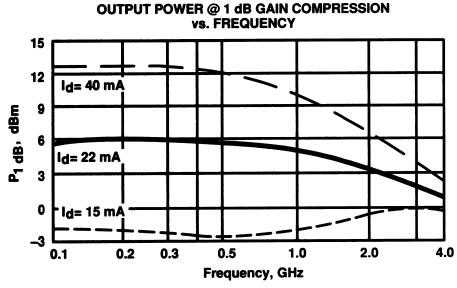
Typical Performance, T_A = 25°C

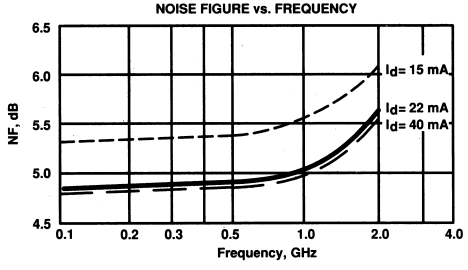
(unless otherwise noted)











Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 22 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.1	.05	166	13.5	4.73	174	–18.4	.120	1	.14	–11
0.2	.05	151	13.4	4.70	169	–18.3	.122	3	.14	–21
0.4	.04	115	13.3	4.63	158	–18.3	.121	6	.14	–40
0.6	.04	65	13.1	4.53	148	–18.0	.125	7	.16	–58
0.8	.05	26	12.9	4.41	138	–17.8	.129	9	.17	–71
1.0	.06	–5	12.6	4.25	127	–17.6	.132	10	.18	–84
1.5	.08	–51	11.6	3.82	104	–16.5	.149	12	.18	–109
2.0	.11	–99	10.5	3.33	82	–15.9	.161	11	.17	–126
2.5	.14	–127	9.3	2.91	68	–15.2	.174	13	.16	–134
3.0	.20	–154	7.9	2.48	52	–14.8	.183	7	.16	–139
3.5	.25	–173	6.7	2.16	37	–14.7	.184	5	.16	–132
4.0	.29	171	5.5	1.88	23	–14.8	.182	1	.18	–130
5.0	.35	139	3.5	1.50	–1	–14.3	.193	–6	.21	–133
6.0	.46	100	1.7	1.22	–26	–14.5	.189	–14	.20	–169

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0786
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

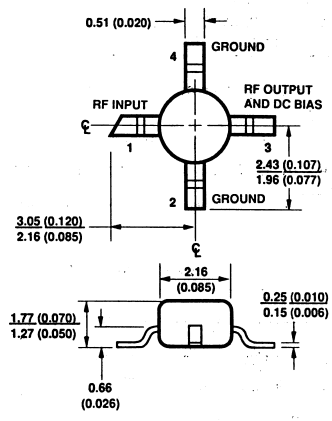
- **Cascadable 50 Ω Gain Block**
- **Low Operating Voltage (4.0 V typical V_d)**
- **3 dB Bandwidth: DC to 2.0 GHz**
- **12.5 dB typical Gain at 1.0 GHz**
- **Unconditionally Stable (k>1)**
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Description

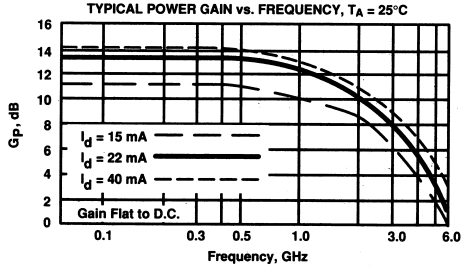
The MSA-0786 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost, surface mount plastic package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

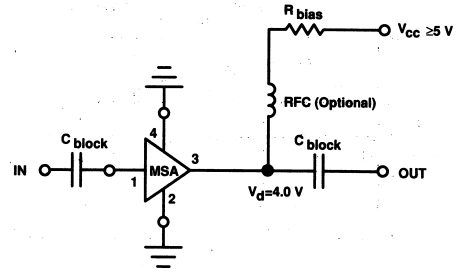
86 Plastic Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)



Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 22 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz	dB	 10.5	13.5 12.5	
ΔG_P	Gain Flatness	f = 0.1 to 1.3 GHz	dB		±0.7	
$f_{3\ dB}$	3 dB Bandwidth		GHz		2.0	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			1.7:1	
	Output VSWR	f = 0.1 to 2.5 GHz			1.7:1	
$P_{1\ dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		5.5	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		5.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		19.0	
t_D	Group Delay	f = 1.0 GHz	psec.		150	
V_d	Device Voltage		V	3.2	4.0	4.8
dV/dT	Device Voltage Temperature Coefficient		mV/°C		-7.0	

Notes: 1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices."
2. The recommended operating current range for this device is 15 mA to 40 mA. Typical gain performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	60 mA
Power Dissipation[2,3]	275 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

Thermal Resistance[2,4]: θ_{jc} = 120°C/W

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 8.3 mW/°C for T_C > 117°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Part Number Ordering Information

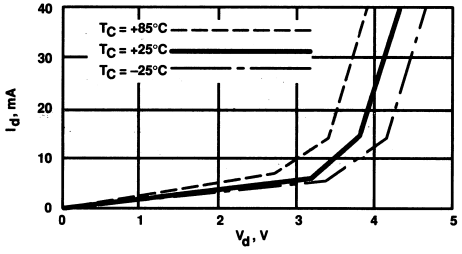
Part Number	Devices Per Reel	Reel Size
MSA-0786-TR1	1000	7"
MSA-0786-TR2	4000	13"

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

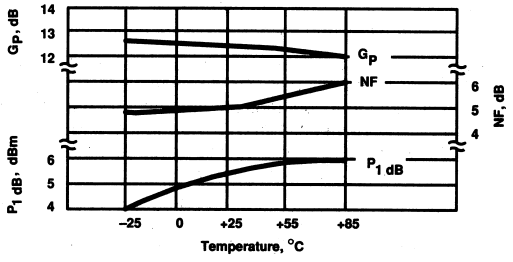
Typical Performance, T_A = 25°C

(unless otherwise noted)

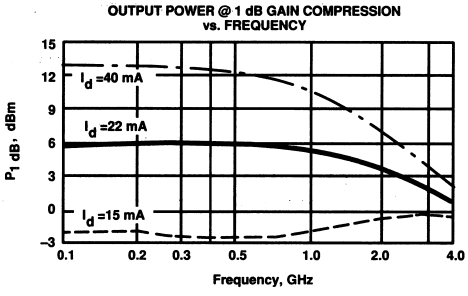
DEVICE CURRENT vs. VOLTAGE



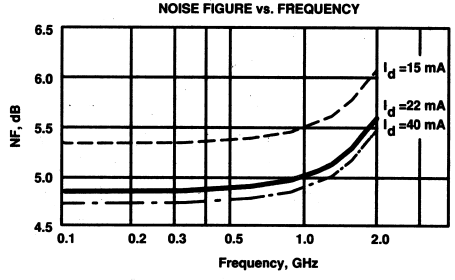
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. CASE TEMPERATURE
f = 1.0 GHz, I_d = 22 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 22 mA

Freq. GHz	S11 Mag	S11 Ang	S21 dB	S21 Mag	S21 Ang	S12 dB	S12 Mag	S12 Ang	S22 Mag	S22 Ang
0.1	.05	175	13.5	4.74	174	–18.7	.116	1	.14	–12
0.2	.05	174	13.4	4.71	169	–18.7	.117	3	.14	–22
0.4	.04	167	13.3	4.64	158	–18.4	.120	4	.15	–44
0.6	.04	175	13.1	4.52	148	–18.3	.122	7	.16	–65
0.8	.05	–156	12.9	4.39	138	–18.0	.126	8	.17	–84
1.0	.06	–134	12.6	4.25	127	–17.5	.134	10	.18	–102
1.5	.08	–142	11.6	3.79	103	–16.6	.148	9	.21	–139
2.0	.15	–159	10.5	3.34	80	–15.7	.164	7	.23	–164
2.5	.25	–176	9.2	2.89	63	–15.1	.176	5	.24	174
3.0	.33	166	7.8	2.45	44	–14.7	.185	1	.24	159
3.5	.41	150	6.5	2.11	27	–14.9	.179	–5	.24	149
4.0	.49	137	5.2	1.82	12	–15.1	.177	–9	.23	145
5.0	.60	116	3.0	1.41	–14	–15.4	.169	–14	.26	145

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0800
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

- **Usable Gain to 6.0 GHz**
- **High Gain:**
  32.5 dB typical at 0.1 GHz
  23.5 dB typical at 1.0 GHz
- **Low Noise Figure:**
  3.0 dB typical at 1.0 GHz

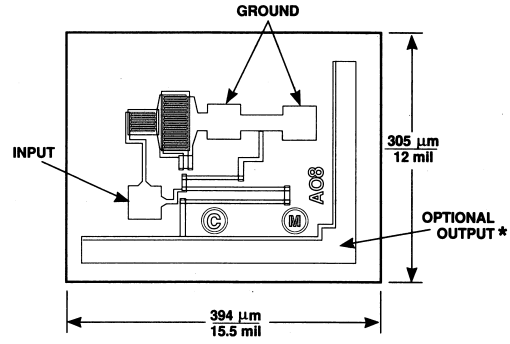
Description

The MSA-0800 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block above 0.5 GHz and can be used as a high gain transistor below this frequency. Typical applications include narrow and broad band IF and RF amplifiers in commercial, industrial and military applications.

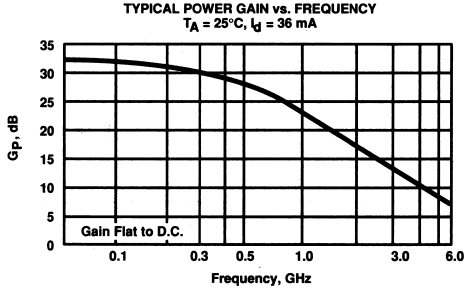
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire. See APPLICATIONS section, "Chip Use".

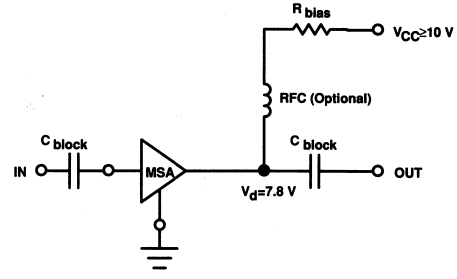
Chip Outline[1]



Unless otherwise specified, tolerances are ±13 µm / ±0.5 mils.
Chip thickness is 114 µm / 4.5 mil. Bond pads are 41 µm / 1.6 mil typical on each side.
*** Output contact is made by die attaching the backside of the die.**



Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions[3]: I_d = 36 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz f = 4.0 GHz	dB		32.5 23.5 11.0	
VSWR	Input VSWR	f = 1.0 to 3.0 GHz			2.0:1	
	Output VSWR	f = 1.0 to 3.0 GHz			1.9:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression,	f = 1.0 GHz	dBm		12.5	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		3.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		27.0	
t_D	Group Delay	f = 1.0 GHz	psec.		125	
V_d	Device Voltage		V	7.0	7.8	8.4
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–17.0	

Notes: 1. Refer to the APPLICATIONS section "MODAMP™ Silicon MMIC Chip Use" for additional information.
2. The recommended operating current range for this device is 20 mA to 40 mA. Typical performance as a function of current is on the following page.
3. RF performance of the chip is determined by packaging and testing 10 devices per wafer in a dual ground configuration.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	750 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	200°C

Thermal Resistance[2,4]: θ_{jc} = 70°C/W

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{MOUNTING\ SURFACE}$ = 25°C
3. Derate at 14.3 mW/°C for $T_{MOUNTING\ SURFACE}$ > 148°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

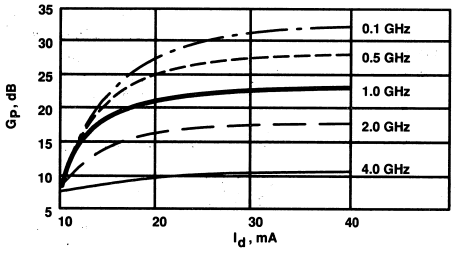
Part Number Ordering Information

Part Number	Devices Per Tray
MSA-0800-GP2	10
MSA-0800-GP4	100
MSA-0800-GP6	up to 300

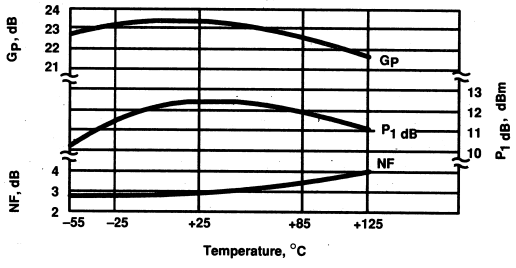
Typical Performance, T_A = 25°C

(unless otherwise noted)

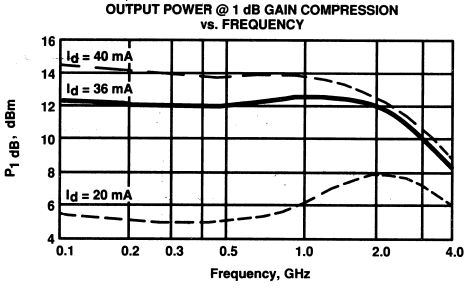
POWER GAIN vs. CURRENT



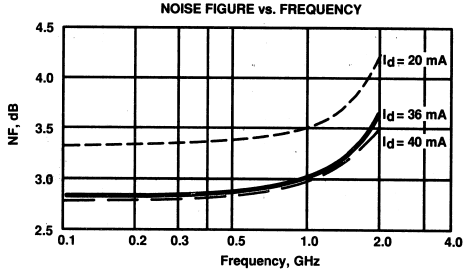
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. MOUNTING
SURFACE TEMPERATURE
f = 1.0 GHz, I_d = 36 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters[4]: Z_O = 50 Ω

T_A = 25°C, I_d = 36 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.1	.65	–17	32.6	42.50	163	–36.9	.014	39	.64	–20	0.80
0.2	.61	–31	31.7	38.59	148	–34.1	.020	47	.59	–39	0.68
0.4	.50	–54	29.6	30.22	126	–31.0	.028	52	.49	–68	0.63
0.6	.43	–70	27.5	23.64	113	–28.5	.038	52	.40	–90	0.69
0.8	.38	–81	25.6	19.05	103	–26.7	.046	53	.35	–106	0.75
1.0	.34	–95	24.2	16.27	93	–25.4	.054	55	.30	–120	0.80
1.5	.31	–110	20.9	11.12	78	–23.6	.066	53	.23	–142	0.88
2.0	.32	–124	18.3	8.22	66	–22.6	.075	53	.17	–158	0.98
2.5	.33	–129	16.3	6.52	61	–20.7	.092	57	.13	–162	1.00
3.0	.34	–138	14.4	5.24	54	–20.3	.097	54	.07	–165	1.11
3.5	.36	–146	12.8	4.36	45	–19.0	.112	50	.07	–140	1.11
4.0	.36	–155	11.3	3.68	37	–18.3	.122	49	.10	–96	1.16
5.0	.35	177	8.7	2.73	23	–17.2	.138	43	.15	–75	1.28
6.0	.43	150	6.3	2.07	10	–16.6	.148	35	.15	–81	1.40

Note: 4. S-parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0835, -0836
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

- **Usable Gain to 6.0 GHz**
- **High Gain: 32.5 dB typical at 0.1 GHz**
  23.0 dB typical at 1.0 GHz
- **Low Noise Figure: 3.0 dB typical at 1.0 GHz**
- **Cost Effective Ceramic Microstrip Package**

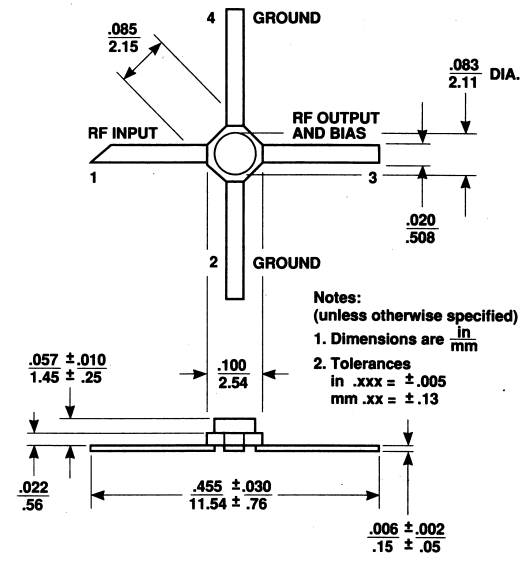
Description

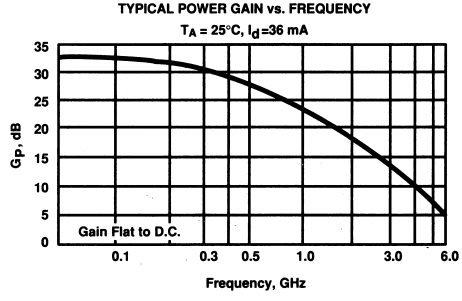
The MSA-0835 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a cost effective, microstrip package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block above 0.5 GHz and can be used as a high gain transistor below this frequency. Typical applications include narrow and moderate band IF and RF amplifiers in commercial and industrial applications.

The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

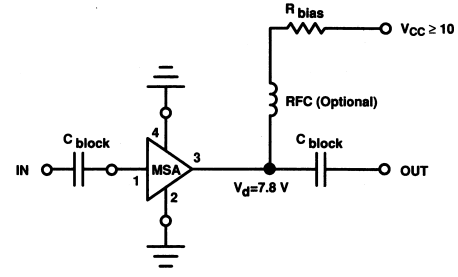
Available in cut lead version (package 36) as MSA-0836.

35 micro-X Package[1]





Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 36 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz f = 4.0 GHz	dB	22.0	32.5 23.0 10.5	25.0
VSWR	Input VSWR	f = 1.0 to 3.0 GHz			2.0:1	
	Output VSWR	f = 1.0 to 3.0 GHz			1.5:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		12.5	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		3.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		27.0	
t_D	Group Delay	f = 1.0 GHz	psec.		125	
V_d	Device Voltage		V	7.0	7.8	8.4
dV/dT	Device Voltage Temperature Coefficient		mV/°C		−17.0	

Notes: 1. Short leaded 36 package available upon request.
2. The recommended operating current range for this device is 20 mA to 40 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	750 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature[4]	–65°C to 200°C

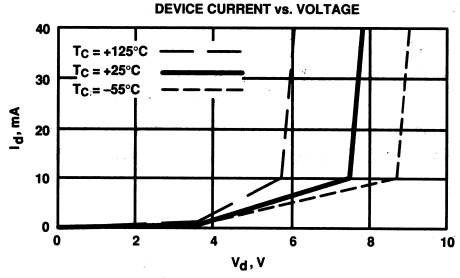
Thermal Resistance[2,5]: θ_{jc} = 175°C/W

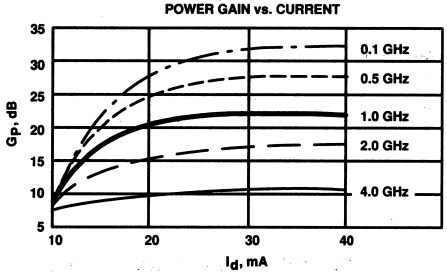
Notes:

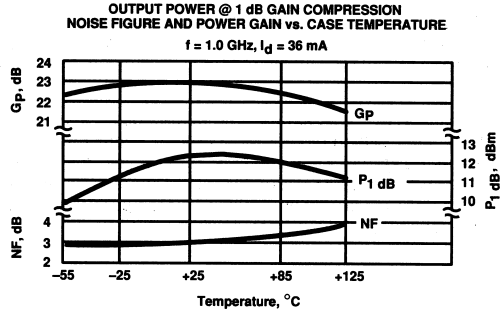
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 5.7 mW/°C for T_C > 69°C.
4. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit.
5. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

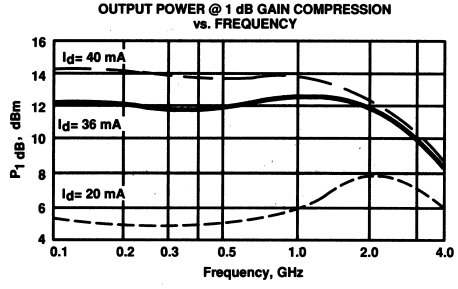
Typical Performance, T_A = 25°C

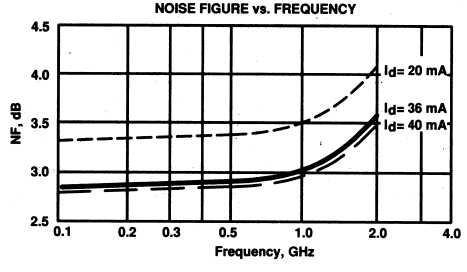
(unless otherwise noted)











Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 36 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang	k
0.1	.63	–17	32.5	42.02	161	–37.7	.013	55	.63	–19	0.72
0.2	.58	–33	31.5	37.52	145	–33.7	.021	47	.56	–37	0.73
0.4	.49	–56	29.1	28.50	119	–29.7	.033	54	.42	–66	0.72
0.6	.40	–70	26.7	21.54	103	–27.9	.040	55	.32	–84	0.78
0.8	.35	–80	24.6	17.01	92	–26.0	.050	53	.24	–98	0.85
1.0	.33	–89	22.9	13.98	82	–24.9	.057	52	.18	–107	0.89
1.5	.30	–111	19.5	9.45	64	–22.1	.079	51	.09	–126	0.95
2.0	.30	–133	16.9	7.03	48	–20.2	.098	44	.07	–141	0.99
2.5	.32	–150	14.9	5.53	39	–19.2	.110	42	.06	–166	1.04
3.0	.34	–170	13.2	4.56	26	–18.3	.122	36	.06	–106	1.06
3.5	.38	175	11.7	3.86	14	–17.5	.133	32	.08	–100	1.08
4.0	.39	162	10.5	3.33	2	–16.7	.146	27	.12	–101	1.08
5.0	.41	132	7.9	2.47	–21	–15.6	.165	19	.21	–113	1.10
6.0	.52	95	5.8	1.94	–45	–14.6	.187	7	.20	–149	1.05

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0870
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

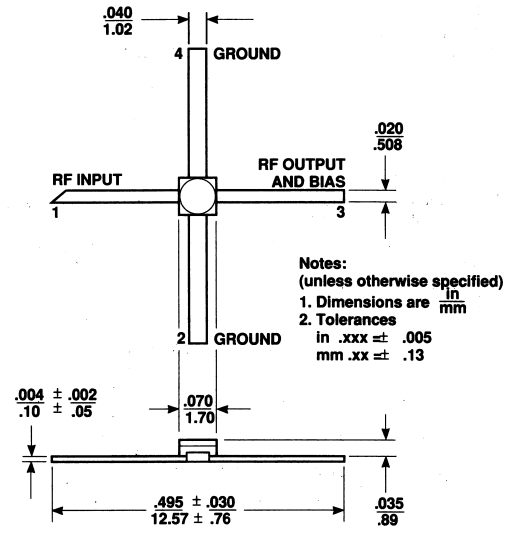
- **Usable Gain to 6.0 GHz**
- **High Gain: 32.5 dB typical at 0.1 GHz**
  23.5 dB typical at 1.0 GHz
- **Low Noise Figure: 3.0 dB typical at 1.0 GHz**
- **Hermetic Gold-ceramic Microstrip Package**

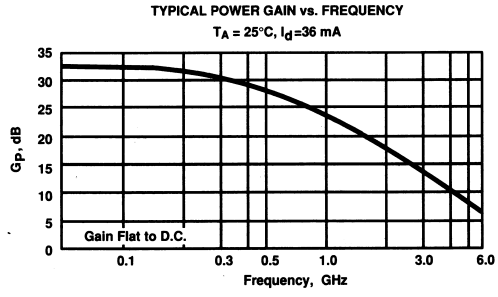
Description

The MSA-0870 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic, high reliability package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block above 0.5 GHz and can be used as a high gain transistor below this frequency. Typical applications include narrow and moderate band IF and RF amplifiers in industrial and military applications.

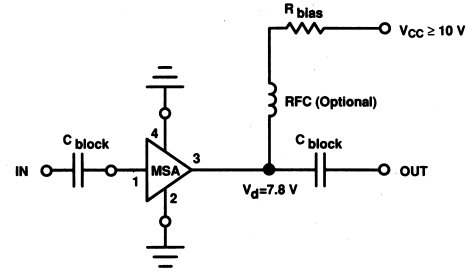
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

70 mil Package





Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 36 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		32.5	
		f = 1.0 GHz		22.0	23.5	25.0
		f = 4.0 GHz		10.0	11.0	12.0
VSWR	Input VSWR	f = 1.0 to 3.0 GHz			2.0:1	
	Output VSWR	f = 1.0 to 3.0 GHz			1.9:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		12.5	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		3.0	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		27.0	
t_D	Group Delay	f = 1.0 GHz	psec.		125	
V_d	Device Voltage		V	7.0	7.8	8.4
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–17.0	

Note: 1. The recommended operating current range for this device is 20 mA to 40 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	750 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 150°C/W

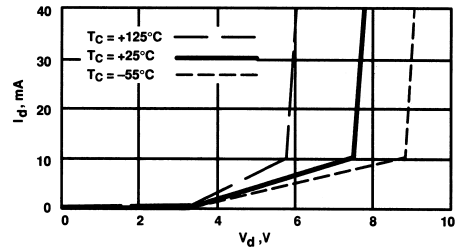
Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 6.7 mW/°C for T_C > 88°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

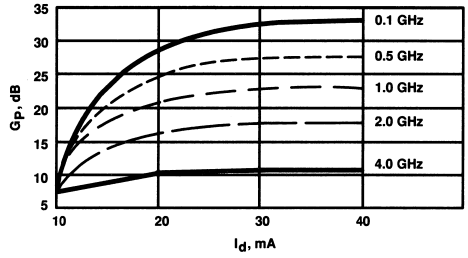
Typical Performance, T_A = 25°C

(unless otherwise noted)

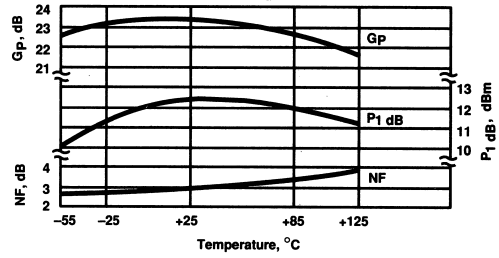
DEVICE CURRENT vs. VOLTAGE



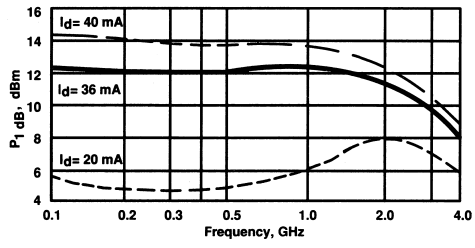
POWER GAIN vs. CURRENT



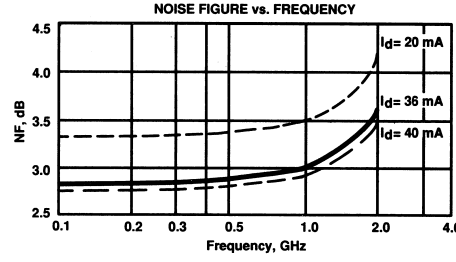
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. CASE TEMPERATURE
f = 1.0 GHz, I_d = 36 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 36 mA

Freq. MHz	S_{11}		S_{21}			S_{12}			S_{22}		
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.1	.65	–19	32.5	42.04	161	–36.3	.015	40	.64	–22	0.78
0.2	.60	–35	31.5	37.54	145	–33.7	.021	47	.58	–43	0.66
0.4	.48	–60	29.1	28.49	122	–30.5	.030	51	.47	–74	0.64
0.6	.40	–76	26.8	21.90	108	–28.0	.040	50	.38	–97	0.72
0.8	.35	–88	24.9	17.48	97	–26.2	.049	50	.33	–113	0.78
1.0	.32	–102	23.4	14.85	87	–24.9	.057	51	.28	–128	0.83
1.5	.29	–118	20.1	10.14	70	–23.0	.071	47	.22	–151	0.91
2.0	.30	–133	17.6	7.55	56	–21.9	.081	45	.16	–167	0.98
2.5	.31	–139	15.6	6.01	49	–20.0	.100	46	.12	–172	1.02
3.0	.32	–149	13.8	4.87	39	–19.5	.106	41	.07	–170	1.11
3.5	.34	–158	12.2	4.09	28	–18.4	.121	35	.07	–143	1.12
4.0	.34	–168	10.8	3.48	17	–17.7	.131	31	.12	–112	1.16
5.0	.33	161	8.4	2.63	–3	–16.6	.147	21	.19	–103	1.26
6.0	.39	128	6.2	2.04	–22	–16.2	.155	10	.21	–115	1.36

A model for this device is available in the DEVICE MODELS section.

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MSA-0885
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

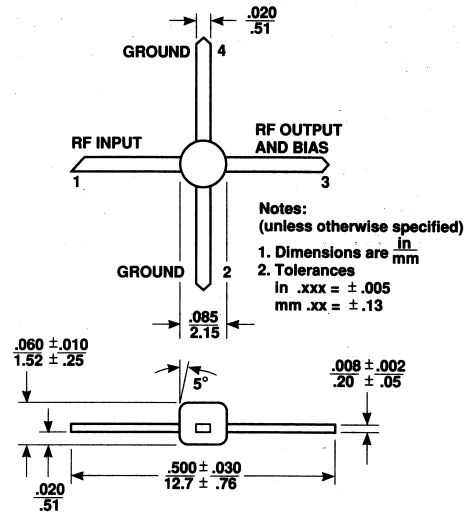
- **Usable Gain to 6.0 GHz**
- **High Gain: 32.5 dB typical at 0.1 GHz**
  22.5 dB typical at 1.0 GHz
- **Low Noise Figure: 3.3 dB typical at 1.0 GHz**
- **Low Cost Plastic Package**

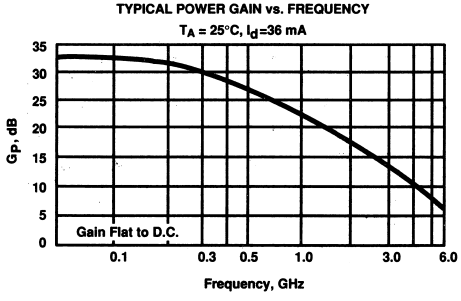
Description

The MSA-0885 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block above 0.5 GHz and can be used as a high gain transistor below this frequency. Typical applications include narrow and moderate band IF and RF amplifiers in commercial and industrial applications.

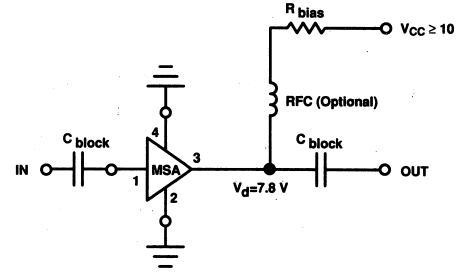
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

85 Plastic Package





Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 36 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz	dB	 21.0	32.5 22.5	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.9:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.6:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		12.5	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		3.3	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		27.0	
t_D	Group Delay	f = 1.0 GHz	psec.		125	
V_d	Device Voltage		V	6.2	7.8	9.4
dV/dT	Device Voltage Temperature Coefficient		mV/°C		−17.0	

Note: 1. The recommended operating current range for this device is 20 mA to 40 mA. Typical performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	65 mA
Power Dissipation[2,3]	500 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

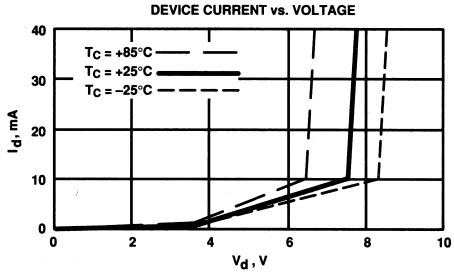
Thermal Resistance[2,4]: θ_{jc} = 130°C/W

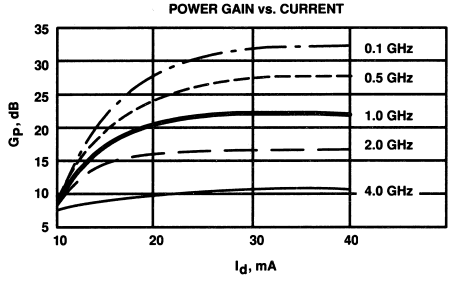
Notes:

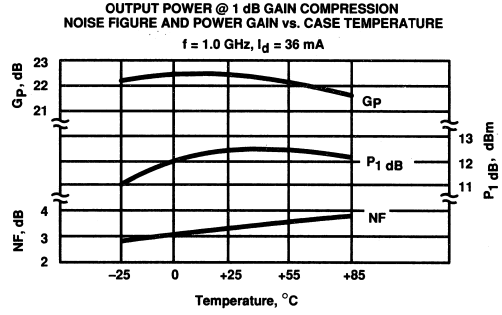
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 7.7 mW/°C for T_C > 85°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

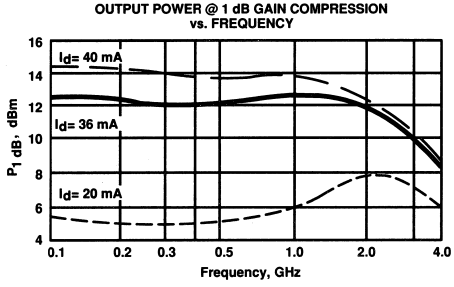
Typical Performance, T_A = 25°C

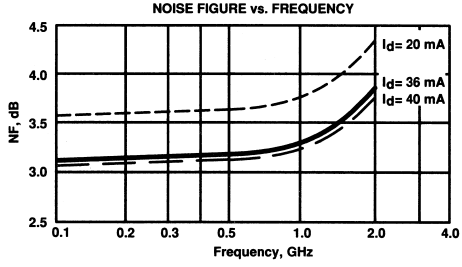
(unless otherwise noted)











Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 36 mA

Freq. GHz	S11 Mag	S11 Ang	S21 dB	S21 Mag	S21 Ang	S12 dB	S12 Mag	S12 Ang	S22 Mag	S22 Ang	k
0.1	.64	–21	32.5	42.29	160	–36.5	.015	40	.61	–24	0.78
0.2	.58	–39	31.3	36.89	144	–32.8	.023	50	.54	–45	0.67
0.4	.44	–65	28.7	27.20	120	–29.4	.034	54	.42	–77	0.69
0.6	.36	–82	26.3	20.57	106	–27.2	.044	53	.33	–98	0.77
0.8	.31	–95	24.3	16.31	96	–25.2	.055	53	.28	–115	0.83
1.0	.27	–105	22.5	13.36	87	–24.2	.061	51	.25	–129	0.87
1.5	.24	–125	19.3	9.24	71	–21.4	.085	50	.18	–153	0.96
2.0	.26	–147	16.7	6.82	56	–19.7	.103	47	.15	–173	0.98
2.5	.29	–159	14.9	5.57	48	–18.4	.120	44	.12	180	1.00
3.0	.34	–175	13.1	4.51	37	–17.7	.130	42	.09	165	1.03
3.5	.38	172	11.6	3.80	25	–16.9	.144	37	.06	172	1.04
4.0	.42	161	10.1	3.21	14	–16.3	.153	33	.04	–139	1.06
5.0	.48	135	7.7	2.43	–7	–15.6	.167	24	.09	–90	1.09
6.0	.60	102	5.5	1.88	–29	–14.9	.179	17	.08	–140	1.06

A model for this device is available in the DEVICE MODELS section.

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MSA-0886
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

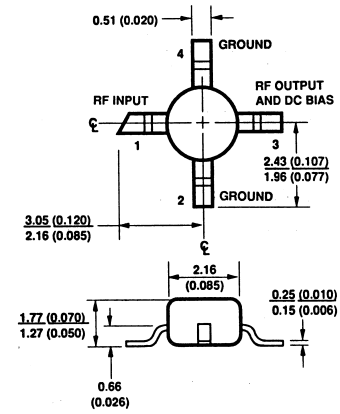
- **Usable Gain to 5.5 GHz**
- **High Gain: 32.5 dB typical at 0.1 GHz**
  22.5 dB typical at 1.0 GHz
- **Low Noise Figure: 3.3 dB typical at 1.0 GHz**
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Description

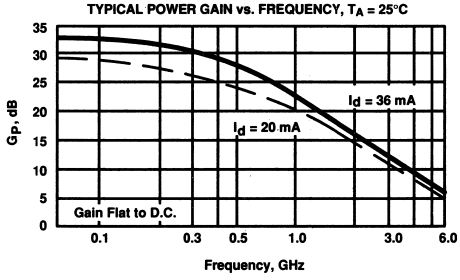
The MSA-0886 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost, surface mount plastic package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block above 0.5 GHz and can be used as a high gain transistor below this frequency. Typical applications include narrow and moderate band IF and RF amplifiers in commercial and industrial applications.

The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

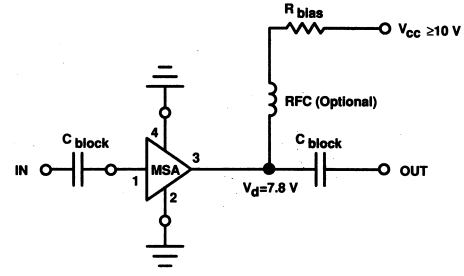
86 Plastic Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)



Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 36 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 1.0 GHz	dB	 20.5	32.5 22.5	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			2.1:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.9:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm		12.5	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		3.3	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		27.0	
t_D	Group Delay	f = 1.0 GHz	psec.		140	
V_d	Device Voltage		V	6.2	7.8	9.4
dV/dT	Device Voltage Temperature Coefficient		mV/°C		−17.0	

Notes: 1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices."
2. The recommended operating current range for this device is 20 mA to 40 mA. Typical gain performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	65 mA
Power Dissipation[2,3]	500 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

Thermal Resistance[2,4]: θ_{jc} = 140°C/W

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 7.1 mW/°C for T_C > 80°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Part Number Ordering Information

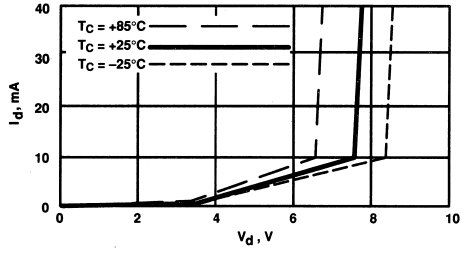
Part Number	Devices Per Reel	Reel Size
MSA-0886-TR1	1000	7"
MSA-0886-TR2	4000	13"

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

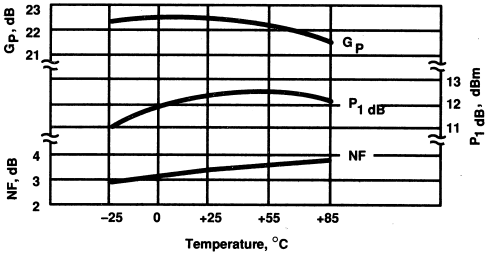
Typical Performance, T_A = 25°C

(unless otherwise noted)

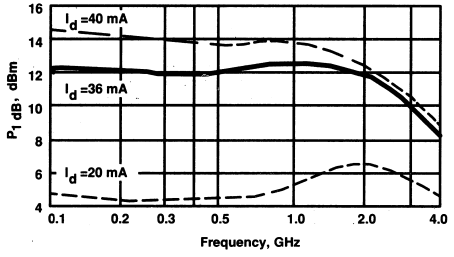
DEVICE CURRENT vs. VOLTAGE



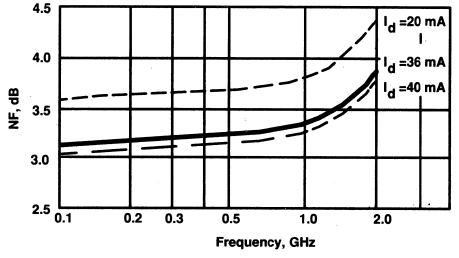
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. CASE TEMPERATURE
f = 1.0 GHz, I_d = 36 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 36 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang	k
0.1	.63	–22	32.5	42.12	160	–36.7	.015	54	.62	–24	0.68
0.2	.56	–41	31.3	36.68	143	–33.9	.020	50	.55	–46	0.64
0.4	.43	–69	28.6	26.94	119	–29.1	.035	52	.43	–79	0.69
0.6	.35	–88	26.4	20.89	104	–27.0	.045	49	.34	–103	0.77
0.8	.30	–104	24.2	16.21	93	–25.3	.054	50	.29	–124	0.83
1.0	.27	–116	22.4	13.20	83	–24.2	.062	49	.26	–139	0.87
1.5	.27	–144	19.2	9.15	65	–21.6	.083	46	.23	–172	0.93
2.0	.31	–166	16.7	6.84	49	–19.5	.105	41	.22	163	0.96
2.5	.35	178	14.8	5.50	38	–17.9	.128	36	.21	149	0.96
3.0	.40	162	12.9	4.41	25	–17.4	.135	30	.20	132	1.01
3.5	.45	149	11.4	3.72	13	–16.8	.145	25	.19	124	1.02
4.0	.51	137	9.9	3.14	1	–16.1	.157	19	.18	121	1.01
5.0	.61	116	7.3	2.31	–22	–15.7	.164	10	.17	130	1.00
6.0	.68	100	4.6	1.69	–42	–15.2	.173	4	.23	143	0.95

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0900
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

- **Broadband, Minimum Ripple Cascadable 50 Ω Gain Block**
- **8.0 ± 0.2 dB Typical Gain Flatness from 0.1 to 4.0 GHz**
- **3 dB Bandwidth: 0.1 to 6.0 GHz**
- **Low VSWR: ≤ 1.5:1 from 0.1 to 4.0 GHz**
- **11.5 dBm Typical P_{1dB} at 1.0 GHz**

Description

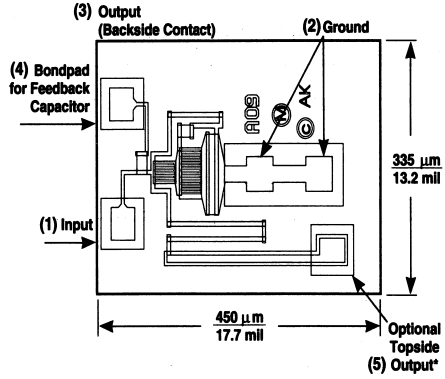
The MSA is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MODAMP™ MMIC is designed for very wide bandwidth industrial and military applications that require flat gain and low VSWR.

The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire.

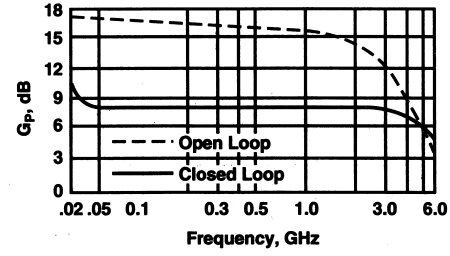
This chip is intended to be used with an external blocking capacitor completing the shunt feedback path (closed loop). Data sheet characterization is given for a 45 pF capacitor. Low frequency performance can be extended by using a larger valued capacitor[1].

Chip Outline[1]



Unless otherwise specified, tolerances are ±13 µm/±0.5 mils.
Chip thickness is 114 µm/4.5 mil Bond Pads are 41 µm/1.6 mil typical on each side.
*Output contact is normally made by die attaching the backside of the die.

Typical Power Gain vs. Frequency
T_A = 25°C, I_d = 35 mA



Electrical Specifications[2], T_A = 25°C

Unless otherwise noted, performance is for a MSA-0900 used with an external 45 pF capacitor. See bonding diagram.

Symbol	Parameters and Test Conditions[3]: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		8.0	
ΔG_P	Gain Flatness[4]	f = 0.1 to 4.0 GHz	dB		±0.2	
$f_{3\,dB}$	3 dB Bandwidth[4,5]		GHz		6.0	
VSWR	Input VSWR	f = 0.1 to 4.0 GHz			1.4:1	
	Output VSWR	f = 0.1 to 4.0 GHz			1.5:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz f = 4.0 GHz	dBm		11.5 6.5	
NF	50 Ω Noise Figure	f = 1.0 GHz f = 4.0 GHz	dB		6.0 6.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		23.0	
t_D	Group Delay	f = 1.0 GHz	psec		60	
V_d	Device Voltage		V	7.0	7.8	8.6
dV/dT	Device Voltage Temperature Coefficient		mV/°C		−16.0	

Notes:
1. See Application Note, AN-S009: MODAMP™ Silicon MMIC Chip Use for additional information.
2. The recommended operating current range for this device is 25 to 45 mA. Typical performance as a function of current is on the following page.
3. RF performance of the chip is determined by packaging and testing 10 devices per wafer.
4. The value is the expected achievable performance for the MSA-0900 used with an external 45 pF capacitor mounted in a 100 mil stripline package.
5. Referenced from 0.1 GHz gain (G_P).

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2, 3]	750 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	-65 to 200°C

Thermal Resistance[2,4]: θ_{jc} = 70°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{MOUNTING\ SURFACE}$ = 25°C.
3. Derate at 14 mW/°C for $T_{MOUNTING\ SURFACE}$ > 148°C.
4. The small spot size of the technique used results in a higher, though more accurate, determination of θ_{jc} than do alternate methods.

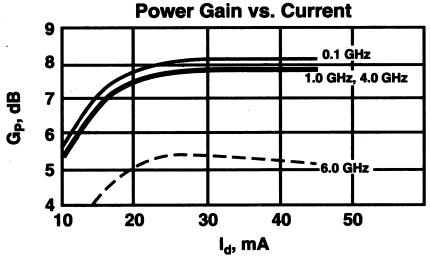
Part Number Ordering Information

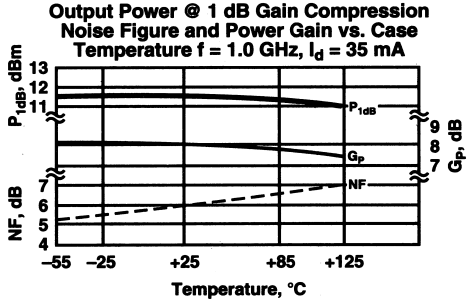
Part Number	Devices Per Tray
MSA-0900-GP2	10
MSA-0900-GP4	100
MSA-0900-GP6	Up to 300

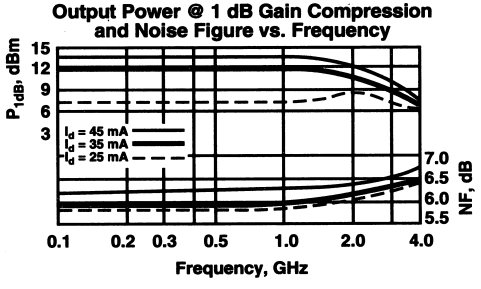
Typical Performance, T_A = 25°C

(Unless otherwise noted)

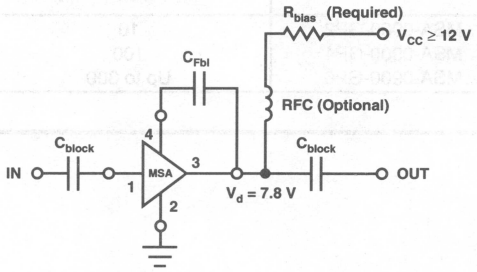
Note: Unless otherwise noted, performance is for a MSA-0900 used with an external 45 pF capacitor mounted in a 100 mil stripline package. See bonding diagram.



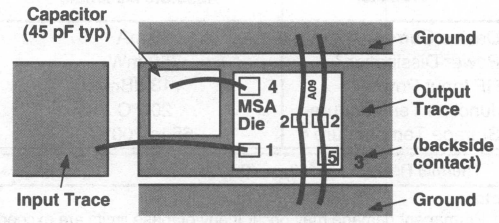




Typical Biasing Configuration



Bonding Diagram



Numbers refer to pin contacts listed on the Chip Outline.

Typical Scattering Parameters[5,6]: $Z_O = 50\ \Omega$

$T_A = 25\ °C$, $I_d = 35$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.02	.32	-107	10.8	3.48	151	-13.9	.203	17	.32	-106	0.83
0.05	.22	-143	8.6	2.70	164	-13.6	.209	6	.22	-142	1.09
0.1	.11	-144	8.2	2.57	171	-13.3	.215	3	.11	-142	1.16
0.2	.10	-160	8.1	2.54	172	-13.5	.211	1	.11	-158	1.19
0.4	.10	-171	8.1	2.54	175	-13.4	.215	2	.10	-166	1.18
0.6	.09	-170	8.1	2.55	166	-13.3	.216	1	.10	-166	1.18
0.8	.08	-171	8.2	2.57	162	-13.3	.216	1	.11	-166	1.17
1.0	.08	-170	8.3	2.59	158	-13.1	.220	1	.11	-167	1.15
1.5	.07	-166	8.6	2.68	147	-13.1	.221	1	.14	-172	1.12
2.0	.07	-138	8.9	2.80	136	-12.6	.234	1	.15	-172	1.07
2.5	.08	-131	9.3	2.92	126	-12.6	.236	1	.18	179	1.04
3.0	.12	-119	9.6	3.01	112	-12.0	.250	1	.21	171	0.99
3.5	.17	-125	9.6	3.02	95	-11.8	.256	-1	.22	157	0.97
4.0	.22	-132	9.1	2.86	78	-11.5	.265	-3	.19	144	0.96
4.5	.27	-140	8.4	2.64	63	-11.5	.265	-5	.16	138	0.97
5.0	.32	-149	7.5	2.36	50	-11.4	.268	-6	.12	138	1.00
5.5	.34	-154	6.4	2.09	38	-11.3	.272	-6	.10	162	1.02
6.0	.36	-158	5.3	1.84	29	-11.3	.272	-6	.10	-166	1.07
6.5	.38	-158	4.2	1.62	22	-11.4	.271	-6	.16	-151	1.12
7.0	.39	-157	3.2	1.45	15	-11.5	.267	-6	.23	-147	1.17

Notes: 5. S-parameters are de-embedded from 100 mil BeO package measured data using the package model found in the DEVICE MODELS section.
6. S-parameter data assumes an external 45 pF capacitor. Low frequency performance can be exended using a larger valued capacitor.

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MSA-0910
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

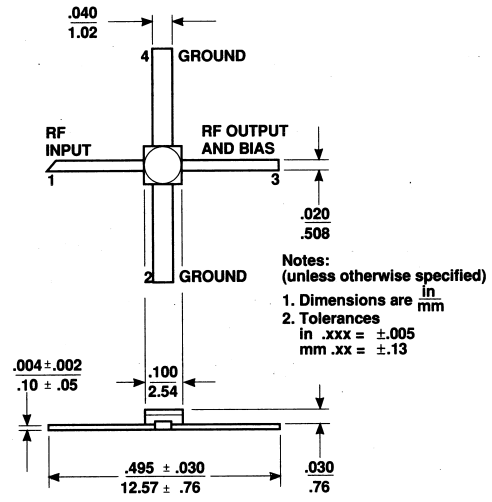
- **Broadband, Minimum Ripple Cascadable 50 Ω Gain Block**
- **8.0 ± 0.2 dB typical Gain Flatness from 0.1 to 4.0 GHz**
- **3 dB Bandwidth: 0.1 to 6.0 GHz**
- **Low VSWR: ≤ 1.5:1 from 0.1 to 4.0 GHz**
- **11.5 dBm typical $P_{1\,dB}$ at 1.0 GHz**
- **Hermetic Gold-ceramic Microstrip Package**

Description

The MSA-0910 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic, high reliability package. This MODAMP™ MMIC is designed for very wide bandwidth industrial and military applications that require flat gain and low VSWR

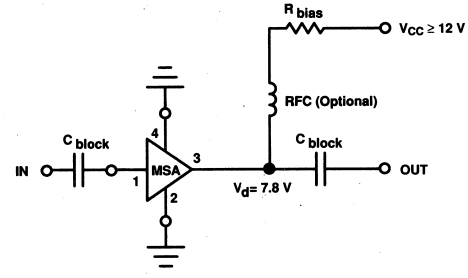
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

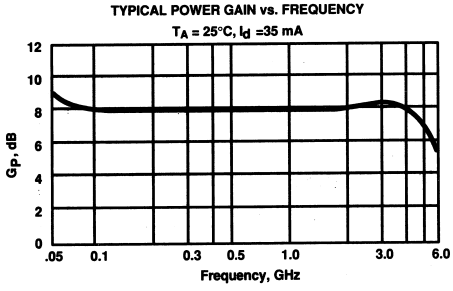
100 mil Package



Outline 10A

Typical Biasing Configuration





Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	7.0	8.0	9.0
ΔG_P	Gain Flatness	f = 0.1 to 4.0 GHz	dB		±0.2	±0.5
$f_{3\,dB}$	3 dB Bandwidth[2]		GHz		6.0	
VSWR	Input VSWR	f = 0.1 to 4.0 GHz			1.3:1	
	Output VSWR	f = 0.1 to 4.0 GHz			1.5:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz f = 4.0 GHz	dBm		11.5 6.5	
NF	50 Ω Noise Figure	f = 1.0 GHz f = 4.0 GHz	dB		6.0 6.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		23.0	
t_D	Group Delay	f = 1.0 GHz	psec.		100	
V_d	Device Voltage		V	7.0	7.8	8.6
dV/dT	Device Voltage Temperature Coefficient		mV/°C		−16.0	

Notes: 1. The recommended operating current range for this device is 25 mA to 45 mA. Typical performance as a function of current is on the following page.
2. Referenced from 0.1 GHz Gain (Gp).

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	750 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 145°C/W

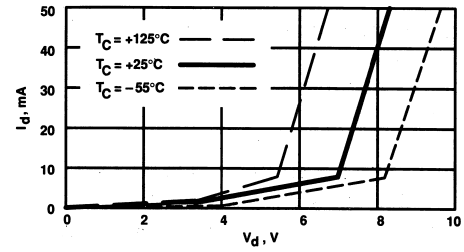
Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 6.9 mW/°C for T_C > 91°C.
4. The small spot size of this technique results in a higher, though more accurate, determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

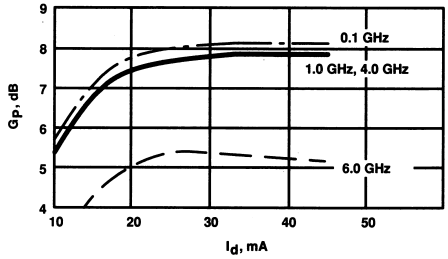
Typical Performance, T_A = 25°C

(unless otherwise noted)

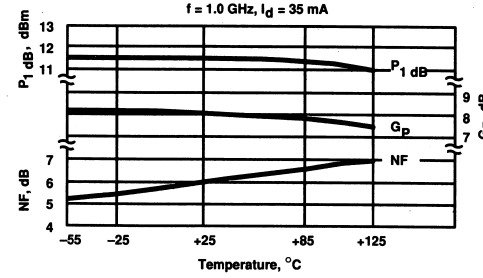
DEVICE CURRENT vs. VOLTAGE



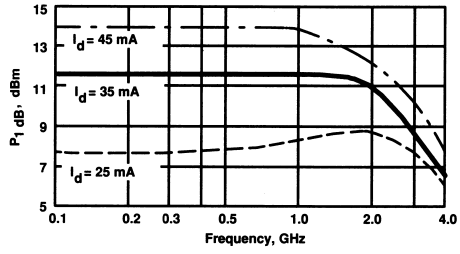
POWER GAIN vs. CURRENT



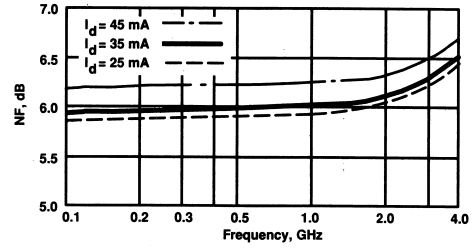
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. CASE TEMPERATURE
f = 1.0 GHz, I_d = 35 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 35 mA

Freq. GHz	S11 Mag	S11 Ang	S21 dB	S21 Mag	S21 Ang	S12 dB	S12 Mag	S12 Ang	S22 Mag	S22 Ang	k
0.02	.31	–108	10.6	3.38	150	–13.8	.202	16	.31	–107	0.85
0.05	.18	–114	8.8	2.75	160	–13.5	.212	8	.20	–117	1.06
0.1	.12	–141	8.1	2.53	166	–13.4	.214	3	.14	–139	1.16
0.2	.10	–166	7.9	2.47	167	–13.4	.215	1	.13	–157	1.19
0.4	.10	170	7.8	2.46	163	–13.3	.215	–1	.12	–165	1.20
0.6	.10	156	7.8	2.45	157	–13.3	.216	–3	.13	–167	1.20
0.8	.10	145	7.8	2.46	151	–13.3	.216	–4	.13	–168	1.19
1.0	.10	133	7.8	2.46	144	–13.3	.217	–6	.14	–169	1.19
1.5	.10	111	7.9	2.49	127	–13.2	.220	–10	.16	–173	1.17
2.0	.09	88	8.0	2.51	110	–13.0	.224	–13	.18	177	1.15
2.5	.07	89	8.2	2.58	96	–12.8	.230	–16	.21	167	1.11
3.0	.04	90	8.2	2.58	78	–12.8	.230	–21	.20	151	1.11
3.5	.06	145	8.2	2.57	59	–12.7	.233	–27	.19	137	1.11
4.0	.12	152	8.0	2.50	40	–12.7	.230	–33	.16	125	1.12
4.5	.19	142	7.5	2.38	22	–13.0	.223	–40	.13	116	1.16
5.0	.26	131	6.9	2.21	4	–13.5	.211	–47	.09	118	1.22
5.5	.32	120	6.2	2.04	–12	–14.1	.198	–52	.07	160	1.28
6.0	.38	109	5.3	1.84	–27	–14.8	.181	–56	.13	–173	1.38
6.5	.43	99	4.4	1.65	–42	–15.6	.167	–59	.21	–172	1.46

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-0986
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

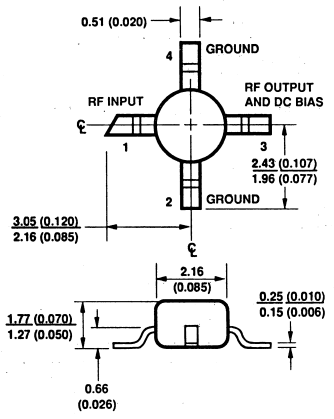
- **Broadband, Minimum Ripple Cascadable 50 Ω Gain Block**
- **7.2 ± 0.5 dB typical Gain Flatness from 0.1 to 3.0 GHz**
- **3 dB Bandwidth: 0.1 to 5.5 GHz**
- **10.5 dBm typical $P_{1\,dB}$ at 2.0 GHz**
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Description

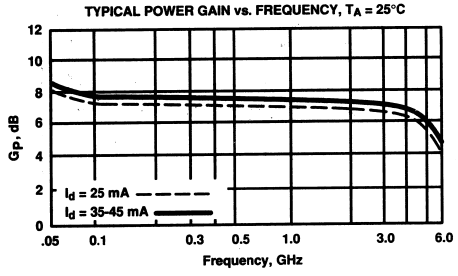
The MSA-0986 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost surface mount plastic package. This MODAMP™ MMIC is designed for very wide bandwidth industrial and commercial applications that require flat gain and low VSWR.

The MODAMP MSA-series is fabricated using a 10 GHz f_T 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alighment, ion implantation and gold metallization to achieve excellent uniformity, performance and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

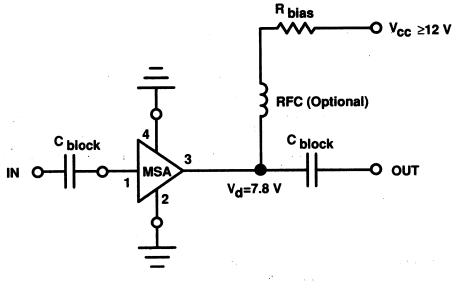
86 Plastic Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)



Typical Biasing Configuration



Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 2.0 GHz	dB	6.0	7.2	
ΔG_P	Gain Flatness	f = 0.1 to 3.0 GHz	dB		±0.5	
$f_{3\,dB}$	3 dB Bandwidth[3]		GHz		5.5	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.6:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.8:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 2.0 GHz	dBm		10.5	
NF	50 Ω Noise Figure	f = 2.0 GHz	dB		6.2	
IP_3	Third Order Intercept Point	f = 2.0 GHz	dBm		26	
t_D	Group Delay	f = 2.0 GHz	psec.		95	
V_d	Device Voltage		V	6.2	7.8	9.4
dV/dT	Device Voltage Temperature Coefficient		mV/°C		−16.0	

Notes: 1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices."
2. The recommended operating current range for this device is 25 mA to 45 mA. Typical gain performance as a function of current is on the following page.
3. Referenced from 0.1 GHz Gain (Gp).

MSA-0986 MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	65 mA
Power Dissipation[2,3]	500 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to +150°C

Thermal Resistance[2,4]: θ_{jc} = 140°C/W

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 7.1 mW/°C for T_C > 80°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Part Number Ordering Information

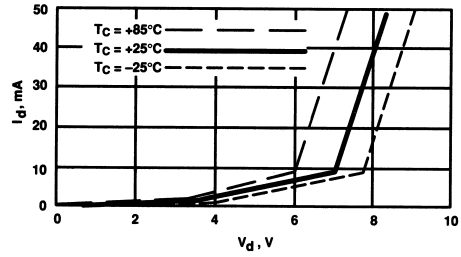
Part Number	Devices Per Reel	Reel Size
MSA-0986-TR1	1000	7"
MSA-0986-TR2	4000	13"

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

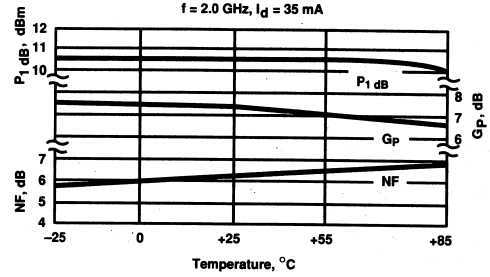
Typical Performance, T_A = 25°C

(unless otherwise noted)

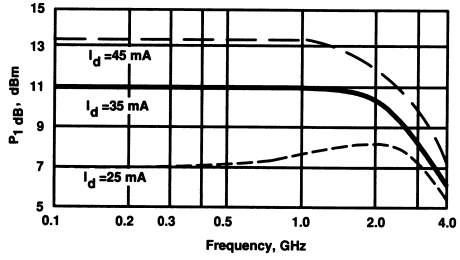
DEVICE CURRENT vs. VOLTAGE



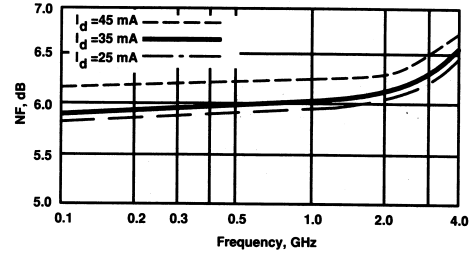
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. CASE TEMPERATURE
f = 2.0 GHz, I_d = 35 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 35 mA

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang	k
0.02	.36	–105	11.4	3.72	145	–14.1	.198	18	.38	–102	0.73
0.05	.24	–145	8.5	2.65	156	–13.7	.205	5	.25	–143	1.08
0.1	.22	–164	7.7	2.43	166	–13.5	.211	4	.22	–158	1.17
0.2	.21	–179	7.5	2.37	167	–13.5	.212	1	.22	–172	1.20
0.4	.21	165	7.4	2.34	162	–13.4	.214	–1	.22	179	1.20
0.6	.22	155	7.4	2.33	156	–13.5	.212	–2	.22	175	1.21
0.8	.22	145	7.3	2.33	149	–13.4	.213	–2	.23	171	1.21
1.0	.23	136	7.3	2.32	142	–13.4	.214	–4	.24	167	1.20
1.5	.24	118	7.2	2.30	125	–13.3	.217	–6	.26	157	1.19
2.0	.25	106	7.2	2.28	109	–13.0	.224	–10	.28	148	1.16
2.5	.26	100	7.2	2.29	94	–13.0	.224	–12	.33	139	1.15
3.0	.26	94	7.1	2.26	77	–13.0	.224	–15	.34	128	1.15
3.5	.26	95	7.0	2.23	60	–12.8	.229	–21	.36	116	1.14
4.0	.28	96	6.7	2.17	43	–13.1	.221	–25	.35	104	1.18
4.5	.31	100	6.5	2.10	26	–13.6	.210	–31	.32	94	1.23
5.0	.37	101	6.0	2.00	9	–14.2	.196	–35	.26	86	1.30
5.5	.44	97	5.4	1.86	–7	–14.9	.181	–38	.19	88	1.38
6.0	.51	94	4.6	1.69	–22	–15.8	.162	–37	.14	107	1.47

A model for this device is available in the DEVICE MODELS section.

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MSA-1000
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

- **High Output Power: +27 dBm typical P_{1dB} at 1.0 GHz**
- **Low Distortion: 37 dBm typical IP_3 at 1.0 GHz**
- **8.5 dB typical Gain at 1.0 GHz**
- **Impedance Matched to 25 Ω for Push-Pull Configurations**

Description

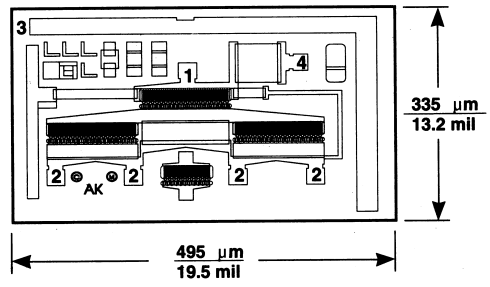
The MSA-1000 is a high performance, medium power silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MODAMP™ MMIC is designed for use in a push-pull configuration in a 25 Ω system. The MSA-1000 can also be used as a single-ended amplifier in a 50 Ω system with slightly reduced performance. Typical applications include narrow and broadband RF amplifiers in industrial and military systems.

The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire.

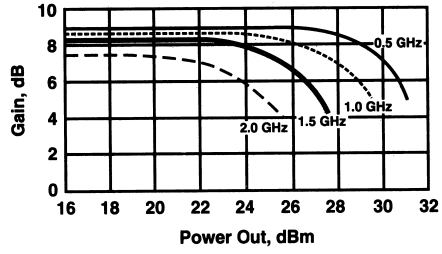
This chip is intended to be used with an external blocking capacitor completing the shunt feedback path (closed loop). Data sheet characterization is given for a 80 pF capacitor. Low frequency performance can be extended by using a larger valued capacitor[1].

Chip Outline[1]



Unless otherwise specified, tolerances are ±13 µm/±0.5 mils.
Chip thickness is 114 µm/4.5 mil Bond Pads are 41 µm/1.6 mil typical on each side.
*Output contact is normally made by die attaching the backside of the die.

Typical Gain vs. Power Out
Z_O = 25°C, I_d = 325 mA



Electrical Specifications[2], T_A = 25°C

Unless otherwise noted, performance is for a MSA-1000 used with an external 80 pF capacitor. See bonding diagram.

Symbol	Parameters and Test Conditions[3]: I_d = 325 mA, Z_O = 25 Ω		Units	Min.	Typ.	Max.
$P_{1\,dB}$	Output Power @1 dB Gain Compression	f = 1.0 GHz	dBm		27.0	
G_P	Power Gain ($\|S_{21}\|^2$)	f = 1.0 GHz	dB		8.5	
ΔG_P	Gain Flatness	f = 0.1 to 2.0 GHz	dB		±0.6	
$f_{3\,dB}$	3 dB Bandwidth[4]		GHz		2.6	
VSWR	Input VSWR	f = 0.1 to 2.0 GHz			2.0:1	
	Output VSWR	f = 0.1 to 2.0 GHz			2.5:1	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		37.0	
$NF_{25\,\Omega}$	25 Ω Noise Figure	f = 1.0 GHz	dB		7.0	
t_D	Group Delay	f = 1.0 GHz	psec		175	
V_d	Device Voltage		V	13.5	15.0	16.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		−18.0	

Notes:
1. See Application Note, AN-S009: MODAMP™ Silicon MMIC Chip Use for additional information.
2. The recommended operating current range for this device is 150 to 400 mA. Typical performance as a function of current is on the following page.
3. RF performance of the chip is determined by packaging and testing 10 devices per wafer.
4. Referenced from 0.01 GHz gain (G_P).

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	425 mA
Power Dissipation[2, 3]	7.0 W
RF Input Power	+25 dBm
Junction Temperature	200°C
Storage Temperature	-65 to 200°C

Thermal Resistance[2,4]: θ_{jc} = 10°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{MOUNTING\ SURFACE}$ = 25°C.
3. Derate at 100 mW/°C for $T_{MOUNTING\ SURFACE}$ > 130°C.
4. The small spot size of the technique used results in a higher, though more accurate, determination of θ_{jc} than do alternate methods.

Part Number Ordering Information

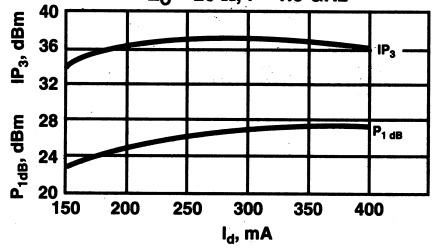
Part Number	Devices Per Tray
MSA-1000-GP2	10
MSA-1000-GP4	100
MSA-1000-GP6	Up to 300

Typical Performance, T_A = 25°C

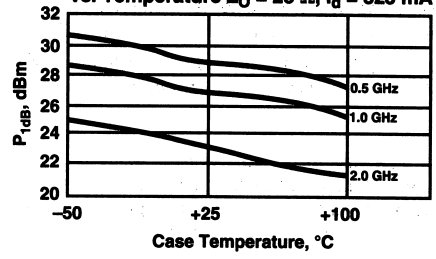
(Unless otherwise noted)

Note: Unless otherwise noted, performance is for a MSA-1000 used with an external 80 pF capacitor. See bonding diagram.

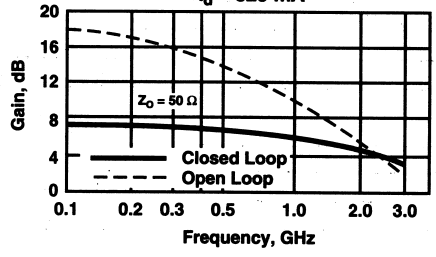
Output Power @ 1 dB Gain Compression, Third Order Intercept Point vs. Current Z_O = 25 Ω, f = 1.0 GHz



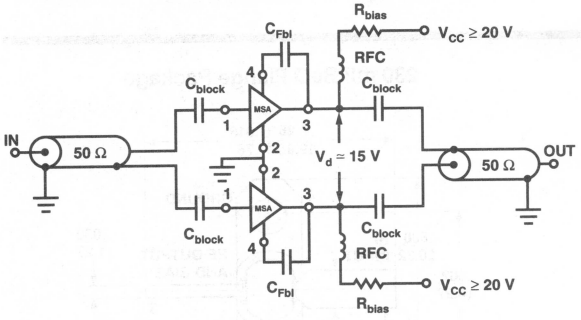
Output Power @ 1 dB Gain Compression vs. Temperature Z_O = 25 Ω, I_d = 325 mA



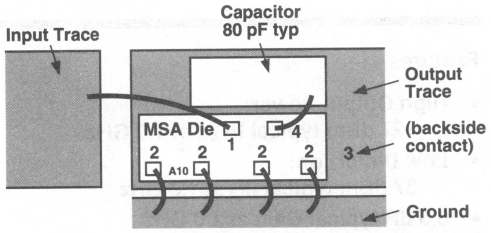
Gain vs. Frequency I_d = 325 mA



Typical Push-Pull Biasing Configuration



Bonding Diagram



Numbers refer to pin contacts listed on the Chip Outline.

Typical Scattering Parameters[5,6]: (50 Ω System)

$T_A = 25°C$, $I_d = 325$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
.001	.41	-121	15.5	5.95	149	-17.7	.130	22	.43	-99	.68
.005	.52	-167	8.7	2.73	156	-15.7	.164	6	.48	-161	1.02
.010	.54	-174	7.7	2.41	166	-15.6	.166	3	.46	-171	1.12
.050	.54	-179	7.3	2.31	174	-15.7	.165	1	.46	-178	1.17
.100	.55	179	7.2	2.30	173	-15.7	.165	-1	.46	-179	1.17
.200	.55	178	7.2	2.30	168	-15.7	.165	-1	.47	177	1.16
.400	.54	176	7.2	2.29	157	-15.7	.165	-3	.48	176	1.16
.600	.52	174	7.2	2.30	146	-15.8	.163	-4	.48	174	1.16
.800	.51	174	7.2	2.29	134	-15.8	.161	-5	.48	173	1.15
1.000	.50	172	7.2	2.29	121	-15.9	.160	-5	.49	172	1.12
1.200	.48	173	7.2	2.28	108	-16.0	.158	-6	.49	172	1.10
1.400	.47	175	7.1	2.26	96	-16.2	.155	-7	.50	174	1.05
1.600	.46	178	6.8	2.20	83	-16.3	.153	-7	.51	175	1.00
1.800	.46	179	6.4	2.09	62	-16.5	.150	-8	.53	176	.94
2.000	.48	-177	6.0	1.99	56	-16.6	.148	-10	.65	-179	.68
2.500	.56	-170	4.4	1.65	35	-17.0	.141	-1	.54	178	.91
3.000	.61	-171	2.7	1.36	12	-16.7	.147	1	.69	-176	.52

Notes: 5. S-parameters are de-embedded from 100 mil BeO package measured data using the package model found in the DEVICE MODELS section.
6. S-parameter data assumes an external 80 pF capacitor. Low frequency performance can be exended using a larger valued capacitor.

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MSA-1023
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

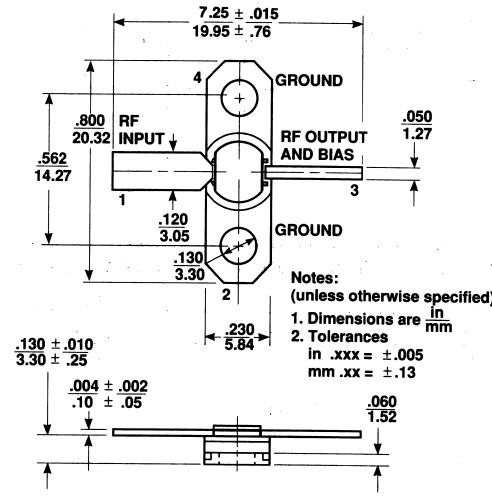
- **High Output Power: +27 dBm typical $P_{1\,dB}$ at 1.0 GHz**
- **Low Distortion: 37 dBm typical IP_3 at 1.0 GHz**
- **8.5 dB typical Gain at 1.0 GHz**
- **Hermetic, Metal/Beryllia Stripline Package**
- **Impedance Matched to 25 Ω for Push-Pull Configuration**

Description

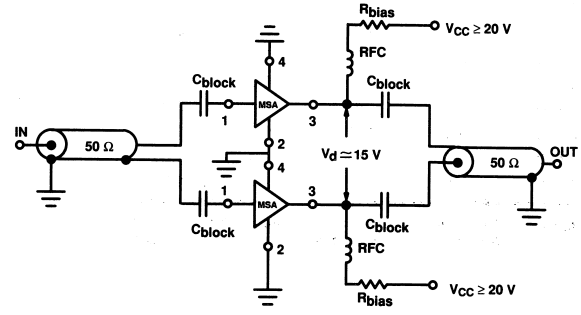
The MSA-1023 is a high performance, medium power silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic, BeO flange package for good thermal characteristics. This MODAMP™ MMIC is designed for use in a push-pull configuration in a 25 Ω system. The MSA-1023 can also be used as a single-ended amplifier in a 50 Ω system with slightly reduced performance. Typical applications include narrow and broadband RF amplifiers in industrial and military systems.

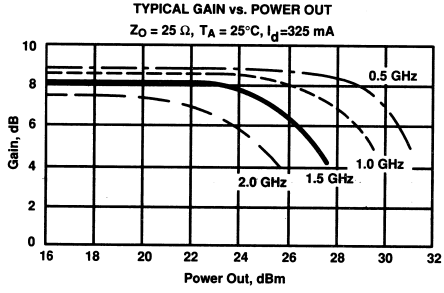
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

230 mil BeO Flange Package



Typical Push-Pull Biasing Configuration





Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 325 mA, Z_O = 25 Ω		Units	Min.	Typ.	Max.
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 1.0 GHz	dBm	25.0	27.0	
G_P	Power Gain ($\|S_{21}\|^2$)	f = 1.0 GHz	dB	7.5	8.5	9.5
ΔG_P	Gain Flatness	f = 0.1 to 2.0 GHz	dB		±0.6	
$f_{3\,dB}$	3 dB Bandwidth[2]		GHz		2.5	
VSWR	Input VSWR	f = 0.1 to 2.0 GHz			2.0:1	
	Output VSWR	f = 0.1 to 2.0 GHz			2.8:1	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		37.0	
$NF_{25\,\Omega}$	25 Ω Noise Figure	f = 1.0 GHz	dB		7.0	
t_D	Group Delay	f = 1.0 GHz	psec.		250	
V_d	Device Voltage		V	13.5	15.0	16.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		−18.0	

Notes: 1. The recommended operating current range for this device is 150 mA to 400 mA. Typical performance as a function of current is on the following page.
2. Referenced from 10 MHz Gain (Gp).

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	425 mA
Power Dissipation[2,3]	7.0W
RF Input Power	+25 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 15°C/W

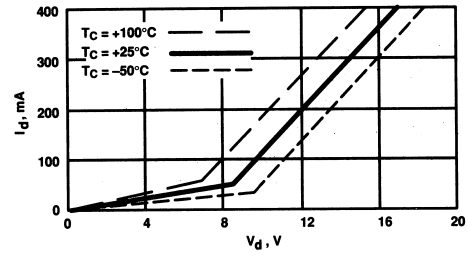
Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 66.7 mW/°C for T_C > 95°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

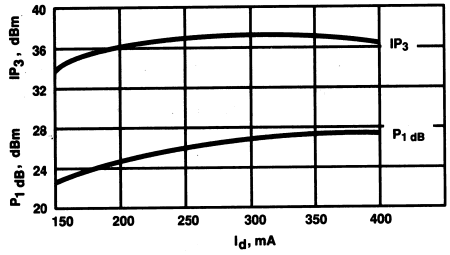
Typical Performance, T_A = 25°C

(unless otherwise noted)

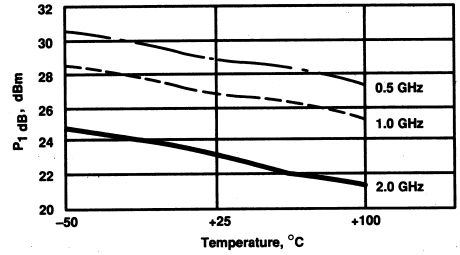
DEVICE CURRENT vs. VOLTAGE



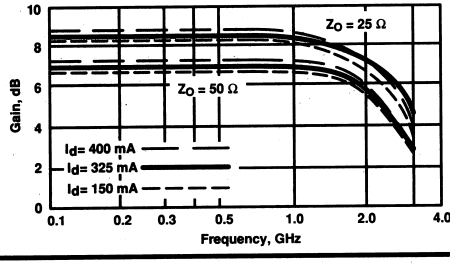
OUTPUT POWER @ 1 dB GAIN COMPRESSION
THIRD ORDER INTERCEPT POINT vs. CURRENT
Z_O = 25 Ω, f = 1.0 GHz



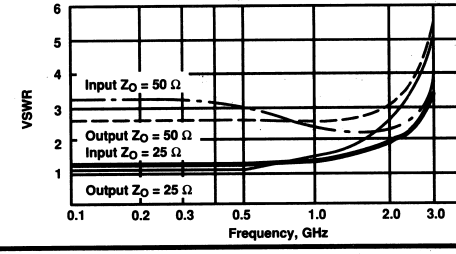
OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. TEMPERATURE
Z_O = 25 Ω, I_d = 325 mA



GAIN vs. FREQUENCY



VSWR vs. FREQUENCY
I_d = 325 mA



Typical Scattering Parameters: (50 Ω System)

T_A = 25°C, I_d = 325 mA

Freq. MHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang	k
1	.40	–121	15.3	5.85	149	–17.9	.128	22	.42	–99	0.69
5	.51	–167	8.5	2.67	156	–15.9	.160	6	.45	–161	1.05
10	.52	–174	7.5	2.36	166	–15.8	.162	3	.45	–171	1.16
25	.52	–178	7.2	2.28	172	–15.8	162	1	.45	–177	1.20
50	.52	179	7.1	2.26	173	–15.8	.161	–1	.45	–179	1.21
100	.53	176	7.0	2.25	170	–15.8	.161	–3	.45	179	1.21
200	.53	172	7.0	2.25	163	–15.8	.161	–5	.46	174	1.21
400	.51	164	7.0	2.24	146	–15.8	.161	–11	.46	170	1.22
600	.48	157	7.0	2.24	130	–16.0	.159	–16	.45	165	1.23
800	.45	151	7.0	2.23	113	–16.1	.157	–21	.44	161	1.24
1000	.42	146	7.0	2.23	95	–16.2	.155	–26	.44	157	1.24
1200	.38	144	6.9	2.22	78	–16.4	.151	–31	.44	155	1.24
1400	.35	145	6.8	2.20	61	–16.7	.146	–36	.45	154	1.24
1600	.34	149	6.6	2.15	44	–17.0	.141	–41	.46	153	1.22
1800	.36	152	6.3	2.07	19	–17.3	.136	–45	.49	150	1.18
2000	.39	153	5.9	1.97	11	–17.7	.130	–49	.62	148	1.13
2500	.51	148	4.6	1.69	–24	–18.3	.121	–52	.52	140	0.91
3000	.60	133	3.0	1.41	–57	–17.9	.127	–57	.70	128	0.59

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-1100
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

- **High Dynamic Range Cascadable 50 Ω or 75 Ω Gain Block**
- **3 dB Bandwidth: 50 MHz to 1.6 GHz**
- **17.5 dBm Typical P_{1dB} at 0.5 GHz**
- **12 dB Typical 50 Ω Gain at 0.5 GHz**
- **3.5 dB Typical Noise Figure at 0.5 GHz**

Description

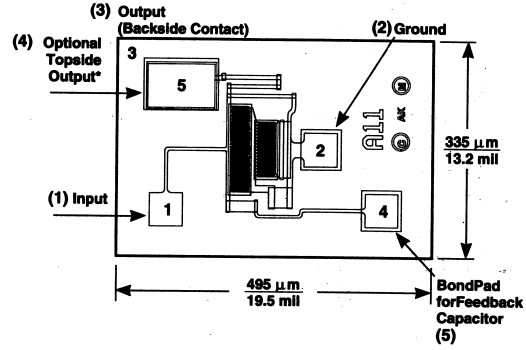
The MSA-1100 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MODAMP™ MMIC is designed for high dynamic range in either 50 or 75 Ω systems by combining low noise figure with high IP_3. Typical applications include narrow and broadband linear amplifiers in industrial and military applications.

The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire.

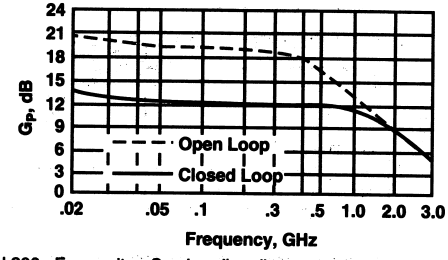
This chip is intended to be used with an external blocking capacitor completing the shunt feedback path (closed loop). Data sheet characterization is given for a 200 pF capacitor. Low frequency performance can be extended by using a larger valued capacitor[1].

Chip Outline[1]



Unless otherwise specified, tolerances are ±13 µm/±0.5 mils.
Chip thickness is 114 µm/4.5 mil Bond Pads are 41 µm/1.6 mil typical on each side.
*Output contact is normally made by die attaching the backside of the die.

Typical Power Gain vs. Frequency
T_A = 25°C, I_d = 60 mA



Electrical Specifications[2], T_A = 25°C

Unless otherwise noted, performance is for a MSA-1100 used with an external 200 pF capacitor. See bonding diagram.

Symbol	Parameters and Test Conditions[3]: I_d = 60 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		12.5	
ΔG_P	Gain Flatness	f = 0.1 to 1.0 GHz	dB		±0.7	
$f_{3\,dB}$	3 dB Bandwidth[4]		GHz		1.6	
VSWR	Input VSWR	f = 0.1 to 1.0 GHz			1.7:1	
	Output VSWR	f = 0.1 to 1.0 GHz			1.9:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 0.5 GHz	dBm		17.5	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		3.5	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		30.0	
t_D	Group Delay	f = 0.5 GHz	psec.		125	
V_d	Device Voltage		V	4.5	5.5	6.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes:
1. See Application Note, AN-S009: MODAMP™ Silicon MMIC Chip Use for additional information.
2. The recommended operating current range for this device is 40 to 75 mA. Typical performance as a function of current is on the following page.
3. RF performance of the chip is determined by packaging and testing 10 devices per wafer.
4. Referenced from 0.05 GHz gain (G_P).

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	100 mA
Power Dissipation[2, 3]	650 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	-65 to 200°C

Thermal Resistance[2,4]: θ_{jc}[2] = 57°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{MOUNTING\ SURFACE}$ = 25°C.
3. Derate at 17.5 mW/°C for $T_{MOUNTING\ SURFACE}$ > 163°C.
4. The small spot size of the technique used results in a higher, though more accurate, determination of θ_{jc} than do alternate methods.

Part Number Ordering Information

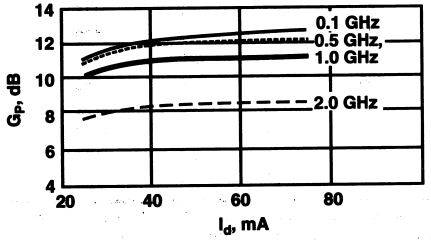
Part Number	Devices Per Tray
MSA-1100-GP2	10
MSA-1100-GP4	100
MSA-1100-GP6	Up to 300

Typical Performance, T_A = 25°C

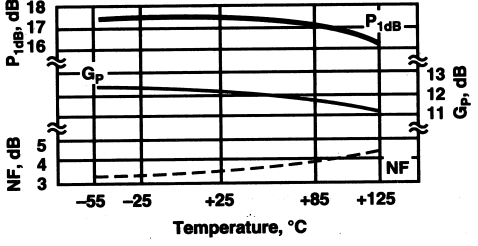
(Unless otherwise noted)

Note: Unless otherwise noted, performance is for a MSA-1100 used with an external 200 pF capacitor. See bonding diagram.

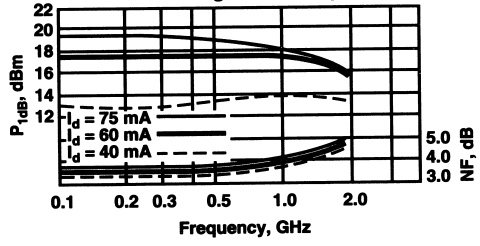
Power Gain vs. Current



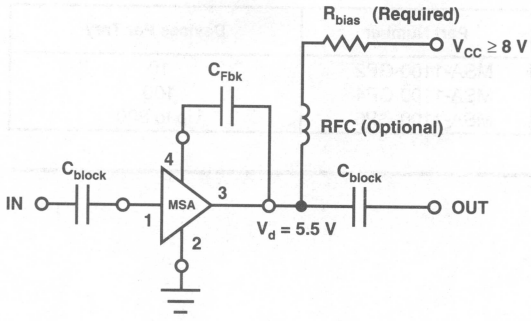
Output Power @ 1 dB Gain Compression Noise Figure and Power Gain vs. Case Temperature f = 0.5 GHz, I_d = 60 mA



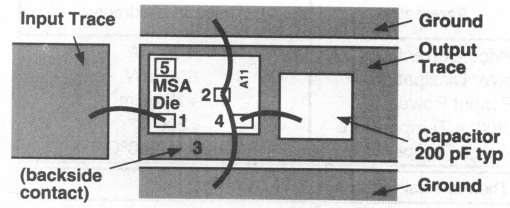
Output Power @ 1 dB Gain Compression and Noise Figure vs. Frequency



Typical Biasing Configuration



Bonding Diagram



Numbers refer to pin contacts listed on the Chip Outline.

Typical Scattering Parameters[5,6]

$T_A = 25°C$, $I_d = 60$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
.001	.72	-26	19.3	9.23	168	-23.4	.067	46	.72	-27	.52
.005	.19	-73	14.1	5.09	165	-16.7	.147	11	.19	-77	.96
.010	.16	-69	13.9	4.97	168	-16.6	.148	9	.16	-79	.99
.050	.04	-59	12.8	4.39	175	-16.0	.159	3	.04	-102	1.06
.100	.05	-66	12.8	4.38	175	-16.0	.158	2	.05	-100	1.06
.200	.07	-78	12.8	4.36	170	-15.9	.161	4	.08	-100	1.05
.400	.14	-92	12.7	4.31	162	-15.6	.165	7	.14	-105	1.01
.600	.19	-102	12.5	4.22	153	-15.3	.171	10	.21	-111	.96
.800	.25	-110	12.3	4.11	144	-14.9	.180	13	.27	-116	.90
1.000	.31	-117	12.0	4.00	137	-14.4	.190	14	.33	-122	.83
1.500	.40	-132	10.9	3.52	117	-13.4	.214	15	.42	-136	.70
2.000	.47	-145	9.6	3.01	100	-12.6	.235	14	.46	-148	.64
2.500	.50	-150	8.3	2.60	89	-12.0	.251	16	.45	-152	.63
3.000	.52	-158	7.0	2.23	77	-11.6	.263	17	.42	-156	.66
3.500	.51	-164	5.7	1.92	68	-11.1	.278	19	.38	-155	.73
4.000	.50	-169	4.6	1.70	61	-10.5	.297	22	.34	-152	.79

Notes: 5. S-parameters are de-embedded from 200 mil BeO package measured data using the package model found in the DEVICE MODELS section.
6. S-parameter data assumes an external 200 pF capacitor. Low frequency performance can be exended using a larger valued capacitor.

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MSA-1104
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

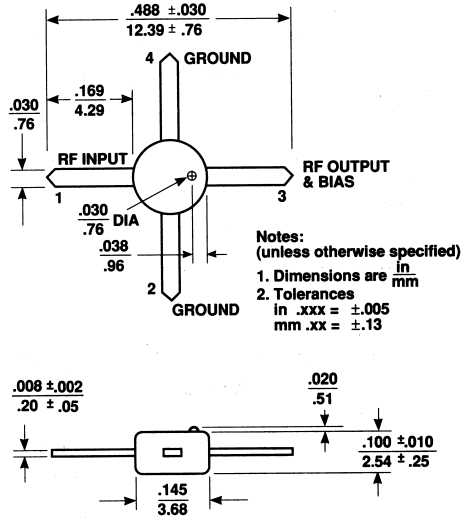
- **High Dynamic Range Cascadable 50 Ω or 75 Ω Gain Block**
- **3 dB Bandwidth: 50 MHz to 1.3 GHz**
- **17.5 dBm typical $P_{1\,dB}$ at 0.5 GHz**
- **12 dB typical 50 Ω Gain at 0.5 GHz**
- **3.6 dB typical Noise Figure at 0.5 GHz**
- **Low Cost Plastic Package**

Description

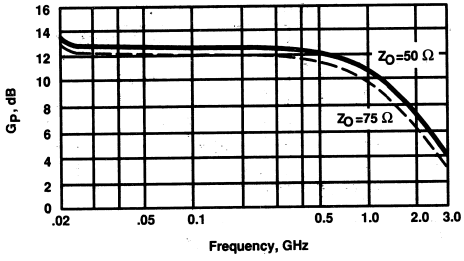
The MSA-1104 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost plastic package. This MODAMP™ MMIC is designed for high dynamic range in either 50 or 75 Ω systems by combining low noise figure with high IP_3. Typical applications include narrow and broad band linear amplifiers in commercial and industrial applications.

The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

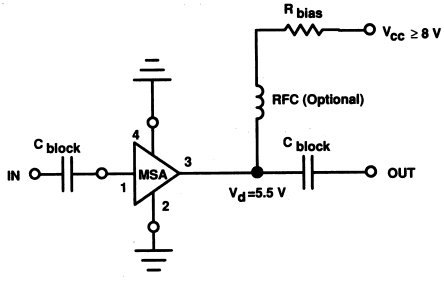
04A Plastic Package



TYPICAL POWER GAIN vs. FREQUENCY
T_A = 25°C, I_d = 60 mA



Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 60 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
GP	Power Gain ($\|S_{21}\|^2$)	f = 0.05 GHz f = 0.5 GHz f = 1.0 GHz	dB dB dB	10.0	12.7 12.0 10.5	
ΔGP	Gain Flatness	f = 0.1 to 1.0 GHz	dB		±1.0	
$f_{3\,dB}$	3 dB Bandwidth[2]		GHz		1.3	
VSWR	Input VSWR	f = 0.1 to 1.0 GHz			1.5:1	
	Output VSWR	f = 0.1 to 1.0 GHz			1.7:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 0.5 GHz	dBm		17.5	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		3.6	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		30	
t_D	Group Delay	f = 0.5 GHz	psec.		200	
V_d	Device Voltage		V	4.4	5.5	6.6
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes: 1. The recommended operating current range for this device is 40 mA to 70 mA. Typical performance as a function of current is on the following page.
2. Referenced from 50 MHz Gain (Gp).

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	550 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

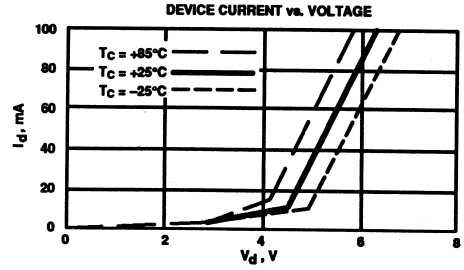
Thermal Resistance[2,4]: θ_{jc} = 115°C/W

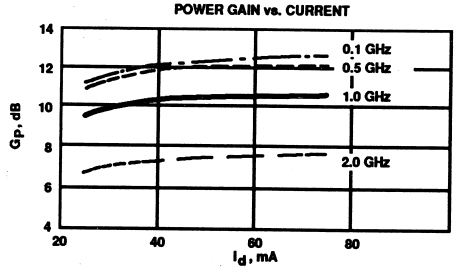
Notes:

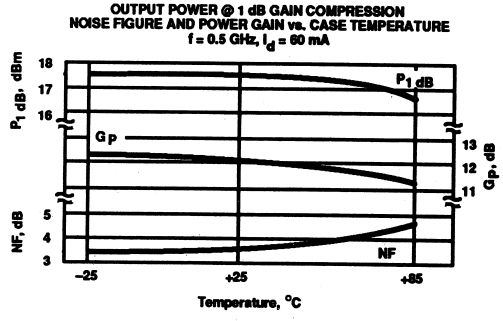
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 8.7 mW/°C for T_C > 87°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

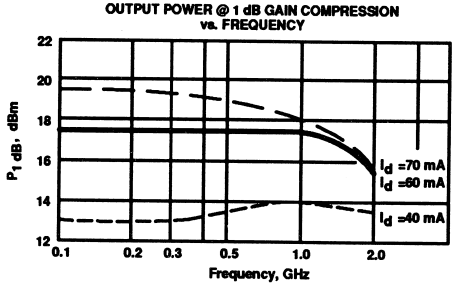
Typical Performance, T_A = 25°C, Z_O = 50 Ω

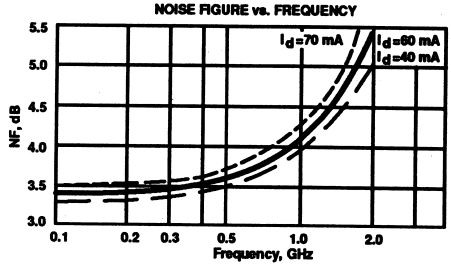
(unless otherwise noted)











Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 60 mA

Freq.	S11		S21			S12			S22		
MHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.5	.76	–22	19.3	9.19	167	–24.4	.060	54	.77	–22	0.48
5.0	.20	–79	13.7	4.83	164	–16.5	.149	12	.21	–83	0.96
25.0	.05	–78	12.8	4.35	174	–16.2	.154	2	.06	–101	1.07
50.0	.04	–75	12.7	4.31	174	–16.4	.151	2	.05	–136	1.09
100.0	.04	–81	12.6	4.29	171	–16.4	.152	2	.05	–137	1.09
200.0	.04	–93	12.6	4.24	164	–16.3	.153	3	.07	–135	1.09
300.0	.06	–105	12.4	4.18	156	–16.2	.155	4	.10	–136	1.08
400.0	.07	–115	12.3	4.11	148	–16.0	.158	5	.12	–139	1.07
500.0	.09	–124	12.1	4.01	141	–15.8	.162	6	.15	–144	1.06
600.0	.11	–132	11.8	3.91	134	–15.6	.166	7	.17	–150	1.06
700.0	.13	–140	11.6	3.80	126	–15.4	.170	7	.19	–156	1.05
800.0	.15	–147	11.3	3.68	120	–15.2	.174	7	.22	–161	1.04
900.0	.16	–154	11.0	3.56	113	–14.9	.180	7	.24	–168	1.03
1000.0	.18	–161	10.7	3.43	106	–14.7	.184	6	.26	–173	1.03
1500.0	.28	171	9.1	2.85	77	–13.5	.211	2	.35	163	0.99
2000.0	.37	149	7.6	2.39	52	–13.0	.224	–5	.43	140	0.99
2500.0	.45	133	6.1	2.02	33	–12.7	.231	–10	.47	125	1.02
3000.0	.52	118	4.6	1.69	14	–12.6	.234	–16	.50	112	1.05

A model for this device is available in the DEVICE MODELS section.

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MSA-1105
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

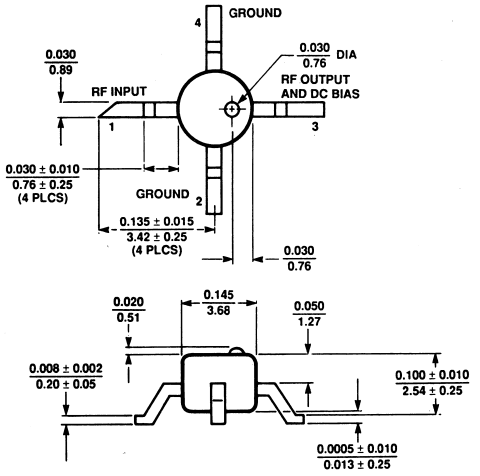
- **High Dynamic Range Cascadable 50 Ω or 75 Ω Gain Block**
- **3 dB Bandwidth: 50 MHz to 1.3 GHz**
- **17.5 dBm typical $P_{1\,dB}$ at 0.5 GHz**
- **3.6 dB typical Noise Figure at 0.5 GHz**
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Description

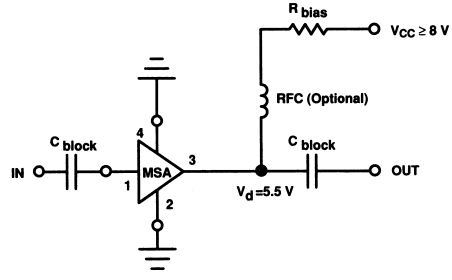
The MSA-1105 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost, surface mount plastic package. This MODAMP™ MMIC is designed for high dynamic range in either 50 or 75 ohm systems by combining low noise figure with high IP_3. Typical applications include narrow and broad band linear amplifiers in commercial and industrial applications.

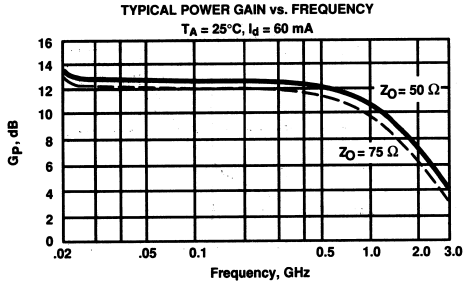
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

05 Plastic Package



Typical Biasing Configuration





Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 60 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.05 GHz f = 0.5 GHz f = 1.0 GHz	dB dB dB	10.0	12.7 12.0 10.5	
ΔG_P	Gain Flatness	f = 0.1 to 1.0 GHz	dB		±1.0	
$f_{3\,dB}$	3 dB Bandwidth[3]		GHz		1.3	
VSWR	Input VSWR	f = 0.1 to 1.0 GHz			1.5:1	
	Output VSWR	f = 0.1 to 1.0 GHz			1.7:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 0.5 GHz	dBm		17.5	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		3.6	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		30	
t_D	Group Delay	f = 0.5 GHz	psec.		200	
V_d	Device Voltage		V	4.4	5.5	6.6
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes: 1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices."
2. The recommended operating current range for this device is 40 mA to 70 mA. Typical gain performance as a function of current is on the following page.
3. Referenced from 50 GHz Gain (Gp).

MSA-1105 MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	550 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	–65°C to 150°C

Thermal Resistance[2,4]: θ_{jc} = 125°C/W

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 8 mW/°C for T_C > 124°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Part Number Ordering Information

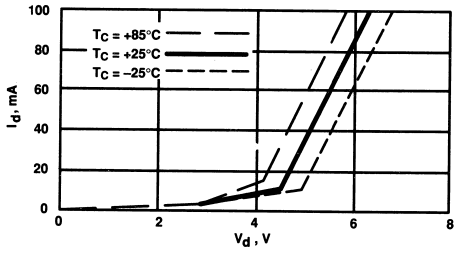
Part Number	Devices Per Reel	Reel Size
MSA-1105-TR1	500	7"
MSA-1105-TR2	1500	13"

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

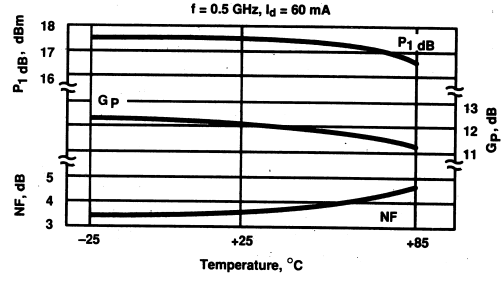
Typical Performance, T_A = 25°C, Z_O = 50 Ω

(unless otherwise noted)

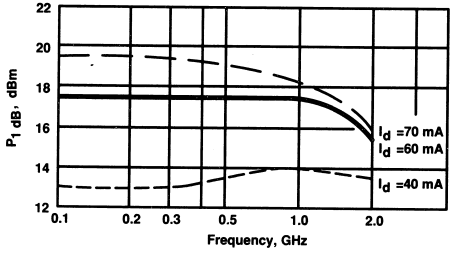
DEVICE CURRENT vs. VOLTAGE



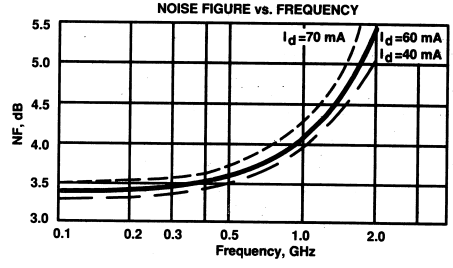
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. CASE TEMPERATURE
f = 0.5 GHz, Id = 60 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 60 mA

Freq. MHz	S11 Mag	S11 Ang	S21 dB	S21 Mag	S21 Ang	S12 dB	S12 Mag	S12 Ang	S22 Mag	S22 Ang	k
0.5	.80	–17	19.0	8.94	171	–26.0	.050	51	.81	–16	0.53
5.0	.26	–62	13.9	4.98	163	–16.8	.144	15	.26	–64	0.93
25.0	.07	–48	12.8	4.36	174	–16.4	.151	4	.08	–52	1.08
50.0	.06	–38	12.7	4.33	174	–16.3	.153	2	.06	–48	1.08
100.0	.05	–41	12.7	4.31	170	–16.4	.152	3	.06	–52	1.09
200.0	.06	–58	12.6	4.26	162	-16.2	.155	5	.08	–73	1.08
300.0	.07	–74	12.4	4.19	154	–16.1	.157	7	.10	–91	1.07
400.0	.09	–91	12.2	4.10	146	–15.8	.163	8	.12	–105	1.06
500.0	.10	–105	12.0	4.00	138	–15.6	.166	8	.14	–116	1.05
600.0	.11	–116	11.8	3.88	131	–15.4	.171	10	.17	–126	1.04
700.0	.13	–128	11.5	3.76	123	–15.0	.178	11	.18	–135	1.03
800.0	.15	–136	11.2	3.63	116	–14.7	.184	11	.21	–144	1.01
900.0	.16	–145	10.9	3.49	109	–15.5	.188	11	.22	–151	1.01
1000.0	.18	–152	10.5	3.37	102	–14.1	.197	11	.24	–159	1.00
1500.0	.28	174	8.8	2.75	72	–13.2	.219	7	.31	170	1.00
2000.0	.38	150	7.1	2.28	48	–12.1	.248	0	.34	151	0.99
2500.0	.46	133	5.6	1.90	28	–11.9	.254	–4	.38	134	1.02
3000.0	.53	118	4.2	1.62	11	–11.6	.262	–8	.40	122	1.04

A model for this device is available in the DEVICE MODELS section.

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MSA-1110
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

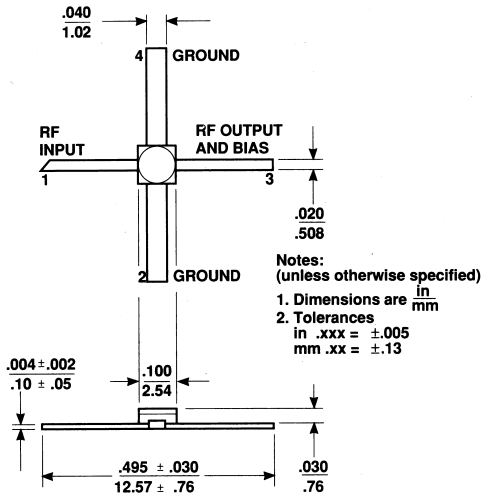
- **High Dynamic Range Cascadable 50 Ω or 75 Ω Gain Block**
- **3 dB Bandwidth: 50 MHz to 1.6 GHz**
- **17.5 dBm typical $P_{1\,dB}$ at 0.5 GHz**
- **12 dB typical 50 Ω Gain at 0.5 GHz**
- **3.5 dB typical Noise Figure at 0.5 GHz**
- **Hermetic Gold-ceramic Microstrip Package**

Description

The MSA-1110 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic high reliability package. This MODAMP™ MMIC is designed for high dynamic range in either 50 or 75 Ω systems by combining low noise figure with high IP_3. Typical applications include narrow and broad band linear amplifiers in industrial and military applications.

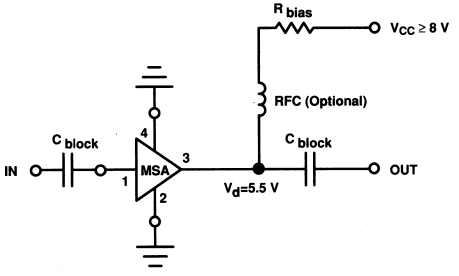
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

100 mil Package

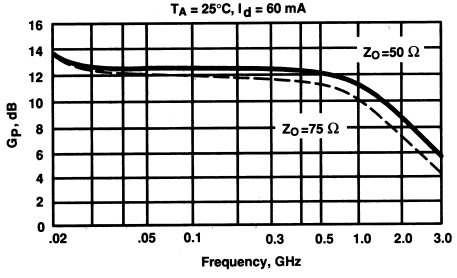


Outline 10A

Typical Biasing Configuration



TYPICAL POWER GAIN vs. FREQUENCY
T_A = 25°C, I_d = 60 mA



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 60 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	11.5	12.5	13.5
ΔG_P	Gain Flatness	f = 0.1 to 1.0 GHz	dB		±0.7	±1.0
$f_{3\,dB}$	3 dB Bandwidth[2]		GHz		1.6	
VSWR	Input VSWR	f = 0.1 to 1.0 GHz			1.7:1	
	Output VSWR	f = 0.1 to 1.0 GHz			1.9:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 0.5 GHz	dBm	16.0	17.5	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		3.5	4.5
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		30.0	
t_D	Group Delay	f = 0.5 GHz	psec.		160	
V_d	Device Voltage		V	4.5	5.5	6.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes: 1. The recommended operating current range for this device is 40 mA to 75 mA. Typical performance as a function of current is on the following page.
2. Referenced from 50 MHz Gain (Gp).

MSA-1110 MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	90 mA
Power Dissipation[2,3]	560 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 135°C/W

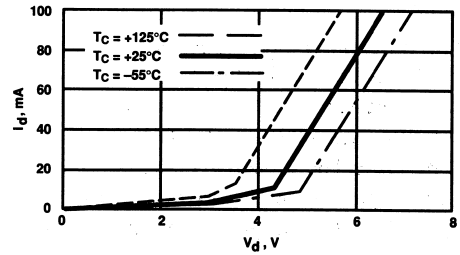
Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 7.4 mW/°C for T_C > 124°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

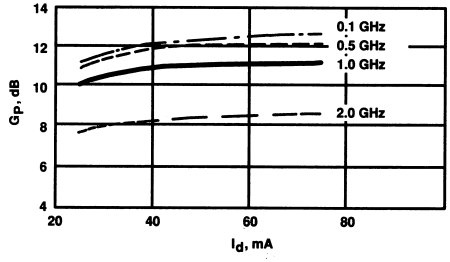
Typical Performance, T_A = 25°C, Z_O = 50 Ω

(unless otherwise noted)

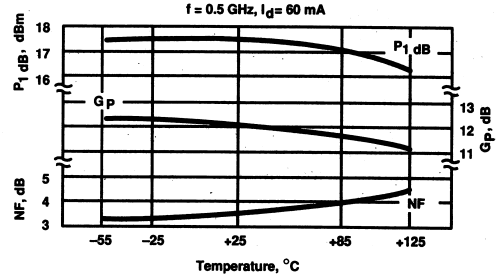
DEVICE CURRENT vs. VOLTAGE



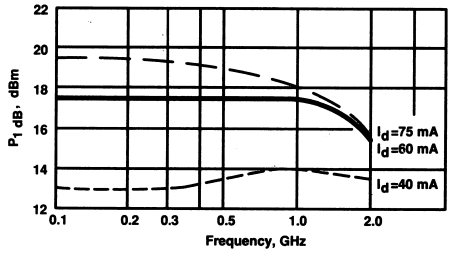
POWER GAIN vs. CURRENT



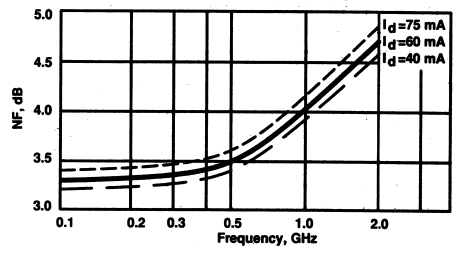
OUTPUT POWER @ 1 dB GAIN COMPRESSION
NOISE FIGURE AND POWER GAIN vs. CASE TEMPERATURE
f = 0.5 GHz, I_d = 60 mA



OUTPUT POWER @ 1 dB GAIN COMPRESSION
vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 60 mA

Freq. MHz	S11 Mag	S11 Ang	S21 dB	S21 Mag	S21 Ang	S12 dB	S12 Mag	S12 Ang	S22 Mag	S22 Ang	k
0.5	.83	–7	19.5	9.44	176	–31.9	.025	39	.84	–7	0.77
5.0	.54	–50	16.8	6.92	158	–18.7	.116	34	.55	–50	0.60
25.0	.15	–78	13.0	4.47	167	–16.6	.148	9	.15	–79	1.03
50.0	.10	–64	12.6	4.26	171	–16.5	.149	5	.10	–67	1.08
100.0	.08	–63	12.5	4.23	171	–16.5	.150	4	.08	–66	1.09
200.0	.09	–74	12.4	4.17	166	–16.4	.152	4	.09	–78	1.09
300.0	.11	–85	12.3	4.10	160	–16.2	.154	5	.12	–89	1.07
400.0	.13	–94	12.3	4.10	154	–16.1	.157	6	.15	–98	1.05
500.0	.16	–102	12.1	4.04	148	–15.9	.161	7	.18	–106	1.02
600.0	.18	–108	12.0	3.98	143	–15.6	.165	8	.20	–113	1.00
700.0	.21	–114	11.8	3.89	137	–15.4	.169	8	.23	–120	0.97
800.0	.23	–120	11.6	3.80	131	–15.2	.173	8	.25	–126	0.95
900.0	.25	–126	11.4	3.71	126	–15.0	.178	8	.28	–132	0.92
1000.0	.27	–131	11.1	3.60	120	–14.8	.182	8	.30	–137	0.91
1500.0	.36	–153	9.8	3.10	96	–13.8	.203	4	.37	–160	0.83
2000.0	.42	–171	8.4	2.64	74	–13.3	.217	1	.40	–178	0.82
2500.0	.47	177	7.2	2.29	59	–12.5	.236	–2	.41	172	0.80
3000.0	.47	159	5.9	1.97	43	–13.2	.220	–10	.38	157	0.95

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSA-1120
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

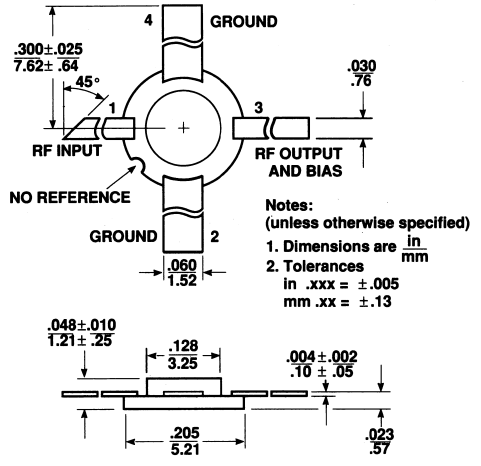
- **High Dynamic Range Cascadable 50 Ω or 75 Ω Gain Block**
- **3 dB Bandwidth: 50 MHz to 1.6 GHz**
- **17.5 dBm typical $P_{1\,dB}$ at 0.5 GHz**
- **12 dB typical 50 Ω Gain at 0.5 GHz**
- **3.5 dB typical Noise Figure at 0.5 GHz**
- **Hermetic Metal/Beryllia Microstrip Package**

Description

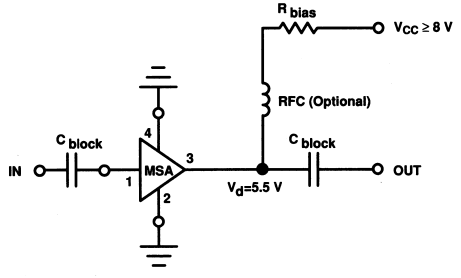
The MSA-1120 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic BeO disk package for good thermal characteristics. This MODAMP™ MMIC is designed for high dynamic range in either 50 or 75 Ω systems by combining low noise figure with high IP_3. Typical applications include narrow and broad band linear amplifiers in industrial and military applications.

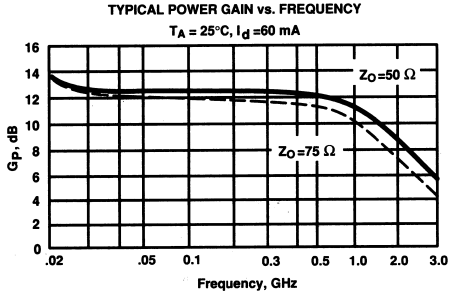
The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

200 mil BeO Package



Typical Biasing Configuration





Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 60 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB	11.5	12.5	13.5
ΔG_P	Gain Flatness	f = 0.1 to 1.0 GHz	dB		±0.7	±1.0
$f_{3\,dB}$	3 dB Bandwidth[2]		GHz		1.6	
VSWR	Input VSWR	f = 0.1 to 1.5 GHz			1.7:1	
	Output VSWR	f = 0.1 to 1.5 GHz			1.9:1	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 0.5 GHz	dBm	16.0	17.5	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		3.5	4.5
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		30.0	
t_D	Group Delay	f = 0.5 GHz	psec.		200	
V_d	Device Voltage		V	4.5	5.5	6.5
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes: 1. The recommended operating current range for this device is 40 mA to 75 mA. Typical performance as a function of current is on the following page.
2. Referenced from 50 MHz gain (Gp).

MSA-1120 MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	100 mA
Power Dissipation[2,3]	650 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

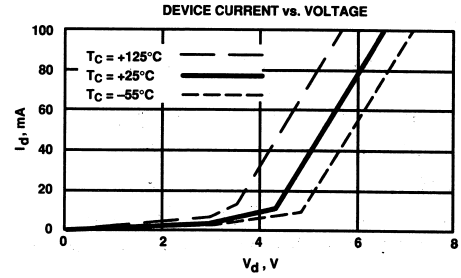
Thermal Resistance[2,4]: θ_{jc} = 60°C/W

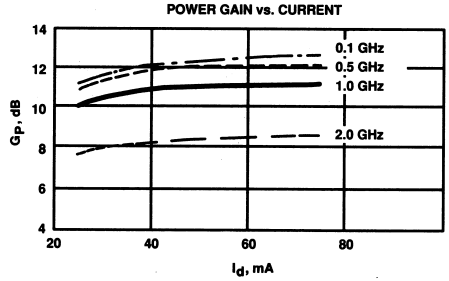
Notes:

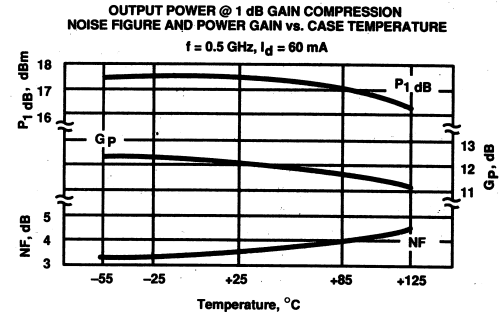
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 16.7 mW/°C for T_C > 161°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

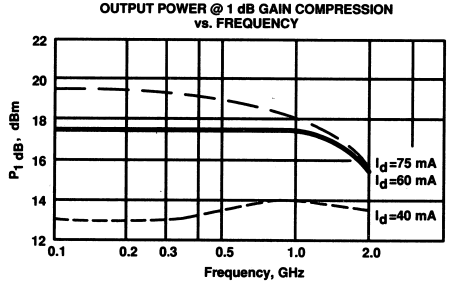
Typical Performance, T_A = 25°C, Z_O = 50 Ω

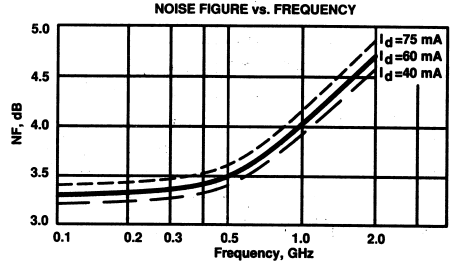
(unless otherwise noted)











Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 60 mA

Freq.	S11		S21			S12			S22		
MHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.5	.78	–21	19.6	9.53	168	–25.1	.057	50	.79	–21	0.51
5.0	.19	–72	13.8	4.91	165	–16.8	.144	11	.19	–72	0.98
25.0	.05	–56	12.9	4.44	174	–16.5	.149	3	.06	–75	1.08
50.0	.04	–52	12.5	4.23	174	–16.1	.156	2	.04	–79	1.08
100.0	.04	–56	12.5	4.22	172	–16.2	.155	1	.04	–78	1.09
200.0	.05	–72	12.4	4.19	165	–16.1	.157	1	.06	–91	1.08
300.0	.07	–84	12.4	4.15	158	–16.0	.159	2	.09	–101	1.07
400.0	.09	–96	12.3	4.10	151	–15.9	.161	2	.11	–109	1.06
500.0	.10	–105	12.1	4.04	144	–15.8	.163	3	.13	–117	1.05
600.0	.12	–113	12.0	3.98	137	–15.6	.166	3	.16	–124	1.04
700.0	.14	–120	11.8	3.89	131	–15.4	.169	2	.18	–130	1.03
800.0	.15	–127	11.6	3.80	124	–15.2	.173	2	.20	–136	1.01
900.0	.17	–134	11.4	3.71	118	–15.0	.178	1	.22	–142	1.00
1000.0	.19	–140	11.1	3.60	112	–14.8	.181	2	.24	–148	0.99
1500.0	.25	–167	9.8	3.10	83	–14.0	.200	–3	.31	–174	0.95
2000.0	.31	171	8.4	2.64	58	–13.3	.216	–10	.35	163	0.95
2500.0	.35	157	7.3	2.31	39	–12.8	.228	–16	.36	148	0.96
3000.0	.40	140	6.1	2.02	19	–12.5	.236	–23	.36	134	0.99

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MODAMP Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifier

Technical Data

MSA-2011

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 1.0 GHz**
- **Medium Power**
  P_{1dB}: 9 dBm at 1 GHz
- **High Gain**
  16.2 dB Typical at 1 GHz
- **Low Noise Figure**
  4.3 dB Typical at 1 GHz
- **Unconditionally Stable**
  (k > 1)
- **Low Cost Surface Mount Plastic Package**
- **Tape and Reel Packaging Option Available**

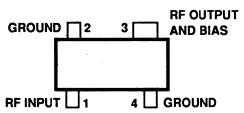
Description

The MSA-2011 is a low cost silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a surface mount plastic SOT-143 package. This MODAMP MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MODAMP MSA series is fabricated using a 10 GHz f_t, 25 GHz f_{max}, silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

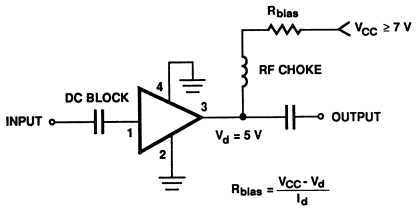
Note: The MSA-2011 replaces the HPMA-2011. Other packages are available.

Package Outline



Outline 143

Typical Biasing Configuration



Absolute Maximum Ratings[1]

Parameter	MSA-2011
Device Current	50 mA
Power Dissipation[2,3]	250 mW
RF Input Power	+20 dBm
Junction Temperature	150°C
Storage Temperature	-65 to 150°C

Thermal Resistance[2]: Θ_{ja} = 505°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.

Electrical Specifications, T_A = 25°C

I_D = 32 mA, Z_o = 50 Ω

Symbol	Parameters and Test Conditions		Unit	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		18.9	
		f = 0.5 GHz			18.1	
		f = 1.0 GHz		15.0	16.2	
ΔG_P	Gain Flatness	f = 0.1 to 0.5 GHz	dB		±0.4	
f_{3dB}	3 dB Bandwidth		GHz		1.0	
VSWR	Input VSWR	f = 0.1 to 3.0 GHz			1.3:1	
	Output VSWR	f = 0.1 to 3.0 GHz			1.4:1	
P_{1dB}	Power Output @ 1 dB Gain Compression:	f = 1.0 GHz	dBm		9.0	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		4.3	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		22	
t_d	Group Delay	f = 1.0 GHz	psec		143	
V_D	Device Voltage	T_C = 25°C	V	4.0	5.0	6.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		-9.3	

Note:
1. Refer to PACKAGING section, "Tape and Reel Packaging for Semiconductor Devices."

Typical Performance

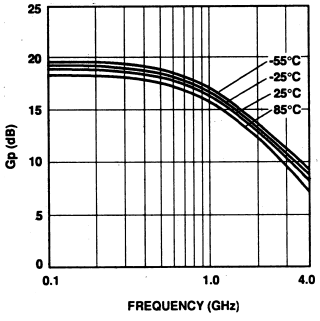


Figure 1. Power Gain vs. Frequency at Four Temperatures, I_D = 32 mA.

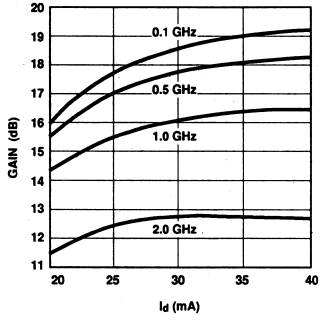


Figure 2. Power Gain vs. Current at 25°C.

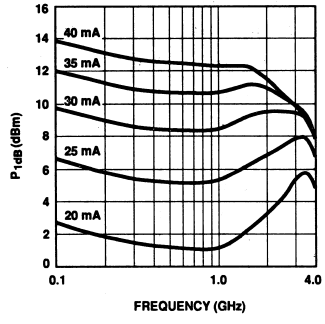


Figure 3. Typical P_{1dB} vs. Frequency at 25°C.

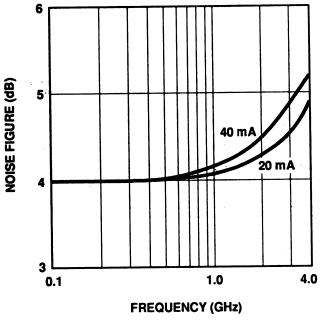


Figure 4. Noise Figure vs. Frequency at I_D = 32 mA..

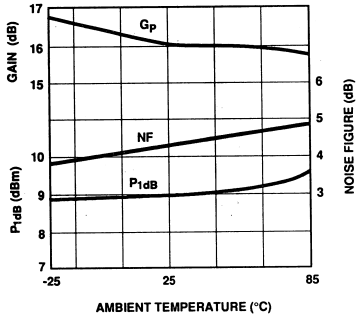


Figure 5. Power Gain, Noise Figure and P_{1dB} vs. Temperature at 1 GHz and I_D = 32 mA.

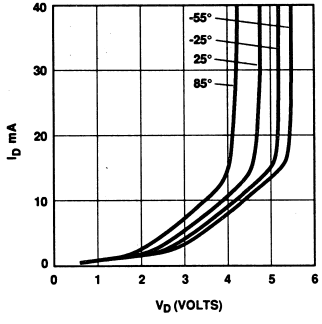


Figure 6. I_D vs. V_D at Four Temperatures.

Typical Scattering Parameters at $T_A = 25°C$

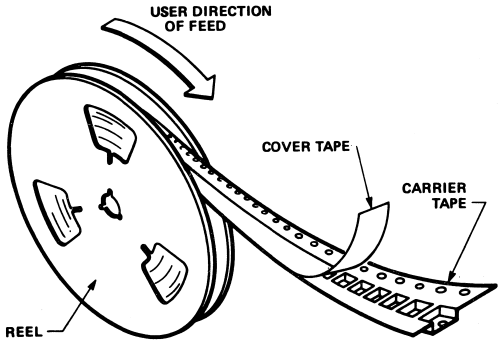
I_D = 32 mA, Z_o = 50 Ω

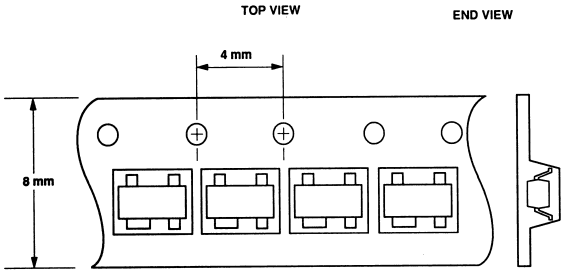
Frequency (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
0.1	0.05	7	18.9	8.81	172	-22.6	0.074	4	0.17	-13
0.2	0.05	9	18.8	8.73	165	-22.4	0.076	8	0.17	-23
0.3	0.06	3	18.6	8.52	157	-22.2	0.077	11	0.17	-34
0.4	0.06	1	18.3	8.25	150	-22.0	0.079	15	0.17	-43
0.5	0.06	0	18.1	8.00	143	-21.7	0.082	17	0.17	-52
0.6	0.07	-5	17.7	7.65	137	-21.4	0.085	20	0.17	-61
0.7	0.07	-8	17.3	7.33	131	-21.1	0.088	22	0.17	-68
0.8	0.08	-12	16.9	7.02	125	-20.7	0.092	24	0.17	-74
0.9	0.08	-18	16.3	6.70	120	-20.3	0.096	26	0.18	-80
1.0	0.08	-22	16.2	6.43	115	-20.0	0.100	28	0.18	-85
1.5	0.09	-46	14.3	5.16	93	-18.2	0.123	31	0.18	-102
2.0	0.11	-69	12.6	4.26	75	-16.7	0.146	31	0.17	-109
2.5	0.11	-93	11.2	3.64	59	-15.6	0.167	29	0.17	-111
3.0	0.12	-118	10.1	3.18	45	-14.7	0.185	26	0.18	-112
3.5	0.12	-152	9.1	2.85	31	-13.9	0.202	24	0.19	-116
4.0	0.15	174	8.1	2.55	18	-13.3	0.216	21	0.20	-124
4.5	0.22	147	7.4	2.33	5	-12.8	0.231	19	0.22	-133
5.0	0.30	127	6.5	2.11	-8	-12.2	0.246	17	0.25	-145
5.5	0.39	113	5.6	1.90	-20	-11.4	0.268	14	0.30	-157
6.0	0.45	100	4.5	1.68	-32	-10.7	0.292	10	0.35	-168

Part Number Ordering Information

Part Number	Devices per Reel	Reel Size
MSA-2011-TR1	3000	7"
MSA-2011-TR2	10000	13"

Conforms to Electronic Industries Standard RS-481, "Taping of Surface Mounted Components for Automated Placement." Standard Quantity is 3,000 Devices/Reel.

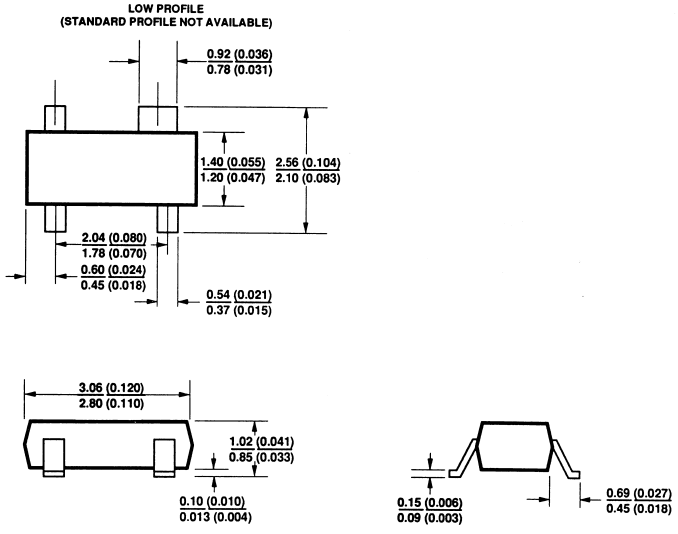




For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

Package Outline

Outline 143 (SOT-143)



ALL DIMENSIONS IN MILLIMETRES (INCHES).

HEWLETT PACKARD

MSA-2111
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

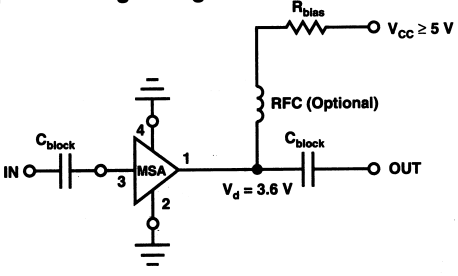
- **Cascadable 50 Ω Gain Block**
- **Medium Power: 10 dBm at 900 MHz**
- **High Gain: 16.5 dB Typical at 900 MHz**
- **Low Noise Figure: 3.3 dB Typical at 900 MHz**
- **Low Cost Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available[1]**

Description

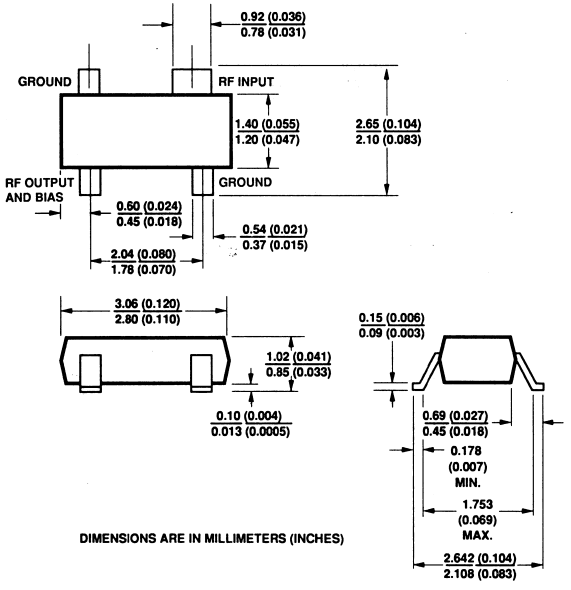
The MSA-2111 is a low cost silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a surface mount plastic SOT-143 package. This MODAMP™ MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

Typical Biasing Configuration



SOT-143 Package



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Electrical Specifications[2], $T_A = 25°C$

Symbol	Parameters and Test Conditions: $I_d = 29$ mA, $Z_O = 50\ \Omega$		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 900 MHz	dB	16.0	16.5	
ΔG_P	Gain Flatness	f = 0.1 to 0.3 GHz	dB		±0.5	
$f_{3\ dB}$	3 dB Bandwidth		GHz		0.5	
VSWR	Input VSWR	f = 0.1 to 2.5 GHz			1.8:1	
	Output VSWR	f = 0.1 to 2.5 GHz			1.8:1	
$P_{1\ dB}$	Output Power @ 1 dB Gain Compression	f = 900 MHz	dBm		10	
NF	50 Ω Noise Figure	f = 900 MHz	dB		3.3	
IP_3	Third Order Intercept Point	f = 900 MHz	dBm		20	
t_D	Group Delay	f = 900 MHz	psec.		158	
V_d	Device Voltage	$T_C = 25°C$	V	2.9	3.6	4.3
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes: 1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices."
2. The recommended operating current range for this device is 12 mA to 35 mA. Typical gain performance as a function of current is on the following page.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	35 mA
Power Dissipation[2, 3]	125 mW
RF Input Power	+13 dBm
Junction Temperature	150°C
Storage Temperature	-65 to 150°C

Thermal Resistance[2]: θ_{jc} = 505°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 2.0 mW/°C for T_C > 85°C.

Part Number Ordering Information

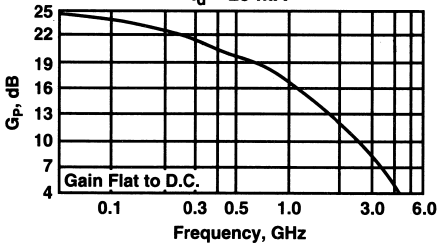
Part Number	Devices Per Reel	Reel Size
MSA-2111-TR1	3000	7"
MSA-2111-TR2	10000	13"

For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

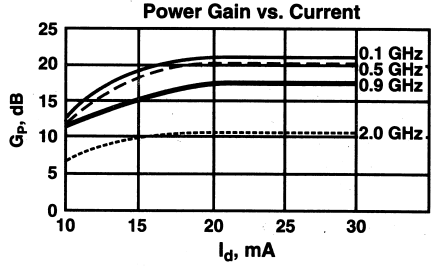
Typical Performance, T_A = 25°C

(Unless otherwise noted)

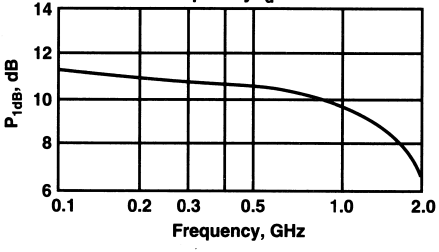
Power Gain vs. Frequency
I_d = 29 mA



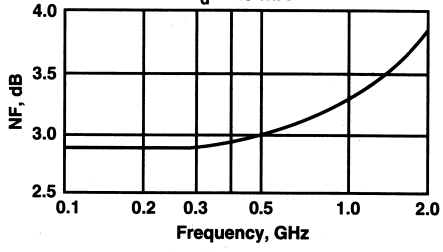
Power Gain vs. Current



Output Power @ 1 dB Gain Compression
vs. Frequency I_d = 29 mA



Noise Figure vs. Frequency
I_d = 29 mA



Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 29 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.1	.28	171	23.0	14.1	167	-26.0	.050	9	.27	177	1.03
0.2	.26	163	22.5	13.4	156	-25.5	.053	18	.27	175	1.03
0.3	.24	156	21.9	12.5	145	-24.9	.057	25	.26	173	1.03
0.4	.21	152	21.2	11.5	136	-24.0	.063	30	.26	171	1.03
0.5	.18	149	20.5	10.6	128	-23.4	.068	35	.24	170	1.03
0.6	.15	148	19.7	9.7	120	-22.6	.074	38	.24	169	1.03
0.7	.13	148	19.0	8.9	114	-21.8	.081	40	.22	169	1.04
0.8	.11	152	18.3	8.2	108	-21.1	.088	42	.21	169	1.04
0.9	.09	158	17.6	7.6	102	-20.4	.095	43	.20	168	1.04
1.0	.07	169	16.9	7.0	98	-19.9	.101	44	.19	169	1.05
1.5	.08	-123	14.0	5.0	79	-17.3	.136	45	.10	179	1.06
2.0	.11	-124	11.8	3.9	63	-15.5	.167	42	.06	-147	1.08
2.5	.15	-167	10.1	3.2	56	-14.3	.193	43	.06	-177	1.10
3.0	.27	158	8.3	2.6	43	-13.5	.211	38	.12	149	1.13
3.5	.38	145	6.8	2.2	32	-13.1	.222	34	.16	145	1.14
4.0	.46	135	5.6	1.9	21	-12.6	.234	30	.17	144	1.14

HEWLETT PACKARD

MODAMP Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifier

Technical Data

MSA-3111

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth: DC to 0.5 GHz**
- **Medium Power**
  P_{1dB}: 9 dBm at 1 GHz
- **High Gain**
  18.4 dB Typical at 1 GHz
- **Low Noise Figure**
  3.5 dB Typical at 1 GHz
- **Unconditionally Stable**
  (k > 1)
- **Low Cost Surface Mount Plastic Package**
- **Tape and Reel Packaging Option Available**

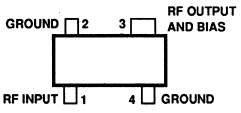
Description

The MSA-3111 is a low cost silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a surface mount plastic SOT-143 package. This MODAMP MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial and industrial applications.

The MODAMP MSA series is fabricated using a 10 GHz f_t, 25 GHz f_{max}, silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

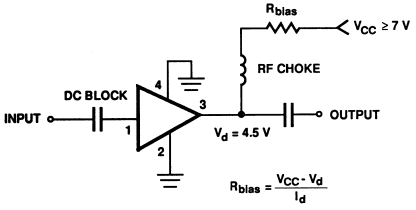
Note: The MSA-3111 replaces the HPMA-2111. Other packages are available.

Package Outline



Outline 143

Typical Biasing Configuration



Absolute Maximum Ratings[1]

Parameter	MSA-3111
Device Current	50 mA
Power Dissipation[2,3]	250 mW
RF Input Power	+20 dBm
Junction Temperature	150°C
Storage Temperature	-65 to 150°C
Thermal Resistance: Θ_{ja} = 505°C/W	

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.

Electrical Specifications, T_A = 25°C

I_D = 29 mA, Z_o = 50 Ω

Symbol	Parameters and Test Conditions		Unit	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz f = 0.5 GHz f = 1.0 GHz	dB	23.5	24.4 22.4 18.4	
ΔG_P	Gain Flatness	f = 0.1 to 0.5 GHz	dB		±0.5	
f_{3dB}	3 dB Bandwidth		GHz		0.5	
VSWR	Input VSWR Output VSWR	f = 0.1 to 3.0 GHz f = 0.1 to 3.0 GHz			1.2:1 1.2:1	
P_{1dB}	Power Ouptut @ 1 dB Gain Compression:	f = 1.0 GHz	dBm		9.0	
NF	50 Ω Noise Figure	f = 1.0 GHz	dB		3.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		23	
t_d	Group Delay	f = 1.0 GHz	psec		130	
V_D	Device Voltage	T_C = 25°C	V	4.0	4.5	6.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		-9.6	

Note:
1. Refer to PACKAGING section, "Tape and Reel Packaging for Semiconductor Devices."

Typical Performance

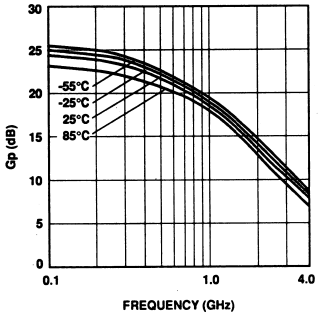


Figure 1. Power Gain vs. Frequency at Four Temperatures, I_D = 29 mA.

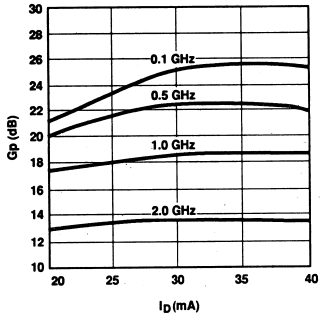


Figure 2. Power Gain vs. Current at 25°C.

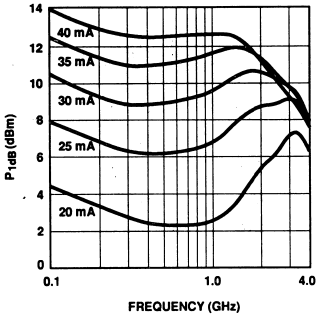


Figure 3. Typical P_{1dB} vs. Frequency at 25°C.

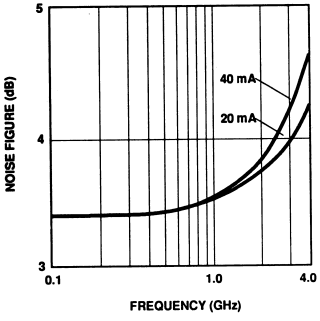


Figure 4. Noise Figure vs. Frequency at I_D = 29 mA..

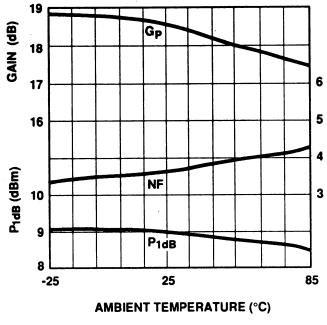


Figure 5. Power Gain, Noise Figure and P_{1dB} vs. Temperature at 1 GHz and I_D = 29 mA.

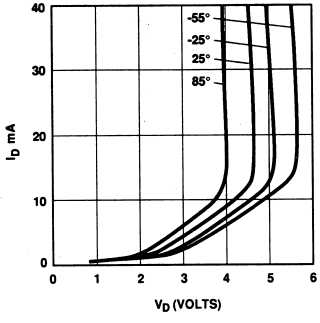


Figure 6. I_D vs. V_D at Four Temperatures.

Typical Scattering Parameters at $T_A = 25°C$

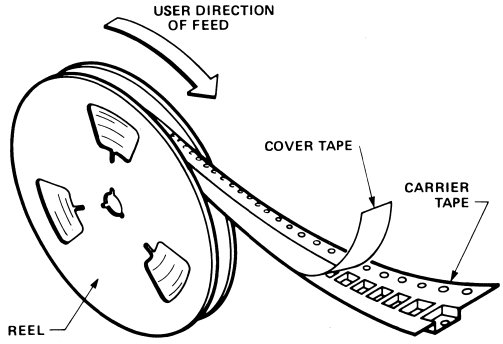
$I_D = 29$ mA, $Z_o = 50\ \Omega$

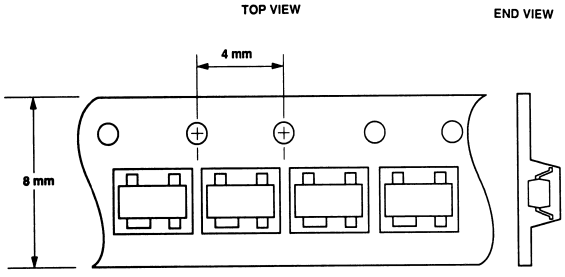
Frequency (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
0.1	0.05	3	24.4	16.53	167	-27.0	0.045	9	0.10	-23
0.2	0.06	4	24.0	15.83	156	-26.5	0.047	16	0.10	-41
0.3	0.07	-4	23.4	14.78	146	-26.0	0.050	23	0.10	-59
0.4	0.07	-8	22.7	13.59	136	-25.3	0.054	28	0.11	-72
0.5	0.07	-12	22.0	12.53	128	-24.6	0.059	33	0.11	-84
0.6	0.07	-18	21.1	11.41	121	-23.9	0.064	36	0.11	-94
0.7	0.07	-22	20.4	10.47	114	-23.1	0.070	39	0.11	-100
0.8	0.08	-26	19.7	9.63	109	-22.4	0.076	41	0.11	-106
0.9	0.08	-32	19.0	8.89	104	-21.7	0.082	42	0.11	-111
1.0	0.08	-35	18.4	8.27	99	-21.1	0.088	43	0.11	-114
1.5	0.08	-59	15.6	5.99	80	-18.5	0.118	44	0.11	-123
2.0	0.10	-79	13.4	4.69	65	-16.6	0.148	42	0.10	-122
2.5	0.10	-104	11.8	3.88	52	-15.2	0.175	38	0.11	-118
3.0	0.10	-129	10.4	3.31	39	-14.1	0.198	33	0.12	-114
3.5	0.12	-163	9.3	2.91	27	-13.2	0.219	28	0.12	-117
4.0	0.15	164	8.2	2.58	16	-12.6	0.236	23	0.13	-125
4.5	0.21	140	7.4	2.34	4	-12.1	0.250	18	0.13	-136
5.0	0.29	121	6.5	2.10	-7	-11.7	0.260	14	0.14	-148
5.5	0.36	109	5.6	1.90	-18	-11.3	0.271	10	0.17	-158
6.0	0.42	98	4.6	1.70	-28	-11.0	0.282	7	0.21	-165

Part Number Ordering Information

Part Number	Devices per Reel	Reel Size
MSA-3111-TR1	3000	7"
MSA-3111-TR2	10000	13"

Conforms to Electronic Industries Standard RS-481, "Taping of Surface Mounted Components for Automated Placement." Standard Quantity is 3,000 Devices/Reel.

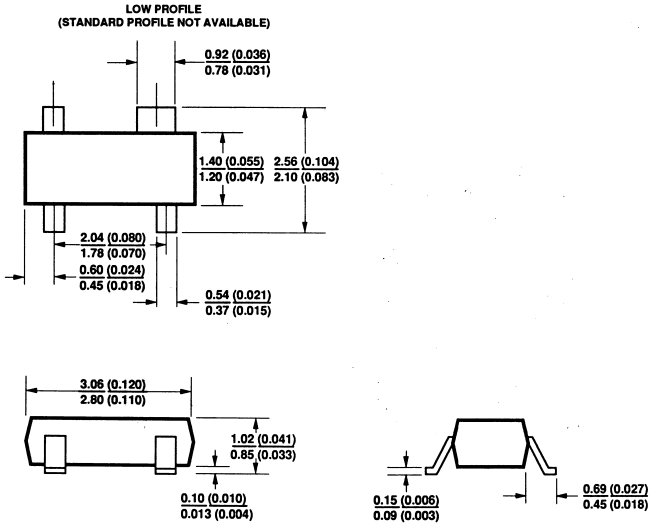




For more information, see "Tape and Reel Packaging for Semiconductor Devices", page 14-14.

Package Outline

Outline 143 (SOT-143)



ALL DIMENSIONS IN MILLIMETRES (INCHES).

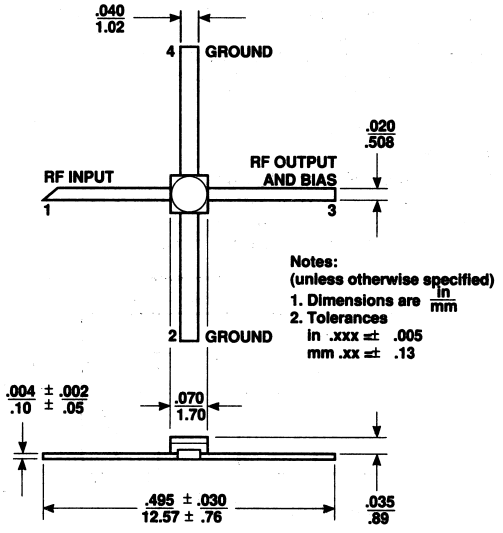
HEWLETT PACKARD

MSA-9970
MODAMP™ Cascadable Silicon Bipolar Monolithic Microwave Integrated Circuit Amplifiers

Features

- **Open Loop Feedback Amplifier**
- **Performance Flexability with User Selected External Feedback for:**
  - **Broadband Minimum Ripple Amplifiers**
  - **Low Return Loss Amplifiers**
  - **Negative Gain Slope Amplifiers**
- **Usable Gain to 6.0 GHz**
- **16.0 dB Typical Open Loop Gain at 1.0 GHz**
- **14.5 dBm Typical $P_{1\,dB}$ at 1.0 GHz**
- **Hermetic Gold-Ceramic Microstrip Package**

70 mil Package



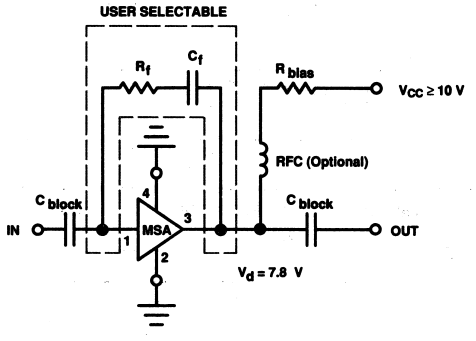
Description

The MSA-9970 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a hermetic high reliability package. This MODAMP™ MMIC is designed with high open loop gain and is intended to be used with external resistive and reactive feedback elements to create a variety of special purpose gain blocks.

Applications include very broadband, minimum ripple amplifiers with extended low frequency performance possible through the use of a high valued external feedback blocking capacitor; extremely well matched (–20 dB return loss) amplifiers; and negative gain slope amplifiers for flattening MODAMP MMIC cascades.

The MODAMP MSA-series is fabricated using a 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which utilizes nitride self-alignment, ion implantation and gold metallization to achieve excellent uniformity, performance, and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

Typical Biasing Configuration



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain[2] ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		17.5	
		f = 1.0 GHz		14.5	16.0	17.5
		f = 4.0 GHz		8.0	9.0	10.0
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression[2]	f = 1.0 GHz	dBm		14.5	
IP_3	Third Order Intercept Point[2]	f = 1.0 GHz	dBm		25.0	
V_d	Device Voltage		V	7.0	7.8	8.6
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–16.0	

Notes: 1. The recommended operating current range for this device is 25 mA to 45 mA. Typical performance as a function of current is on the following page.
2. Open loop value. Adding external feedback will alter device performance.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	750 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

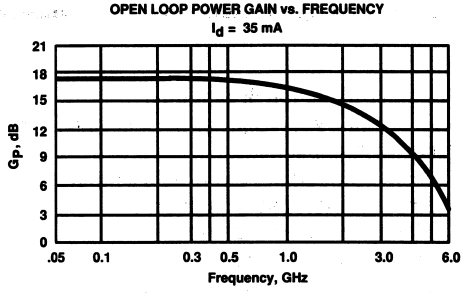
Thermal Resistance[2,4]: θ_{jc} = 150°C/W

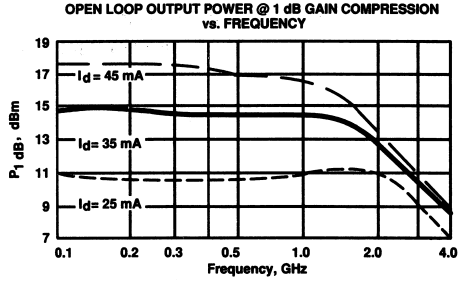
Notes:

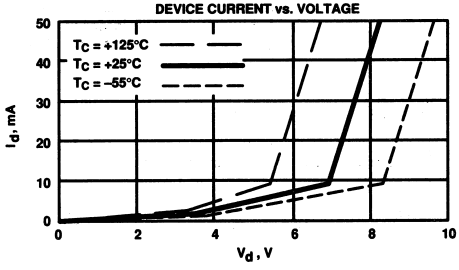
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 6.7 mW/°C for T_C > 88°C.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section "Thermal Resistance" for more information.

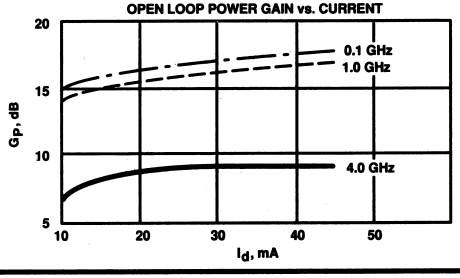
Typical Performance, T_A = 25°C

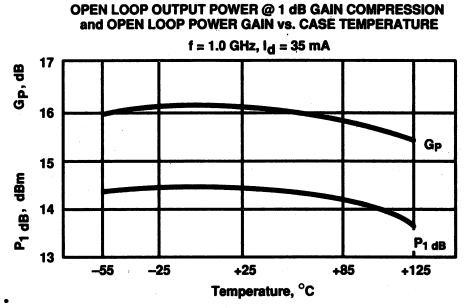
(unless otherwise noted)











Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, I_d = 35 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.02	.89	–1	17.5	7.51	179	–37.2	.014	4	.93	–1	1.01
0.05	.90	–3	17.5	7.47	177	–35.6	.017	34	.92	–3	.83
0.1	.90	–6	17.4	7.45	174	–33.2	.022	43	.93	–6	.70
0.2	.89	–12	17.4	7.43	168	–29.6	.033	61	.93	–13	.39
0.4	.87	–24	17.2	7.27	156	–24.4	.061	63	.91	–27	.24
0.6	.85	–36	17.0	7.06	145	–20.8	.091	58	.90	–40	.21
0.8	.82	–47	16.6	6.78	134	–18.8	.115	52	.87	–53	.21
1.0	.79	–59	16.2	6.49	124	–17.0	.141	44	.84	–66	.24
1.5	.72	–86	15.3	5.79	100	–14.6	.186	29	.74	–96	.28
2.0	.65	–113	14.2	5.10	77	–13.4	.215	16	.64	–123	.34
2.5	.59	–133	13.0	4.45	61	–12.9	.227	7	.57	–143	.39
3.0	.54	–155	11.6	3.79	42	–12.5	.236	–3	.51	–163	.46
3.5	.53	–174	10.3	3.28	26	–12.4	.239	–14	.45	178	.53
4.0	.52	168	9.2	2.87	10	–12.5	.238	–22	.39	164	.59
4.5	.53	152	8.0	2.51	–4	–12.6	.234	–30	.34	155	.66
5.0	.55	140	6.9	2.21	–17	–12.8	.228	–37	.31	153	.72
5.5	.55	130	5.8	1.94	–31	–13.2	.220	–44	.30	154	.80
6.0	.55	121	4.6	1.70	–43	–13.6	.209	–48	.32	157	.88
6.5	.56	114	3.5	1.50	–53	–13.8	.203	–54	.37	158	.94
7.0	.56	107	2.6	1.34	–63	–14.0	.201	–59	.42	157	.97

A model for this device is available in the DEVICE MODELS section.

HEWLETT PACKARD

MSF-86 Series
Silicon Bipolar MMIC
Frequency Converter

Features

- **Up or Down Frequency Conversion with up to 12 dB Conversion Gain**
- **RF Input from 0.1 to 2.0 GHz**
- **Low Phase Noise Self-Oscillating LO from 0.1 to 2.0 GHz Using External Tank Circuit**
- **Downconverted IF Output from DC to 0.5 GHz**
- **Uniform Performance**
- **Low Power Consumption per Function**
- **Low Cost per Function**
- **Low Bias Voltage**

Description

The MSF-86 Series is a family of silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) Frequency Converters. These MMIC's are characterized as simple, 2-port active mixers with low power injected LO. They can also function as self-oscillating active mixers.

The MSF-86 Series is ideally suited for very low cost or size constrained designs where adequate conversion gain flatness, LO-RF and LO-IF isolation or spurious signal rejection can be achieved using simple external filters.

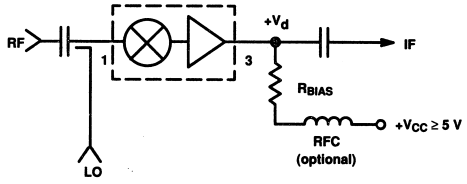
Typical applications include GPS navigation and INMARSAT receivers, mobile and cellular radio receivers, VHF/UHF converters, and communications and radar systems.

The MSF-86 Series is fabricated using a 10 GHz f_T silicon bipolar MMIC process that features sub-micrometer nitride self-alignment and ion-implantation to achieve excellent unit-to-unit uniformity. Biasing requires a fixed single polarity supply with an external current stabilizing resistor.

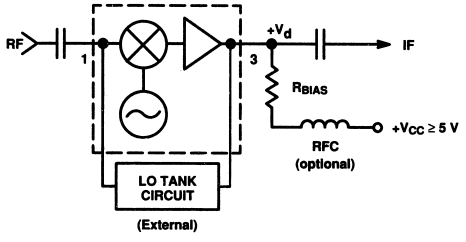
These MMIC's are offered in package styles suitable for industrial, military and commercial applications; model MSF-8635 is housed in a cost effective, glass sealed ceramic package, model MSF-8670 is in a high reliability, hermetically sealed gold-ceramic package, and model MSF-8685 is in a low cost, plastic package.

Functional Block Diagrams

2-Port Active Mixer



Self-Oscillating Mixer



Electrical Specifications, T_A = 25°C, I_d = 16 mA,[1] Z_O = 50 Ω
–20 dBm RF Input at 1.575 GHz and –8 dBm injected[2] LO at 1.4 GHz

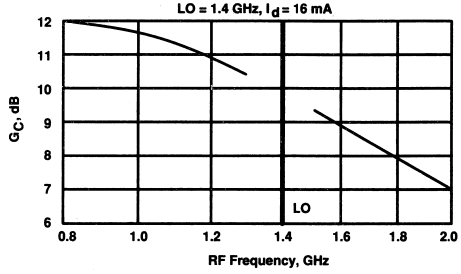
Symbol	Parameters/Test Conditions		Units	MSF-8635			MSF-8670			MSF-8685		
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
G_C	Conversion Gain at 0.175 GHz IF	f = 1.575 GHz	dB	7.5	9.0		7.5	9.0		6.0	8.0	
$P_{1\,dB}$	Output Power at 1 dB Compression	f = 0.175 GHz	dBm		–2.5			–2.5			–2.5	
IP_3	3rd Order Output Intercept Point	f = 0.175 GHz	dBm		7.0			7.0			7.0	
NF	Single-Side-Band Noise Figure	f = 1.575 GHz	dB		15.0			15.0			16.0	
VSWR	Input VSWR	f = 0.1 to 1.5 GHz	–		1.4:1			1.9:1			1.5:1	
	Output VSWR	f = 0.1 to 1.5 GHz	–		1.3:1			1.8:1			1.4:1	
V_d	Device Voltage		V	3.2	3.5	3.8	3.2	3.5	3.8	3.2	3.5	3.8
dV/dT	Device Voltage Temp. Coefficient		mV/°C		–8.0			–8.0			–8.0	

Notes: 1. The recommended operating range for this device is 12 mA to 25 mA. Typical performance as a function of current is on the following page.
2. For the 2-port active mixer application, the LO power is specified at port 1 of the MMIC.

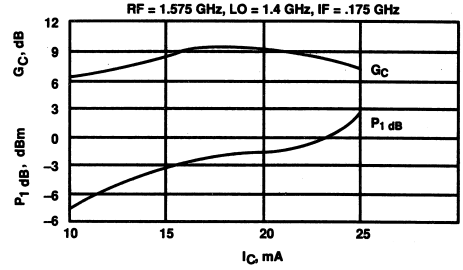
Typical Performance, T_A = 25°C

(unless otherwise noted)

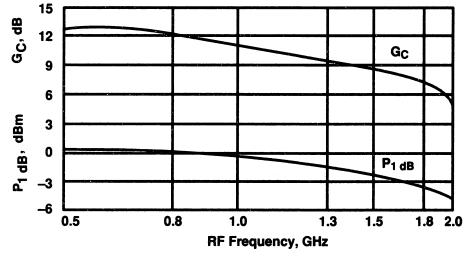
ACTIVE MIXER:
CONVERSION GAIN vs. RF FREQUENCY
LO = 1.4 GHz, I_d = 16 mA



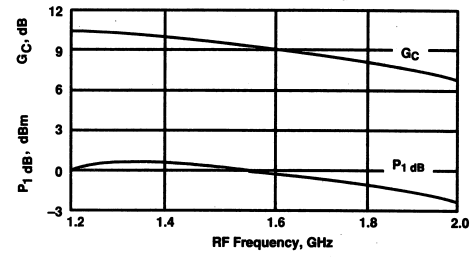
ACTIVE MIXER:
CONVERSION GAIN and OUTPUT POWER @ 1 dB
GAIN COMPRESSION vs. CURRENT
RF = 1.575 GHz, LO = 1.4 GHz, IF = .175 GHz



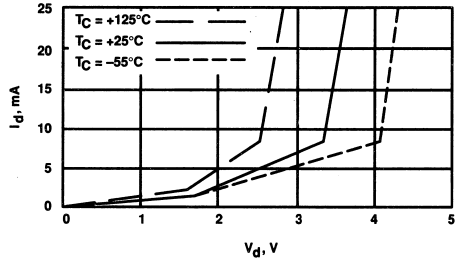
ACTIVE MIXER:
CONVERSION GAIN and IF OUTPUT POWER
@ 1 dB GAIN COMPRESSION vs. FREQUENCY
IF = 70 MHz with LOW-SIDE LO, I_d = 16 mA



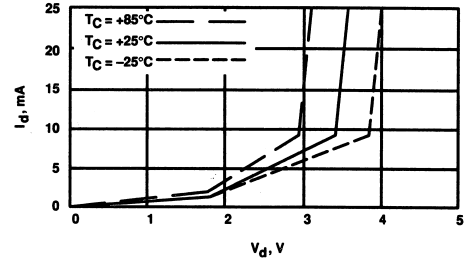
ACTIVE MIXER:
CONVERSION GAIN and IF OUTPUT POWER
@ 1 dB GAIN COMPRESSION vs. FREQUENCY
IF = 500 MHz with LOW-SIDE LO, I_d = 16 mA



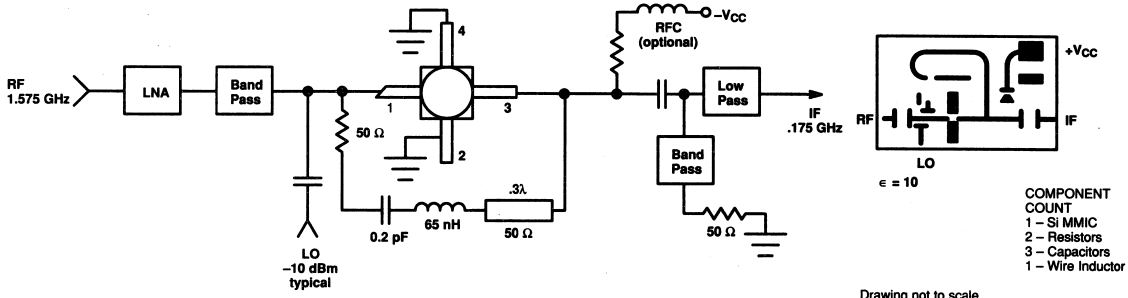
DEVICE CURRENT vs. VOLTAGE
MSF-8635, MSF-8670



DEVICE CURRENT vs. VOLTAGE
MSF-8685



EXAMPLE OF GPS DOWN CONVERTER USING MSF-86XX SERIES–CONVERSION GAIN = 8.5 dB AT 1.575 GHz WITH INJECTION-LOCKED SELF–OSCILLATING LO AT 1.4 GHz



COMPONENT
COUNT
1 – Si MMIC
2 – Resistors
3 – Capacitors
1 – Wire Inductor

Drawing not to scale
See AN-S005, "Using HP MSF Series Silicon Bipolar
MMIC Frequency Converters".

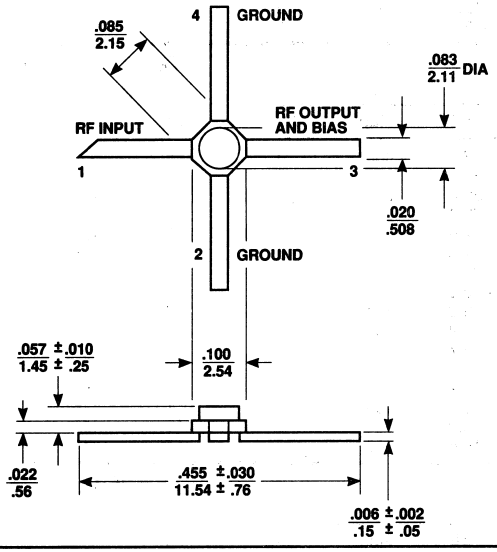
Absolute Maximum Ratings

Parameter	Absolute Maximum[1]		
	MSF-8635	MSF-8670	MSF-8685
Device Current	50 mA	50 mA	50 mA
Power Dissipation[2,4]	200 mW	200 mW	200 mW
RF Input Power	+20 dBm	+20 dBm	+20 dBm
Junction Temperature	200 °C	200 °C	150 °C
Storage Temperature	200 °C[3]	200 °C	150 °C
Thermal Resistance[4]	155 °C/W	130 °C/W	110 °C/W

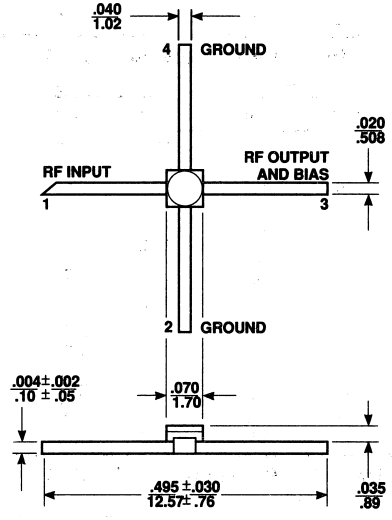
Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. Derate at 6.5 mW/°C for T_C > 169°C (MSF-8635); 7.7 mW/°C for T_C > 174°C (MSF-8870); 9.1 mW/°C for T_C > 128°C (MSF-8685).
3. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit.
4. T_{CASE} = 25°C.

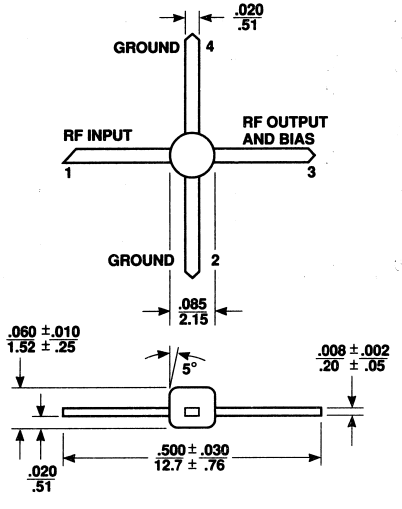
MSF-8635 micro-X package



MSF-8670 70 mil package



MSF-8685 85 mil plastic package



Notes:

1. Dimensions are in $\frac{\text{in}}{\text{mm}}$

2. Tolerances (unless otherwise specified)
   in: .xxx = ±.005
   mm: .xx = ±.13

Typical Scattering Parameters: MSF-8635

$T_A = 25°C$, $I_d = 16$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.1	.03	–178	20.5	10.59	171	–23.4	.068	5	.04	–44	1.05
0.2	.02	–177	20.3	10.31	161	–22.9	.071	8	.05	–68	1.04
0.3	.02	–164	20.0	9.96	152	–22.4	.076	14	.06	–87	1.04
0.4	.02	–116	19.6	9.55	144	–22.0	.079	19	.07	–104	1.03
0.5	.02	–100	19.2	9.08	136	–21.8	.081	21	.09	–114	1.04
0.6	.04	–89	18.7	8.59	128	–21.3	.086	24	.09	–123	1.04
0.8	.07	–96	17.7	7.66	115	–20.2	.098	29	.10	–140	1.03
1.0	.10	–108	16.6	6.79	103	–19.4	.107	31	.11	–156	1.02
1.5	.17	–134	14.2	5.13	79	–17.2	.138	30	.12	172	1.03
2.0	.24	–160	12.1	4.01	60	–15.8	.163	26	.12	148	1.04
2.5	.31	–178	10.3	3.26	48	–15.1	.175	27	.12	140	1.08
3.0	.37	166	8.7	2.72	34	–14.4	.190	24	.11	135	1.10
3.5	.42	151	7.4	2.33	21	–13.9	.203	19	.10	144	1.11
4.0	.46	139	6.2	2.04	9	–13.3	.216	16	.08	167	1.11
4.5	.48	126	5.1	1.81	–3	–12.8	.229	12	.08	–173	1.11
5.0	.52	110	4.2	1.62	–15	–12.2	.245	8	.09	–173	1.09

Typical Scattering Parameters: MSF-8670

$T_A = 25°C$, $I_d = 16$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.1	.05	–147	20.5	10.62	172	–23.3	.068	4	.05	–69	1.05
0.2	.07	–134	20.4	10.41	164	–23.0	.070	8	.09	–92	1.04
0.3	.09	–126	20.1	10.16	156	–22.6	.074	12	.13	–104	1.02
0.4	.11	–123	19.9	9.85	148	–22.4	.076	14	.16	–113	1.00
0.5	.13	–123	19.6	9.50	141	–22.0	.079	16	.20	–121	0.99
0.6	.15	–123	19.2	9.09	135	–21.8	.082	18	.22	–128	0.97
0.8	.19	–126	18.4	8.28	122	–20.7	.093	22	.25	–141	0.94
1.0	.24	–129	17.5	7.46	110	–19.8	.103	22	.27	–154	0.92
1.5	.31	–141	15.2	5.76	87	–18.2	.124	23	.27	–176	0.91
2.0	.38	–157	13.0	4.47	68	–17.2	.138	19	.24	166	0.94
2.5	.42	–167	11.1	3.59	57	–16.7	.146	20	.21	158	1.01
3.0	.46	178	9.5	2.97	45	–16.4	.152	16	.17	156	1.07
3.5	.48	173	7.9	2.49	33	–16.2	.155	11	.14	163	1.15
4.0	.48	164	6.6	2.13	22	–16.1	.156	9	.11	–175	1.27
4.5	.48	155	5.5	1.87	13	–15.9	.161	5	.11	–154	1.35
5.0	.48	143	4.5	1.67	3	–15.8	.163	3	.14	–141	1.46

Typical Scattering Parameters: MSF-8685

$T_A = 25°C$, $I_d = 16$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.1	.04	171	20.1	10.09	171	–22.5	.075	5	.04	–30	1.04
0.2	.02	–180	19.8	9.75	161	–22.4	.076	10	.05	–56	1.04
0.3	.02	–143	19.4	9.38	153	–22.2	.077	15	.07	–76	1.05
0.4	.03	–113	19.1	8.99	145	–21.8	.081	17	.08	–91	1.04
0.5	.05	–105	18.7	8.57	138	–21.3	.086	21	.10	–104	1.04
0.6	.07	–101	18.2	8.14	131	–20.7	.092	25	.11	–116	1.03
0.8	.10	–111	17.3	7.32	119	–19.7	.103	28	.13	–134	1.01
1.0	.13	–118	16.4	6.57	107	–18.8	.115	28	.14	–150	0.99
1.5	.21	–140	14.1	5.06	84	–17.1	.140	28	.15	180	1.00
2.0	.29	–163	12.0	3.98	65	–15.8	.163	26	.16	157	1.02
2.5	.34	–176	10.3	3.26	55	–15.2	.174	28	.16	150	1.06
3.0	.41	169	8.7	2.71	42	–14.8	.181	25	.15	143	1.10
3.5	.46	157	7.2	2.31	30	–14.2	.194	22	.13	144	1.11
4.0	.49	146	6.1	2.01	18	–13.8	.203	20	.10	156	1.13
4.5	.52	135	5.0	1.77	7	–13.4	.215	17	.09	173	1.14
5.0	.54	123	4.1	1.60	–3	–12.9	.226	15	.09	–178	1.14

HEWLETT PACKARD

MSF-88 Series
Silicon Bipolar MMIC
Frequency Converter

Features

- **Up or Down Frequency Conversion with up to 20 dB Conversion Gain**
- **RF Input from 0.5 to 8.0 GHz**
- **Low Phase Noise Self-Oscillating LO from 0.5 to 8.0 GHz Using External Tank Circuit**
- **Downconverted IF Output from DC to 2.0 GHz**
- **Uniform Performance**
- **Low Power Consumption per Function**
- **Low Cost per Function**

Description

The MSF-88 Series is a family of silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) Frequency Converters. These MMIC's are characterized as simple, 2-port active mixers with low power injected LO. They can also function as self-oscillating active mixers.

The MSF-88 Series is ideally suited for very low cost or size constrained designs where adequate conversion gain flatness, LO-RF and LO-IF isolation or spurious signal rejection can be achieved using simple external filters.

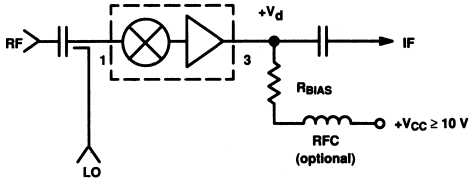
Typical applications include Satellite MATV and TVRO block converters, GPS navigation and INMARSAT receivers, mobile and cellular radio receivers, and communications and radar systems.

The MSF-88 Series is fabricated using a 10 GHz f_T silicon bipolar MMIC process that features sub-micrometer nitride self-alignment and ion-implantation to achieve excellent unit-to-unit uniformity. Biasing requires a fixed single polarity supply with an external current stabilizing resistor.

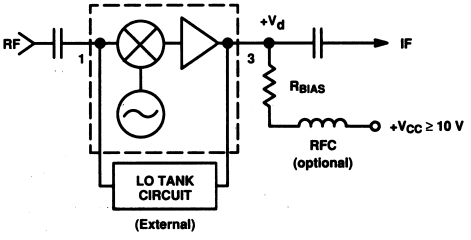
These MMIC's are offered in package styles suitable for industrial, military and commercial applications; model MSF-8835 is housed in a cost effective, glass sealed ceramic package, model MSF-8870 is in a high reliability, hermetically sealed gold-ceramic package, and model MSF-8885 is in a low cost, plastic package.

Functional Block Diagrams

2-Port Active Mixer



Self-Oscillating Mixer



Electrical Specifications, T_A = 25°C, I_d = 36 mA,[1] Z_O = 50 Ω
–20 dBm RF Input at 4.2 GHz and +5 dBm injected[2] LO at 5.15 GHz

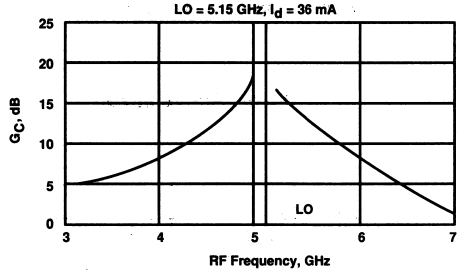
Symbol	Parameters/Test Conditions		Units	MSF-8835			MSF-8870			MSF-8885		
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
G_C	Conversion Gain at 0.95 GHz IF	f = 4.2 GHz	dB	7.5	9.0		7.5	9.0		7.0	8.5	
$P_{1\,dB}$	Output Power at 1 dB Compression	f = 0.95 GHz	dBm		9.0			9.0			9.0	
IP_3	3rd Order Output Intercept Point	f = 0.95 GHz	dBm		16.0			16.0			16.0	
NF	Single-Side-Band Noise Figure	f = 4.2 GHz	dB		12.0			12.0			13.0	
VSWR	Input VSWR	f = 0.5 to 5.0 GHz	–		2.3:1			2.3:1			2.5:1	
	Output VSWR	f = 0.5 to 5.0 GHz	–		2.0:1			2.0:1			2.0:1	
V_d	Device Voltage		V	7.0	7.8	8.4	7.0	7.8	8.4	7.0	7.8	8.4
dV/dT	Device Voltage Temp. Coefficient		mV/°C		–17.0			–17.0			–17.0	

Notes: 1. The recommended operating range for this device is 20 mA to 40 mA. Typical performance as a function of current is on the following page.
2. For the 2-port active mixer application, the LO power is specified at port 1 of the MMIC.

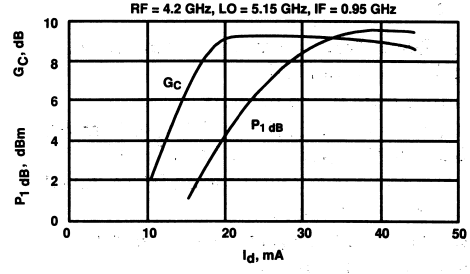
Typical Performance, T_A = 25°C

(unless otherwise noted)

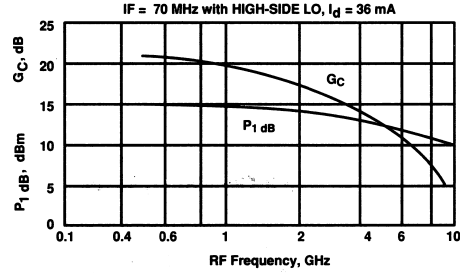
ACTIVE MIXER:
CONVERSION GAIN vs. RF FREQUENCY
LO = 5.15 GHz, I_d = 36 mA



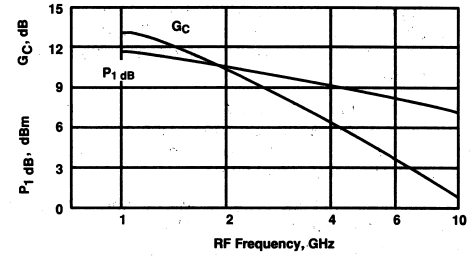
ACTIVE MIXER:
CONVERSION GAIN and OUTPUT POWER @ 1 dB
GAIN COMPRESSION vs. CURRENT
RF = 4.2 GHz, LO = 5.15 GHz, IF = 0.95 GHz



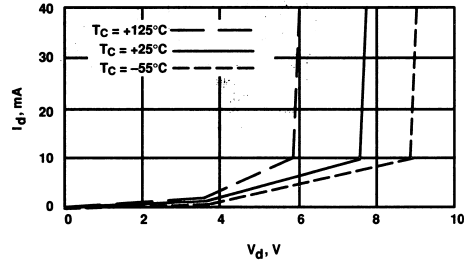
ACTIVE MIXER:
CONVERSION GAIN and IF OUTPUT POWER
@ 1 dB GAIN COMPRESSION vs. FREQUENCY
IF = 70 MHz with HIGH-SIDE LO, I_d = 36 mA



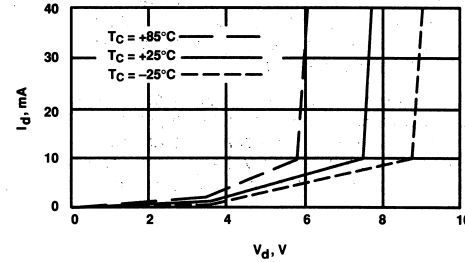
ACTIVE MIXER:
CONVERSION GAIN and IF OUTPUT POWER
@ 1 dB GAIN COMPRESSION vs. FREQUENCY
IF = 1.0 GHz with HIGH-SIDE LO, I_d = 36 mA



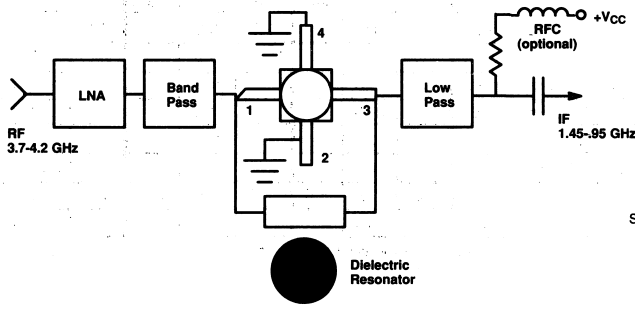
DEVICE CURRENT vs. VOLTAGE
MSF-8835, MSF-8870

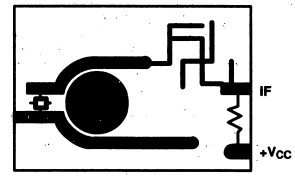


DEVICE CURRENT vs. VOLTAGE
MSF-8885



EXAMPLE OF TVRO BLOCK DOWN CONVERTER USING MSF-88XX SERIES–CONVERSION GAIN = 7.5 ± .5 dB FROM 3.7-4.2 GHz WITH SELF–OSCILLATING LO AT 5.15 GHz





COMPONENT COUNT
1 – SI MMIC
2 – PC Filters
1 – Resistor
1 – Capacitor
1 – Dielectric Puck

Drawing not to scale
See AN-S005, "Using HP MSF Series Silicon Bipolar MMIC Frequency Converters".

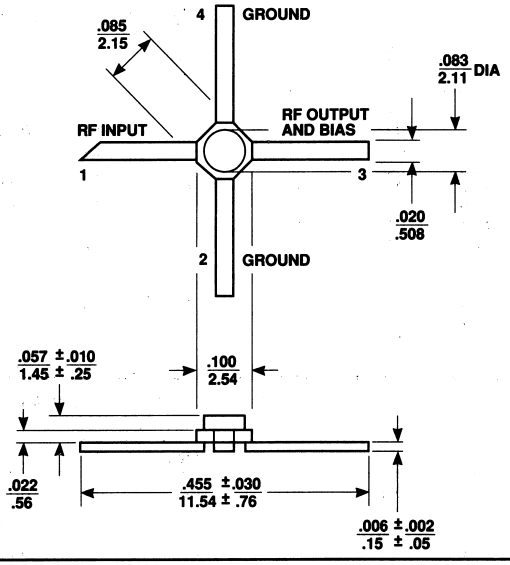
Absolute Maximum Ratings

Parameter	Absolute Maximum[1]		
	MSF-8835	MSF-8870	MSF-8885
Device Current	80 mA	80 mA	65 mA
Power Dissipation[2,4]	750 mW	750 mW	500 mW
RF Input Power	+20 dBm	+20 dBm	+20 dBm
Junction Temperature	200 °C	200 °C	150 °C
Storage Temperature	200 °C[3]	200 °C	150 °C
Thermal Resistance[4]	175 °C/W	150 °C/W	130 °C/W

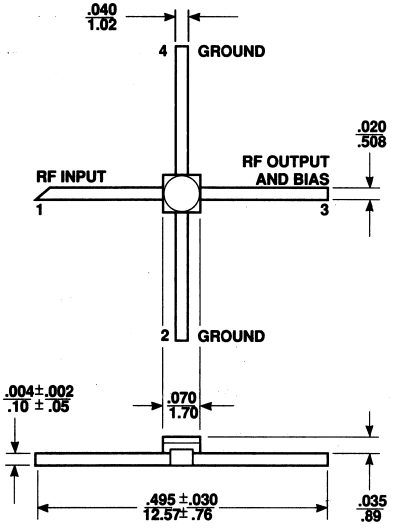
Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. Derate at 5.7 mW/°C for T_C > 69°C (MSF-8835); 6.7 mW/°C for T_C > 88°C (MSF-8870); 7.7 mW/°C for T_C > 85°C (MSF-8885).
3. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit.
4. T_{CASE} = 25°C.

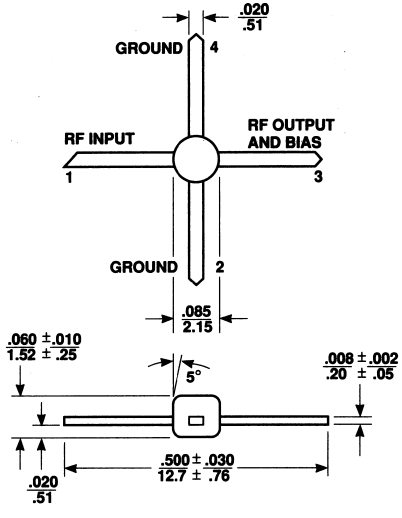
MSF-8835 micro-X package



MSF-8870 70 mil package



MSF-8885 85 mil plastic package



Notes:

1. Dimensions are in $\frac{\text{in}}{\text{mm}}$

2. Tolerances (unless otherwise specified)
   in: .xxx = ±.005
   mm: .xx = ±.13

Typical Scattering Parameters: MSF-8835

$T_A = 25°C$, $I_d = 36$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.1	.63	–17	32.5	42.02	161	–37.7	.013	55	.63	–19	0.72
0.2	.58	–33	31.5	37.52	145	–33.7	.021	47	.56	–37	0.73
0.4	.49	–56	29.1	28.50	119	–29.7	.033	54	.42	–66	0.72
0.6	.40	–70	26.7	21.54	103	–27.9	.040	55	.32	–84	0.78
0.8	.35	–80	24.6	17.01	92	–26.0	.050	53	.24	–98	0.85
1.0	.33	–89	22.9	13.98	82	–24.9	.057	52	.18	–107	0.89
1.5	.30	–111	19.5	9.45	64	–22.1	.079	51	.09	–126	0.95
2.0	.30	–133	16.9	7.03	48	–20.2	.098	44	.07	–141	0.99
2.5	.32	–150	14.9	5.53	39	–19.2	.110	42	.06	–166	1.04
3.0	.34	–170	13.2	4.56	26	–18.3	.122	36	.06	–106	1.06
3.5	.38	175	11.7	3.86	14	–17.5	.133	32	.08	–100	1.08
4.0	.39	162	10.5	3.33	2	–16.7	.146	27	.12	–101	1.08
5.0	.41	132	7.9	2.47	–21	–15.6	.165	19	.21	–113	1.10
6.0	.52	95	5.8	1.94	–45	–14.6	.187	7	.20	–149	1.05

Typical Scattering Parameters: MSF-8870

$T_A = 25°C$, $I_d = 36$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.1	.65	–19	32.5	42.04	161	–36.3	.015	40	.64	–22	0.78
0.2	.60	–35	31.5	37.54	145	–33.7	.021	47	.58	–43	0.66
0.4	.48	–60	29.1	28.49	122	–30.5	.030	51	.47	–74	0.64
0.6	.40	–76	26.8	21.90	108	–28.0	.040	50	.38	–97	0.72
0.8	.35	–88	24.9	17.48	97	–26.2	.049	50	.33	–113	0.78
1.0	.32	–102	23.4	14.85	87	–24.9	.057	51	.28	–128	0.83
1.5	.29	–118	20.1	10.14	70	–23.0	.071	47	.22	–151	0.91
2.0	.30	–133	17.6	7.55	56	–21.9	.081	45	.16	–167	0.98
2.5	.31	–139	15.6	6.01	49	–20.0	.100	46	.12	–172	1.02
3.0	.32	–149	13.8	4.87	39	–19.5	.106	41	.07	–170	1.11
3.5	.34	–158	12.2	4.09	28	–18.4	.121	35	.07	–143	1.12
4.0	.34	–168	10.8	3.48	17	–17.7	.131	31	.12	–112	1.16
5.0	.33	161	8.4	2.63	–3	–16.6	.147	21	.19	–103	1.26
6.0	.39	128	6.2	2.04	–22	–16.2	.155	10	.21	–115	1.36

Typical Scattering Parameters: MSF-8885

$T_A = 25°C$, $I_d = 36$ mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.1	.64	–21	32.5	42.29	160	–36.5	.015	40	.61	–24	0.78
0.2	.58	–39	31.3	36.89	144	–32.8	.023	50	.54	–45	0.67
0.4	.44	–65	28.7	27.20	120	–29.4	.034	54	.42	–77	0.69
0.6	.36	–82	26.3	20.57	106	–27.2	.044	53	.33	–98	0.77
0.8	.31	–95	24.3	16.31	96	–25.2	.055	53	.28	–115	0.83
1.0	.27	–105	22.5	13.36	87	–24.2	.061	51	.25	–129	0.87
1.5	.24	–125	19.3	9.24	71	–21.4	.085	50	.18	–153	0.96
2.0	.26	–147	16.7	6.82	56	–19.7	.103	47	.15	–173	0.98
2.5	.29	–159	14.9	5.57	48	–18.4	.120	44	.12	180	1.00
3.0	.34	–175	13.1	4.51	37	–17.7	.130	42	.09	165	1.03
3.5	.38	172	11.6	3.80	25	–16.9	.144	37	.06	172	1.04
4.0	.42	161	10.1	3.21	14	–16.3	.153	33	.04	–139	1.06
5.0	.48	135	7.7	2.43	–7	–15.6	.167	24	.09	–90	1.09
6.0	.60	102	5.5	1.88	–29	–14.9	.179	17	.08	–140	1.06

Gallium Arsenide Monolithic Microwave Integrated Circuits



Gallium Arsenide Microwave Monolithic Integrated Circuits

The high mobility of Gallium Arsenide can be put to use in MMICs as well as discrete devices, leading to families of high performance amplifiers and control MMICs. These devices are designed to work optimally in the 1 to 18 GHz frequency range, although operation to lower and higher frequencies is possible in individual offerings. In general these devices are targeted for specialty applications where excellent electrical performance is the primary consideration.

Processes

A number of processes are used to manufacture these devices.

- MESFET processes: Hewlett-Packard has a number of MESFET processes, variously optimized for gain, noise performance, or power.
- PHEMT process: MMICs processed using this technology are targeted for markets putting a premium on low noise figure and improved device-to-device consistency.
- Control Process: For devices such as switches and attenuators, a special process is used that provides more robust gate structures for higher power handling capability.

Product Families

The MGA family are high frequency amplifiers of various kinds. Included are general broad band traveling wave amplifier gain blocks (MGA-61100 and MGA-61000), low noise amplifiers (MGA-62100), partially matched FET cascades requiring external tuning for medium power applications (MGA-63100 and MGA-65100), and broad-band feedback amplifiers (MGA-64135 and MGA-66100) for commercial applications. The MGA-64135 is the only packaged offering in this family; the remaining products are supplied only in chip form.

The HMMC product line offers a variety of chip products. The HMMC-1001 is a voltage variable attenuator operational from DC to 50 GHz. The HMMC-5021, -5022, and -5026 are 2-22 and 2-26.5 GHz traveling wave amplifier MMICs. The HMMC-5008 and HMMC-5009 are single and dual output 2-8 GHz amplifiers with up to 24 dBm output power. The HMMC-2006 is a DC-6 GHz SPDT reflective switch.

The MGS family are single-pole double-throw switches designed for commercial applications. Both an absorptive version (MGS-71 series) and a reflective version (MGS-70 series A) are offered. Package options include SO-8 plastic surface mount and hermetic glass-metal packages. The very low current draw of these MMIC switches makes them a superior choice in applications where power consumption is a major concern. Operation is from DC to 6 GHz, depending on packaging.

These high performance MMICs are ideal for communications, instrumentation, and other commercial and military applications.

Gallium Arsenide Monolithic Microwave Integrated Circuits

General Purpose Amplifiers (Typical Specifications at +25°C Case Temperature)

Part Number	Bandwidth (GHz)	G_p (dB)	DG_p (dB)	NF (dB)	$P_{1\,dB}$ (dBm)	Package	Page
MGA-61000	2-18	7.0	0.5	6.0	+4.0	chip	9-25
HMMC-5021	2-22	8	1.0	5	21	chip	9-15
HMMC-5022*	2-22	9.5	1.0	5	21	chip	9-19
HMMC-5026*	2-26.5	9.5	1.0	5	21	chip	9-19
MGA-61100	6-18	7.0	0.5	6.0	+14.0	chip	9-28
MGA-66100	2-6	12.0	0.8	7.5	+12.0	chip	9-42
MGA-64135	2-6	12.0	0.8	7.5	+12.0	micro-X ceramic	9-37

Low Noise Amplifiers (Typical Specifications at +25°C Case Temperature)

Part Number	Optimum Freq. Range (GHz)	Test Freq. (GHz)	G_p (dB)	NF (dB)	P_{1dB} (dBm)	Package	Page
MGA-62100	2-14	4	14.0	2.5	+12.5	chip	9-31

Medium Power FET Cascades (Typical Specifications at +25°C Case Temperature)

Part Number	Optimum Freq. Range (GHz)	Test Freq. (GHz)	P_{1dB}[a] (dBm)	G_{1dB}[a] (dB)	Package	Page
MGA-63100	6-18	14	+22.0	10.5	chip	9-34
MGA-65100	2-18	14	+24.0	9.5	chip	9-39

Switches (Typical Specifications at +25°C Case Temperature)

Part Number	Optimum Freq. Range (GHz)	Type	Insertion Loss @ 1 GHz (dB)	Isolation @ 1 GHz (dB)	Switching Speed (ns)	IP_3 (dBm)	Package	Page
MGS-70008	DC-3.0	SPDT reflective	0.8	33	2	+45	SO-8	9-45
MGS-71008	DC-3.0	SPDT absorbtive	1.2	37	3	+45	SO-8	9-51
MGS-70018	DC-5.0	SPDT reflective	0.9	40	2	+45	180 mil SM	9-48
MGS-71018	DC-5.0	SPDT absorbtive	1.3	45	3	+45	180 mil SM	9-48
HMMC-2006	DC-6.0	SPDT reflective	0.7	45	1		chip	9-11

Attenuators (Typical Specifications at +25°C Case Temperature)

Part Number	Frequency (GHz)	Min Atten. (dB)	Max. Atten. (dB)	Input/Output Return Loss (dB)	Package	Page
HMMC-1001	DC-50	2.0	4.0	10	chip	9-4

Notes:
[a] Tuned measurement.
†Contact Sales Office.
•Standard Hi-Rel version available.

HEWLETT PACKARD

GaAs MMIC DC-50 GHz Voltage Variable Absorptive Attenuator

Technical Data

HMMC-1001

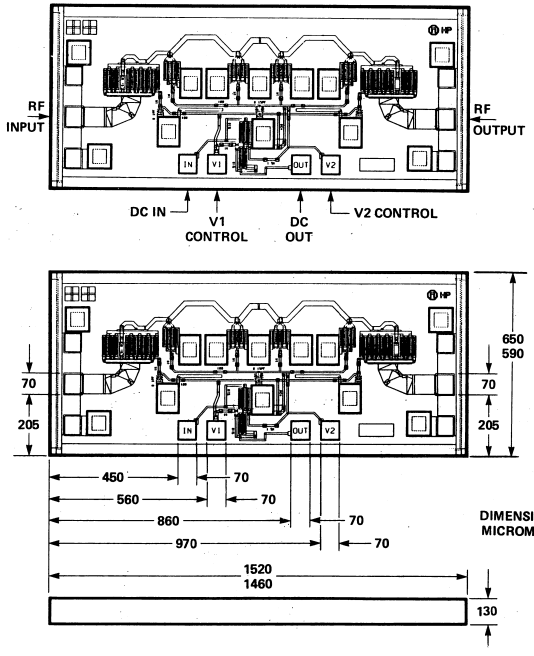
Features

- **Wide Attenuation Range >30 dB**
- **Exceptional Bandwidth DC – 50 GHz**
- **VSWR <2:1 Cascadable**
- **Very Low DC Power Dissipation <50 milliwatts**

Description

The HMMC-1001 GaAs MMIC attenuator is designed for wide dynamic attenuation range with excellent input/output match over the full DC to 50 GHz band. The circuit employs six MESFET devices as voltage variable resistors. A DC reference circuit, on chip, may be used for enhanced performance such as automatic impedance matching, linear attenuation, and temperature compensation. The chips have silicon nitride passivation and polyimide scratch protection.

Outline Drawing



Absolute Maximum Ratings* T_A = 25°C

Symbol	Parameters	Units	Min.	Max.
V_{RF}	DC Voltage to RF Ports	volts	-0.6	+5.0
V1,V2	Control Voltages	volts	-5.0	+0.5
V_{DC}	DC In/DC Out	volts	-0.6	+1.0
P_{IN}**	RF Input Power	dBm		+17
T_{CH}	Operating Channel Temperature	°C	-55	+140
T_{ST}	Storage Temperature	°C	-65	+165
T_{MAX}	Maximum Assembly Temperature (for 60 seconds maximum)	°C		+300

*Operation in excess of any one of these conditions may result in permanent damage to this device.

**Derate linearly to zero at maximum rated temperature.

Applications

The HMMC-1001 can be used as a voltage controlled attenuator in ECM, EW, radar, and telecommunication systems. The combination of wide attenuation range, low minimum attenuation, and flat frequency response, combined with excellent input/output match makes it useful in applications such as automatic gain control, amplitude and pulse modulation, and SPST switching.

Electrical Specifications

$T_A = 25°C$, $Z_O = 50\ \Omega$

Parameters	Frequency (GHz)	Units	Min.	Typ.	Max.
Minimum Attenuation (S21) V1 = 0 V, V2 = -4	1.5	dB		1.0	2.4
	8.0			1.4	2.4
	20.0			1.7	2.4
	26.5			2.0	2.4
Input/Output Return Loss V1 = 0 V, V2 = -4 V	<26.5	dB	10	16	
Maximum Attenuation (S21) V1 = –4 V, V2 = 0 V	1.5	dB	27	31	
	8.0		27	34	
	20.0		27	38	
	26.5		27	40	
Input/Output Return Loss V1 = –4 V, V2 = 0 V	<26.5	dB	8	>11	
DC Power Dissipation (does not include input signals)		mW			50
Input Power at 1 dB Attenuation Change	<26.5	dBm		0	

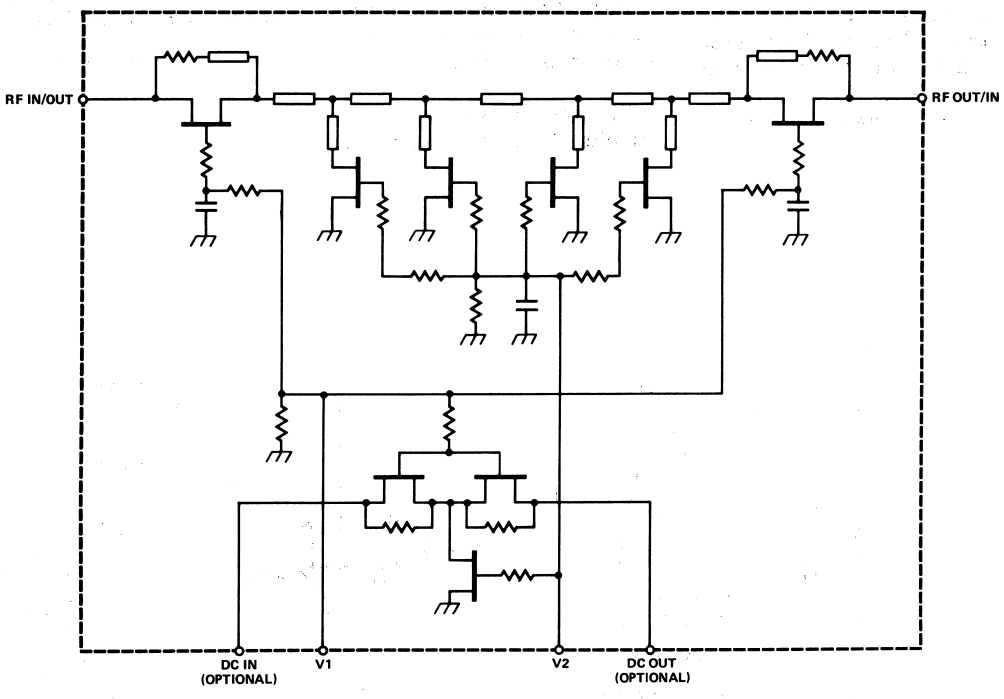


Figure 1. Schematic.

Operation

In the HMMC-1001 schematic (Figure 1) the six MESFETs in the RF signal path are in the configuration of a resistive TEE attenuator. The circuit is symmetrical, allowing either RF port to be the signal input or output. The attenuation level is set by the control voltages V1 (which controls the series resistors in the TEE) and V2 (which controls the shunt resistor in the TEE). Typical values for V1 and V2, chosen to provide optimum input and output VSWR, are shown in Figure 2. The DC_{IN} and DC_{OUT} terminals may be used with an external driver circuit (see below). If not used, these terminals may either be grounded or left open.

If operation from a single control voltage is desired, either one of two driver circuits may be used. The first is shown in Figure 3. An operation amplifier connected to the DC_{IN} and V1 terminals provides automatic input and output impedance matching by comparing the (nominal 500 Ω) resistance of the DC reference circuit to the value of R1. A second operational amplifier, connected to the DC_{OUT} and V2 terminals, provides linear attenuation settings from the single control voltage as shown in Figure 4. In this driver network, V_{REF} is typically set at –0.6 V and R1 is adjusted to achieve optimum return loss. The attenuation is then set at the desired level by varying V_{IN} between 0 and –2 V.

A simplified driver circuit is shown in Figure 5. Here, one of the operational amplifiers is eliminated and attenuation is set directly by varying the voltage at V2. The result is the attenuation vs. control voltage curve shown in Figure 6.

With either of these driver circuits, R1 and R2 are adjusted for best return loss. Nominal values for both are 420 Ω. For operation with either driver, the typical attenuation, return loss characteristics, and group delay are shown in Figures 7, 8 and 9 respectively.

Assembly Techniques

Solder die attach using an AuSn solder preform is recommended. Gold thermosonic wedge bonding is recommended for all wire bonds. The top and bottom metallization is gold. Other assembly methods may also be used. For more detailed information see HP Application Note #999 "GaAs MMIC Assembly and Handling Guidelines".

GaAs MMICs are ESD sensitive. Proper precautions should be used when handling these devices.

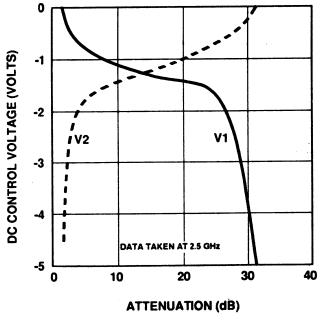


Figure 2. Typical DC Control Voltages.

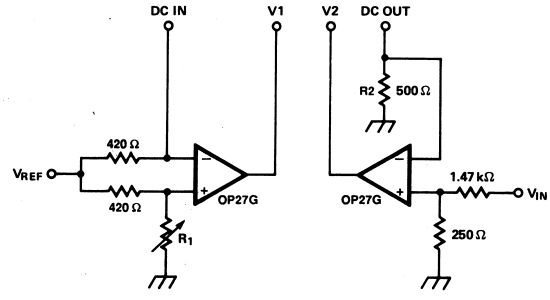


Figure 3. Linear Driver Circuit.

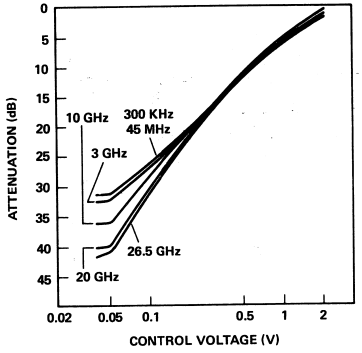


Figure 4. Typical Attenuation vs. Control Voltage (V_{IN}) for the Linear Driver Circuit.

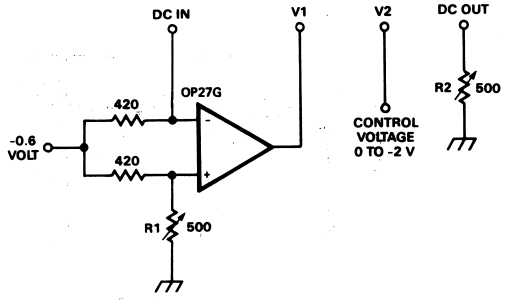


Figure 5. Simplified Driver Circuit.

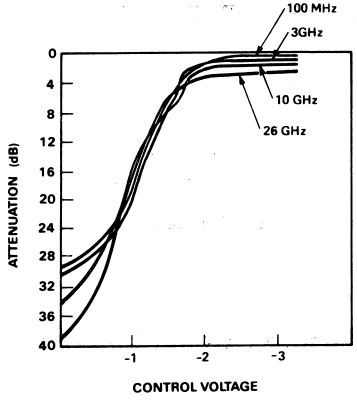


Figure 6. Typical Attenuation vs. Control Voltage (V_{IN}) Simplified Driver Circuit.

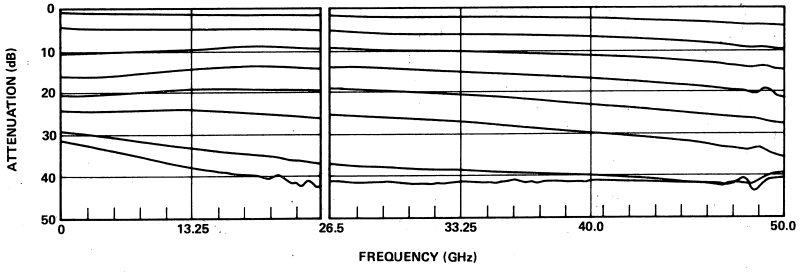


Figure 7. Typical Attenuation Characteristics.

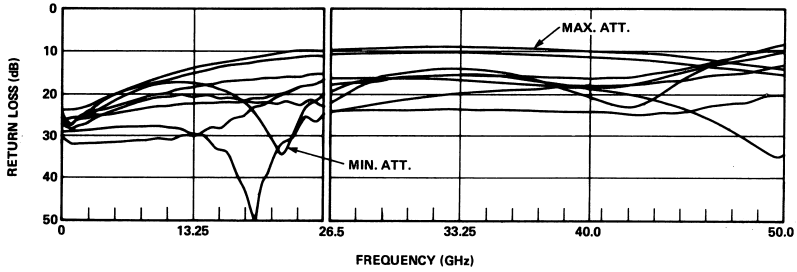


Figure 8. Typical Input and Output Return Loss.

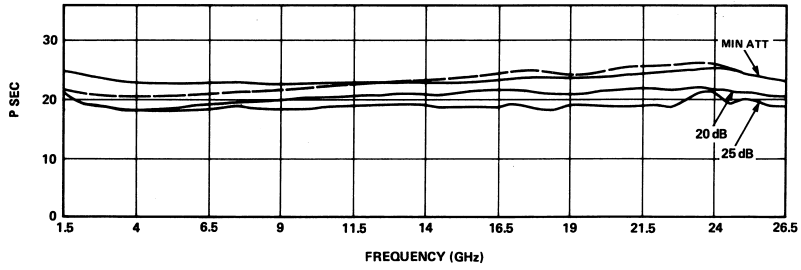


Figure 9. Typical Group Delay.

Typical S-Parameters at Various Attenuation Settings, T_A = 25°C

Minimum Attenuation Setting

Frequency (MHz)	S_{11}		S_{21}			S_{12}		S_{22}	
	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.
45	0.065	-11.0	-0.59	0.934	-1.0	0.932	-1.2	0.065	-12.5
100	0.056	-18.0	-0.72	0.921	-1.9	0.920	-1.8	0.058	-18.9
500	0.044	-30.4	-0.88	0.904	-5.1	0.903	-5.0	0.043	-30.0
1000	0.043	-45.3	-0.94	0.897	-9.3	0.896	-9.2	0.043	-46.5
2000	0.052	-71.0	-1.00	0.891	-17.7	0.891	-17.6	0.054	-71.3
4000	0.080	-105.8	-1.08	0.883	-34.5	0.883	-34.4	0.081	-104.9
6000	0.105	-131.1	-1.15	0.876	-51.2	0.876	-51.2	0.107	-127.9
8000	0.129	-154.7	-1.22	0.869	-67.8	0.866	-68.0	0.127	-151.1
10000	0.143	-176.5	-1.32	0.859	-84.6	0.860	-84.6	0.142	-171.6
12000	0.151	162.7	-1.37	0.854	-101.1	0.856	-101.0	0.144	168.7
15000	0.137	130.8	-1.39	0.852	-126.2	0.852	-126.4	0.130	138.7
18000	0.100	101.1	-1.45	0.846	-151.9	0.847	-152.0	0.095	106.8
22000	0.012	-5.1	-1.56	0.835	172.3	0.831	172.8	0.011	34.2
26000	0.091	-140.5	-1.97	0.797	137.0	0.794	135.9	0.093	-142.0

5dB Setting

Frequency (MHz)	S_{11} Mag.	S_{11} Ang.	S_{21} dB	S_{21} Mag.	S_{21} Ang.	S_{12} Mag.	S_{12} Ang.	S_{22} Mag.	S_{22} Ang.
100	0.081	-173.8	-5.08	0.557	-1.8	0.557	-1.8	0.083	-173.5
500	0.092	-175.0	-5.26	0.546	-5.3	0.545	-5.1	0.094	-175.2
1000	0.097	-176.9	-5.32	0.542	-9.4	0.541	-9.3	0.099	-175.9
2000	0.102	-178.0	-5.35	0.540	-17.9	0.539	-17.8	0.105	-176.3
4000	0.117	178.4	-5.43	0.535	-35.0	0.535	-34.9	0.120	-179.2
6000	0.134	170.1	-5.47	0.533	-52.0	0.532	-52.0	0.137	173.2
8000	0.153	158.0	-5.50	0.531	-69.1	0.530	-69.2	0.154	161.3
10000	0.166	143.5	-5.53	0.529	-86.4	0.530	-86.5	0.165	147.1
12000	0.172	126.9	-5.48	0.532	-103.8	0.531	-103.8	0.169	130.6
15000	0.162	98.7	-5.43	0.535	-130.9	0.534	-130.8	0.158	103.4
18000	0.128	66.6	-5.47	0.533	-159.3	0.532	-159.1	0.128	69.8
22000	0.055	-5.4	-5.80	0.513	161.4	0.514	161.3	0.055	-.7
26000	0.069	-131.1	-6.65	0.465	121.5	0.470	121.2	0.062	-132.2

10 dB Setting

Frequency (MHz)	S_{11} Mag.	S_{11} Ang.	S_{21} dB	S_{21} Mag.	S_{21} Ang.	S_{12} Mag.	S_{12} Ang.	S_{22} Mag.	S_{22} Ang.
45	0.067	-2.8	-10.1	0.314	-0.6	0.313	-0.8	0.061	-3.7
100	0.064	-6.5	-10.1	0.311	-1.7	0.310	-1.7	0.058	-8.3
500	0.056	-12.8	-10.4	0.303	-4.6	0.303	-4.4	0.050	-14.3
1000	0.053	-18.8	-10.4	0.301	-7.9	0.301	-7.8	0.048	-22.8
2000	0.053	-33.9	-10.4	0.301	-14.8	0.300	-14.8	0.049	-40.7
4000	0.056	-64.5	-10.4	0.302	-28.9	0.303	-28.9	0.056	-73.5
6000	0.059	-94.1	-10.3	0.307	-43.1	0.308	-43.1	0.064	-101.1
8000	0.062	-123.4	-10.0	0.316	-57.6	0.316	-57.8	0.070	-127.3
10000	0.063	-153.0	-9.71	0.327	-72.9	0.328	-72.9	0.072	-152.7
12000	0.062	177.8	-9.27	0.344	-89.0	0.343	-88.9	0.070	-178.0
15000	0.052	128.8	-8.66	0.369	-115.3	0.367	-115.2	0.054	140.4
18000	0.033	49.7	-8.25	0.387	-144.2	0.386	-144.5	0.029	64.2
22000	0.073	-77.1	-8.38	0.381	174.7	0.383	174.7	0.067	-75.2
26000	0.137	-127.7	-9.12	0.350	134.9	0.350	134.0	0.127	-129.8

15 dB Setting

Frequency (MHz)	S_{11} Mag.	S_{11} Ang.	S_{21} dB	S_{21} Mag.	S_{21} Ang.	S_{12} Mag.	S_{12} Ang.	S_{22} Mag.	S_{22} Ang.
45	0.093	-1.3	-15.0	0.178	-0.4	0.178	-0.7	0.086	-2.2
100	0.093	-3.7	-15.1	0.176	-1.6	0.176	-1.6	0.085	-4.5
500	0.086	-8.3	-15.2	0.173	-3.7	0.172	-3.5	0.078	-9.2
1000	0.085	-13.6	-15.3	0.172	-6.1	0.171	-6.0	0.077	-15.7
2000	0.085	-25.8	-15.2	0.173	-11.5	0.172	-11.4	0.078	-29.5
4000	0.086	-51.2	-15.0	0.177	-22.5	0.177	-22.5	0.082	-57.0
6000	0.087	-76.5	-14.6	0.187	-34.4	0.188	-34.4	0.088	-82.0
8000	0.087	-101.6	-14.0	0.200	-47.6	0.200	-47.7	0.092	-105.9
10000	0.085	-126.9	-13.3	0.216	-62.5	0.217	-62.6	0.093	-128.4
12000	0.080	151.6	-12.7	0.233	-78.9	0.234	-78.8	0.089	-150.3
15000	0.063	175.0	-11.8	0.256	-106.2	0.256	-106.3	0.072	-179.4
18000	0.034	159.6	-11.4	0.269	-136.0	0.268	-136.1	0.042	164.8
22000	0.047	-135.5	-11.6	0.262	-176.7	0.264	-176.7	0.044	-144.1
26000	0.099	-151.7	-12.4	0.241	144.0	0.241	142.6	0.090	-159.5

20 dB Setting

Frequency (MHz)	S_{11}		S_{21}			S_{12}		S_{22}	
	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.
45	0.070	-1.5	-20.0	0.100	-0.4	0.100	-0.5	0.063	-2.0
100	0.070	-4.0	-20.1	0.099	-1.4	0.099	-1.6	0.063	-5.1
500	0.065	-10.1	-20.2	0.097	-3.4	0.097	-3.1	0.057	-11.4
1000	0.065	-17.7	-20.2	0.097	-5.6	0.096	-5.4	0.058	-20.6
2000	0.067	-33.8	-20.2	0.097	-10.5	0.097	-10.6	0.061	-38.6
4000	0.075	-64.6	-19.9	0.101	-20.8	0.100	-20.8	0.073	-70.7
6000	0.085	-92.2	-19.5	0.106	-32.3	0.107	-32.3	0.088	-96.3
8000	0.095	-116.6	-18.9	0.114	-45.5	0.114	-45.7	0.101	-118.6
10000	0.105	-138.7	-18.3	0.122	-60.5	0.122	-60.7	0.111	-138.1
12000	0.112	-158.3	-17.8	0.129	-76.9	0.129	-76.8	0.119	-156.2
15000	0.116	176.9	-17.3	0.136	-103.3	0.136	-103.1	0.122	-178.9
18000	0.113	158.7	-17.2	0.138	-130.5	0.136	-130.5	0.119	161.6
22000	0.109	145.8	-17.7	0.131	-166.8	0.132	-167.9	0.112	145.1
26000	0.111	133.6	-18.6	0.117	155.6	0.117	155.2	0.117	131.6

25 dB Setting

Frequency (MHz)	S_{11}		S_{21}			S_{12}		S_{22}	
	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.
45	0.047	-2.1	-25.0	0.056	-0.5	0.056	-0.5	0.039	-3.1
100	0.047	-5.1	-25.2	0.055	-1.9	0.055	-1.6	0.040	-7.1
500	0.042	-15.3	-25.4	0.054	-4.0	0.054	-3.7	0.035	-18.2
1000	0.044	-27.1	-25.4	0.054	-7.0	0.054	-6.8	0.038	-32.1
2000	0.051	-49.1	-25.5	0.053	-13.2	0.053	-13.2	0.047	-56.1
4000	0.072	-82.8	-25.5	0.053	-25.5	0.053	-25.7	0.072	-88.0
6000	0.096	-106.9	-25.5	0.053	-38.7	0.054	-38.5	0.099	-109.4
8000	0.121	-126.4	-25.5	0.053	-51.8	0.054	-51.9	0.124	-127.5
10000	0.145	-144.3	-25.4	0.054	-66.1	0.054	-66.2	0.148	-143.6
12000	0.168	-160.4	-25.4	0.054	-80.9	0.054	-81.0	0.170	-158.7
15000	0.197	178.0	-25.7	0.052	-102.2	0.052	-103.3	0.196	-179.5
18000	0.219	158.6	-26.0	0.050	-123.4	0.049	-124.1	0.215	160.3
22000	0.243	136.4	-26.9	0.045	-153.2	0.045	-154.1	0.235	136.6
26000	0.259	112.6	-27.5	0.042	173.6	0.039	175.0	0.246	112.8

Maximum Attenuation Setting

Frequency (MHz)	S_{11}		S_{21}			S_{12}		S_{22}	
	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.
45	0.048	-2.0	-30.2	0.031	-0.6	0.031	-0.9	0.045	-2.7
100	0.048	-5.0	-30.2	0.031	-1.7	0.031	-2.2	0.044	-6.3
500	0.045	-15.6	-30.5	0.030	-5.7	0.030	-5.4	0.041	-17.1
1000	0.047	-27.9	-30.8	0.029	-10.4	0.029	-10.2	0.045	-31.0
2000	0.056	-50.0	-31.1	0.028	-19.3	0.028	-19.4	0.055	-53.8
4000	0.083	-82.0	-31.7	0.026	-35.4	0.026	-35.6	0.085	-84.4
6000	0.115	-104.8	-32.8	0.023	-49.2	0.024	-49.2	0.119	-105.3
8000	0.149	-123.3	-33.6	0.021	-61.4	0.021	-62.0	0.152	-123.1
10000	0.183	-139.9	-34.0	0.020	-73.3	0.020	-73.4	0.185	-138.9
12000	0.216	-155.4	-34.9	0.018	-84.0	0.018	-82.6	0.217	-153.8
15000	0.261	-176.7	-35.9	0.016	-97.3	0.016	-99.3	0.257	-174.9
18000	0.299	163.7	-36.5	0.015	-110.8	0.015	-112.3	0.292	165.2
22000	0.346	140.0	-38.4	0.012	-130.3	0.013	-134.5	0.331	140.4
26000	0.394	114.5	-38.4	0.012	-150.4	0.011	-147.2	0.359	114.7

HEWLETT PACKARD

GaAs MMIC SPDT Switch

Technical Data

HMMC-2006 (DC - 6 GHz)

Features

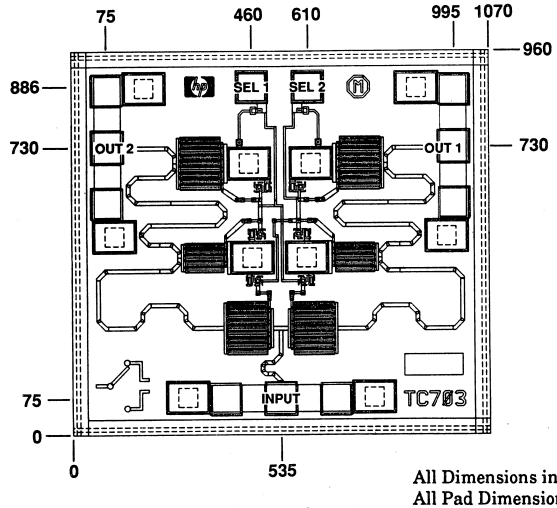
- **Broad Bandwidth:**
  DC - 6 GHz
- **Low Insertion Loss: 1 dB**
- **High Isolation:**
  60 dB at 300 MHz
  35 dB at 6 GHz
- **High P_{1dB}:**
  23 dBm at 50 MHz
  >27 dBm at 6 GHz
- **Low DC Power Dissipation**
- **Fast Switching: 1 nsec**

Description

The HMMC-2006 is a broadband, single-pole-double-throw (SPDT), reflective switch chip designed and fabricated using HP's GaAs MMIC process. It has low insertion loss and excellent input/output match to 50 ohms over the full DC to 6 GHz band. Quality, performance, and reliability are achieved through the use of MBE technology, TiPtAu metallization, silicon nitride passivation, and polyimide scratch protection. Gold-plated through-substrate vias provide the ground connection to the chip backside.

Applications

The HMMC-2006 is ideal for use in ECM, EW, radar, communications, and many other systems requiring SPDT switching. It can also be used as a terminated SPST (single pole single throw) switch by placing a 50Ω load on either RF output port.



Outline Drawing

All Dimensions in microns
All Pad Dimensions are
75 x 75 µm
Chip Thickness is 130 +/- 10 µm

Assembly Techniques

Epoxy die attach is recommended. The top and bottom metallization is gold. For bonding and other assembly methods see HP application note #999 "GaAs MMIC Assembly and Handling Guidelines".

GaAs MMICs are ESD sensitive. Proper precautions should be used when handling these devices.

RF Electrical Specifications, T_A = 25°C, Z_O = 50 Ω,
V_{sel} high = 0V, V_{sel} low = -10V

Symbol	Parameters	Units	Min.	Typ	Max.
BW	Guaranteed Operating Bandwidth	GHz	DC		6
I.L.	Insertion Loss, RF_{in} to RF_{out}, f=6 GHz	dB		.95	1.2
I_{so}	Isolation, RF Port to RF Port, f=6 GHz	dB	35	40	
$\|S_{11}\|$	Input Return Loss	dB	12	14	
$\|S_{22}\|$	Output Return Loss	dB	12	14	
P_{1dB}	Input Power Where I.L. Increases by 1dB, f=50 MHz	dBm	18	23	
t_S	Switching Speed, 10%-90% RF	nsec		1	

DC Electrical Specifications, T_A = 25°C

Symbol	Parameters	Units	Min.	Typ.	Max.
I_L	Leakage Current, V_{sel} = -10V	μA		80	200
V_P	Pinch Off Voltage @ 8.0 mA Max.	V	-6.75		-3.25

Absolute Maximum Ratings*

Symbol	Parameters	Units	Min.	Max.
V_{sel}	Select Voltages 1 and 2**	volts	-12.5	+2
P_{IN}	RF Input Power	dBm		30
T_{op}	Ambient Operating Temperature	°C	-55	+125
T_{stg}	Storage Temperature	°C	-65	+165
T_{max}	Maximum Assembly Temperature (for 60 seconds maximum)	°C		+200

*Operation in excess of any of these conditions may result in permanent damage to this device.
**V_{rf} (peak) + $\|V_{sel}$ min$\|$ <12.5 volts

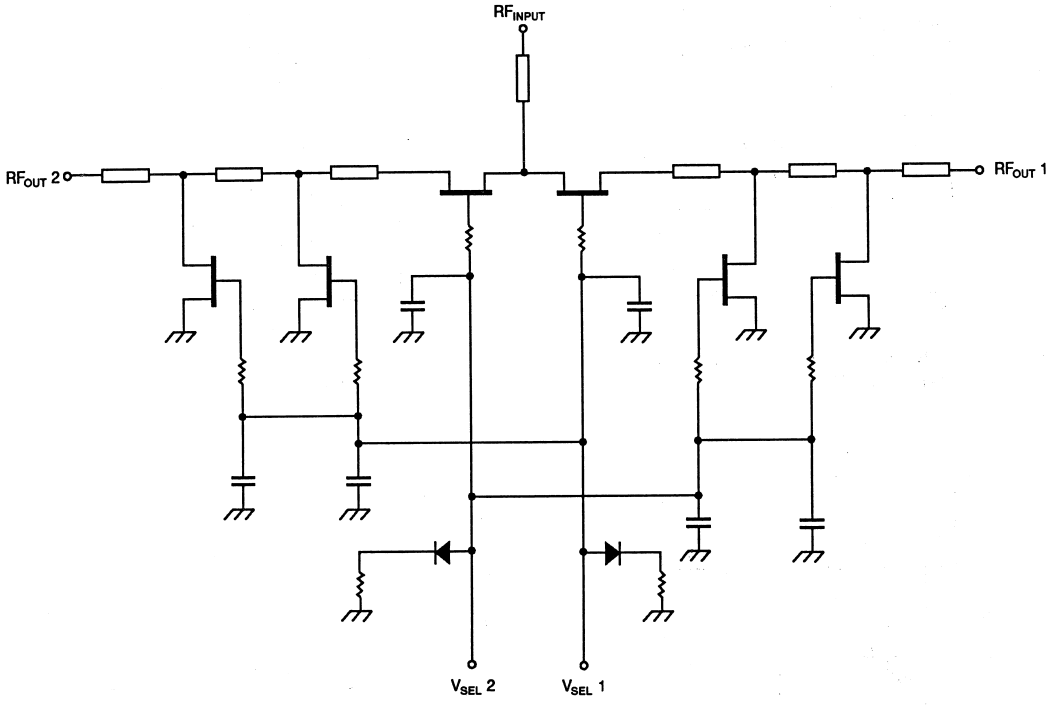


Figure 1. HMMC-2006 Simplified Schematic

Select Line		Input to	
$V_{sel}1$	$V_{sel}2$	$RF_{out}1$	$RF_{out}2$
low	high	off	on
high	low	on	off

low = -10 volts
high = 0 volts

Figure 2. Truth table for switch operation

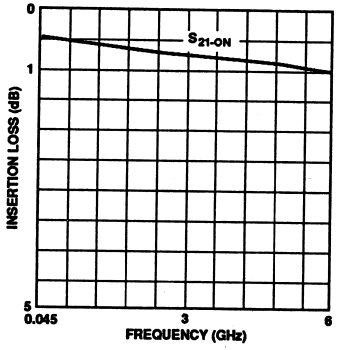


Figure 3. HMMC-2006 Typical Insertion Loss, RF_{INPUT} to RF_{OUT} 1 or RF_{OUT} 2.

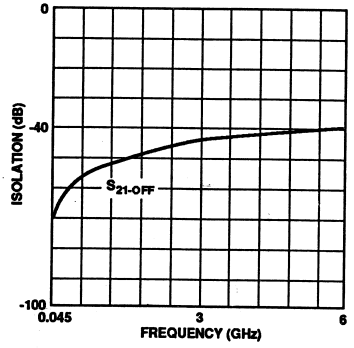


Figure 4. HMMC-2006 Typical Isolation

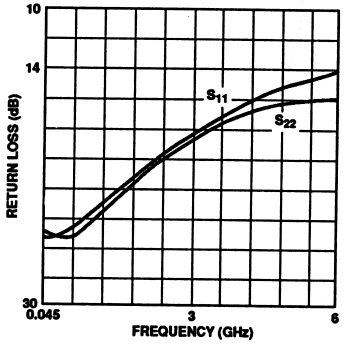


Figure 5. HMMC-2006 Typical Input and Output Return Loss, RF_{INPUT} and RF_{OUT} on.

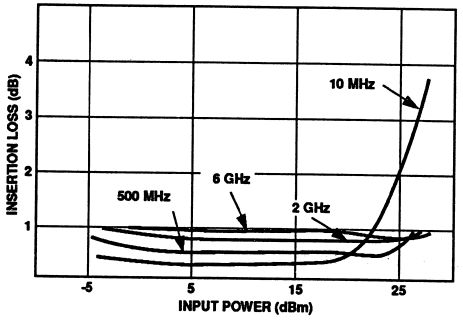


Figure 6. Typical Power Handling Characteristics

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GaAs MMIC Traveling Wave Amplifier

Technical Data

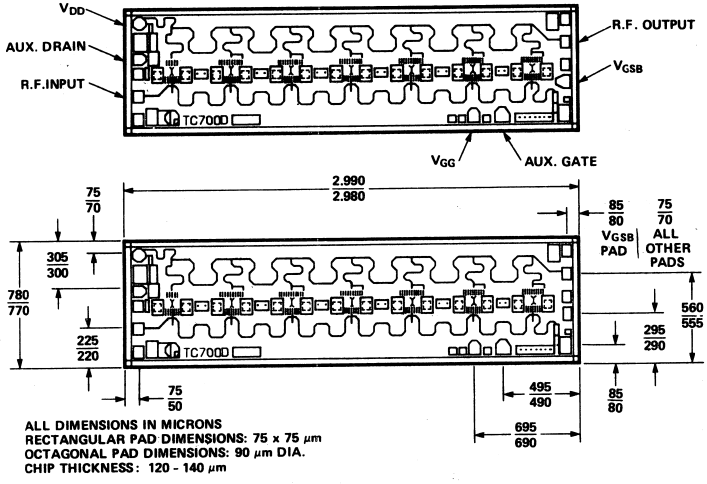
HMMC-5021 (2-22 GHz)

Features

- **Superior Bandwidth: 2-22 GHz**
- **Low VSWR: <1.5:1**
- **Flat Gain Response: ±1.0 dB Typical**
- **High Gain: 8.0 dB Typical**
- **Gain Control: 30 dB Range**
- **High P_{1dB}: 19 dBm at 22 GHz**

Description

The HMMC-5021 GaAs MMIC amplifier is designed for high gain and excellent input and output match to 50 ohms over the full specified band. This bandwidth is achieved through the use of 7 MESFET cascode gain stages. Advanced MBE technology, TiPtAu metallization, silicon nitride passivation, and polyimide scratch protection combine for superior performance and reliability. The backside of the chip is RF and DC ground. It is recommended that the RF input and output connections be made using a gold wire mesh.



Outline Drawing

Absolute Maximum Ratings, T_A = 25°C*

Symbol	Parameters	Min.	Max	Units
V_{DD}	Positive Drain Supply		8.0	volts
V_{GG}	Gate Bias	-5.0	0	volts
V_{GSB}	2nd Gate Bias	-2	+5	V
P_{IN}	RF Input Power		25	dBm
T_{CH}	Operating Channel Temperature	-55	150	°C
T_{st}	Storage Temperature	-65	165	°C
T_{max}	Maximum Assembly Temperature (for 60 seconds maximum)		300	°C
I_D	Drain Supply Current		250	mA
I_G	Gate Current		10	mA
P_{DC}	DC Power Dissipation		2.00	watts

*Operation in excess of any one of these conditions may result in permanent damage to this device.

Applications

The HMMC-5021 is designed for use as gain blocks in ECM, EW, radar, and communication systems. It is ideally suited for wideband applications requiring very flat gain response.

Operation

This amplifier is biased with a single drain supply, V_{DD}, and a single gate supply, V_{GG} (see Figure 1). The auxiliary gate and auxiliary drain can be used for extended low frequency response, however, proper external bypass circuitry is required (do not attempt to apply bias to these pads). The second gate can be used to obtain 30 dB (typical) dynamic range control. The auxiliary gate, auxiliary drain, and second gate should be left open when not in use.

Figure 2 shows a suggested bias schematic. A bypass capacitor C1 (>50 pF) and series inductor L1 (>4 nH) are required for the drain supply connection. DC blocking capacitors C2 and C3 are >50 pF. V_{GG} should be applied prior to V_{DD}. V_{GG} can then be adjusted to set I_D to the desired current (typ -0.3 V for I_D = 150 mA).

Assembly Techniques

Solder die attach using a AuSn solder preform is recommended. Gold thermosonic wedge bonding is recommended for all bonds. The top and bottom metallization is gold. Other assembly methods may also be used. For more detailed information see HP application note #999 "GaAs MMIC Assembly and Handling Guidelines."

GaAs MMICs are ESD sensitive. Proper precautions should be used when handling these devices.

RF Electrical Specifications, T_A = 25°C, V_{DD} = 7 V, I_D = 150 mA or I_{DSS} (whichever is less), Z_0 = 50 ohms

Symbol	Parameters	Typical	Units
BW	Guaranteed Operating Bandwidth	2-22	GHz
$\|S_{21}\|^2$	Small Signal Gain	8.0	dB
$\Delta\|S_{21}\|^2$	Small Signal Gain Flatness	±1	dB
P_{1dB}	Output Power at 1 dB Compression, f = 2 GHz	21	dBm
P_{1dB}	Output Power at 1 dB Compression, f = 22 GHz	19	dBm
$\|S_{11}\|$	Input Return Loss	18	dB
$\|S_{22}\|$	Output Return Loss	14	dB
$\|S_{12}\|^2$	Isolation	32	dB
NF	Noise Figure	8.0	dB
	Second Harmonic Level, P_o = 17 dBm, f = 6 GHz	-31	dBc
	Third Harmonic Level, P_o = 17 dBm, f = 6 GHz	-37	dBc
IP_2	2nd Order Intercept Point, f = 6 GHz	46	dBm
IP_3	3rd Order Intercept Point, f = 6 GHz	30	dBm

DC Electrical Specifications, T_A = 25°C,

Symbol	Parameters	Typical	Units
I_{DSS}	Saturated Drain Current, V_{DD} = 7 V, V_{GG} = 0 V	150	mA
θ_{ch-s}	Thermal Resistance, Channel to Substrate (at 116°C)	36	°C/W

HMMC-5021 (2-22 GHz)

Typical S-Parameters, T_A = 25°C, V_{DD} = 7 V, I_D = 150 mA or I_{DSS} (whichever is less)

Frequency (MHz)	S_{11}		S_{21}			S_{12}		S_{22}	
	Mag	Ang	Mag	Ang	dB	Mag	Ang	Mag	Ang
2000	0.103	-131.4	3.105	117.1	9.8	0.001	-177.7	0.013	122.0
2500	0.094	-139.5	3.025	106.9	9.6	0.001	-168.7	0.069	70.9
3000	0.092	-151.9	3.050	93.6	9.7	0.001	85.7	0.061	61.5
3500	0.084	-159.7	2.993	81.4	9.5	0.002	124.7	0.094	56.2
4000	0.079	-168.2	2.968	69.2	9.4	0.001	99.4	0.118	48.1
4500	0.073	-176.4	2.948	56.8	9.4	0.001	90.8	0.144	38.8
5000	0.065	176.6	2.939	44.4	9.4	0.002	74.2	0.162	28.1
5500	0.055	171.5	2.945	31.8	9.4	0.002	66.3	0.174	17.3
6000	0.044	170.0	2.934	19.0	9.3	0.002	52.0	0.187	7.2
6500	0.033	178.1	2.950	6.2	9.4	0.003	58.7	0.181	-4.9
7000	0.029	-168.6	2.944	-7.2	9.4	0.002	-4.3	0.186	-12.4
7500	0.032	-148.2	2.941	-20.5	9.4	0.001	10.7	0.180	-21.7
8000	0.041	-137.2	2.936	-33.8	9.4	0.002	42.9	0.162	-31.0
8500	0.055	-139.7	2.922	-47.4	9.3	0.002	2.5	0.155	-38.3
9000	0.066	-145.2	2.906	-60.7	9.3	0.003	-18.6	0.141	-51.4
9500	0.074	-150.9	2.889	-74.1	9.2	0.003	-24.4	0.116	-65.5
10000	0.077	-158.6	2.873	-87.6	9.2	0.003	-45.8	0.089	-79.1
10500	0.078	-166.3	2.860	-100.9	9.1	0.003	-42.7	0.056	-95.1
11000	0.074	-174.3	2.849	-114.2	9.1	0.004	-61.4	0.022	-129.3
11500	0.067	178.8	2.848	-127.8	9.1	0.004	-78.9	0.025	114.8
12000	0.057	176.4	2.851	-141.6	9.1	0.005	-70.2	0.056	84.3
12500	0.043	-175.7	2.839	-155.6	9.1	0.005	-83.4	0.089	65.6
13000	0.037	-157.2	2.824	-169.7	9.0	0.006	-98.4	0.118	48.3
13500	0.044	-133.9	2.805	176.1	9.0	0.006	-116.2	0.149	34.1
14000	0.062	-124.8	2.779	161.7	8.9	0.007	-119.5	0.171	21.4
14500	0.087	-127.2	2.744	147.4	8.8	0.009	-144.0	0.186	10.5
15000	0.110	-134.4	2.706	133.1	8.6	0.008	-162.7	0.194	-2.2
15500	0.131	-142.7	2.653	118.9	8.5	0.008	-170.1	0.196	-14.4
16000	0.148	-151.8	2.608	104.8	8.3	0.007	177.0	0.193	-26.8
16500	0.159	-161.1	2.567	90.8	8.2	0.008	159.1	0.187	-38.4
17000	0.162	-171.1	2.530	76.8	8.1	0.007	151.5	0.171	-50.3
17500	0.162	178.2	2.501	62.9	8.0	0.007	131.7	0.149	-62.9
18000	0.150	168.0	2.486	48.8	7.9	0.007	131.2	0.123	-72.7
18500	0.133	159.1	2.478	34.7	7.9	0.007	121.1	0.093	-84.5
19000	0.108	151.9	2.484	20.2	7.9	0.008	107.4	0.059	-98.0
19500	0.079	151.1	2.492	5.2	7.9	0.008	95.1	0.026	-104.2
20000	0.048	169.3	2.495	-10.4	7.9	0.010	85.3	0.015	21.8
20500	0.054	-146.1	2.490	-26.5	7.9	0.012	67.5	0.054	26.7
21000	0.089	-136.8	2.470	-42.7	7.9	0.014	48.9	0.094	16.7
21500	0.124	-139.1	2.442	-59.1	7.8	0.012	31.7	0.127	4.6
22000	0.159	-145.9	2.384	-75.8	7.5	0.013	15.1	0.156	-9.8

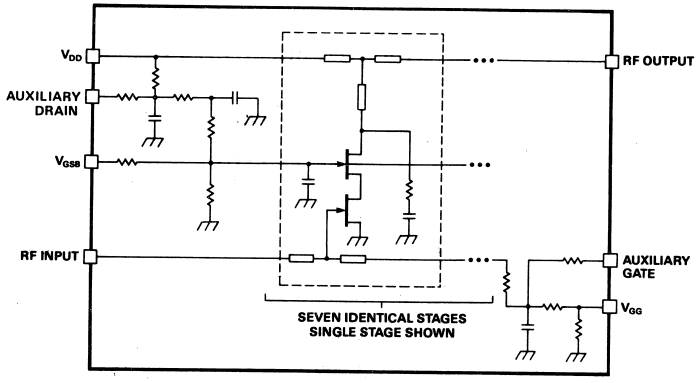


Figure 1. Simplified Schematic.

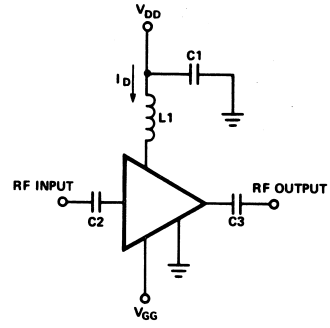


Figure 2. Suggested Bias Configuration.

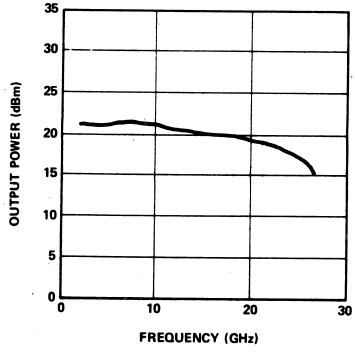


Figure 3. Typical Output Power at 1 dB Gain Compression vs. Frequency.

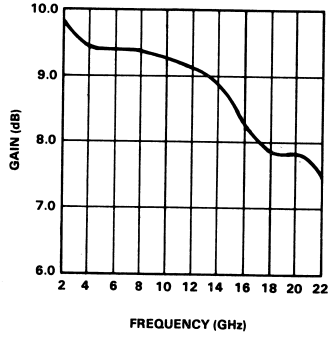


Figure 4. Typical Gain Response vs. Frequency at T_A = 25°C.

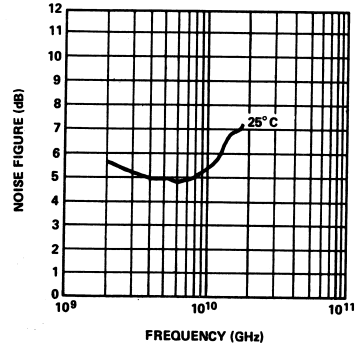


Figure 5. Typical Noise Figure vs. Frequency at T_A = 25°C (V_D = 7 V, I_D = 150 mA, Frequency = 18 GHz).

HEWLETT PACKARD

GaAs MMIC Traveling Wave Amplifiers

Technical Data

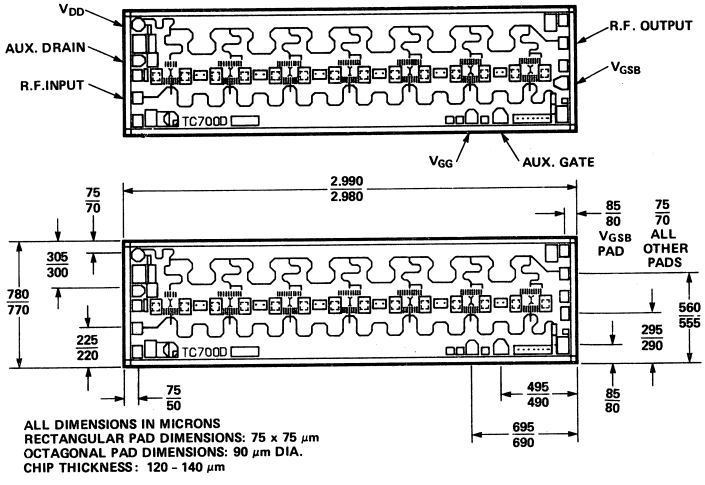
HMMC-5022 (2-22 GHz)
HMMC-5026 (2-26.5 GHz)

Features

- **Superior Bandwidth: 2-26.5 GHz**
- **Low VSWR: <1.5:1**
- **Flat Gain Response: ±1 dB**
- **High Gain: >8.5 dB**
- **Gain Control: 30 dB Range**
- **High P_{1dB}: 19 dBm at 22 GHz 15 dBm at 26.5 GHz**

Description

The HMMC-5022 and the HMMC-5026 GaAs MMIC amplifiers are designed for high gain and excellent input and output match to 50 ohms over the full specified band. This bandwidth is achieved through the use of 7 MESFET cascode gain stages. Advanced MBE technology, TiPtAu metallization, silicon nitride passivation, and polyimide scratch protection combine for superior performance and reliability. The backside of the chip is RF and DC ground. It is recommended that the RF input and output connections be made using a gold wire mesh.



Outline Drawing

Absolute Maximum Ratings, T_A = 25°C*

Symbol	Parameters	Min.	Max	Units
V_{DD}	Positive Drain Supply		8.0	volts
V_{GG}	Gate Bias	-5.0	0	volts
V_{GSB}	2nd Gate Bias	-2	+5	V
P_{IN}	RF Input Power		25	dBm
T_{CH}	Operating Channel Temperature	-55	150	°C
T_{st}	Storage Temperature	-65	165	°C
T_{max}	Maximum Assembly Temperature (for 60 seconds maximum)		300	°C
I_D	Drain Supply Current		250	mA
I_G	Gate Current		10	mA
P_{DC}	DC Power Dissipation		2.00	watts

*Operation in excess of any one of these conditions may result in permanent damage to this device.

Applications

The HMMC-5022 and HMMC-5026 are designed for use as gain blocks in ECM, EW, radar, and communication systems. They are ideally suited for wideband applications requiring very flat gain response.

Operation

These amplifiers are biased with a single drain supply, V_{DD}, and a single gate supply, V_{GG} (see Figure 1). The auxiliary gate and auxiliary drain can be used for extended low frequency response, however, proper external bypass circuitry is required (do not attempt to apply bias to these pads). The second gate can be used to obtain 30 dB (typical) dynamic range control. The auxiliary gate, auxiliary drain, and second gate should be left open when not in use.

Figure 2 shows a suggested bias schematic. A bypass capacitor C1 (>50 pF) and series inductor L1 (>4 nH) are required for the drain supply connection. DC blocking capacitors C2 and C3 are >50 pF. V_{GG} should be applied prior to V_{DD}. V_{GG} can then be adjusted to set I_D to the desired current (typ -0.3 V for I_D = 150 mA).

Assembly Techniques

Solder die attach using a AuSn solder preform is recommended. Gold thermosonic wedge bonding is recommended for all bonds. The top and bottom metallization is gold. Other assembly methods may also be used. For more detailed information see HP application note #999 "GaAs MMIC Assembly and Handling Guidelines."

GaAs MMICs are ESD sensitive. Proper precautions should be used when handling these devices.

RF Electrical Specifications, T_A = 25°C, V_{DD} = 7 V, I_D = 150 mA or I_{DSS} (whichever is less), Z_0 = 50 ohms

Symbol	Parameters	HMMC-5022			HMMC-5026			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
BW	Guaranteed Operating Bandwidth	2-22			2-26.5			GHz
$\|S_{21}\|^2$	Small Signal Gain	8.0	9.5		7.5	9.5		dB
$\Delta\|S_{21}\|^2$	Small Signal Gain Flatness			±1			±1	dB
P_{1dB}	Output Power at 1 dB Compression, f = 2 GHz	15	21		15	21		dBm
P_{1dB}	Output Power at 1 dB Compression, f = 22 GHz	15	19		15	19		dBm
P_{1dB}	Output Power at 1 dB Compression, f = 26.5 GHz				12	15		dBm
$\|S_{11}\|$	Input Return Loss	10	18		10	15		dB
$\|S_{22}\|$	Output Return Loss	10	14		10	14		dB
$\|S_{12}\|^2$	Isolation	20	32		20	30		dB
NF	Noise Figure		8.0			10.0		dB
	Second Harmonic Level, P_o = 17 dBm, f = 6 GHz		-31			-31		dBc
	Third Harmonic Level, P_o = 17 dBm, f = 6 GHz		-37			-37		dBc
IP_2	2 nd Order Intercept Point f = 6 GHz		46			46		dBm
IP_3	3rd Order Intercept Point, f = 6 GHz		30			30		dBm

DC Electrical Specifications, T_A = 25°C,

Symbol	Parameters	HMMC-5022			HMMC-5026			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{DSS}	Saturated Drain Current, V_{DD} = 7 V, V_{GG} = 0 V	110	150	250	110	150	250	mA
θ_{ch-s}	Thermal Resistance, Channel to Substrate (at 116°C)		36			36		°C/W

HMMC-5022 (2-22 GHz), HMMC-5026 (2-26 GHz)
Typical S-Parameters, T_A = 25°C, V_{DD} = 7 V, I_D = 150 mA or I_{DSS} (whichever is less)

Frequency (MHz)	S11		S21			S12		S22	
	Mag	Ang	dB	Mag	Ang	Mag	Ang	Mag	Ang
1500	0.135	-121.1	10.7	3.416	128.2	0.002	179.5	0.058	-34.3
2000	0.087	-134.8	10.3	3.255	118.6	0.002	154.9	0.024	14.4
2500	0.068	-144.8	10.1	3.198	107.7	0.001	112.0	0.048	52.7
3000	0.054	-164.3	10.0	3.155	96.3	0.002	105.3	0.081	55.7
3500	0.046	-162.1	9.9	3.135	84.4	0.002	93.3	0.109	49.0
4000	0.040	-173.6	9.9	3.126	72.4	0.002	79.9	0.137	42.6
4500	0.033	176.6	9.9	3.122	60.2	0.003	61.7	0.158	34.5
5000	0.026	163.8	9.9	3.125	47.8	0.003	57.4	0.177	26.0
5500	0.017	150.6	9.9	3.134	35.3	0.003	38.4	0.192	17.4
6000	0.009	125.0	10.0	3.146	22.6	0.004	23.5	0.202	7.5
6500	0.005	20.1	10.0	3.161	9.6	0.003	15.3	0.201	-1.4
7000	0.014	-41.8	10.0	3.171	-3.4	0.003	-7.8	0.201	-10.0
7500	0.025	-63.2	10.0	3.166	-16.7	0.003	0.3	0.197	-19.4
8000	0.037	-78.1	10.0	3.166	-29.9	0.004	-29.8	0.184	-29.6
8500	0.050	-91.7	10.0	3.161	-43.2	0.003	-34.8	0.168	-38.7
9000	0.060	-106.0	9.9	3.141	-56.6	0.004	-40.8	0.146	-48.9
9500	0.069	-118.3	9.9	3.125	-70.0	0.004	-48.8	0.121	-59.6
10000	0.076	-131.8	9.8	3.105	-83.3	0.004	-64.3	0.088	-69.3
10500	0.080	-146.2	9.8	3.077	-96.6	0.004	-75.8	0.053	-75.8
11000	0.081	-158.6	9.7	3.060	-109.9	0.005	-78.0	0.020	-74.4
11500	0.080	-170.8	9.7	3.042	-123.2	0.005	-91.6	0.021	57.4
12000	0.074	176.3	9.6	3.028	-136.5	0.006	-102.3	0.054	55.4
12500	0.063	161.0	9.6	3.017	-149.9	0.006	-113.5	0.087	46.0
13000	0.046	148.6	9.6	3.010	-163.4	0.007	-121.1	0.119	36.4

HMMC-5022 (2-22 GHz), HMMC-5026 (2-26 GHz), continued

Typical S-Parameters, T_A = 25°C, V_{DD} = 7 V, I_D = 150 mA or I_{DSS} (whichever is less)

Frequency (MHz)	S11		S21			S12		S22	
	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.
13500	0.028	136.3	9.6	3.003	-177.1	0.007	-133.0	0.144	24.5
14000	0.009	150.7	9.5	2.984	169.0	0.008	-151.8	0.164	13.4
14500	0.018	-98.2	9.4	2.964	155.2	0.010	-160.8	0.178	2.6
15000	0.039	-103.7	9.4	2.941	141.2	0.010	-176.1	0.187	-10.7
15500	0.059	-110.5	9.3	2.914	127.4	0.010	174.1	0.190	-21.4
16000	0.075	-121.6	9.2	2.894	113.5	0.010	160.4	0.181	-34.3
16500	0.094	-131.4	9.2	2.868	99.4	0.010	140.9	0.177	-46.5
17000	0.104	-143.1	9.1	2.841	85.6	0.010	130.4	0.155	-60.0
17500	0.113	-154.2	9.1	2.837	71.7	0.011	119.1	0.136	-73.5
18000	0.115	-164.9	9.0	2.828	57.5	0.011	103.1	0.107	-88.7
18500	0.110	-173.8	9.0	2.824	43.3	0.011	91.2	0.083	-106.1
19000	0.102	178.6	9.0	2.824	28.9	0.012	82.5	0.050	-124.8
19500	0.088	175.2	9.1	2.836	14.0	0.012	70.6	0.024	-166.7
20000	0.073	177.6	9.1	2.858	-1.1	0.013	62.0	0.025	83.8
20500	0.064	-174.9	9.2	2.868	-16.8	0.015	41.3	0.055	52.8
21000	0.066	-159.7	9.2	2.869	-32.8	0.016	27.5	0.083	24.5
21500	0.083	-150.6	9.1	2.840	-49.3	0.018	18.5	0.106	8.5
22000	0.109	-146.8	9.0	2.811	-65.3	0.018	-1.8	0.131	-15.9
22500	0.131	-151.8	8.9	2.781	-81.5	0.019	-19.5	0.151	-34.4
23000	0.146	-157.0	8.8	2.745	-97.9	0.018	-36.4	0.161	-51.1
23500	0.153	-164.6	8.6	2.702	-114.2	0.018	-54.6	0.166	-68.9
24000	0.163	-173.2	8.6	2.683	-130.1	0.019	-62.2	0.163	-92.1
24500	0.164	-179.1	8.6	2.690	-146.7	0.021	-81.4	0.157	-113.9
25000	0.157	178.6	8.7	2.731	-163.9	0.022	-96.5	0.152	-134.8
25500	0.147	-179.2	9.0	2.802	177.7	0.025	-115.2	0.137	-159.1
26000	0.140	-174.1	9.1	2.839	159.1	0.023	-138.5	0.087	168.1
26500	0.147	-169.8	9.3	2.925	137.9	0.026	-155.0	0.049	116.0

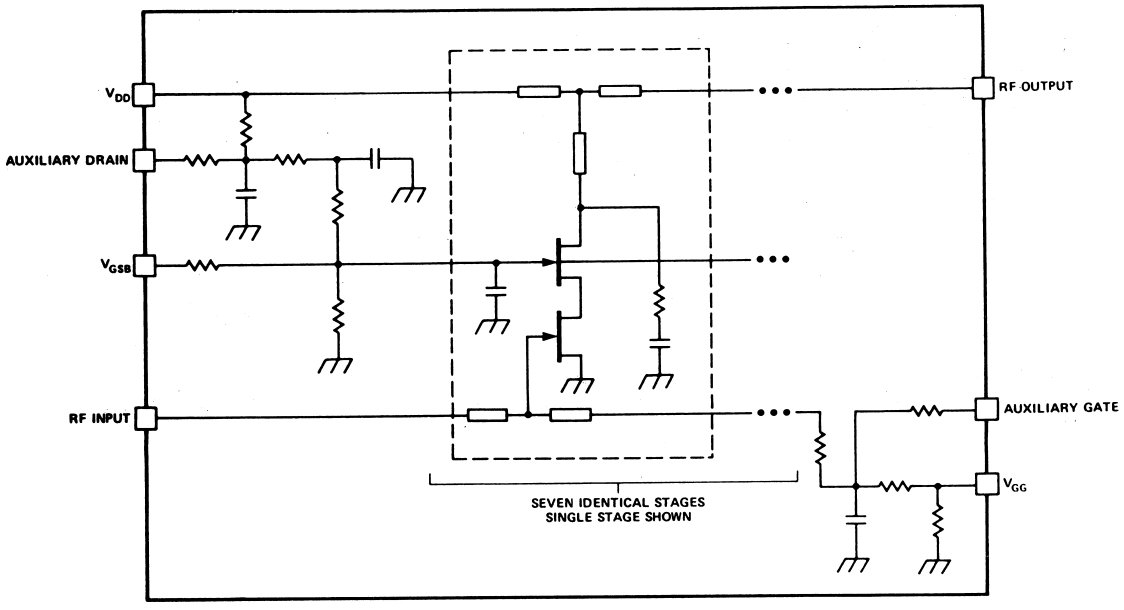


Figure 1. Simplified Schematic.

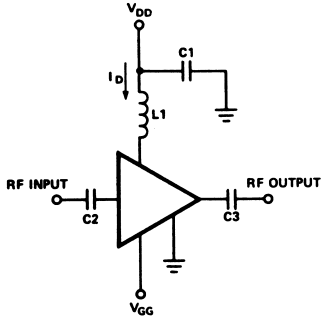


Figure 2. Suggested Bias Configuration.

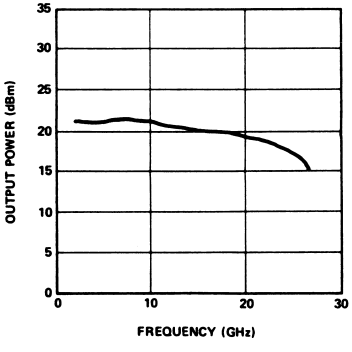


Figure 3. Typical Output Power at 1 dB Gain Compression vs. Frequency.

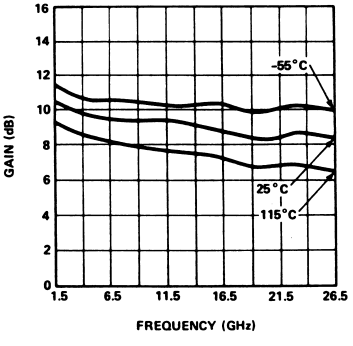


Figure 4. Typical Gain Response vs. Frequency at Three Temperatures.

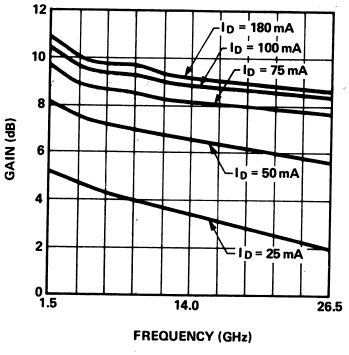


Figure 5. Typical Gain Response vs. Frequency at Five Different Settings of I_D and V_D = 7 V.

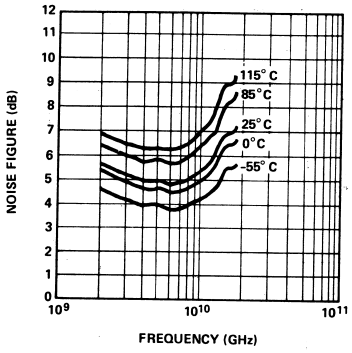


Figure 6. Typical Noise Figure vs. Frequency at Five Different Temperatures (V_D = 7 V, I_D = 150 mA, Frequency = 18 GHz).

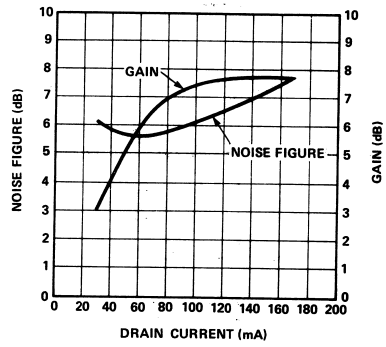


Figure 7. Typical Noise Figure and Gain vs. Drain Curent (V_D = 7 V, Frequency = 18 GHz).

HEWLETT PACKARD

MGA-61000
2-18 GHz Cascadable GaAs MMIC Amplifier

Features

- **Cascadable 50 Ω Gain Block**
- **Broadband Performance: 2-18 GHz**
  7.0 dB typical Gain
  ± 0.5 dB typical Gain Flatness
- **14.0 dBm typical $P_{1\,dB}$ at 18 GHz**
- **Single Supply Bias**

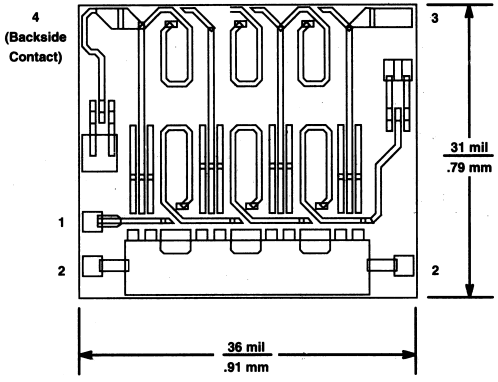
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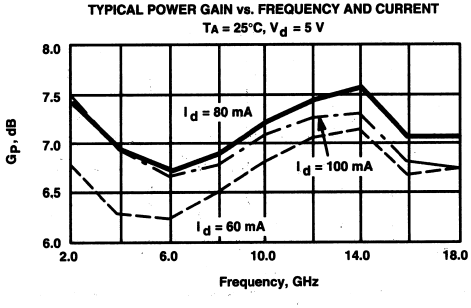
The MGA-61000 is a high performance gallium arsenide Monolithic Microwave Integrated Circuit (MMIC) chip designed for use as a broadband high frequency gain stage in industrial and military applications.

This MMIC is a distributed amplifier utilizing dual gate FETs, resulting in a fully matched gain block useful in the 2 to 18 GHz frequency range. An external self-bias source resistor allows for bias flexibility from a single positive power supply.

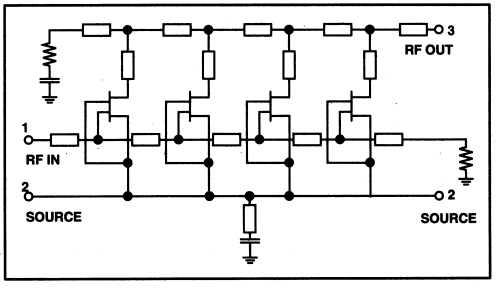
The die is fabricated using HP's nominal 0.3 micron recessed Schottky-barrier-gate, gold metallization, and silicon nitride passivation to achieve excellent performance, uniformity, and reliability.

Chip Outline





Chip Schematic



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions: V_d = 5 V; Z_O = 50 Ω		Units	Min.[1]	Typ.	Max.[1]
G_P	Power Gain ($\|S_{21}\|^2$)	f = 2 to 18 GHz	dB	6.0	7.0	
ΔG_P	Gain Flatness	f = 2 to 18 GHz	dB		±0.5	±0.75
VSWR	Input VSWR	f = 2 to 18 GHz				2.0:1
	Output VSWR	f = 2 to 18 GHz				2.0:1
–	Reverse Isolation ($\|S_{21}\|^2$)	f = 2 to 18 GHz	dB		30	
NF	50 Ω Noise Figure	f = 2 to 18 GHz	dB		6.0	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression V_d = 6 V	f = 2 to 18 GHz	dBm		14	
IP_3	Third Order Intercept Point	V_d = 6 V, f = 18 GHz	dBm		20	
I_d	Device Current		mA	60	80	100

Note: 1. RF performance is determined by assembling and testing 10 devices per wafer.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	7.0 V
Total Power Dissipation[2]	600 mW
CW RF Input Power	+20 dBm
Channel Temperature	175°C
Storage Temperature	–65°C to +175°C

Thermal Resistance: θ_{jc} = 60°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm spot size[3]

Notes:

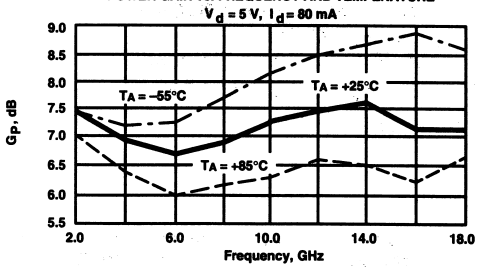
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Derate linearly at 16.7 mW/°C for T_A > 139°C.
3. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Part Number Ordering Information

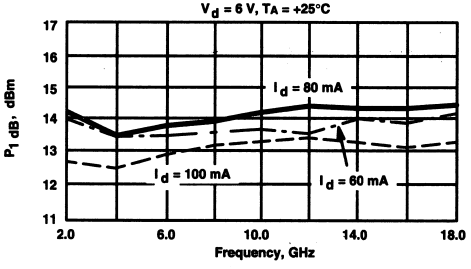
Part Number	Devices Per Tray
MGA-61000-GP0	1
MGA-61000-GP2	10
MGA-61000-GP6	Up to 300

Typical Performance

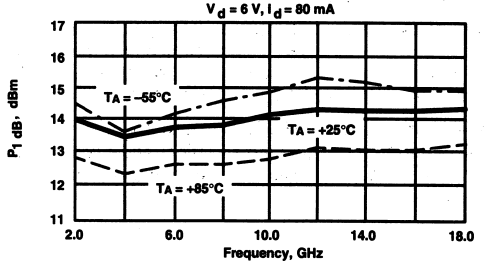
POWER GAIN vs. FREQUENCY AND TEMPERATURE
V_d = 5 V, I_d = 80 mA



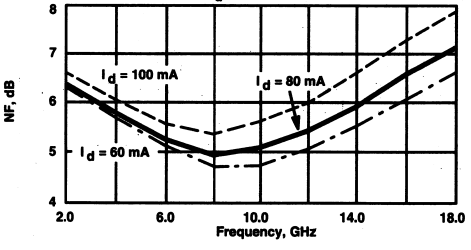
POWER OUTPUT @ 1 dB GAIN COMPRESSION vs. FREQUENCY AND CURRENT
V_d = 6 V, T_A = +25°C



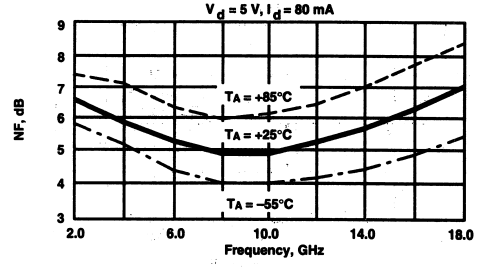
POWER OUTPUT @ 1 dB GAIN COMPRESSION vs. FREQUENCY AND TEMPERATURE
V_d = 6 V, I_d = 80 mA



NOISE FIGURE vs. FREQUENCY AND CURRENT
V_d = 5 V, T_A = 25°C



NOISE FIGURE vs. FREQUENCY AND TEMPERATURE
V_d = 5 V, I_d = 80 mA

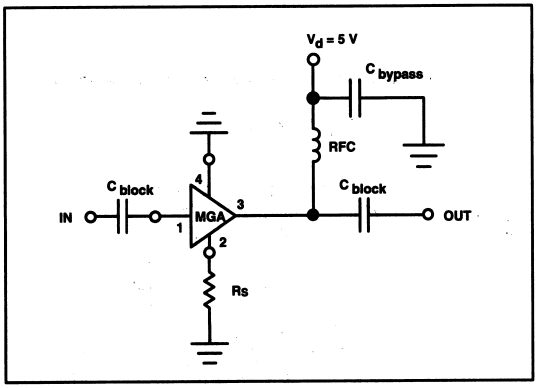


Typical Scattering Parameters: Z_O = 50 Ω

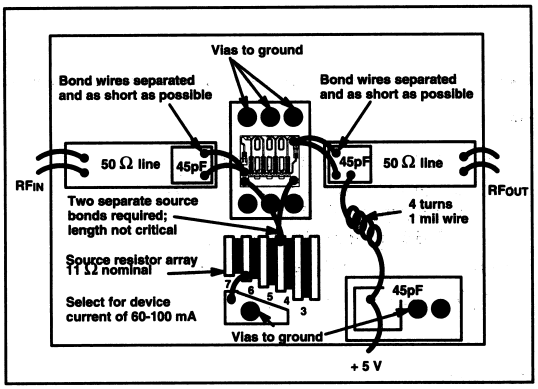
T_A = 25°C, V_d = 5 V, I_d = 80 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
2.0	.15	143	7.4	2.36	145	–37.9	.013	59	.25	–130
3.0	.14	138	7.2	2.28	124	–35.4	.017	56	.17	–163
4.0	.15	134	6.9	2.22	105	–34.0	.020	47	.14	165
5.0	.16	126	6.8	2.19	86	–33.3	.022	39	.13	137
6.0	.16	118	6.8	2.18	68	–33.4	.021	31	.12	113
7.0	.16	111	6.8	2.20	50	–34.0	.020	24	.11	88
8.0	.16	106	6.9	2.22	32	–35.0	.018	20	.10	64
9.0	.15	103	7.0	2.25	13	–36.5	.015	15	.10	39
10.0	.15	105	7.2	2.30	–6	–38.4	.012	16	.10	17
11.0	.17	106	7.4	2.34	–27	–38.8	.011	21	.09	3
12.0	.19	104	7.4	2.36	–48	–38.0	.013	19	.07	–3
13.0	.22	98	7.4	2.35	–68	–36.5	.015	10	.06	19
14.0	.24	90	7.6	2.39	–88	–34.1	.020	–10	.08	46
15.0	.26	77	7.4	2.36	–111	–31.0	.028	–35	.15	51
16.0	.24	62	7.0	2.26	–133	–28.5	.037	–67	.21	41
17.0	.19	52	6.8	2.20	–154	–26.9	.045	–94	.24	31
18.0	.09	64	7.0	2.26	–173	–28.2	.039	–122	.24	39

Typical Biasing Configuration



Substrate Bonding Diagram



EXTERNAL ELEMENTS REQUIRED:

- Source Resistor Array (Rs): Select resistor for device current of 60-100 mA (11 Ω nominal).
- Input and Output DC Blocking Capacitors: 45 pF typical.
- RF Choke Network and Bypass Capacitor: 4 turns 1 mil wire; 45 pF capacitor typical.
- Input and Output RF Transmission Lines: 50 Ω typical.

RECOMMENDED DIE ATTACH PROCEDURE

1. Die attach should be performed under an inert atmosphere of either nitrogen or forming gas.
2. Set heater block temperature to 300 ± 10°C.
3. Place circuit on heater block and heat thoroughly; typically 5 - 15 seconds.
4. Place Au-Sn preform on circuit in die attach location, using sufficient quantity to ensure wetting and to produce a fillet around the die.
5. Using sharp tweezers, pickup the die and orient it properly on the circuit.
6. Scrub the die into the preform with a back-and-forth motion taking care not to scratch the top surface of the chip. Continue until wetting occurs; normally within 3 to 4 scrubs.
7. Wetting should occur on 100% of the chip perimeter to form a visible fillet around the die.
8. Remove the circuit from the heater block and allow it to cool in air. Total time for die attach should be less than 10 seconds.

RECOMMENDED WEDGE BONDING PROCEDURE

1. Set heater block temperature to 260 ± 10°C (If the wedge is heated, the heater block temperature should be lowered slightly from this setting. The exact setting will need to be determined empirically, and will vary from machine to machine).
2. Use prestressed (annealed) gold wire of .0007 or .001 inches diameter.
3. Tip bonding pressure should be between 15 and 20 grams, and should not exceed 20 grams. The footprint left by the wire should be between 1.5 and 2.5 wire diameters across.
4. Proceed with bonding according to machine instructions. Bonds should be made from the circuit to the chip bonding pads to minimize the potential for pad damage. Bonds should be made to the source (common) and drain (output) pads of the MMIC before bonding to the gate (input) pad to minimize the potential for ESD damage.

CAUTION: This device makes use of GaAs FET devices with very small gate geometries. Such devices are subject to damage by electro-static discharge (ESD), and must only be handled by properly grounded personnel working at grounded assembly stations.

HEWLETT PACKARD

MGA-61100
6-18 GHz Cascadable GaAs MMIC Amplifier

Features

- **Cascadable 50 Ω Gain Block**
- **Broadband Performance: 6-18 GHz**
  7.0 dB typical Gain
  ± 0.5 dB typical Gain Flatness
- **14.0 dBm typical $P_{1\,dB}$ at 18 GHz**
- **Single Supply Bias**

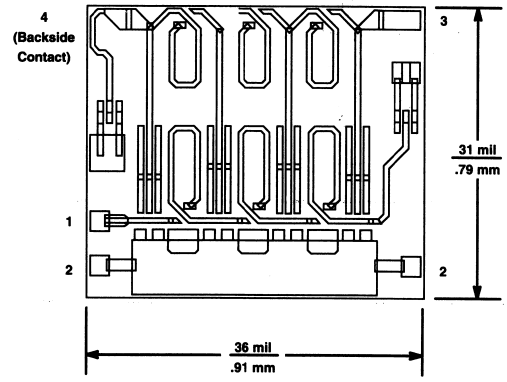
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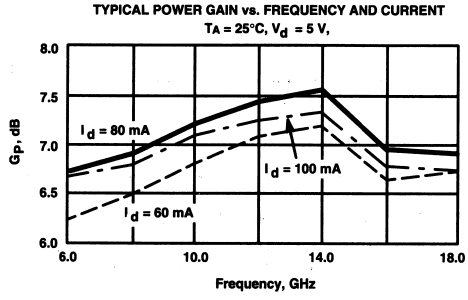
The MGA-61100 is a high performance gallium arsenide Monolithic Microwave Integrated Circuit (MMIC) chip designed for use as a broadband high frequency gain stage in industrial and military applications.

This MMIC is a distributed amplifier utilizing dual gate FETs, resulting in a fully matched gain block useful in the 6 to 18 GHz frequency range. An external self-bias source resistor allows for bias flexibility from a single positive power supply.

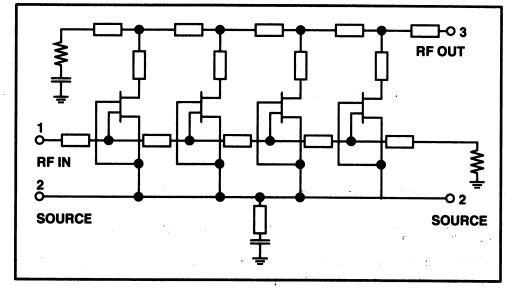
The die is fabricated using HP's nominal .3 micron recessed Schottky-barrier-gate, gold metallization, and silicon nitride passivation to achieve excellent performance, uniformity, and reliability.

Chip Outline





Chip Schematic



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions: V_d = 5 V; Z_O = 50 Ω		Units	Min.[1]	Typ.	Max.[1]
G_P	Power Gain ($\|S_{21}\|^2$)	f = 6 to 18 GHz	dB	6.0	7.0	
ΔG_P	Gain Flatness	f = 6 to 18 GHz	dB		±0.5	±0.75
VSWR	Input VSWR	f = 6 to 18 GHz				2.0:1
	Output VSWR	f = 6 to 18 GHz				2.0:1
–	Reverse Isolation ($\|S_{21}\|^2$)	f = 6 to 18 GHz	dB		30	
NF	50 Ω Noise Figure	f = 6 to 18 GHz	dB		6.0	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression V_d = 6 V	f = 6 to 18 GHz	dBm		14.0	
IP_3	Third Order Intercept Point	V_d = 6 V, f = 18 GHz	dBm		20	
I_d	Device Current		mA	60	80	100

Note: 1. RF performance is determined by assembling and testing 10 devices per wafer.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	7.0 V
Total Power Dissipation[2]	600 mW
CW RF Input Power	+20 dBm
Channel Temperature	175°C
Storage Temperature	–65°C to +175°C

Thermal Resistance: θ_{jc} = 60°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm spot size[3]

Notes:

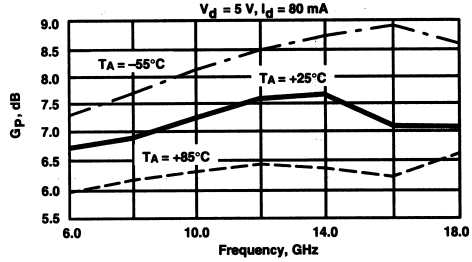
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Derate linearly at 16.7 mW/°C for T_A > 139°C.
3. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Part Number Ordering Information

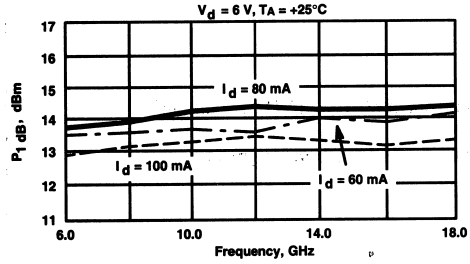
Part Number	Devices Per Tray
MGA-61100-GP0	1
MGA-61100-GP2	10
MGA-61100-GP6	Up to 300

Typical Performance

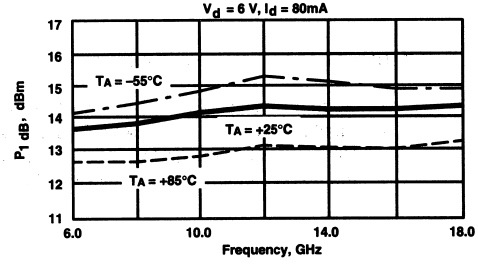
POWER GAIN vs. FREQUENCY AND TEMPERATURE
V_d = 5 V, I_d = 80 mA



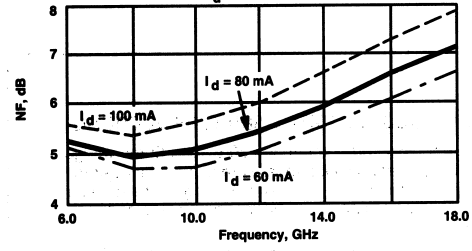
POWER OUTPUT @ 1 dB GAIN COMPRESSION vs. FREQUENCY AND CURRENT
V_d = 6 V, T_A = +25°C



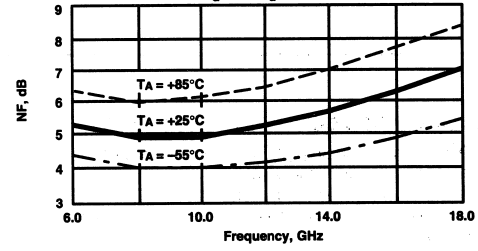
POWER OUTPUT @ 1 dB GAIN COMPRESSION vs. FREQUENCY AND TEMPERATURE
V_d = 6 V, I_d = 80mA



NOISE FIGURE vs. FREQUENCY AND CURRENT
V_d = 5 V, T_A = 25°C



NOISE FIGURE vs. FREQUENCY AND TEMPERATURE
V_d = 5 V, I_d = 80 mA

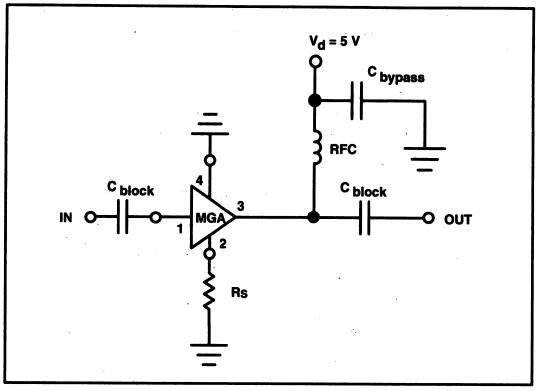


Typical Scattering Parameters: Z_O = 50 Ω

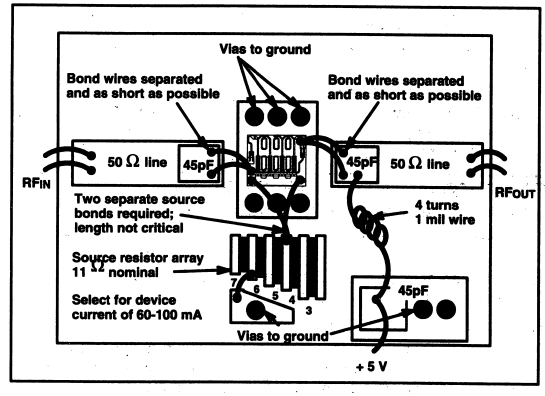
T_A = 25°C, V_d = 5 V, I_d = 80 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
6.0	.16	118	6.8	2.18	68	–33.4	.021	31	.12	113
7.0	.16	111	6.8	2.20	50	–34.0	.020	24	.11	88
8.0	.16	106	6.9	2.22	32	–35.0	.018	20	.10	64
9.0	.15	103	7.0	2.25	13	–36.5	.015	15	.10	39
10.0	.15	105	7.2	2.30	–6	–38.4	.012	16	.10	17
11.0	.17	106	7.4	2.34	–27	–38.8	.011	21	.09	3
12.0	.19	104	7.4	2.36	–48	–38.0	.013	19	.07	–3
13.0	.22	98	7.4	2.35	–68	–36.5	.015	10	.06	19
14.0	.24	90	7.6	2.39	–88	–34.1	.020	–10	.08	46
15.0	.26	77	7.4	2.36	–111	–31.0	.028	–35	.15	51
16.0	.24	62	7.0	2.26	–133	–28.5	.037	–67	.21	41
17.0	.19	52	6.8	2.20	–154	–26.9	.045	–94	.24	31
18.0	.09	64	7.0	2.26	–173	–28.2	.039	–122	.24	39

Typical Biasing Configuration



Substrate Bonding Diagram



EXTERNAL ELEMENTS REQUIRED:

- Source Resistor Array (Rs): Select resistor for device current of 60-100 mA (11 Ω nominal).
- Input and Output DC Blocking Capacitors: 45 pF typical.
- RF Choke Network and Bypass Capacitor: 4 turns 1 mil wire; 45 pF capacitor typical.
- Input and Output RF Transmission Lines: 50 Ω typical.

RECOMMENDED DIE ATTACH PROCEDURE

1. Die attach should be performed under an inert atmosphere of either nitrogen or forming gas.
2. Set heater block temperature to 300 ± 10°C.
3. Place circuit on heater block and heat thoroughly; typically 5 - 15 seconds.
4. Place Au-Sn preform on circuit in die attach location, using sufficient quantity to ensure wetting and to produce a fillet around the die.
5. Using sharp tweezers, pickup the die and orient it properly on the circuit.
6. Scrub the die into the preform with a back-and-forth motion taking care not to scratch the top surface of the chip. Continue until wetting occurs; normally within 3 to 4 scrubs.
7. Wetting should occur on 100% of the chip perimeter to form a visible fillet around the die.
8. Remove the circuit from the heater block and allow it to cool in air. Total time for die attach should be less than 10 seconds.

RECOMMENDED WEDGE BONDING PROCEDURE

1. Set heater block temperature to 260 ± 10°C (If the wedge is heated, the heater block temperature should be lowered slightly from this setting. The exact setting will need to be determined empirically, and will vary from machine to machine).
2. Use prestressed (annealed) gold wire of .0007 or .001 inches diameter.
3. Tip bonding pressure should be between 15 and 20 grams, and should not exceed 20 grams. The footprint left by the wire should be between 1.5 and 2.5 wire diameters across.
4. Proceed with bonding according to machine instructions. Bonds should be made from the circuit to the chip bonding pads to minimize the potential for pad damage. Bonds should be made to the source (common) and drain (output) pads of the MMIC before bonding to the gate (input) pad to minimize the potential for ESD damage.

CAUTION: This device makes use of GaAs FET devices with very small gate geometries. Such devices are subject to damage by electro-static discharge (ESD), and must only be handled by properly grounded personnel working at grounded assembly stations.

HEWLETT PACKARD

MGA-62100
Low Noise
GaAs MMIC Amplifier

Features

- **Output Matched 2 Stage FET Cascade**
- **Broadband Performance: 2 - 14 GHz**
- **Low Noise Figure (50 Ω):**
  2.5 dB typical at 4 GHz
  5.0 dB typical at 14 GHz
- **8.5 dB typical Gain at 14 GHz**
- **Single Supply Bias**

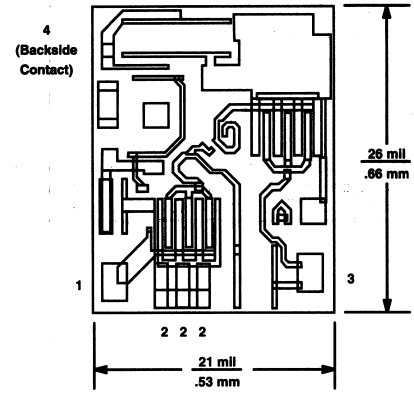
Description

The MGA-62100 is a high performance gallium arsenide Monolithic Microwave Integrated Circuit (MMIC) chip designed for use as a broadband high frequency gain stage in industrial and military applications in the 2 to 14 GHz frequency band.

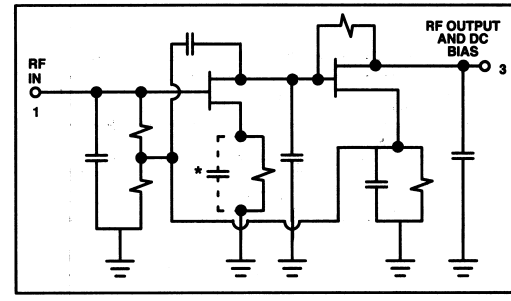
This MMIC consists of a two FET cascade with feedback around the output stage to yield and output matched structure. Flexibility is maintained by having the input match provided externally by the user. AC grounded sources and an internal resistive network allow for biasing from a single positive power supply. The source grounding capacitor for the input stage is an external element to allow for extended low frequency performance.

The die is fabricated using HP's nominal .3 micron recessed Schottky-barrier-gate, gold metallization, and silicon nitride passivation to achieve excellent performance, uniformity, and reliability.

Chip Outline



Chip Schematic



*This capacitor is an off-chip element selected by the user to set lower frequency performance.

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions: V_d = 8 V, Z_O = 50 Ω		Units	Min.[1]	Typ.	Max.[1]
G_P	Power Gain ($\|S_{21}\|^2$)	f = 4.0 GHz f = 10.0 GHz f = 14.0 GHz	dB	 7.5	14.0 9.0 8.5	
NF	50 Ω Noise Figure	f = 4.0 GHz f = 10.0 GHz f = 14.0 GHz	dB		2.5 4.0 5.0	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 4.0 GHz f = 10.0 GHz f = 14.0 GHz	dBm		12.5 11.5 14.0	
VSWR	Output VSWR	f = 2 to 14 GHz			1.6:1	
—	Reverse Isolation	f = 2 to 14 GHz	dB		33.0	
I_d	Device Current		mA	55	65	80

Note 1. RF performance is determined by assembling and testing 10 devices per wafer.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	10.0 V
Total Power Dissipation[2]	640 mW
CW RF Input Power	+14 dBm
Channel Temperature	175°C
Storage Temperature	–65°C to 175°C

Thermal Resistance: θ_{jc} = 100°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm spot size[3]

Notes:

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Derate linearly at 10 mW/°C for T_A > 111°C.
3. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

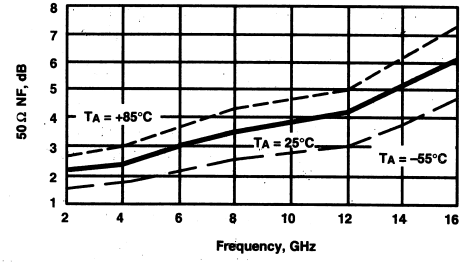
Part Number Ordering Information

Part Number	Devices Per Tray
MGA-62100-GP0	1
MGA-62100-GP2	10
MGA-62100-GP6	Up to 300

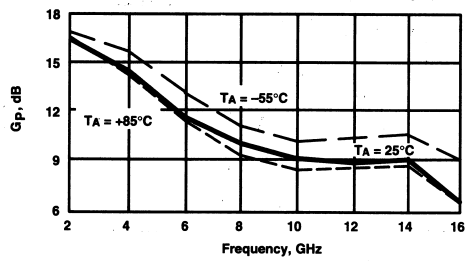
Typical Performance, T_A = 25°C

(unless otherwise noted)

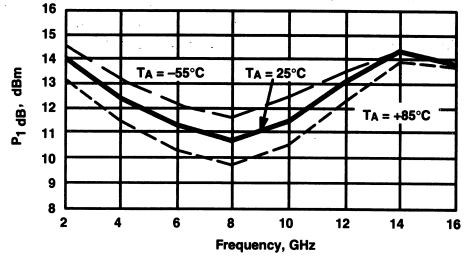
50 Ω NOISE FIGURE vs. FREQUENCY AND TEMPERATURE



POWER GAIN vs. FREQUENCY AND TEMPERATURE



OUTPUT POWER @ 1 dB GAIN COMPRESSION vs. FREQUENCY AND TEMPERATURE

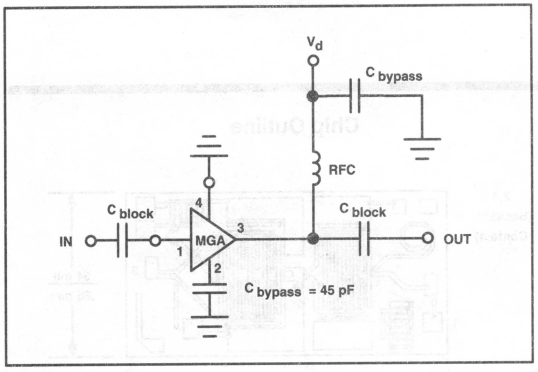


Typical Scattering Parameters: Z_O = 50 Ω

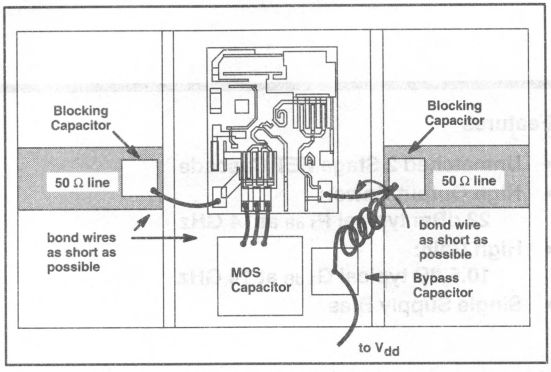
T_A = 25°C, V_d = 8 V

Freq. GHz	S11		S21			S12			S22	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
2.0	.85	–41	16.2	6.42	–46	–39.1	.011	49	.14	–177
3.0	.79	–56	15.4	5.91	–78	–37.4	.013	57	.16	126
4.0	.70	–75	14.3	5.19	–111	–36.3	.015	66	.20	96
5.0	.62	–94	12.9	4.40	–139	–35.5	.017	66	.23	81
6.0	.58	–109	11.6	3.80	–162	–35.5	.017	69	.24	72
7.0	.55	–123	10.7	3.41	175	–34.8	.018	75	.22	66
8.0	.52	–132	9.9	3.11	159	–34.5	.019	83	.20	61
9.0	.50	–146	9.2	2.89	140	–34.1	.020	85	.17	47
10.0	.50	–159	9.0	2.80	120	–33.5	.021	86	.16	30
11.0	.49	–175	8.9	2.78	98	–33.1	.022	80	.17	18
12.0	.53	164	8.8	2.76	75	–33.2	.022	69	.16	18
13.0	.62	147	8.8	2.76	50	–33.6	.021	48	.12	41
14.0	.71	139	8.7	2.73	29	–35.1	.018	21	.15	98
15.0	.75	124	8.2	2.56	–3	–35.6	.017	–26	.33	109
16.0	.75	111	6.4	2.09	–39	–34.6	.019	–76	.53	98

Typical Biasing Configuration



Substrate Bonding Diagram



EXTERNAL ELEMENTS REQUIRED:

- Source Bypass Capacitor: 45 pF typical
- Input and Output DC Blocking Capacitors: 45 pF typical
- RF Choke Network and Bypass Capacitor: 4 turns 1 mil wire; 45 pF typical
- Input and Output RF Transmission Lines: 50 Ω typical

OPTIONAL EXTERNAL ELEMENTS/SPECIAL USE:

- Input Impedance Matching Network: Device guarantees and typical performance are with a 50 Ω generator impedance. Input matching can be used with the MMIC, either to improve noise figure slightly in a narrow band of operation, or to improve the input VSWR and increase the gain at the cost of some loss in noise figure.

RECOMMENDED DIE ATTACH PROCEDURE

1. Die attach should be performed under an inert atmosphere of either nitrogen or forming gas.
2. Set heater block temperature to 300 ± 10°C.
3. Place circuit on heater block and heat thoroughly; typically 5 - 15 seconds.
4. Place Au-Sn preform on circuit in die attach location, using sufficient quantity to ensure wetting and to produce a fillet around the die.
5. Using sharp tweezers, pickup the die and orient it properly on the circuit.
6. Scrub the die into the preform with a back-and-forth motion taking care not to scratch the top surface of the chip. Continue until wetting occurs; normally within 3 to 4 scrubs.
7. Wetting should occur on 100% of the chip perimeter to form a visible fillet around the die.
8. Remove the circuit from the heater block and allow it to cool in air. Total time for die attach should be less than 10 seconds.

RECOMMENDED WEDGE BONDING PROCEDURE

1. Set heater block temperature to 260 ± 10°C (If the wedge is heated, the heater block temperature should be lowered slightly from this setting. The exact setting will need to be determined empirically, and will vary from machine to machine).
2. Use prestressed (annealed) gold wire of .0007 or .001 inches diameter.
3. Tip bonding pressure should be between 15 and 20 grams, and should not exceed 20 grams. The footprint left by the wire should be between 1.5 and 2.5 wire diameters across.
4. Proceed with bonding according to machine instructions. Bonds should be made from the circuit to the chip bonding pads to minimize the potential for pad damage. Bonds should be made to the source (common) and drain (output) pads of the MMIC before bonding to the gate (input) pad to minimize the potential for ESD damage.

CAUTION: This device makes use of GaAs FET devices with very small gate geometries. Such devices are subject to damage by electro-static discharge (ESD), and must only be handled by properly grounded personnel working at grounded assembly stations.

HEWLETT PACKARD

MGA-63100
Medium Power
2 Stage GaAs FET Cascade

Features

- **Unmatched 2 Stage FET Cascade**
- **High Output Power:**
  22 dBm typical $P_{1\,dB}$ at 14 GHz
- **High Gain:**
  10.5 dB typical $G_{1\,dB}$ at 14 GHz
- **Single Supply Bias**

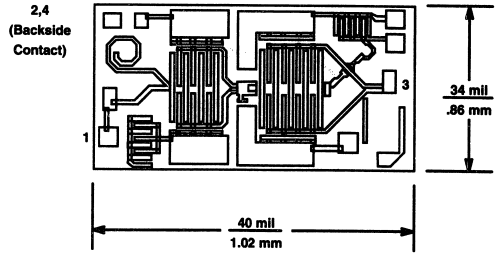
Description

The MGA-63100 is a high performance gallium arsenide Monolithic Microwave Integrated Circuit (MMIC) chip designed for use as a broadband high frequency gain stage in industrial and military applications.

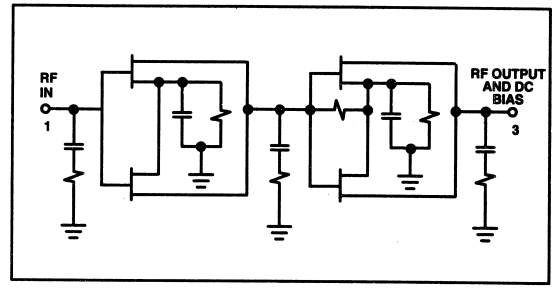
This MMIC uses a cascade of two FET pairs to yield a device with higher gain and higher input impedance than a conventional discrete FET. AC grounded sources and an internal resistive network allow for biasing from a single positive power supply.

The die is fabricated using HP's nominal .3 micron recessed Schottky-barrier-gate, gold metallization, and silicon nitride passivation to achieve excellent performance, uniformity, and reliability.

Chip Outline



Chip Schematic



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions: V_d = 10 V, Z_O = 50 Ω		Units	Min.[1]	Typ.	Max.[1]
$P_{1\,dB}$[2]	Power Output @ 1 dB Gain Compression	f = 6.0 GHz f = 14.0 GHz f = 18.0 GHz	dBm	20.0	21.0 22.0 21.0	
$G_{1\,dB}$[2]	1 dB Compressed Gain	f = 6.0 GHz f = 14.0 GHz f = 18.0 GHz	dB	8.0	22.5 10.5 7.5	
P_{SAT}[2]	Saturated Output Power (3 dB Compressed)	f = 14.0 GHz	dB		25.0	
—	Reverse Isolation	f = 14.0 GHz	dB		30.0	
I_d	Device Current		mA	100	150	200

Notes: 1. RF performance is determined by assembling and testing 10 devices per wafer.
2. Tuned Measurement.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	12.0 V
Total Power Dissipation[2]	2.0 W
CW RF Input Power	+25 dBm
Channel Temperature	175°C
Storage Temperature	–65°C to –175°C

Thermal Resistance: θ_{jc} = 33°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm spot size[3]

Notes:

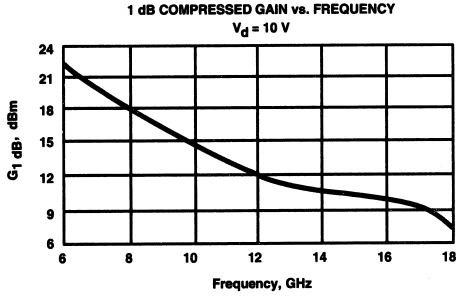
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Derate linearly at 30 mW/°C for T_A > 109°C.
3. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

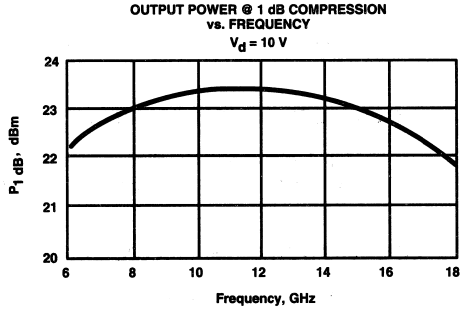
Part Number Ordering Information

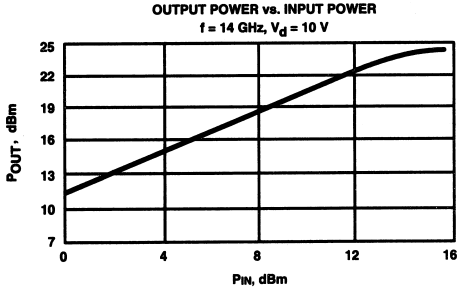
Part Number	Devices Per Tray
MGA-63100-GP0	1
MGA-63100-GP2	10
MGA-63100-GP6	Up to 300

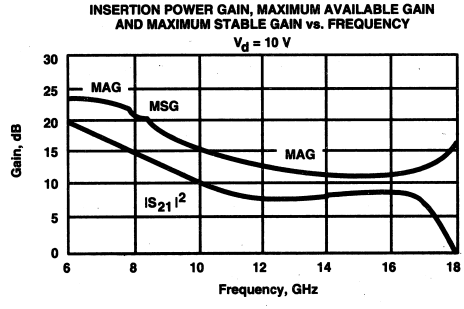
Typical Performance, T_A = 25°C

(unless otherwise noted)







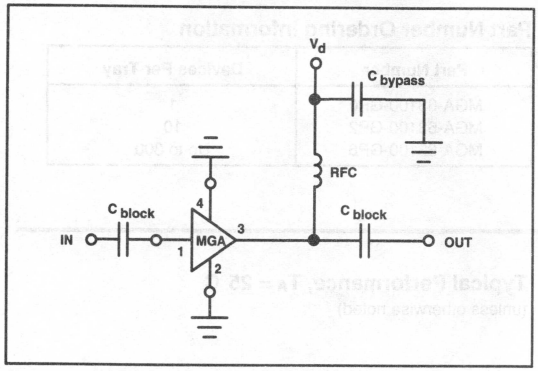


Typical Scattering Parameters: Z_O = 50 Ω

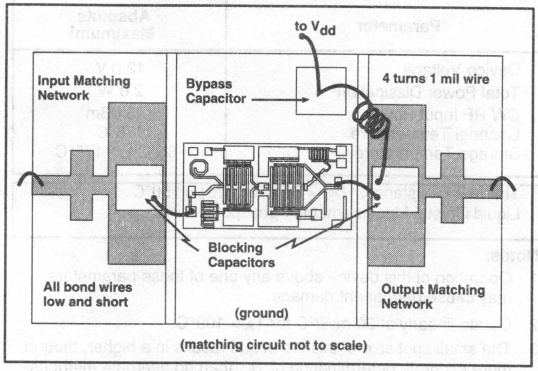
T_A = 25°C, V_d = 10 V

Freq. GHz	S11 Mag	S11 Ang	S21 dB	S21 Mag	S21 Ang	S12 dB	S12 Mag	S12 Ang	S22 Mag	S22 Ang	k
4.0	.89	130	8.6	2.14	92	37.7	.013	86	.44	–93	3.03
5.0	.93	106	13.2	4.56	5	95.0	.016	60	.58	–115	1.39
6.0	.63	40	19.9	9.85	–66	–37.1	.014	110	.59	–144	1.81
7.0	.60	–122	19.8	9.77	–155	–29.6	.033	108	.44	–168	1.08
8.0	.82	–178	15.2	5.74	156	–28.4	.038	94	.37	–169	0.92
9.0	.83	155	11.8	3.88	131	–27.5	.042	79	.39	–170	1.12
10.0	.83	138	10.0	3.17	106	–27.3	.043	65	.41	–177	1.31
11.0	.81	124	8.7	2.73	83	–27.3	.043	59	.42	–179	1.59
12.0	.80	109	8.1	2.53	61	–27.7	.041	48	.44	176	1.80
13.0	.74	89	7.8	2.45	36	–28.6	.037	35	.47	168	2.34
14.0	.61	68	7.7	2.42	10	–30.5	.030	18	.50	163	3.56
15.0	.33	48	7.5	2.37	–20	–34.9	.018	11	.56	157	7.34
16.0	.05	134	8.3	2.59	–63	–43.1	.007	13	.65	145	15.87
17.0	.32	–159	6.9	2.21	–106	–37.1	.014	65	.73	128	6.56
18.0	.71	168	–1.6	0.83	–149	–36.5	.015	49	.74	117	8.53

Typical Biasing Configuration



Substrate Bonding Diagram



EXTERNAL ELEMENTS REQUIRED:

- Input and Output DC Blocking Capacitors: 45pF typical
- RF Choke Network and Bypass Capacitor: 4 turns 1 mil wire; 45 pF capacitor typical

INPUT and OUTPUT IMPEDANCE MATCHING NETWORKS:

- This MMIC is not impedance matched. As with a discrete transistor, the S-parameter data provided should be used to design input and output impedance matching networks that will optimize device performance for the designer's application.
  All device guarantees and typical performance information represents performance of the MMIC in a tuned (optimally matched) environment.

RECOMMENDED DIE ATTACH PROCEDURE

1. Die attach should be performed under an inert atmosphere of either nitrogen or forming gas.
2. Set heater block temperature to 300 ± 10°C.
3. Place circuit on heater block and heat thoroughly; typically 5 - 15 seconds.
4. Place Au-Sn preform on circuit in die attach location, using sufficient quantity to ensure wetting and to produce a fillet around the die.
5. Using sharp tweezers, pickup the die and orient it properly on the circuit.
6. Scrub the die into the preform with a back-and-forth motion taking care not to scratch the top surface of the chip. Continue until wetting occurs; normally within 3 to 4 scrubs.
7. Wetting should occur on 100% of the chip perimeter to form a visible fillet around the die.
8. Remove the circuit from the heater block and allow it to cool in air. Total time for die attach should be less than 10 seconds.

RECOMMENDED WEDGE BONDING PROCEDURE

1. Set heater block temperature to 260 ± 10°C (If the wedge is heated, the heater block temperature should be lowered slightly from this setting. The exact setting will need to be determined empirically, and will vary from machine to machine).
2. Use prestressed (annealed) gold wire of .0007 or .001 inches diameter.
3. Tip bonding pressure should be between 15 and 20 grams, and should not exceed 20 grams. The footprint left by the wire should be between 1.5 and 2.5 wire diameters across.
4. Proceed with bonding according to machine instructions. Bonds should be made from the circuit to the chip bonding pads to minimize the potential for pad damage. Bonds should be made to the source (common) and drain (output) pads of the MMIC before bonding to the gate (input) pad to minimize the potential for ESD damage.

CAUTION: This device makes use of GaAs FET devices with very small gate geometries. Such devices are subject to damage by electro-static discharge (ESD), and must only be handled by properly grounded personnel working at grounded assembly stations.

HEWLETT PACKARD

MGA-64135
2-6 GHz Cascadable GaAs MMIC Amplifier

Features

- **Cascadable 50 Ω Gain Block**
- **Broadband Performance: 2-6 GHz**
  - **12.0 dB typical Gain**
  - **± 0.8 dB Gain Flatness**
  - **12.0 dBm $P_{1\,dB}$**
- **Single Supply Bias**
- **Cost Effective Ceramic Microstrip Package**

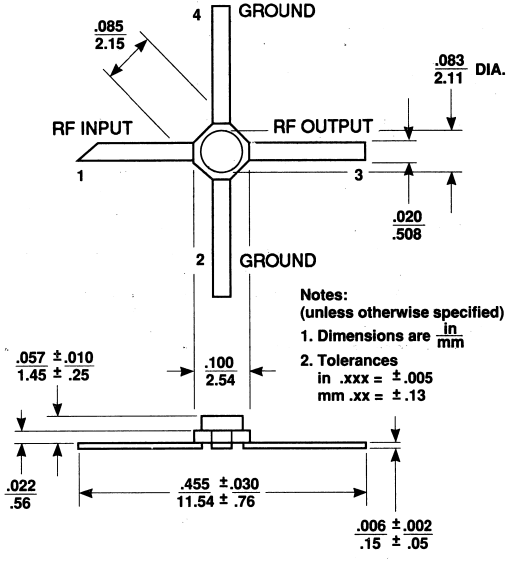
Description

The MGA-64135 is a high performance gallium arsenide Monolithic Microwave Integrated Circuit (MMIC) housed in a cost effective, microstrip package. This device is designed for use as a general purpose 50 ohm gain block in the 2 to 6 GHz frequency range. Typical applications include narrow and broadband IF and RF amplifiers for commercial, industrial, and military requirements.

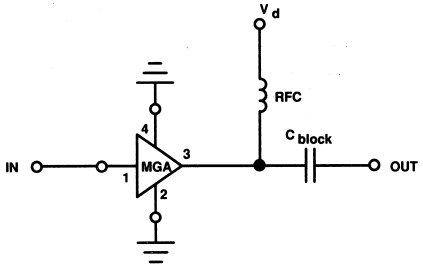
This MMIC is a cascade of two stages, each utilizing shunt feedback to establish a broadband impedance match. The source of each stage is AC grounded to allow biasing from a single positive power supply. The interstage blocking capacitor as well as a resistive "self-bias" network are included on chip.

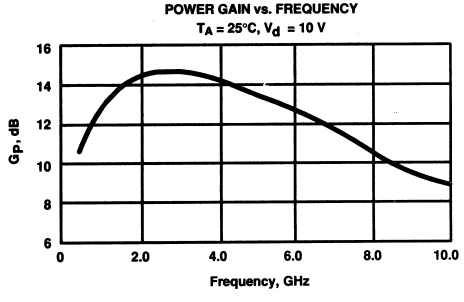
The die is fabricated using HP's nominal .5 micron recessed Schottky-barrier-gate, gold metallization and silicon nitride passivation to achieve excellent performance, uniformity, and reliability.

35 Micro-X Package



Typical Biasing Configuration





Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions: V_d = 10 V, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 2 to 6 GHz	dB	10.0	12.0	
ΔG_P	Gain Flatness	f = 2 to 6 GHz	dB		±0.8	
–	Gain Variation vs. Temperature T_{CASE} = –25°C to +85°C	f = 2 to 6 GHz	dB		±0.5	
VSWR	Input VSWR	f = 2 to 6 GHz			1.5:1	2.0:1
	Output VSWR	f = 2 to 6 GHz			1.4:1	2.0:1
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression	f = 2 to 6 GHz	dBm	10.0	12.0	
NF	50 Ω Noise Figure	f = 2 to 2 GHz	dB		7.5	
–	Reverse Isolation ($\|S_{12}\|^2$)	f = 2 to 6 GHz	dB		35	
I_d	Device Current		mA	35	50	65

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	12 V
Total Power Dissipation[2]	600 mW
CW RF Input Power	+13 dBm
Channel Temperature	175°C
Storage Temperature[3]	–65°C to +175°C

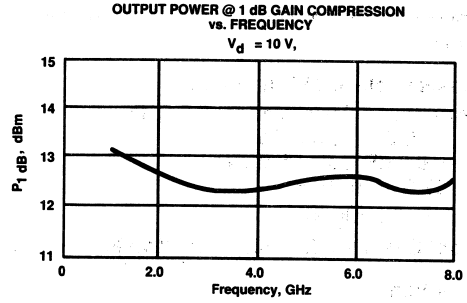
Thermal Resistance: θ_{jc} = 150°C/W[4]; T_{CH} = 150°C
Liquid Crystal Measurement; 1 µm spot size[5]

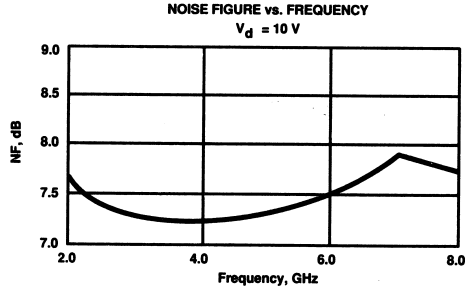
Notes:

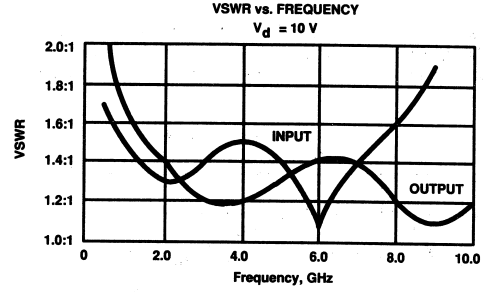
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Derate linearly at 8.3 mW/°C for T_{CASE} > 103°C.
3. Storage above +150°C may tarnish the leads of this package making it difficult to solder into a circuit. After a device has been soldered into a circuit it may be safely stored up to 175°C.
4. The thermal resistance value is based on measurements taken with the device soldered to a 25 mil Teflon PCB.
5. The small spot of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Typical Performance, T_A = 25°C

(unless otherwise noted)







Typical Scattering Parameters: Z_O = 50 Ω

T_A = 25°C, V_d = 10 V

Freq. GHz	S_{11} Mag	S_{11} Ang	S_{21} dB	S_{21} Mag	S_{21} Ang	S_{12} dB	S_{12} Mag	S_{12} Ang	S_{22} Mag	S_{22} Ang
0.5	.27	–38	10.6	3.38	14	–31.0	.028	–13	.38	–41
1.0	.18	–44	12.9	4.42	–9	–33.1	.022	–20	.26	–48
2.0	.14	–67	14.3	5.21	–54	–34.9	.018	–19	.16	–59
3.0	.17	–91	14.5	5.33	–93	–37.1	.014	–21	.11	–75
4.0	.20	–105	14.2	5.11	–131	–37.8	.013	–15	.11	–71
5.0	.18	–114	13.6	4.79	–167	–37.3	.014	–10	.14	–57
6.0	.07	–162	12.8	4.35	157	–38.5	.012	–1	.17	–41
7.0	.15	96	11.8	3.89	123	–36.0	.016	3	.16	–42
8.0	.23	76	10.8	3.46	92	–34.3	.019	4	.10	–54
9.0	.32	63	9.5	2.98	63	–29.3	.034	12	.04	159
10.0	.43	52	8.6	2.68	38	–27.6	.041	–11	.09	116

HEWLETT PACKARD

MGA-65100
Medium Power
2 Stage GaAs FET Cascade

Features

- **Unmatched 2 Stage FET Cascade**
- **High Output Power:**
  24 dBm typical $P_{1\,dB}$ at 14 GHz
- **High Gain:**
  9.5 dB typical $G_{1\,dB}$ at 14 GHz
- **Single Supply Bias**

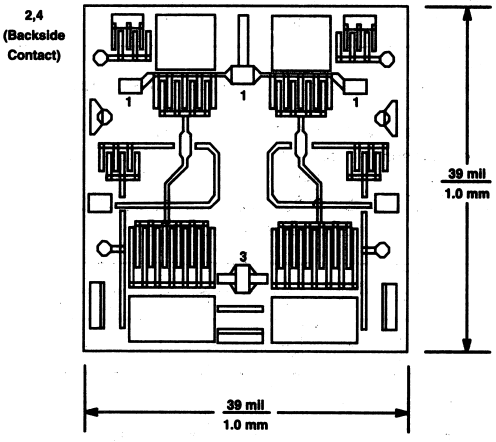
Description

The MGA-65100 is a high performance gallium arsenide Monolithic Microwave Integrated Circuit (MMIC) chip designed for use as a medium power high frequency gain stage in industrial and military applications.

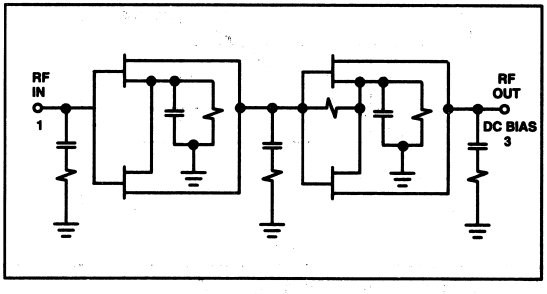
This MMIC uses a cascade of two FET pairs to yield a device with higher gain and higher input impedances than a conventional discrete FET. AC grounded sources and an internal resistive network allow for biasing from a single positive power supply.

The die is fabricated using HP's nominal .3 micron recessed Schottky-barrier-gate, gold metallization, and silicon nitride passivation to achieve excellent performance, uniformity, and reliability.

Chip Outline



Chip Schematic



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions: V_d = 10 V, Z_O = 50 Ω		Units	Min.[1]	Typ.	Max.[1]
$P_{1\,dB}$[2]	Power Output @ 1 dB Gain Compression	f = 6.0 GHz f = 14.0 GHz f = 18.0 GHz	dBm	23.0	26.0 24.0 22.0	
$G_{1\,dB}$[2]	1 dB Compressed Gain	f = 6.0 GHz f = 14.0 GHz f = 18.0 GHz	dB	8.0	19.0 9.5 7.5	
P_{SAT}[2]	Saturated Output Power (3 dB Compressed)	f = 14.0 GHz	dB		25.0	
—	Reverse Isolation	f = 6 to 18 GHz	dB		27.0	
I_d	Device Current		mA	150	200	300

Notes: 1. RF performance is determined by assembling and testing 10 devices per wafer.
2. Tuned Measurement.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	12.0 V
Total Power Dissipation[2]	3.0 W
CW RF Input Power	+26 dBm
Channel Temperature	175°C
Storage Temperature	–65°C to –175°C

Thermal Resistance: θ_{jc} = 22°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm spot size[3]

Notes:

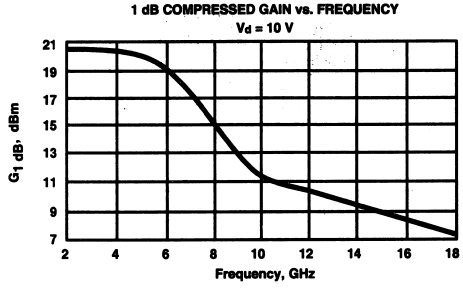
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Derate linearly at 45 mW/°C for T_A > 109°C.
3. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

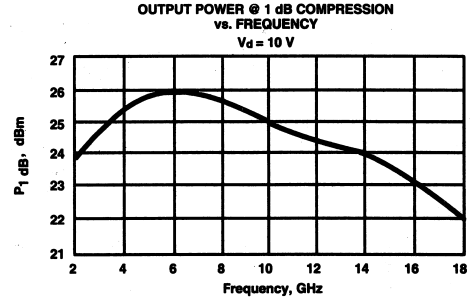
Part Number Ordering Information

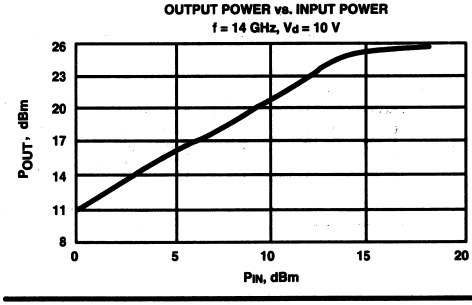
Part Number	Devices Per Tray
MGA-65100-GP0	1
MGA-65100-GP2	10
MGA-65100-GP6	Up to 300

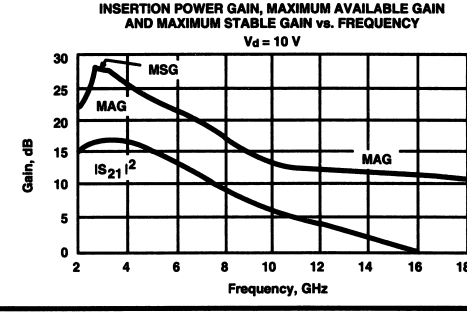
Typical Performance, T_A = 25°C

(unless otherwise noted)







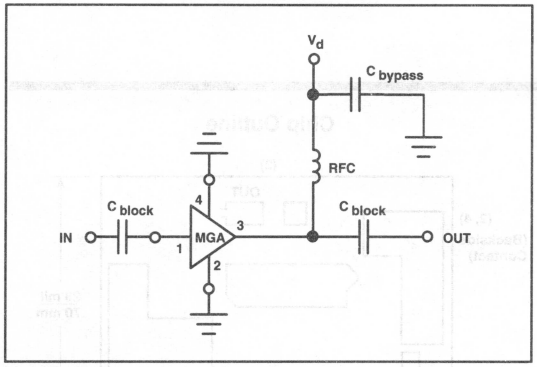


Typical Scattering Parameters: Z_O = 50 Ω

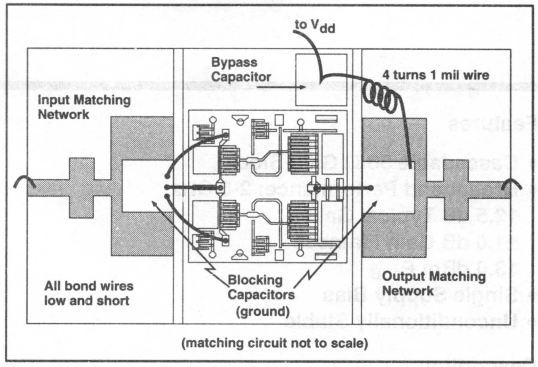
T_A = 25°C, V_d = 10 V

Freq. GHz	S11 Mag	S11 Ang	S21 dB	S21 Mag	S21 Ang	S12 dB	S12 Mag	S12 Ang	S22 Mag	S22 Ang	k
2.0	.88	–75	15.0	5.61	–30	–43.1	.007	131	.31	–100	2.59
3.0	.94	–113	16.6	6.75	–74	–40.9	.009	118	.50	–122	0.68
4.0	.93	–136	15.6	6.00	–110	–40.0	.010	55	.61	–143	1.15
5.0	.91	–147	15.9	6.22	–137	–38.4	.012	–5	.61	–157	1.29
6.0	.92	–161	14.0	5.01	176	–38.4	.012	53	.57	–165	1.40
7.0	.92	–170	11.4	3.72	145	–33.2	.022	74	.55	177	1.13
8.0	.91	–176	9.4	2.96	123	–31.1	.028	73	.54	167	1.22
9.0	.91	178	7.8	2.46	102	–29.9	.032	70	.54	161	1.29
10.0	.90	173	6.3	2.07	81	–29.1	.035	68	.56	154	1.44
11.0	90	168	5.0	1.77	63	–28.9	.036	65	.57	148	1.55
12.0	.91	162	4.2	1.63	45	–28.9	.036	63	.61	142	1.48
13.0	.91	157	3.2	1.45	23	–28.4	.038	61	.64	136	1.46
14.0	.91	152	2.1	1.27	6	–27.1	.044	58	.69	127	1.35
15.0	.92	147	1.4	1.18	–15	–28.0	.040	44	.70	117	1.22
16.0	.92	140	0.4	1.05	–38	–28.9	.036	38	.71	107	1.28
17.0	.93	134	–1.1	0.88	–63	–29.6	.033	30	.72	96	1.22
18.0	.93	131	–2.5	0.75	–85	–30.5	.030	20	.73	88	1.25

Typical Biasing Configuration



Substrate Bonding Diagram



EXTERNAL ELEMENTS REQUIRED:

- Input and Output DC Blocking Capacitors: 45pF typical
- RF Choke Network and Bypass Capacitor: 4 turns 1 mil wire; 45 pF capacitor typical

INPUT and OUTPUT IMPEDANCE MATCHING NETWORKS:

- This MMIC is not impedance matched. As with a discrete transistor, the S-parameter data provided should be used to design input and output impedance matching networks that will optimize device performance for the designer's application.
  All device guarantees and typical performance information represents performance of the MMIC in a tuned (optimally matched) environment.

RECOMMENDED DIE ATTACH PROCEDURE

1. Die attach should be performed under an inert atmosphere of either nitrogen or forming gas.
2. Set heater block temperature to 300 ± 10°C.
3. Place circuit on heater block and heat thoroughly - typically 5 - 15 seconds.
4. Place Au-Sn preform on circuit in die attach location, using sufficient quantity to ensure wetting and to produce a fillet around the die.
5. Using sharp tweezers, pickup the die and orient it properly on the circuit.
6. Scrub the die into the preform with a back-and-forth motion taking care not to scratch the top surface of the chip. Continue until wetting occurs; normally within 3 to 4 scrubs.
7. Wetting should occur on 100% of the chip perimeter to form a visible fillet around the die.
8. Remove the circuit from the heater block and allow it to cool in air. Total time for die attach should be less than 10 seconds.

RECOMMENDED WEDGE BONDING PROCEDURE

1. Set heater block temperature to 260 ± 10°C (If the wedge is heated, the heater block temperature should be lowered slightly from this setting. The exact setting will need to be determined empirically, and will vary from machine to machine).
2. Use prestressed (annealed) gold wire of .0007 or 1.000 inches diameter.
3. Tip bonding pressure should be between 15 and 20 grams, and should not exceed 20 grams. The footprint left by the wire should be between 1.5 and 2.5 wire diameters across.
4. Proceed with bonding according to machine instructions. Bonds should be made from the circuit to the chip bonding pads to minimize the potential for pad damage. Bonds should be made to the source (common) and drain (output) pads of the MMIC before bonding to the gate (input) pad to minimize the potential for ESD damage.

CAUTION: This device makes use of GaAs FET devices with very small gate geometries. Such devices are subject to damage by electro-static discharge (ESD), and must only be handled by properly grounded personnel working at grounded assembly stations.

HEWLETT PACKARD

MGA-66100
2-6 GHz Cascadable GaAs MMIC Amplifier

Features

- **Cascadable 50 Ω Gain Block**
- **Broadband Performance: 2-6 GHz**
  12.5 dB Typical Gain
  ±1.0 dB Gain Flatness
  13.0 dBm P_{1dB}
- **Single Supply Bias**
- **Unconditionally Stable**

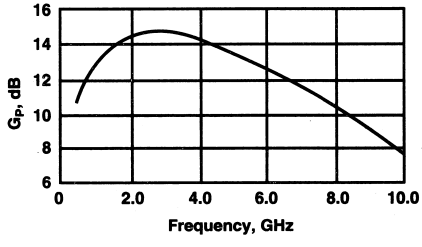
Description

The MGA-66100 is a high performance gallium arsenide Monolithic Microwave Integrated Circuit (MMIC) chip. This device is designed for use as a general purpose 50 Ω gain block in the 2 to 6 GHz frequency range. Typical applications include narrow and broadband IF and RF amplifiers for commercial, industrial, and military requirements.

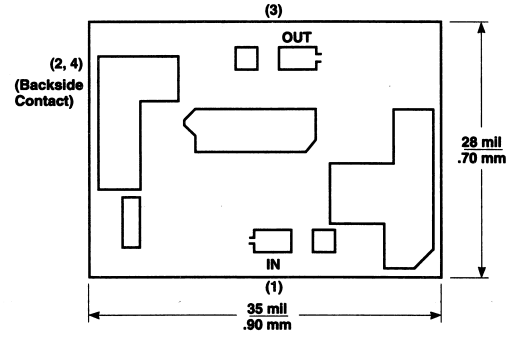
This MMIC is a cascade of two stages, each utilizing shunt feedback to establish a broadband impedance match. The source of each stage is AC grounded to allow biasing from a single positive power supply. The interstage blocking capacitor as well as a resistive "self-bias" network are included on chip.

The die is fabricated using HP's nominal .5 micron recessed Schottky-barrier-gate, gold metallization and silicon nitride passivation to achieve excellent performance, uniformity, and reliability.

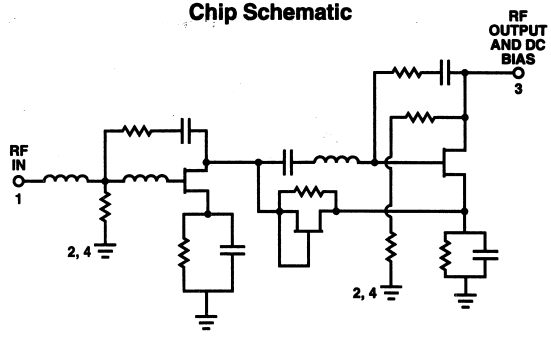
Power Gain vs. Frequency
T_A = 25°C, V_d = 10 V



Chip Outline



Chip Schematic



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions: V_d = 10 V, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 2 to 6 GHz	dB	10.0	12.5	
ΔG_P	Gain Flatness	f = 2 to 6 GHz	dB		±1.0	
—	Gain Variation vs. Temperature T_{CASE} = −25°C to +85°C	f = 2 to 6 GHz	dB		±0.5	
VSWR	Input VSWR	f = 2 to 6 GHz			1.4:1	2.0:1
	Output VSWR	f = 2 to 6 GHz			1.4:1	2.0:1
$P_{1\ dB}$	Output Power @ 1 dB Gain Compression	f = 2 to 6 GHz	dBm	10.0	13.0	
NF	50 Ω Noise Figure	f = 2 to 6 GHz	dB		7.5	
—	Reverse Isolation ($\|S_{12}\|^2$)	f = 2 to 6 GHz	dB		35	
I_d	Device Current		mA	35	50	65

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	12 V
Total Power Dissipation[2, 3]	800 mW
CW RF Input Power	+13 dBm
Channel Temperature	175°C
Storage Temperature	-65 to 175°C

Thermal Resistance: θ_{jc} = 40°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1μm spot size[4]

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Mounting Surface Temperature = 25°C.
3. Derate linearly at 25 mW/°C for $T_{MOUNTING\ SURFACE}$ > 143°C.
4. The small spot size of the technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See Primer IIIA for more information.

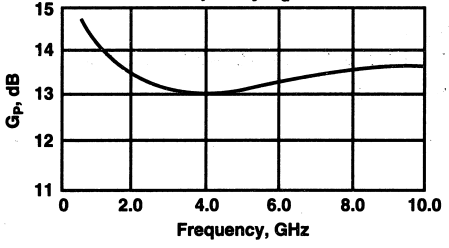
Part Number Ordering Information

Part Number	Devices Per Tray
MGA-66100-GP1	5
MGA-66100-GP3	50
MGA-66100-GP6	Up to 300

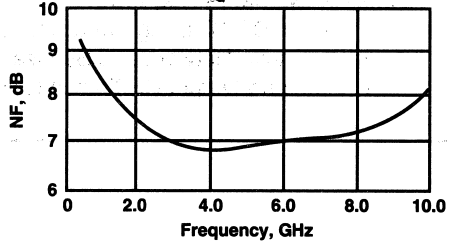
Typical Performance, T_A = 25°C

(Unless otherwise noted)

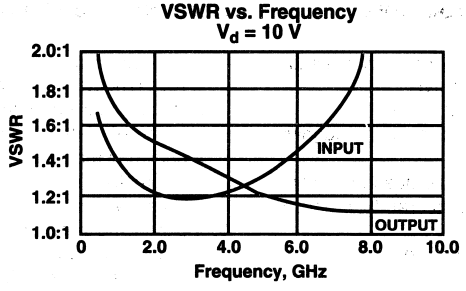
Output Power @ 1 dB Gain Compression vs. Frequency V_d = 10 V



Noise Figure vs. Frequency V_d = 10 V



VSWR vs. Frequency V_d = 10 V

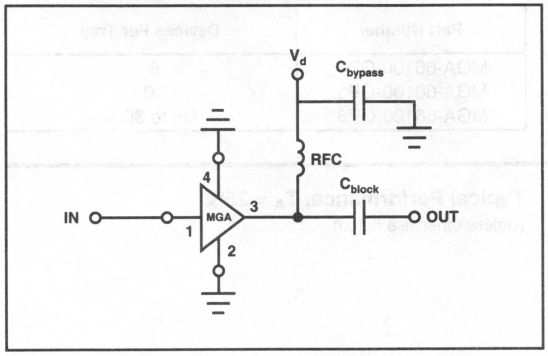


Typical Scattering Parameters: Z_O = 50 Ω

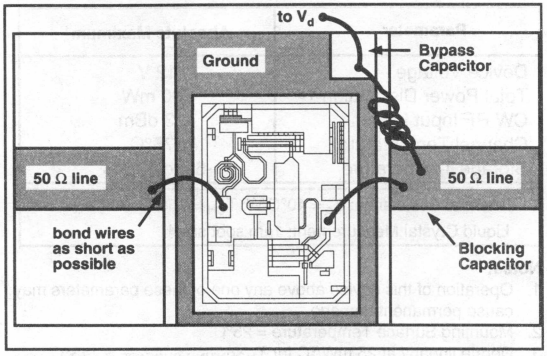
T_A = 25°C, V_d = 10 V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
0.5	.25	39	10.2	3.23	14	-29.8	.032	-8	.36	-41
1.0	.16	36	12.3	4.12	-2	-32.0	.025	-17	.25	-45
2.0	.10	-22	14.1	5.06	-40	-34.2	.019	-14	.19	-46
3.0	.08	-37	14.5	5.28	-74	-35.9	.016	-11	.16	-54
4.0	.09	-105	14.2	5.15	-109	-38.0	.013	-9	.12	-65
5.0	.14	-152	13.5	4.71	-142	-40.9	.009	2	.09	-77
6.0	.20	176	12.4	4.19	-172	-44.3	.006	18	.07	-69
7.0	.27	141	11.3	3.67	160	-45.5	.005	54	.07	-48
8.0	.37	114	10.1	3.21	135	-45.0	.006	67	.07	-28
9.0	.50	96	8.7	2.73	111	-46.5	.005	90	.05	-10
10.0	.59	86	7.4	2.34	90	-46.8	.005	100	.03	7

Typical Biasing Configuration



Substrate Bonding Diagram



External Elements Required:

- Output DC Blocking Capacitor: 45 pF typical
- RF Choke Network and Bypass Capacitor: 4 turns 1 mil wire; 45 pF typical
- Input and Output RF Transmission Lines: 50 Ω typical

Recommended Die Attach Procedure

1. Die attach should be performed under an inert atmosphere of either nitrogen or forming gas.
2. Set heater block temperature to 300° ± 10°C.
3. Place circuit on heater block and heat thoroughly; typically 5-15 seconds.
4. Place Au-Sn preform on circuit in die attach location, using sufficient quantity to ensure wetting and to produce a fillet around the die.
5. Using sharp tweezers, pick up the die and orient it properly on the circuit.
6. Scrub the die into the preform with a back-and-forth motion taking care not to scratch the top surface of the chip. Continue until wetting occurs; normally within 3 to 4 scrubs.
7. Wetting should occur on 100% of the chip perimeter to form a visible fillet around the die.
8. Remove the circuit from the heater block and allow it to cool in air. Total time for die attach should be less than 10 seconds.

Recommended Wedge Bonding Procedure

1. Set heater block temperature to 260° ± 10°C (If the wedge is heated, the heater block temperature should be lowered slightly from this setting. The exact setting will need to be determined empirically, and will vary from machine to machine).
2. Use prestressed (annealed) gold wire of .0007 or .001 inches diameter.
3. Tip bonding pressure should be between 15 and 20 grams, and should not exceed 20 grams. The footprint left by the wire should be between 1.5 and 2.5 wire diameters across.
4. Proceed with bonding according to machine instructions. Bonds should be made from the circuit to the chip bonding pads to minimize the potential for pad damage. Bonds should be made to the source (common) and drain (output) pads if the MMIC before bonding to the gate (input) pad to minimize the potential for ESD damage.

CAUTION: This device makes use of GaAs FET devices with very small gate geometries. Such devices are subject to damage by electro-static discharge (ESD), and must only be handled by properly grounded personnel working at grounded assembly stations.

HEWLETT PACKARD

MGS-70008
Reflective SPDT GaAs MMIC Switch

Features

- **Single-Pole, Double-Throw Output**
- **Broad Bandwidth: DC to 3 GHz**
- **Low Insertion Loss: 0.8 dB Typical at 1 GHz**
- **Fast Switching Time: 3 ns Typical**
- **Ultra Low DC Power Consumption**
- **Small Surface-Mount Plastic Package**

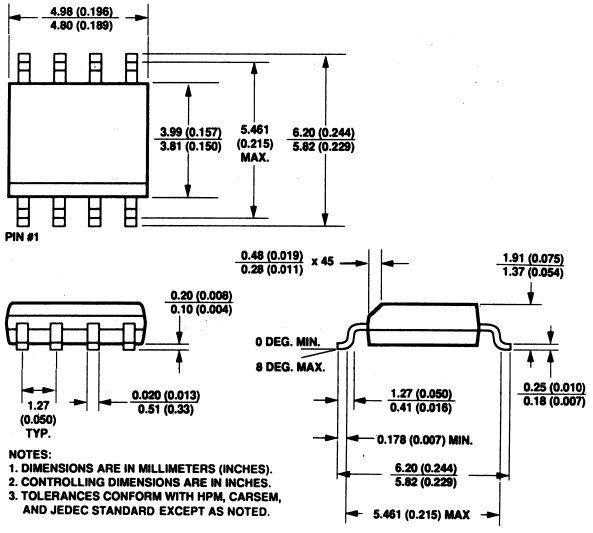
Description

The MGS-70008 is a single-pole, double-throw monolithic GaAs MMIC switch. The J2 and J3 of the MGS-70008 are terminated to ground when "off" (an absorptive version, the MGS-71008, which terminates the "off" port in an internal 50 Ω resistor, is also available). The switches are sealed in a small, plastic, surface-mount SO-8 package. Switching is actuated by a -5 V control voltage per the truth table shown on the next page. -3.3 V operation is also possible with some reduction in P_{1dB} and IP_3.

The MGS-70008 is designed for high volume commercial applications where low insertion loss, high isolation, and fast switching speed are required. Its low cost and high performance make it suitable for a wide variety of uses such as digital cellular, spread spectrum, GPS, and other RF switching applications. Refer to applications note AN-G007 for more application details.

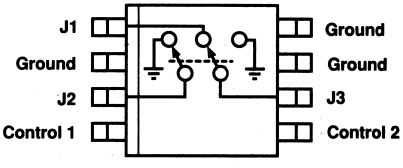
The die is fabricated using HP's nominal 0.7 µm Schottky-barrier-gate, gold metallization, and silicon nitride passivation to achieve excellent performance, uniformity, and reliability.

SO-8 Package



OUTLINE 08A

AC Equivalent Circuit/ Pinout



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions*		Units	Min.	Typ.	Max.
I_C	Control Input Current	DC	µA		12	
BW	Bandwidth		GHz	DC-3		
II	Insertion Loss	200 MHz	dB		0.6	1.0
		1000 MHz	dB		0.8	1.1
		2000 MHz	dB		1.0	1.2
		2500 MHz	dB		1.1	1.5
		3000 MHz	dB		1.2	
ISO	Isolation	200 MHz	dB	50	51	
		1000 MHz	dB	29	33	
		2000 MHz	dB	20	23	
		2500 MHz	dB	16	19	
		3000 MHz	dB		16	
VSWR J1, J2 or J3	Voltage Standing Wave Ration (on port)	DC-2000 MHz	–		1.2:1	1.4:1
		2000 - 3000 MHz	–		1.3:1	1.7:1
VSWR J2 or J3	Voltage Standing Wave Ration (off port)	DC-2000 MHz	–		≥10:1	
		2000 - 3000 MHz	–		≥10:1	
I_{SW}	Switching Speed	10% to 90%	ns		3	
P_{1dB}**	Output @ 1 dB Gain Compression	200 MHz	dBm	16	18.5	
		1000 MHz	dBm	23	26.0	
		2000 MHz	dBm		26.0	
IP_3**	3rd Order Intercept	200 MHz	dBm		41	
		1000 MHz	dBm	40	45	
		2000 MHz	dBm		45	

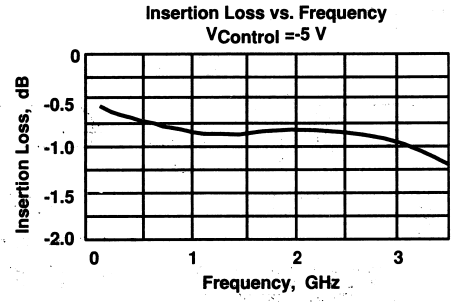
Notes: *Measured in a 50 Ω system at 1 GHz, unless otherwise specified, V_C = -5 V
**Measured in a 50 Ω system with V_C = -7 V

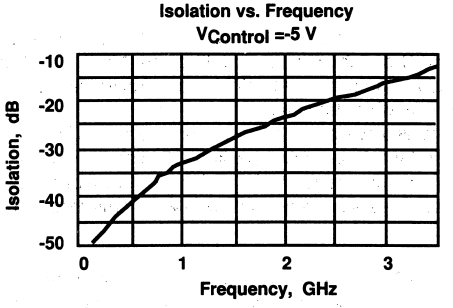
Absolute Maximum Ratings

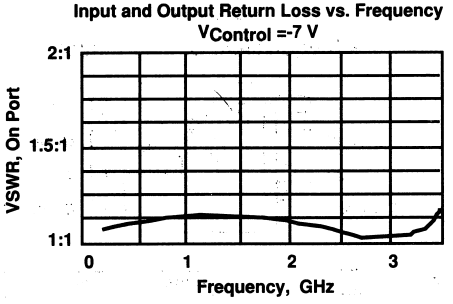
Parameter	Absolute Maximum[1]
Maximum Input Power	
below 500 MHz	+27 dBm
above 500 MHz	+30 dBm
Control Voltage	-8.0 V
Storage Temperature	-65 to +150°C

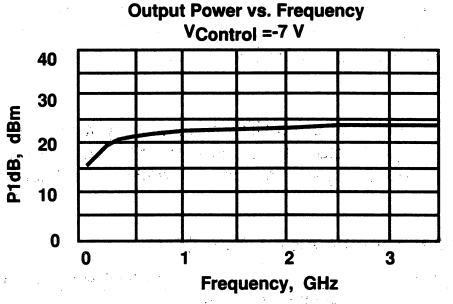
Notes:
1. Operation of this device above any one of these limits may cause permanent damage.

Typical Performance, T_A = 25°C
(unless otherwise noted)









MGS-70008 Truth Table (Typical Performance at 1 GHz)

	Control Input		Insertion Loss		Return Loss		
	C1	C2	J1-J2	J1-J3	J1	J2	J3
	0 V	0 V	16 dB	16 dB	1 dB	1 dB	1 dB
For normal SPDT use	0 V	-5 V	33 dB	.8 dB	22 dB	1 dB	22 dB
For normal SPDT use	-5 V	0 V	.8 dB	33 dB	22 dB	22 dB	1 dB
	-5 V	-5 V	19 dB	19 dB	1 dB	1 dB	1 dB

MGS-70008 Typical Power Performance vs. Frequency and Control Voltage (V_C)
(All other typical specifications remain constant.)

	V_C= -7V		V_C = -5V		V_C = -3.3V	
Frequency	P_{1dB}	IP_3	P_{1dB}	IP_3	P_{1dB}	IP_3
200 MHz	18.5 dBm	41 dBm	18.0 dBm	41 dBm	16.5 dBm	35 dBm
1000 MHz	26.0 dBm	45 dBm	23.7 dBm	44 dBm	17.5 dBm	38 dBm
2000 MHz	26.0 dBm	45 dBm	23.0 dBm	44 dBm	16.0 dBm	38 dBm

Typical Scattering Parameters: ON Switch Port

$Z_O = 50\ \Omega$, $T_A = 25°C$, $V_C = -5$ V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
MHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
.2	.04	-6.2	-.6	.93	-4.5	-.6	.934	-4.4	.04	-2.5
.4	.04	0.3	-.6	.93	-8.5	-.6	.934	-8.3	.03	10.6
.6	.04	7.6	-.6	.93	-12.7	-.6	.930	-12.4	.03	30.7
.8	.05	13.6	-.6	.93	-16.8	-.7	.927	-16.3	.04	52.8
1.0	.06	14.7	-.6	.93	-21.0	-.7	.927	-20.4	.05	63.0
1.2	.07	14.5	-.6	.93	-25.7	-.6	.931	-24.5	.07	67.1
1.4	.09	14.0	-.6	.93	-30.3	-.6	.930	-28.7	.08	69.1
1.6	.10	10.2	-.6	.93	-34.8	-.6	.930	-32.9	.10	69.2
1.8	.11	8.1	-.6	.93	-39.4	-.6	.928	-37.6	.10	66.6
2.0	.11	1.4	-.6	.93	-44.5	-.6	.928	-41.8	.11	65.2
2.2	.11	-3.2	-.7	.92	-49.9	-.7	.922	-46.8	.09	62.2
2.4	.10	-8.5	-.8	.91	-54.5	-.7	.927	-51.5	.09	60.8
2.6	.08	-13.1	-.7	.92	-58.9	-.7	.920	-56.2	.07	60.0
2.8	.05	-14.1	-.7	.92	-64.0	-.7	.922	-62.4	.04	70.8
3.0	.01	7.4	-.8	.91	-69.0	-1.0	.894	-68.7	.02	127.9
3.2	.04	141.4	-1.1	.88	-75.0	-1.3	.864	-74.4	.05	-178.2
3.4	.11	143.2	-1.2	.87	-79.2	-1.7	.823	-79.9	.10	-169.4
3.6	.17	129.5	-1.4	.85	-81.7	-1.6	.828	-85.7	.12	-178.5
3.8	.22	135.9	-1.3	.86	-85.4	-2.1	.788	-91.8	.19	-168.0
4.0	.32	133.2	-1.6	.83	-94.4	-3.0	.708	-95.0	.22	165.6
4.2	.37	129.2	-2.2	.78	-96.8	-3.7	.652	-99.2	.24	166.9
4.4	.46	128.5	-2.0	.79	-98.4	-4.2	.619	-102.5	.30	163.4

Typical Scattering Parameters: OFF Switch Port

$Z_O = 50\ \Omega$, $T_A = 25°C$, $V_C = -5$ V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
MHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
.2	.05	5.6	-50.0	.00	92.1	-44.4	.006	92.4	.81	176.3
.4	.05	20.6	-40.0	.01	94.2	-38.4	.012	95.2	.82	172.6
.6	.06	36.0	-35.0	.02	98.1	-35.4	.017	100.3	.83	168.9
.8	.09	39.3	-31.9	.03	100.9	-32.4	.024	104.4	.83	165.3
1.0	.11	35.8	-30.5	.03	103.9	-30.5	.030	108.5	.85	161.6
1.2	.13	30.9	-28.0	.04	103.6	-28.4	.038	110.4	.86	158.3
1.4	.14	25.0	-26.0	.05	107.5	-26.4	.048	116.2	.87	154.9
1.6	.15	18.9	-24.4	.06	107.0	-24.7	.058	116.8	.89	151.9
1.8	.16	14.5	-23.1	.07	108.5	-23.0	.071	119.6	.90	148.6
2.0	.16	10.6	-21.9	.08	105.9	-21.6	.083	118.0	.92	146.7
2.2	.17	7.8	-20.0	.10	105.3	-19.9	.101	118.6	.92	145.0
2.4	.17	3.0	-19.2	.11	105.4	-18.8	.115	119.8	.95	143.1
2.6	.18	-2.9	-17.7	.13	103.9	-16.9	.143	120.4	.95	141.7
2.8	.16	-9.2	-16.5	.15	102.1	-15.7	.165	119.3	.98	141.2
3.0	.14	-19.6	-14.9	.18	98.5	-13.9	.202	116.4	.99	140.6
3.2	.11	-33.2	-14.0	.20	97.6	-12.2	.246	115.5	1.01	139.6
3.4	.06	-78.5	-12.0	.25	88.8	-10.3	.307	105.1	1.00	139.0
3.6	.08	-156.7	-10.5	.30	79.5	-8.4	.379	89.9	.91	140.4
3.8	.13	153.0	-11.1	.28	70.0	-10.3	.306	77.4	.94	146.5
4.0	.18	134.3	-11.7	.26	68.9	-8.6	.370	88.3	1.26	142.8
4.2	.22	129.6	-10.8	.29	72.1	-7.8	.407	85.3	1.33	133.7
4.4	.27	128.9	-9.9	.32	72.0	-6.8	.458	83.0	1.45	131.6

HEWLETT PACKARD

MGS-70018
MGS-71018
SPDT GaAs Switches

Features

- **Broad Bandwidth: DC to 4.6 GHz**
- **High Isolation: >45 dB typ @ 1 GHz**
- **Fast Switching Speed: 2 ns Typical**
- **Surface Mount Package**
- **Reflective and Absorptive Versions**

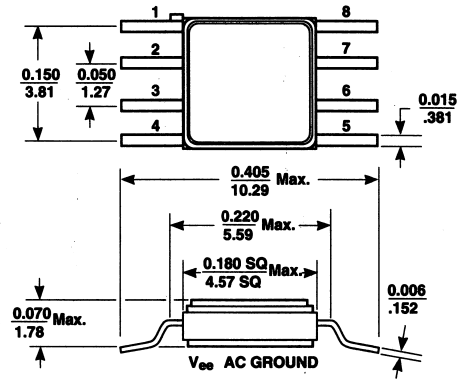
Description

The MGS-70018 is a broadband, single-pole, double-throw monolithic reflective GaAs switch which terminates "off" signals to ground. The MGS-71018 is an absorptive version which terminates "off" signals to a 50 Ω load. These devices come packaged in a small 8-leaded glass/metal hermetically sealed package designed for surface mounting. Switching is actuated by a –5 V control voltage per the truth table below. Current draw for the ON port is less than 100 μA.

These products are designed for cost effective, fast switching speed applications where low insertion loss and high isolation are desired. Their wide bandwidth and isolated control ports make them suitable for a broad variety of uses. Typical applications include instrumentation, communications circuits, radar circuits, and ECM systems.

The die is fabricated using HP's nominal 0.7 μm Schottky-barrier gate, gold metallization, and silicon nitride passivation to achieve excellent performance, uniformity, and reliability.

180 mil Package



PIN DESCRIPTION	
1 Control-2	8 RF Out-2
2 RF IN	7 Ground
3 Control-1	6 Ground
4 Ground	5 RF Out-1
Bottom of Package is Ground	

Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
in .xxx = ±.005
mm .xx = ±.13

Truth Table		
Control 1	-5 V	0 V
Control 2	0 V	-5 V
RF Out 1	ON	OFF
RF Out 2	OFF	ON

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions[2]:		Unit	MGS-70018 Reflective Min.	Typ.	Max.	MGS-71018 Absorptive Min.	Typ.	Max.
BW	Bandwidth		GHz	DC		4.6	DC		4.6
IL	Insertion Loss	200 MHz	dB		0.7	0.9		0.9	1.1
		1.0 GHz	dB		0.9	1.2		1.3	1.4
		4.6 GHz	dB		1.7	2.0		1.9	2.4
ISO	Isolation	200 MHz	dB	47	55		50	55	
		1.0 GHz	dB	37	40		42	45	
		4.6 GHz	dB	30	33		30	35	
VSWR	On				1.4			1.4	
	Off				N/A			1.4	
t_{SW}	Switching Speed	10% to 90%	ns		2			3	
P_{OUT}	Output Power	200 MHz	dBm	+16	+17		+16	+17	
	@ 1 dB Compression	4.6 GHz	dBm	+23	+25		+23	+25	
IP_3	3rd Order Intercept	1.0 GHz	dBm	+40	+45		+40	+45	

Note: 1. Measured in a 50 Ω system at 1 GHz, unless otherwise specified, at -5 V control voltage, except P_{OUT} and IP_3 at -7 V control voltage.

Absolute Maximum Ratings[1]

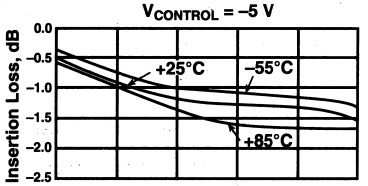
Parameter	Absolute Maximum
Maximum Input Power	
below 500 MHz	+27 dBm
above 500 MHz	+30 dBm
Control Voltage	-8.0 V
Storage Temperature	-65 to 150°C

Note: 1. Operation of this device above any one of these parameters may cause permanent damage.

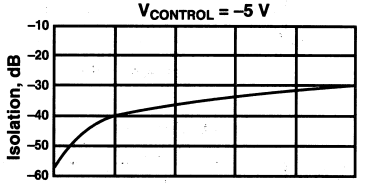
MGS-70018
SPDT GaAs FET Switch (Reflective)

Typical Performance, T_A = -55°C to +85°C
(Unless otherwise noted)

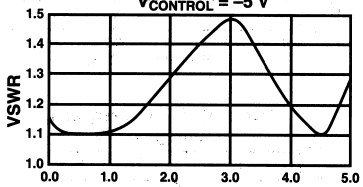
Insertion Loss vs. Frequency
$V_{CONTROL}$ = −5 V



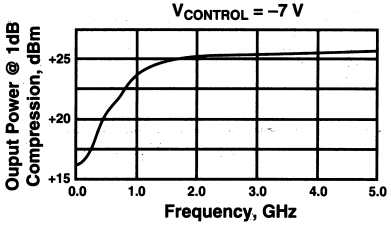
Isolation vs. Frequency
$V_{CONTROL}$ = −5 V



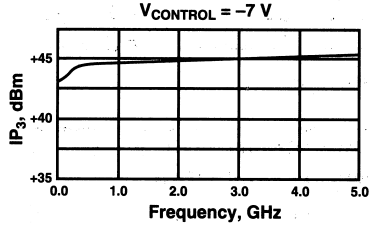
Input VSWR vs. Frequency
$V_{CONTROL}$ = −5 V



Output Power vs. Frequency
$V_{CONTROL}$ = −7 V



3rd Order Intercept vs. Frequency
$V_{CONTROL}$ = −7 V



Typical MGS-70018 Scattering Parameters: Z_O = 50 Ω
T_A = 25°C, $V_{control\ 1}$ = -5 V, $V_{control\ 2}$ = 0 V
Test Ports: Input to RF Out 1 (ON)

Freq.	S_{11}			S_{21}			S_{12}			S_{22}		
GHz	SWR	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	SWR	Mag	Ang
0.1	1.1	.04	-21	-0.5	.94	20	-0.5	.94	20	1.1	.04	-22
0.5	1.1	.04	-54	-0.7	.92	101	-0.7	.92	101	1.1	.04	-44
1.0	1.1	.05	-22	-0.8	.91	-156	-0.8	.91	-156	1.1	.06	-17
1.5	1.2	.10	17	-0.9	.90	-55	-0.9	.90	-54	1.3	.11	5
2.0	1.3	.13	16	-1.2	.88	47	-1.2	.88	47	1.4	.15	27
2.5	1.4	.16	19	-1.2	.87	151	-1.3	.86	151	1.4	.18	52
3.0	1.5	.20	24	-1.3	.86	-102	-1.3	.87	-103	1.6	.24	61
3.5	1.3	.15	15	-1.3	.85	-1	-1.3	.86	1	1.5	.19	57
4.0	1.2	.07	-26	-1.3	.86	98	-1.3	.87	98	1.1	.06	-19
4.5	1.1	.05	38	-1.4	.84	-159	-1.4	.85	-160	1.3	.13	-98
5.0	1.3	.15	75	-1.6	.83	-60	-1.4	.85	-61	1.1	.06	-83

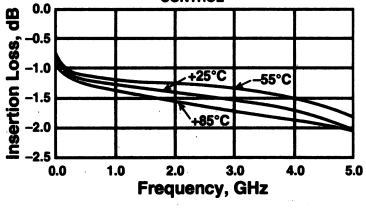
Typical MGS-70018 Scattering Parameters: Z_O = 50 Ω
T_A = 25°C, $V_{control\ 1}$ = -5 V, $V_{control\ 2}$ = 0 V
Test Ports: Input to RF Out 2 (OFF)

Freq.	S_{11}			S_{31}			S_{13}			S_{33}		
GHz	SWR	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	SWR	Mag	Ang
0.1	1.1	.06	-15	-56	.00	-60	-63	.00	-78	9.6	.81	177
0.5	1.1	.05	-55	-43	.01	-15	-43	.00	-25	8.5	.79	167
1.0	1.1	.04	-34	-39	.01	55	-39	.01	51	7.4	.76	147
1.5	1.2	.08	26	-36	.01	134	-36	.01	138	6.7	.74	130
2.0	1.3	.13	28	-36	.02	-140	-36	.02	-134	7.2	.76	106
2.5	1.5	.20	23	-35	.02	-35	-35	.02	-33	7.8	.77	106
3.0	1.6	.25	19	-35	.02	77	-35	.02	68	8.2	.78	98
3.5	1.5	.19	11	-34	.02	168	-34	.02	170	8.1	.78	96
4.0	1.3	.13	-8	-32	.02	-96	-32	.02	-95	7.1	.75	90
4.5	1.3	.13	15	-32	.02	-7	-32	.02	20	6.3	.73	68
5.0	1.4	.15	47	-30	.03	88	-31	.03	90	7.1	.75	39

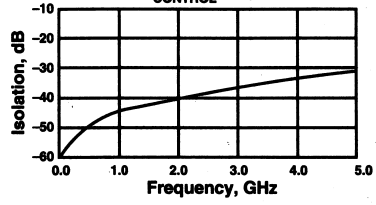
MGS-71018
SPDT GaAs FET Switch (Absorptive)

Typical Performance, T_A = -55°C to +85°C
(Unless otherwise noted)

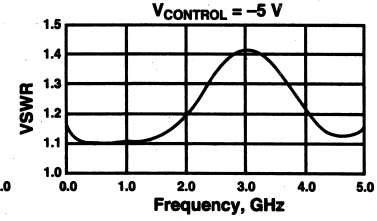
Insertion Loss vs. Frequency
$V_{CONTROL}$ = –5 V



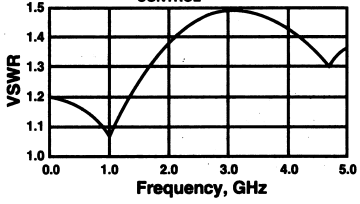
Isolation vs. Frequency
$V_{CONTROL}$ = –5 V



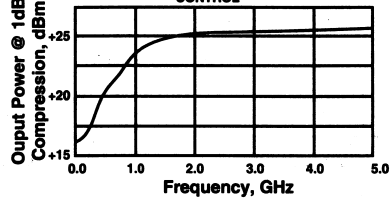
Input VSWR vs. Frequency
$V_{CONTROL}$ = –5 V



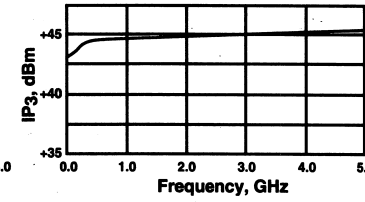
Output VSWR vs. Frequency
$V_{CONTROL}$ = –5 V



Output Power vs. Frequency
$V_{CONTROL}$ = –7 V



3rd Order Intercept vs. Frequency
$V_{CONTROL}$ = –7 V



Typical MGS-71018 Scattering Parameters: Z_O = 50 Ω
T_A = 25°C, $V_{control\ 1}$ = -5 V, $V_{control\ 2}$ = 0 V
Test Ports: Input to RF Out 1 (ON)

Freq.	S_{11}			S_{21}			S_{12}			S_{22}		
GHz	SWR	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	SWR	Mag	Ang
0.1	1.1	.06	-22	-0.87	.91	19	-0.87	.91	19	1.1	.06	-24
0.5	1.1	.06	-57	-1.0	.88	100	-1.0	.88	100	1.1	.06	-52
1.0	1.2	.07	-54	-1.2	.87	-158	-1.2	.87	-159	1.2	.09	-42
1.5	1.2	.07	-17	-1.3	.86	-57	-1.3	.86	-57	1.3	.11	-26
2.0	1.2	.08	-14	-1.5	.85	44	-1.5	.85	44	1.2	.11	1
2.5	1.2	.09	-2	-1.5	.84	147	-1.5	.84	147	1.2	.10	41
3.0	1.3	.12	19	-1.6	.83	-108	-1.6	.84	-108	1.4	.16	66
3.5	1.1	.04	14	-1.6	.82	-10	-1.6	.84	-9	1.2	.09	67
4.0	1.1	.05	-156	-1.7	.82	90	-1.7	.83	90	1.2	.08	-133
4.5	1.2	.09	129	-1.7	.82	-168	-1.7	.82	-170	1.4	.17	-137
5.0	1.4	.17	107	-2.0	.79	-70	-1.9	.81	-71	1.1	.05	178

Typical MGS-71018 Scattering Parameters: Z_O = 50 Ω
T_A = 25°C, $V_{control\ 1}$ = -5 V, $V_{control\ 2}$ = 0 V
Test Ports: Input to RF Out 2 (OFF)

Freq.	S_{11}			S_{31}			S_{13}			S_{33}		
GHz	SWR	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	SWR	Mag	Ang
0.1	1.2	.08	-18	-65	.00	-45	-65	.00	-101	1.0	.02	-154
0.5	1.2	.07	-62	-50	.00	6	-51	.00	-7	1.0	.02	-115
1.0	1.1	.07	-56	-45	.01	90	-45	.01	88	1.1	.04	-43
1.5	1.1	.06	-13	-42	.01	178	-42	.01	180	1.2	.07	-0
2.0	1.2	.08	0	-39	.01	-77	-40	.01	-80	1.2	.11	26
2.5	1.3	.14	3	-40	.01	16	-39	.01	22	1.3	.14	51
3.0	1.4	.17	5	-38	.01	140	-37	.01	142	1.4	.16	70
3.5	1.2	.09	-14	-35	.02	-130	-35	.02	-132	1.3	.14	90
4.0	1.1	.05	-91	-35	.02	-26	-35	.02	-21	1.2	.08	113
4.5	1.1	.03	90	-33	.02	83	-32	.03	82	1.1	.06	-37
5.0	1.3	.12	102	-32	.02	-173	-30	.03	-174	1.3	.14	-21

HEWLETT PACKARD

MGS-71008
Absorptive SPDT GaAs MMIC Switch

Features

- **Single-Pole, Double-Throw Output**
- **Broad Bandwidth: DC to 3 GHz**
- **High Isolation: 37 dB Typical at 1 GHz**
- **Fast Switching Time: 3 ns Typical**
- **Ultra Low DC Power Consumption**
- **Small Surface-Mount Plastic Package**

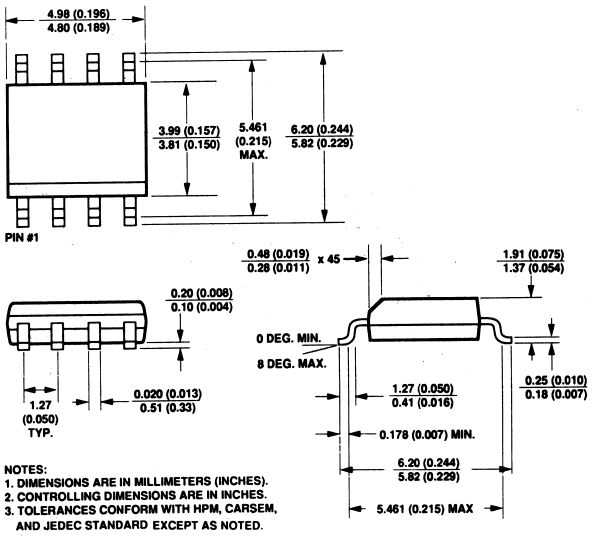
Description

The MGS-71008 is a single-pole, double-throw monolithic GaAs MMIC switch. The J2 and J3 of the MGS-71008 are terminated by internal 50 Ω load resistors when "off" (a reflective version, the MGS-70008, which terminates the "off" port to ground, is also available). The switch is sealed in a small, plastic, surface-mount SO-8 package. Switching is actuated by a -5 V control voltage per the truth table shown on the next page. -3.3 V operation is also possible with some reduction in P_{1dB} and IP_3.

The MGS-71008 is designed for high volume commercial applications where low insertion loss, high isolation, and fast switching speed are required. Its low cost and high performance make it suitable for a wide variety of uses such as digital cellular, spread spectrum, GPS, and other RF switching applications. Refer to applications note AN-G007: for more application details.

The die is fabricated using HP's nominal 0.3 micron recessed Schottky-barrier-gate, gold metallization, and silicon nitride passivation to achieve excellent performance, uniformity, and reliability.

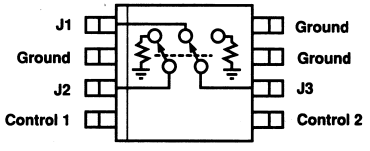
SO-8 Package



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSIONS ARE IN INCHES.
3. TOLERANCES CONFORM WITH HPM, CARSEM, AND JEDEC STANDARD EXCEPT AS NOTED.

OUTLINE 08A

AC Equivalent Circuit/ Pinout



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions*		Units	Min.	Typ.	Max.
I_C	Control Input Current	DC	µA		12	
BW	Bandwidth		GHz	DC-3		
II	Insertion Loss	200 MHz	dB		0.9	1.4
		1000 MHz	dB		1.2	1.5
		2000 MHz	dB		1.3	1.6
		2500 MHz	dB		1.4	1.9
		3000 MHz	dB		1.5	
ISO	Isolation	200 MHz	dB	50	52	
		1000 MHz	dB	30	37	
		2000 MHz	dB	22	26	
		2500 MHz	dB	16	22	
		3000 MHz	dB		16	
VSWR J1, J2 or J3	Voltage Standing Wave Ration (on port)	DC-2000 MHz	–		1.2:1	1.4:1
		2000 - 3000 MHz	–		1.3:1	1.7:1
VSWR J2 or J3	Voltage Standing Wave Ration (off port)	DC-2000 MHz	–		1.2:1	
		2000 - 3000 MHz	–		1.3:1	
ISW	Switching Speed	10% to 90%	ns		3	
P_{1dB}**	Output @ 1 dB Gain Compression	200 MHz	dBm	16	16.5	
		1000 MHz	dBm	23	25.2	
		2000 MHz	dBm		25.2	
IP_3**	3rd Order Intercept	200 MHz	dBm		41	
		1000 MHz	dBm	40	45	
		2000 MHz	dBm		45	

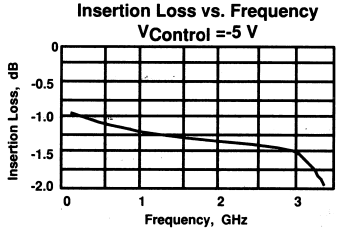
Notes: *Measured in a 50 Ω system at 1 GHz, unless otherwise specified, V_C = -5 V
**Measured in a 50 Ω system with V_C = -7 V

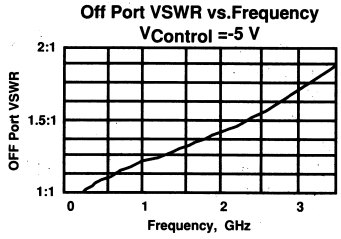
Absolute Maximum Ratings

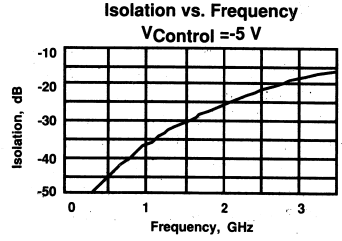
Parameter	Absolute Maximum[1]
Maximum Input Power	
below 500 MHz	+27 dBm
above 500 MHz	+30 dBm
Control Voltage	-8.0 V
Storage Temperature	-65 to +150°C

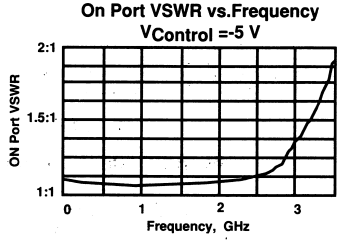
Notes:
1. Operation of this device above any one of these limits may cause permanent damage.

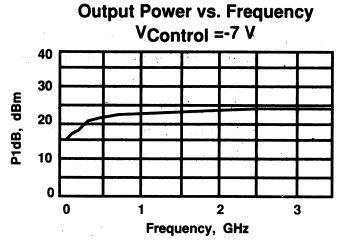
Typical Performance, T_A = 25°C
(unless otherwise noted)











MGS-71008 Truth Table (Typical Performance at 1 GHz)

	Control Input		Insertion Loss		Return Loss		
	C1	C2	J1-J2	J1-J3	J1	J2	J3
	0 V	0 V	16 dB	16 dB	1 dB	1 dB	1 dB
For normal SPDT use	0 V	-5 V	37 dB	1.2 dB	22 dB	22 dB	22 dB
For normal SPDT use	-5 V	0 V	1.2 dB	37 dB	22 dB	22 dB	22 dB
	-5 V	-5 V	26 dB	26 dB	1 dB	1 dB	1 dB

MGS-71008 Typical Power Performance vs. Frequency and Control Voltage (V_C)
(All other typical specifications remain constant.)

	V_C= -7V		V_C = -5V		V_C = -3.3V	
Frequency	P_{1dB}	IP_3	P_{1dB}	IP_3	P_{1dB}	IP_3
200 MHz	16.5 dBm	41 dBm	16.5 dBm	41 dBm	15.5 dBm	35 dBm
1000 MHz	25.2 dBm	45 dBm	23.7 dBm	44 dBm	19.0 dBm	38 dBm
2000 MHz	25.2 dBm	45 dBm	22.5 dBm	44 dBm	18.5 dBm	38 dBm

Typical Scattering Parameters: ON Switch Port

$Z_O = 50\ \Omega$, $T_A = 25°C$, $V_C = -5$ V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
MHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
.2	.05	-18.2	-.9	.90	-5.1	-.9	.904	-5.0	.05	-14.1
.4	.05	-18.3	-.9	.90	-9.4	-.9	.906	-9.2	.04	-10.1
.6	.05	-20.6	-.9	.90	-13.9	-.9	.898	-13.6	.03	-8.2
.8	.05	-18.7	-.9	.90	-18.2	-.9	.898	-17.8	.02	8.9
1.0	.05	-20.4	-1.0	.89	-22.8	-1.0	.890	-22.3	.02	30.5
1.2	.06	-26.3	-1.0	.89	-27.8	-1.0	.893	-26.9	.01	42.3
1.4	.06	-29.1	-1.0	.89	-32.7	-1.0	.891	-31.5	.02	55.2
1.6	.07	-38.1	-1.1	.88	-37.5	-1.0	.889	-36.3	.02	59.1
1.8	.06	-46.4	-1.1	.88	-42.4	-1.1	.884	-41.5	.01	19.1
2.0	.06	-63.8	-1.2	.87	-47.8	-1.1	.879	-46.6	.01	-75.6
2.2	.06	-82.3	-1.2	.87	-53.5	-1.2	.871	-52.2	.03	-103.5
2.4	.07	-109.8	-1.3	.86	-58.5	-1.2	.867	-57.8	.05	-115.3
2.6	.08	-128.7	-1.4	.85	-63.2	-1.4	.851	-62.9	.08	-126.2
2.8	.11	-153.4	-1.5	.84	-68.7	-1.5	.838	-70.0	.11	-134.4
3.0	.14	-169.6	-1.6	.83	-74.0	-2.0	.791	-76.5	.16	-144.1
3.2	.20	178.3	-2.0	.79	-80.3	-2.5	.746	-82.8	.20	-152.8
3.4	.26	167.7	-2.3	.77	-83.8	-3.1	.700	-87.2	.26	-163.4
3.6	.31	154.5	-2.4	.76	-87.3	-3.3	.686	-93.8	.29	-168.1
3.8	.40	152.0	-2.5	.75	-90.3	-4.0	.632	-99.3	.37	-169.7
4.0	.51	145.4	-3.0	.71	-100.2	-4.6	.588	-99.6	.37	167.2
4.2	.63	139.5	-3.3	.68	-101.6	-5.4	.534	-101.6	.43	168.5
4.4	.82	133.0	-3.1	.70	-10 3.8	-6.1	.498	-104.6	.46	162.7

Typical Scattering Parameters: OFF Switch Port

$Z_O = 50\ \Omega$, $T_A = 25°C$, $V_C = -5$ V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
MHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
.2	.06	-9.8	-52.0	.00	73.6	-46.0	.005	74.7	.01	146.5
.4	.05	0.0	-42.4	.01	94.8	-41.9	.008	95.5	.03	130.7
.6	.05	27.3	-36.4	.02	113.0	-36.5	.015	113.7	.05	125.1
.8	.06	20.7	-35.2	.02	92.3	-35.4	.017	93.0	.07	116.9
1.0	.06	21.7	-33.7	.02	106.1	-33.6	.021	107.1	.08	115.7
1.2	.07	20.6	-31.4	.03	114.5	-32.0	.025	116.4	.10	114.8
1.4	.08	15.7	-30.5	.03	122.9	-29.1	.035	125.5	.12	114.6
1.6	.08	-5.6	-28.0	.04	112.0	-27.7	.041	114.2	.14	116.3
1.8	.08	-11.8	-26.0	.05	122.0	-26.2	.049	124.9	.16	115.2
2.0	.07	-17.0	-24.4	.06	121.9	-24.2	.062	125.4	.18	117.1
2.2	.08	-24.6	-21.9	.08	124.3	-22.3	.077	128.3	.21	118.5
2.4	.07	-40.0	-20.9	.09	119.5	-20.4	.095	123.5	.23	117.9
2.6	.06	-46.7	-20.0	.10	119.4	-19.6	.105	124.0	.25	117.8
2.8	.05	-66.2	-18.4	.12	119.0	-17.8	.129	122.9	.27	117.9
3.0	.05	-112.4	-16.5	.15	116.5	-16.1	.157	119.7	.30	118.0
3.2	.08	-158.0	-15.4	.17	111.0	-14.4	.191	113.1	.32	116.2
3.4	.16	170.2	-14.4	.19	100.7	-13.8	.204	100.3	.33	119.8
3.6	.23	158.7	-13.6	.21	100.8	-13.0	.223	96.7	.35	120.5
3.8	.34	146.0	-12.4	.24	97.3	-12.8	.229	90.9	.36	124.0
4.0	.45	138.0	-11.4	.27	83.0	-11.7	.260	78.3	.33	113.0
4.2	.54	129.9	-12.0	.25	82.7	-12.6	.234	78.8	.39	120.7
4.4	.65	125.4	-10.8	.29	81.1	-11.9	.253	74.5	.39	116.1

High Speed Digital Communications Products



High Speed Digital Communications Products

Each device type in this family was developed using one of the high performance, silicon bipolar processes available within Hewlett-Packard. The performance requirements of each device is matched to the most appropriate process. This offers a superior blend of reliability, performance, and manufacturability. Hewlett-Packard's silicon bipolar processes are capable of sub-micron dimensions, and an f_t as high as 25 GHz.

Products in this family operate at data rates as high as 2.8 Gbps, and cover many standard rates for telecom and datacom systems. Product complexity varies from basic building block ICs such as laser drivers, transimpedance amplifier, variable gain control amplifiers, decision circuits, and retiming circuits, to that of complete gigabit rate, subsystem ICs and fiber channel interface cards.

High Speed Digital Communications

Variable Gain Control Amplifiers (Typical Specifications at +25°C Case Temperature)

Part Number	G_P @ (dB)	Gain Control Range (dB)	3 dB Bandwidth (GHz)	P_{1dB} @ 0.5 GHz	Supply Voltage (V)	Device Current (mA)	Package	Page
IVA-05200	30 @ 0.5 GHz	30 @ 0.5 GHz	1.5	-3	5	35	chip	10-100
IVA-05118[a]	30 @ 0.5 GHz	30 @ 0.5 GHz	1.5	-2	5	35	180 mil SM	10-98
IVA-05218[a]	30 @ 0.5 GHz	30 @ 0.5 GHz	1.5	-3	5	35	180 mil SM	10-104
IVA-05208	30 @ 0.5 GHz	30 @ 0.5 GHz	1.5	-3	5	35	SO-8 SM plastic	10-102
HPVA-0180	21 @ 0.3 GHz	20 @ 0.3 GHz	2.5	-3	6	41	SO-8 SM plastic	10-78
IVA-14208	24 @ 1.0 GHz	34 @ 1.0 GHz	2.5		6	3.8	SO-8 SM plastic	10-106
IVA-14228	24 @ 1.0 GHz	34 @ 1.0 GHz	2.5		6	3.8	180 mil hermetic SM	10-106

Transimpedance Amplifiers (Typical Specifications at +25°C Case Temperature)

Part Number	Data Rate (Gb/s)	Bandwidth (GHz)	Gain (W)	Input Current Noise (pA/√Hz)	Supply Voltage (V)	Device Current (mA)	Package	Page
ITA-06300	1.5	1.5	2800	3.5	5	34	chip	10-90
ITA-12300	0.8	0.9	4200	2.8	5	43	chip	10-94
ITA-06318	1.5	1.3	2800	3.5	5	34	180 mil SM	10-92
ITA-12318	0.8	0.75	4200	2.8	5	43	180 mil SM	10-94

Decision Circuits (Typical Specifications at +25°C Ambient Temperature)

Part Number	Maximum Rate (Gb/s)	Amplitude Margin (mV)	Phase Margin (ps)	Data Input Amplitude (mVp-p)	t_r (ps)	t_f (ps)	Package	Page
HDMP-2003	2.0	115	370	—	120	90	HBIC-0.5" SM	10-35
HDMP-2004	2.8	90	190	—	120	90	HBIC-0.5" SM	10-35/113
HDMP-2006	1.5	130	800	—	200	200	SOIC-8 SM hermetic	10-46/114
IDC-51418	1.5	—	620	20	200	190	180 mil SM	10-88

Data and Clock Recovery Circuit (Typical Specifications at +25°C Ambient Temperature)

Part Number	Data Rate (Mb/s)	Lock Time (ms)	Clock & Data Rise & Fall Time (ps)	Jitter Generation (per rms)	Clock Output Voltage (V)	Data Output Voltage (V)	Package	Page
HDMP-2501	600-650	2.3	200	7.5	0.7	0.7	F6 16 lead herrmetic	10-54

Note:
[a] IVA-05118 is single-ended input and IVA-05218 is differential input.

High Speed Digital Communications (cont.)

Laser Driver (Typical Specifications at +25°C Ambient Temperature)

Part Number	Data Rate (Gb/s)	Bandwidth (GHz)	Prebias Current (mA)	Modulation Current (mA)	Input VSWR	Supply Voltage (V)	Package	Page
IDA-07318	1.5	1.0	0-50	5-50	2:1	-5 or -5.2	180 mil SM	10-86

Gigabit Rate Transmit Receive Chip Set

Part Number	Description	Package	Page
HDMP-1000*	Transmitter Receiver Chip set, Parallel data (16, 17, 20, or 21 bits wide) is loaded into the Tx and delivered to the Rx over optical fiber or coax cable. Contains encoding, mux, clock extraction, demux, and decoding.	ceramic quad flat pack (CQFP)	10-5
HDMP-100K	Gigabit Rate Transmit Receive Chipset Evaluation Board. Evaluation board; literature.		10-34

*HDMP-1000 is the Tx/Rx pair. The transmitter chip can be ordered separately as the HDMP-1002; the receiver as the HDMP-1004.

Fiber Channel Optical Link Card

Part Number	Data Rate (Mbaud/s)	Wavelength λ (nm)	Description	Page
HOLC-0266	266	780	Transmitter/Receiver card which implements the emerging ANSI X3T9.3 Fiber Channel Standard (FC-O layer). Contains all functions necessary for sending 10-bit wide encoded data serially. SC connectors.	10-63
HOLC-K266	266	780	Evaluation kit. Two HOLC-0266 cards; 4m SC duplex 50/125 µm cable; electrical connectors; literature.	10-77

HEWLETT PACKARD

Gigabit Rate Transmit Receive Chip Set

Technical Data

HDMP-1000 Tx/Rx Pair
HDMP-1002
Transmitter
HDMP-1004 Receiver

Features

- **Transparent, Extended Ribbon Cable Replacement**
- **High-Speed Serial Rate** 110-1400 MBaud
- **Standard 100K ECL Interface** 16, 17, 20, or 21 Bits Wide
- **Reliable Monolithic Silicon Bipolar Implementation**
- **On-chip Phase-Locked Loops**
  - Transmit Clock Generation
  - Receive Clock Extraction

Applications

- **Point to Point Data Links**
- **Implement SCI-FI Standard**
- **Implement Serial HIPPI Specification**
- **Backplane Extender**

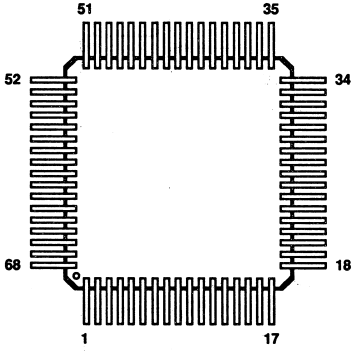
Description

The HDMP-1002 transmitter and the HDMP-1004 receiver are used to build a high speed data link for point to point communication. The HDMP-1000 consists of one HDMP-1002 and one HDMP-1004. The monolithic silicon bipolar transmitter chip and receiver chip are each provided in a standard, 68 pin, ceramic quad flat pack (CQFP).

From the user's viewpoint, these products can be thought of as providing a "virtual ribbon cable" interface for the transmission of data. Parallel data loaded into the Tx (transmitter) chip is delivered to the Rx (receiver) chip over a serial channel, which can be either a coaxial copper cable or optical link.

The chip set hides from the user all the complexity of encoding, multiplexing, clock extraction, demultiplexing and decoding. Unlike other links, the phase-locked-loop clock extraction circuit also transparently provides for frame synchronization - the user is not troubled with the periodic insertion of frame synchronization words. In addition, the dc balance of the line code is automatically maintained by the chip set. Thus, the user can transmit arbitrary data without restriction. The Rx chip also includes a state-machine controller (SMC) that provides a startup handshake protocol for the duplex link configuration.

Package Outline



The serial data rate of the T/R link is selectable in four ranges (see tables on page 3), and extends from 110Mbits/s up to 1.4Gbits/s. The parallel data interface is 16 or 20 bit single-ended ECL, pin selectable. A flag bit is available and can be used as an extra 17th or 21st bit under the user's control. The flag bit can also be used as an even or odd frame indicator for dual-frame transmission. If not used, the link performs expanded error detection. The serial link is synchronous, and both frame synchronization and bit synchronization are maintained. When data is not available to send, the link

maintains synchronization by transmitting fill frames. Two (training) fill frames are reserved for handshaking during link startup.

User control words are supported. If CAV* is asserted at the Tx chip, the least significant 14 or 18 bits of the data are sent and the Rx CAV* line will indicate the data as a control word.

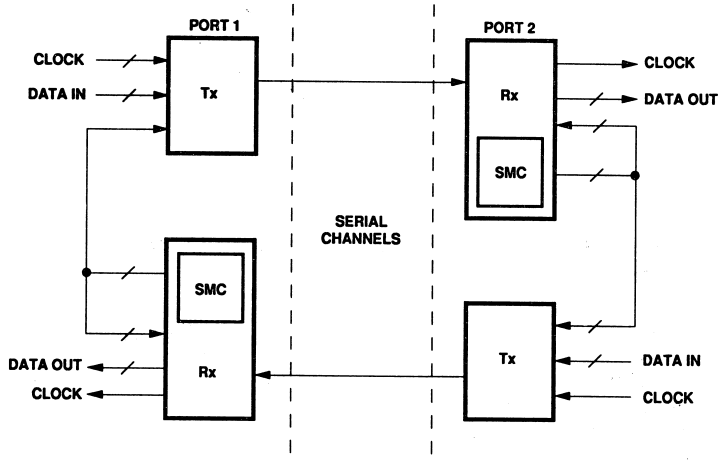


Figure 1. Point-to-Point Gigabit Data Link.

HDMP-1002 (Tx), HDMP-1004 (Rx) Absolute Maximum Ratings

T_c = 25°C, except as specified. Operation in excess of any one of these conditions may result in permanent damage to this device.

Symbol	Parameter	Units	Minimum	Maximum
V_{EE}	Supply Voltage	V	-7	+0.5
$V_{IN,ECL}$	ECL Input Voltage	V	-3	+0.5
$V_{IN,BBL}$	H50 Input Voltage	V	-2	+1
$I_{O,ECL}$	ECL Output Source Current	mA		+50
T_{stg}	Storage Temperature	°C	-40	+130
T_J	Junction Temperature	°C	-40	+130
T_{max}	Maximum Assembly Temperature (for 10 seconds maximum)	°C		+260

HDMP-1002 (Tx), HDMP-1004 (Rx)
Guaranteed Operating Rates For 16 Bit Mode[1]

T_c = 0°C to +85°C, V_{EE} = -4.5 V to -5.5 V

DIV1	DIV0	Parallel Word Rate (Mbit/sec)		Serial Data Rate (Mbit/sec)		Serial Baud Rate (MBaud)	
		Min.	Max.	Min.	Max.	Min.	Max.
0	0	42.5	65	680	1040	850	1300
0	1	21.3	41	340	656	425	820
1	0	10.6	20.7	169.6	332	212	415
1	1	5.5	10.2	88	164	110	205

Note:
1. Extended operating rates to 1520 MBaud/sec (typ) are possible for T_c = 0°C to +55°C.

HDMP-1002 (Tx), HDMP-1004 (Rx)
Guaranteed Operating Rates For 20 Bit Mode[1]

T_c = 0°C to +85°C, V_{EE} = -4.5 V to -5.5 V

DIV1	DIV0	Parallel Word Rate (Mbit/sec)		Serial Data Rate (Mbit/sec)		Serial Baud Rate (MBaud)	
		Min.	Max.	Min.	Max.	Min.	Max.
0	0	35.4	58.3	708.3	1166.7	850	1400
0	1	17.7	34.2	354.2	683.3	425	820
1	0	8.8	17.3	176.6	345.8	212	415
1	1	4.6	8.5	91.7	170.8	110	205

Note:
1. Extended operating rates to 1640 MBaud/sec (typ) are possible for T_c = 0°C to +55°C.

HDMP-1002 (Tx), HDMP-1004 (Rx)
DC Electrical Specifications

T_c = 0°C to +85°C, V_{GND} = Ground, V_{EE} = -4.5 V to -5.5 V

Symbol	Parameter	Unit	Minimum	Typical	Maximum
$V_{IH,ECL}$	ECL Input High Voltage Level, Guaranteed high signal for all inputs	mV	-1150		
$V_{IL,ECL}$	ECL Input Low Voltage Level, Guaranteed low signal for all inputs	mV			-1600
$V_{OH,ECL}$	ECL Output High Voltage Level, Terminated with 300 Ω to -2.0 V	mV	-1050		
$V_{OL,ECL}$	ECL Output Low Voltage Level, Terminated with 300 Ω to -2.0 V	mV			-1500
$V_{IP,H50}$	H50 Input Peak-to-Peak Voltage	mV	200		
$V_{OH,BLL}$	BLL Output High Voltage Level, Terminated with 50 Ω to -1.3 V	V		-0.9	
$V_{OL,BLL}$	BLL Output Low Voltage Level, Terminated with 50 Ω to -1.3 V	V		-1.70	
$V_{OP,BLL}$	BLL Output Peak-to-Peak Voltage, Terminated with 50 Ω, ac coupled	V		+0.8	
$I_{EE,Tx}$	Transmitter V_{EE} Supply Current, with HCLKSEL off, V_{EE} = -5.0 V, T_c = 25°C	mA		+340	
$I_{EE,Rx}$	Receiver V_{EE} Supply Current, V_{EE} = -5.0 V, T_c = 25°C	mA		+427	

HDMP-1002 (Tx), HDMP-1004 (Rx)
AC Electrical Specifications, T_c = 25°C

Symbol	Parameter	Unit	Min.	Typ.	Max.
$t_{r,ECL}$	ECL Rise Time, (20-80%), Terminated with 300 Ω to -2.0 V	nsec		1	
$t_{f,ECL}$	ECL Fall Time, (80-20%), Terminated with 300 Ω to -2.0 V	nsec		2	
$t_{r,BLL}$	BLL Rise Time, (20-80%), Terminated with 50 Ω, ac coupled	psec		170	
$t_{f,BLL}$	BLL Fall Time, (80-20%), Terminated with 50 Ω, ac coupled	psec		200	
$VSWR_{i,H50}$	H50 Input VSWR			2:1	
$VSWR_{o,BLL}$	BLL Output VSWR			2:1	

HDMP-1002 (Tx)
Timing Characteristics

T_c = 0°C to +85°C, V_{EE} = -4.5 V to -5.5 V

Symbol	Parameter	Unit	Min.	Typ.	Max.
t_s	Setup Time, for Rising Edge of STRBIN Relative to D_0-D_{19}, ED, FF, DAV*, CAV*, and FLAG	nsec		2.0	
t_h	Hold Time, for Rising Edge of STRBIN Relative to D_0-D_{19}, ED, FF, DAV*, CAV*, and FLAG	nsec		2.0	
t_d	Delay Time, from Rising Edge of STRBIN to First Data Bit Out (D_0)	nsec		1.0	
ΔT_{strb}	STRBOUT - STRBIN Delay	nsec	1	3	5

HDMP-1004 (Rx)
Timing Characteristics

T_c = 0°C to +85°C

Symbol	Parameter	Unit	Min.	Typ.	Max.
t_{d1}	Synchronous Output Delay	nsec		2.0	
t_{d2}	State Machine Output Delay	nsec		4.0	

HDMP-1002 (Tx), HDMP-1004 (Rx)
Typical Lock-Up Time, T_c = 25°C

DIV1	DIV0	HDMP-1002, msec	HDMP-1004, msec	LINK[1], msec
0	0	2.0	2.2	2.5
0	1	3.0	3.2	3.5
1	0	4.5	4.7	5.0
1	1	8.0	11.0	12.0

Note:
1. Measured in Local Loop-Back mode with the state machine engaged and 0 cable length.

HDMP-1002 (Tx)
Thermal Characteristics, T_A = 25°C

Symbol	Parameter	Units	Typical
θ_{jc}	Thermal Resistance Die to Case	°C/Watt	12
P_D	Power Dissipation, V_{EE} = -5 V	Watt	1.75

HDMP-1004 (Rx)
Thermal Characteristics, T_A = 25°C

Symbol	Parameter	Units	Typical
θ_{jc}	Thermal Resistance Die to Case	°C/Watt	12
P_D	Power Dissipation, V_{EE} = -5 V	Watt	2.25

I/O Type Definitions

I/O Type	Definition
I-ECL	Input ECL. Similar to 100K ECL, but with pull-down. Thus, if the input is left unconnected, the buffer generates a default value of "0". The input can also be directly connected to ground to generate a "1".
O-ECL	Output ECL. Similar to 100K ECL but should be terminated with RTT ≥300 Ω, and do not exceed 10 cm connection distance.
IT-ECL	Input Test ECL. Can be turned off when not used.
OT-ECL	Output Test ECL. Can be turned off when not used.
O-BLL	50 Ω buffer line logic output driver. Will put out ECL levels if terminated with 50 Ω to -1.3 V, otherwise can be AC coupled to drive any 50 Ω loads. It can also drive the I-H50 inputs through differential direct coupling. Note: all unused outputs should be terminated with 50 Ω to ground.
I-H50	Input with internal 50 Ω terminations. Input is diode level shifted so that it can swing around ground. Can be driven with single-end configuration. Commonly used with input single-end AC coupling from an O-BLL driver or another 50 Ω source, or differential direct coupling from an O-BLL driver.
C	Filter capacitor node.
S	Power supply or ground.

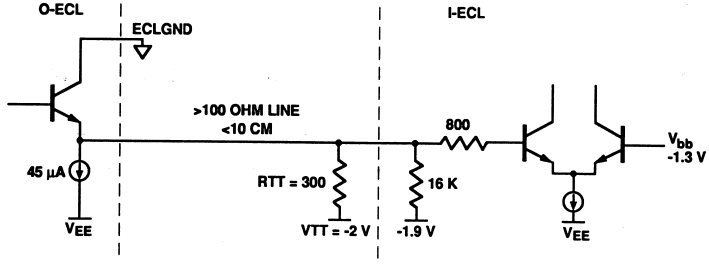


Figure 2. O-ECL and I-ECL Simplified Circuit Schematic.

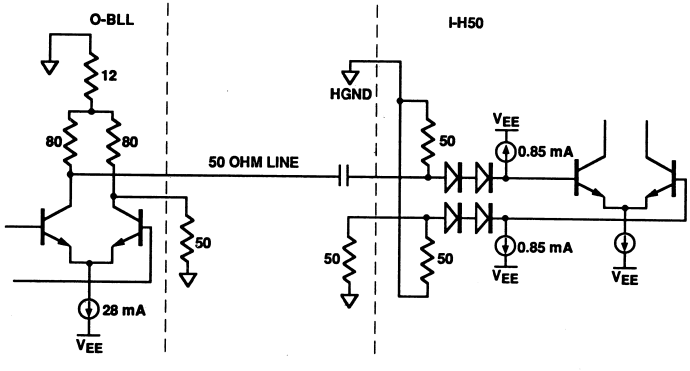


Figure 3. O-BLL and I-H50 Simplified Circuit Schematic.

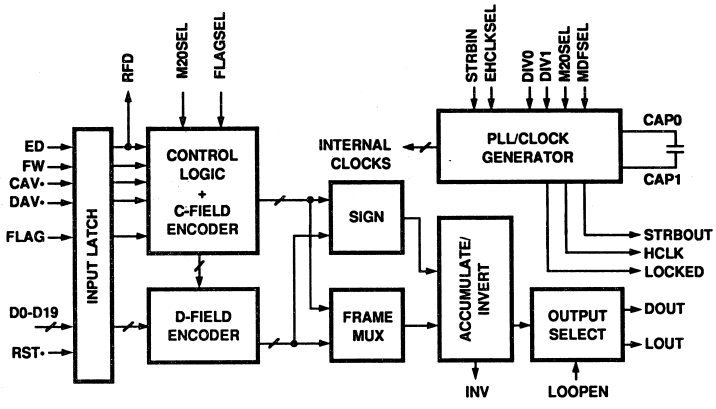


Figure 4. HDMP-1002 (Transmitter) Block Diagram.

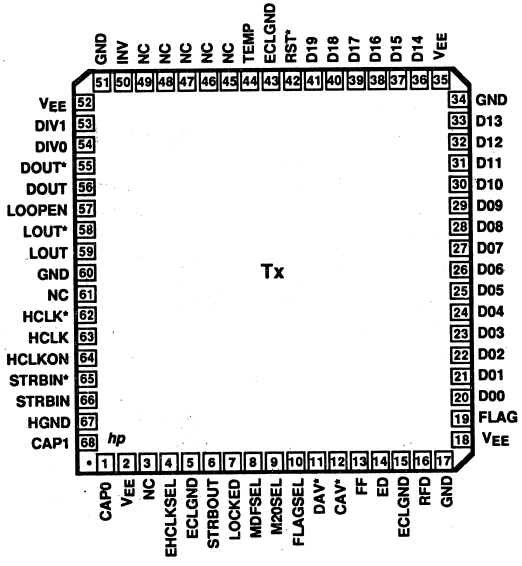


Figure 5. HDMP-1002 Package Layout, Pin View.

Tx I/O Definition

Name	Pin	Type	Signal
D00 D01 D02 D03 D04 D05 D06 D07 D08 D09 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19	20 21 22 23 24 25 26 27 28 29 30 31 32 33 36 37 38 39 40 41	I-ECL	**Data Inputs:** 20 Bit data is encoded and transmitted when M20SEL is active; otherwise the 16 least significant bits are encoded and transmitted. The encoded bits are transmitted LSB first, e.g.: D0 is sent first, through to either D15 or D19, followed by the 4 coding bits C0-C3.
FLAG	19	I-ECL	**Extra Flag Bit:** When FLAGSEL is active, this input is sent as an extra data bit in addition to the normal Data inputs. When FLAGSEL is not Asserted, this input is ignored and the transmitted Flag bit is internally alternated to allow the Rx chip to perform enhanced frame error detection.
DAV*	11	I-ECL	**Data Available Input:** This active-low input tells the chip that the user has valid data to be transmitted. This pin should be asserted only after the user has determined that the RFD line is active for a given frame cycle. When this pin is asserted, the information on the Data and Flag inputs is encoded and sent as a Data frame.
CAV*	12	I-ECL	**Control Word Available Input:** This active-low input tells the chip that the user is requesting a control word be transmitted. This pin should only be asserted after the user has determined the RFD line is active for a given frame cycle. When this pin is asserted, the information on the Data inputs is sent as a control frame. If CAV and DAV are asserted simultaneously, CAV takes precedence.
RFD	16	O-ECL	**Ready for Data:** Output to tell the user the Link is ready to transmit data. This pin is a retimed version of the ED input, which is driven by the Rx chip state machine controller.
STRBIN STRBIN*	66 65	I-H50	**Data Clock Input:** When EHCLKSEL is low, this input is phase locked and multiplied to generate the high speed serial clock. The chip expects a clock frequency which is equal to the input frame rate if MDFSEL (double frame mode) is low, and 1/2 the frame rate if MDFSEL is high. When EHCLKSEL is high, the PLL is bypassed, and STRBIN directly becomes the high speed serial clock. In all cases, STRBOUT is derived from the high speed serial clock, and the input data is latched in on the rising edge of STRBOUT.

Tx I/O Definition (cont'd.)

Name	Pin	Type	Signal
STRBOUT	6	O-ECL	**Frame-rate Data Clock Output:** This output is always a frame rate clock derived from STRBIN. Input data is latched on the rising edge of STRBOUT. With a buffer or pulled down with a 1 K resistor to V_{EE} and ac-coupled, this output is ideal for triggering an oscilloscope for examining the serial output eye pattern DOUT or LOUT.
DOUT DOUT*	56 55	O-BLL	**Normal Serial Data Output:** Output used when LOOPEN is not active. This output is a special *buffer line logic* driver which is a 50 Ω back-terminated ECL compatible output.
LOUT LOUT*	59 58	O-BLL	**Loop Back Serial Data Output:** Output used when LOOPEN is active. Typically, this output will be used to drive the LIN, LIN* inputs of the Rx chip.
LOOPEN	57	I-ECL	**Loop Back Control:** Input which controls whether the DOUT, DOUT* or the LOUT, LOUT* outputs are currently enabled. If active, LOUT, LOUT* are enabled. The unused output is powered down to reduce dissipation.
FLAGSEL	10	I-ECL	**Flat Bit Mode Select:** When this input is high, the extra FLAG bit input is sent as an extra transparent data bit. Otherwise, the FLAG input is ignored and the transmitted flag bit is internally alternated by the transmitter. The Rx chip can provide enhanced frame error detection by checking for strict alternation of the flag bit during data frames. The FLAGSEL input on the Rx chip should be set to the same value as the Tx FLAGSEL input.
M20SEL	9	I-ECL	**16 or 20 Bit Word Select:** When this signal is high, the link operates in 20 Bit data transmission mode. Otherwise, the link operates in 16 Bit mode.
MDFSEL	8	I-ECL	**Select Double Frame Mode:** When this signal is high, the PLL expects a 1/2 speed parallel clock at STRBIN. The chip then internally multiplies this clock and produces a full-rate parallel clock at STRBOUT. This feature is provided so that either a 40 bit or 32 bit word can be easily transmitted as two 20, or two 16 bit words. When MDFSEL is low, the PLL expects a full-rate parallel clock at STRBIN, and returns a locked replica of STRBIN on the STRBOUT pin. In both modes Data is latched on the rising edge of STRBOUT.
DIV0 DIV1	54 53	ECL	**VCO Divider Select:** These two pins program the VCO divider chain to operate at full speed, half speed, quarter speed, or one-eighth speed.
RST*	42	I-ECL	**Chip Reset:** This active-low pin initializes the internal chip registers. It should be asserted during power up for a minimum of 5 parallel-rate clock cycles to ensure a complete reset.
ED	14	I-ECL	**Enable Data:** This signal comes from the Rx chip state machine and is used to control the RFD output of the Tx chip. The state machine only allows data to be enabled when both sides of the link have established stable lock.

Tx I/O Definition (cont'd.)

Name	Pin	Type	Signal
FF	13	I-ECL	**Fill Frame Select:** When neither CAV or DAV is asserted, or when ED is false, fill frames are automatically transmitted to allow the Rx chip to maintain lock. The type of fill frame sent is determined by the state of this pin. FF0s are sent if low, and either FF1a or FF1b is sent if FF is high. The choice of FF1a or FF1b is determined by the state of the cumulative line DC balance.
LOCKED	7	O-ECL	**Loop In-lock Indication:** This signal indicates the lock status of the Tx PLL. A high value indicates lock. This signal is normally connected to the SMTRST1 reset input of the Rx state machine to force the link into the start-up state until the Tx PLL has locked. This signal may give multiple false-lock indications during the acquisition process, so should be debounced if it is used for any other purpose than to drive the Rx chip.
CAP0D CAP0S CAP1D CAP1S	1 1 68 68	C	**Loop Filter Capacitor:** A loop filter capacitor may be connected across the CAP0 and CAP1 inputs to increase the loop time constant. The packaged part contains a nominal capacitance internally so that under normal conditions no external capacitor is required.
INV	50	O-ECL	**Invert Signal:** A high value of INV implies that the current frame is being sent inverted to maintain long-term DC balance. With a buffer, or pulled down with a 1K resistor to V_{EE} and ac coupled, this signal is useful as an aid to analyzing the serial output stream with an oscilloscope.
TEMP	44	T	**Temperature Sense Diode:** Used during wafer and package test only. It should be left open otherwise.
HCLKON	64	I-ECL	**HCLK Power-down Control:** When this pin is de-asserted, the HCLK, HCLK* outputs are powered down to reduce power dissipation.
HCLK HCLK*	63 62	O-BLL	**High Speed Clock Monitor:** Used to monitor actual clock signal used to transmit the serial data. This signal will either be the divided VCO output, or the divided external clock input, depending on the value of the EHCLKSEL input.
EHCLKSEL	4	I-ECL	**EHCLK Enable:** When active, this input causes the STRBIN inputs to be used for the transmit serial clock, rather than the internal VCO clock. This is useful for generating extremely low jitter test signals, or for operating the link at speeds that are not within the VCO range. When the EHCLKSEL is active, it is necessary for the data source to take its clock from the link rather than the usual operation where the Link phase-locks onto the data source clock.
GND	60 51 34 17	S	**Ground:** Normally 0 volts. This ground is used for everything other than the noisy ECL outputs

Tx I/O Definition (cont'd.)

Name	Pin	Type	Signal
HGND	67	S	**High Speed Ground:** Normally 0 volts. This ground is used to provide a clean reference for STRBIN and STRBIN* inputs. For optimum impedance matching, it is suggested that the physical distance between this pin and the ground plane be minimized.
ECLGND	43 15 5	S	**ECL Ground:** Normally 0 volts. This ground is used for the ECL pad drivers. For best performance it is suggested that coupling of the noisy ECLGND to the clean GND and HGND grounds be minimized.
V_{EE}	52 35 18 2	S	**Power:** Normally -5 V ± 10%.

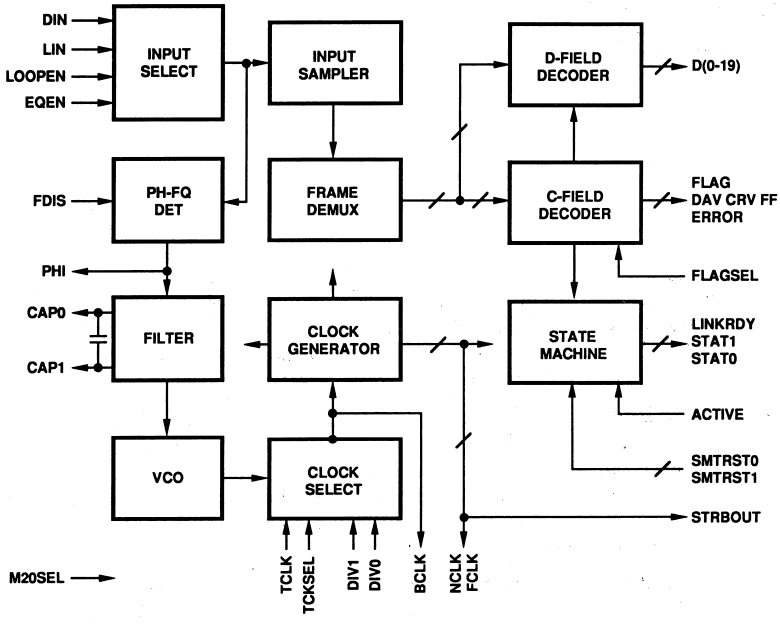


Figure 6. HDMP-1004 (Receiver) Block Diagram.

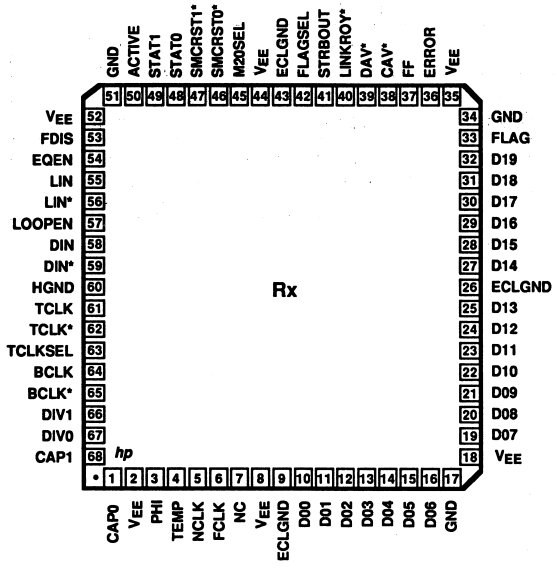


Figure 7. HDMP-1004 (Rx) Package Layout, Pin View.

Rx I/O Definition

Name	Pin	Type	Signal
DIN DIN*	58 59	I-H50	**Normal Serial Data Input:** This is the input used when LOOPEN is not active. When LOOPEN is high, the loop back data inputs LIN, LIN* are used instead. An optional cable equalizer may be enabled for the DIN, DIN* inputs by asserting EQEN.
LIN LIN*	55 56	I-H50	**Loop Back Serial Data Input:** Use this input when LOOPEN is active. Unlike the DIN, DIN* inputs, this input does not have a cable equalizer. In normal usage, this input will be connected to the Tx chip LOUT, LOUT* outputs. This allows the user to check the near-end functionality of the Tx and Rx pair independent of the transmission medium.
LOOPEN	57	I-ECL	**Loop Back Control:** When asserted, this signal causes the loop back inputs LIN, LIN* to be used instead of the normal data inputs DIN, DIN*.
EQEN	54	I-ECL	**Enable Input for Cable Equalization:** When asserted, this signal activates the cable equalization amplifier on the DIN, DIN* serial data inputs.

Rx I/O Definition (cont'd.)

Name	Pin	Type	Signal
D00 D01 D02 D03 D04 D05 D06 D07 D08 D09 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19	10 11 12 13 14 15 16 19 20 21 22 23 24 25 27 28 29 30 31 32	O-ECL	**Data Outputs:** 20 Bit data is received and decoded when M20SEL is active; otherwise 16 bit data is decoded and the D16-D19 bits are undefined.
FLAG	33	O-ECL	**Flag Bit:** If both Tx and Rx have FLAGSEL asserted, this output indicates the value of the transmitted flag bit, then this received bit can be treated just like an extra data bit. If both Tx and Rx have FLAGSEL set to low, FLAG is used to differentiate the even frame from the odd frame in the line code.
LINKRDY*	40	O-ECL	**Link Ready Indicator:** This active-low output is a retimed version of the ACTIVE input. ACTIVE is normally driven by the Rx state machine output. LINKRDY then indicates that the startup sequence is complete and that the data and control indications are valid.
DAV*	39	O-ECL	**Data Available Output:** This active-low output indicates that the Rx chip data outputs are received Data frames. Data should be latched on the rising edge of STRBOUT. Note that during link startup, false data indications may be given. If the user is concerned about this possibility, then the DAV indication should be combined with the LINKRDY output before being used.
CAV*	38	O-ECL	**Control Frame Available Output:** This active-low output indicates that the Rx chip data outputs are receiving Control Frames. False CAV indications may be generated during link startup.
FF	37	O-ECL	**Fill Frame Status:** During a given STRBOUT clock cycle, if neither DAV, CAV, or ERROR are active, then the currently received frame is a Fill frame. The type of Fill frame received is indicated by the FF pin. If FF is low, then FF0 has been received. If FF is high, then either FF1a or FF1b has been received.
ERROR	36	O-ECL	**Received Data Error:** Asserted when a frame is received that does not correspond to either a *valid* Data, Control, or Fill frame encoding.When FLAGSEL is not active, the Rx chip also tests for strict alternation of flag bits during data frames. A flag bit alternation error will also cause an ERROR indication.

Rx I/O Definition (cont'd.)

Name	Pin	Type	Signal
STRBOUT	41	O-ECL	**Recovered Frame-rate Data Clock Output:** This output is the PLL recovered frame rate clock. D0-D19, FLAG, DAV CAV, FF, LINKRDY, and ERROR should all be latched on the rising edge of STRBOUT.
FLAGSEL	42	I-ECL	**Flag Bit Mode Select:** When this input is high, the extra FLAG bit output is effectively an extra transparent data bit. Otherwise, the FLAG bit is checked for alternation during data frames. Any break in strict alternation results in an ERROR indication to the user.
M20SEL	45	I-ECL	**16 or 20 Bit Word Select:** When this signal is high, the link operates in 20 Bit data reception mode. Otherwise, the link operates in 16 Bit mode and data outputs D16-D19 are undefined.
DIV0 DIV1	67 66	I-ECL	**VCO Divider Select:** These two pins program the VCO divider chain to operate at full speed, half speed, quarter speed or one-eighth speed.
FDIS	53	I-ECL	**Frequency Detector Disable Input:** When active, this input disables the Rx PLL Frequency detector and enables a phase detector. The Frequency detector is used during the start-up sequence to acquire wide-band lock on Fill Frames, but must be disabled prior to sending data patterns. This input is normally controlled by the Rx state machine.
ACTIVE	50	I-ECL	**Chip Enable:** This input is normally driven by the Rx state machine output. The ACTIVE signal is internally retimed by STRBOUT and presented to the user as the LINKRKDY signal. This is how the Rx state machine signals the user that the start-up sequence is complete.
SMCRST0* SMCRST1*	46 47	I-ECL	**State Machine Reset Inputs:** Each of these active-low input pins reset the Rx state machine to the initial start-up state. This initiates a complete PLL restart and handshake at both ends of the duplex link. Normally, SMCRST0* is connected to a power-up reset circuit or a host system reset signal. The SMCRST1* input is normally connected to the Tx LOCKED output. The LOCKED signal holds the state-machine in the start-up state until the Tx PLL is locked.
STAT0 STAT1	48 49	O-ECL	**State Machine Status Outputs:** These outputs indicate the current state-machine state. They are used to directly control the Tx ED, Tx FF, Rx FDIS, and Rx ACTIVE lines.
CAP0D CAP0S CAP1D CAP1S	1 1 68 68	C	**Loop Filter Capacitor:** A loop filter capacitor may be connected across the CAP0 and CAP1 inputs to increase the loop time constant. The packaged part contains a nominal capacitance internally so that under normal conditions no external capacitor is required. Each package pin is split into two die pads: suffixed "D" for drive and "S" for sense. This enables a four-point probe arrangement to be used to reduce noise in the loop.

Rx I/O Definition (cont'd.)

Name	Pin	Type	Signal
PHI	3	O-ECL	**Phase Detector Test Output:** The output from the phase/ frequency detector in the Rx PLL. When PHI is high, the VCO should increase frequency. If low, the VCO should decrease frequency.
NCLK	5	O-ECL	**Nibble Clock Monitor:** Leave unterminated in normal use.
FCLK	6	O-ECL	**Frame Clock Monitor:** Leave unterminated in normal use.
TEMP	4	T	**Temperature Sense Diode:** Used during wafer and package test only. It should be left open otherwise.
BCLK BCLK*	64 65	O-BLL	**VCO Monitor Output:** These pins provide access to the internal VCO clock.
TCLKSEL	63	I-ECL	**Enable Test Clock Input:** When this input is active, the TCLK, TCLK* inputs are used in place of the normal VCO signal. This feature is useful both for synchronous systems and for chip testing.
TCLK TCLK*	61 62	I-H50	**External VCO Replacement Test Clock:** When TCLKSEL is enabled, this input is used in place of the normal VCO signal, effectively disabling the PLL and allowing the user to provide an external retiming clock for testing.
GND	17 34 51	S	**Ground:** Normally 0 volts. This ground is used for all the core logic other than the output drivers.
HGND	60	S	**High Speed Ground:** Normally 0 volts. This ground is used to provide clean references for the high speed DIN, DIN*, LIN, LIN*, TCLK, TCLK* inputs.
ECLGND	9 26 43	S	**ECL Ground:** Normally 0 volts. This ground is used for the ECL pad drivers. For best performance it is suggested that coupling of the noisy ECLGND to the clean GND and HGND grounds be minimized.
V_{EE}	2 8 18 35 44 52	S	**Power:** Normally -5 V ± 10%
NC	5 6 7	B	**Pins Not Connected:** Pins that are not used, or are reserved for future use. No connection should be made to any of these signals to ensure compatibility with future releases.

HDMP-1002 (Tx) Timing

Figure 8 shows the Tx timing diagram. Under normal operation, the Tx PLL locks to the STRBIN input with an internal frame clock. This frame clock is buffered to form STRBOUT with a delay of ΔT_{strb}. For the case when MDFSEL is low, INFRMCLK is a phase locked version of STRBIN. If MDFSEL is high, it is assumed that STRBIN is a one half frame rate clock and INFRMCLK is twice the frequency of STRBIN. If EHCLKSEL is high, the Tx uses the external high-speed clock from STRBIN instead of its internal VCO, and generates the appropriate INFRMCLK from the STRBIN inputs. When M20SEL is high, INFRMCLK is 1/24th the frequency of HCLK. When M20SEL is low, INFRMCLK is 1/20th the frequency of HCLK.

The input signals, D0-D19, ED, FF, CAV*, DAV*, and FLAG are latched on the rising edge of INFRMCLK. These inputs must be valid for the set-up time (t_s) before the rising edge and for the hold time (t_h) after the rising edge of INFRMCLK.

The start of a frame in the high speed serial output occurs after a delay of (t_d) after the rising edge of INFRMCLK.

The LOCKED output will stay low for at least 2 frame rate clock cycles when lock is lost.

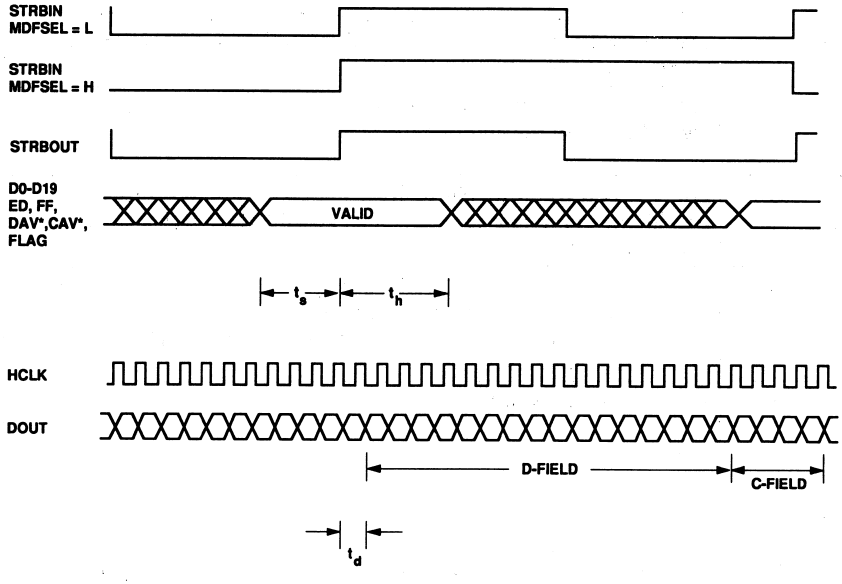


Figure 8. HDMP-1002 (Tx) Timing Diagram.

HDMP-1004 (Rx) Timing

Figure 9 is the Rx timing diagram when the internal phase-locked loop is in synchronization with the incoming serial data. When the PLL is locked, the BCLK's frequency is the same as the input data rate. The nibble clock, NCLK, is derived from the BCLK and a divide-by-4 divider. The size of the input data frame can be either 24 bits (6 nibbles) or 20 bits (5 nibbles), depending on the setting of M20SEL. Whatever the frame size, the FCLK rising edge is located at the frame's boundary, while the falling edge is at the frame's center. STRBOUT is an inverted version of FCLK.

In Figure 9, the Synchronous Outputs are the Rx's output signals clocked by STRBOUT. They are LINKRDY*, FLAG, DAV, CAV, FF, ERROR, and D00-D19. The Synchronous Outputs are updated for every data frame, and changed at the falling edge of STRBOUT. There is a delay of two frames between the serial input and the Synchronous Outputs. As for the state machine status outputs, STATI and STATO, they are also changed upon the STRBOUT's falling edge, but are only updated once in 128 frames.

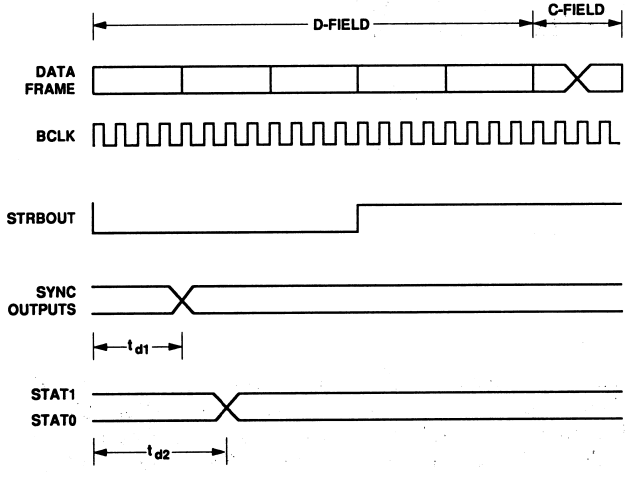


Figure 9. HDMP-1004 (Rx) Timing Diagram.

Line Code Description

The HDMP-1000 line code, Conditional Invert Master Transition (CIMT), is illustrated in Figure 10. The CIMT line code uses three types of frames; Data frames, Control frames, and Fill frames. Fill frames are internally generated by the Tx chip for use during link start up and when there is no input from the user. Each frame consists of a Data Field (D-Field) followed by a Coding Field (C-Field). The D-Field can be either 16 bit or 20-bits wide, depending on link configuration. The C-Field has a master transition which serves as a fixed timing reference for the receivers clock recovery circuit. Users can send arbitrary data carried by Data or Control Frames. The dc balance of the line code is automatically enforced by the Tx. Fill frames have a single rising edge at the master transition which is used for clock recovery and frame synchronization at the receiver.

Detailed coding schemes are described in the following subsections. All the tables given in this section show data bits in the same configuration as a scope display. In other words, the leftmost bit in each table is the first bit to be transmitted in time, while the rightmost bit is the last bit to be transmitted.

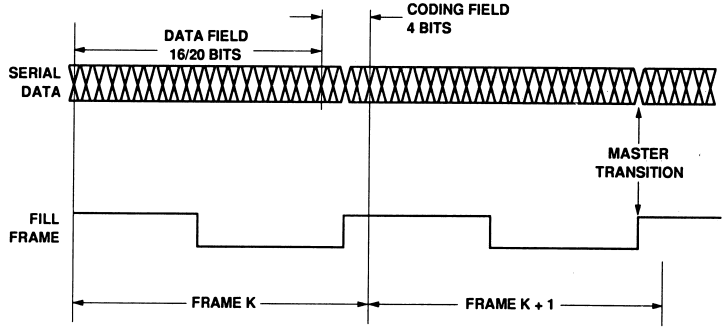


Figure 10. HDMP-1000 (Tx/Rx Pair) Line Code.

Data Frame Codes

When not in FLAGSEL mode, the FLAG bit is not user controllable and is alternately sent as 0 and 1 by the Tx chip during data frames to provide enhanced error detection. Control and Fill frames do not cause toggling between even and odd frames to occur (The FLAG bit is not available during control frames). The receiver performs a differential detection to make sure that every data frame received is the opposite pattern from the previous frame. If a break in the strict alternation is observed, a frame error is flagged by asserting the Rx ERROR output. This pattern detection makes it impossible for a static input data pattern to generate an undetectable false lock point in the transmitted data stream. The detection also reduces the probability that the loop could lock onto random data at a point away from the true master transition for any significant time before it would be detected as a false lock. This mode can detect all single-bit errors in the C-field (non-data bit fields) of the frame.

When the chip is in FLAGSEL mode, the extra FLAG bit is freely user definable as an extra data bit. This provides a 17th bit in 16 bit mode, and a 21st bit in 20 bit mode. The probability of undetected false lock is higher, but the users (e.g., SCI-FI) that need the extra bit can detect false lock at a higher level of the network protocol with CRCs, etc. If the higher level protocols consistently receive wrong data, they can initiate a link restart by resetting the Rx state machine.

HDMP-1002 (Tx), HDMP-1004 (Rx)

Operating Modes

M20SEL	FLAGSEL	Description
0	0	16 bit data plus EO checking
0	1	16 bit data plus FLAG
1	0	20 bit data plus EO checking
1	1	20 bit data plus FLAG

HDMP-1002 (Tx), HDMP-1004 (Rx)

Data Frame Structure
M20SEL Not Asserted (16 bit data mode)

Data Status	Flag Bit	D-Field	C-Field
True	0	$D_0 - D_{15}$	1101
Inverted	0	$\overline{D_0 - D_{15}}$	0010
True	1	$D_0 - D_{15}$	1011
Inverted	1	$\overline{D_0 - D_{15}}$	0100

HDMP-1002 (Tx), HDMP-1004 (Rx)

Data Frame Structure
M20SEL Asserted (20 bit data mode)

Data Status	Flag Bit	D-Field	C-Field
True	0	$D_0 - D_{19}$	1101
Inverted	0	$\overline{D_0 - D_{19}}$	0010
True	1	$D_0 - D_{19}$	1011
Inverted	1	$\overline{D_0 - D_{19}}$	0100

Control Frame Codes

There are 2^{18} control words provided in 20 bit mode. If the user desires to send a control word, his lower 9 bits (D_0-D_8) are sent as bits D0-D8 of the D-Field. The user's next 9 bits (D_9-D_{17}) are sent as bits D11-D19 of the D-Field. The control frame is either inverted or not inverted as needed to maintain balance, with the coding bits 0011 used to indicate true control, and the bits 1100 used to indicate complement control. The bits D9 and D10 are always forced to 0 1 for true control frames and 1 0 for complement control frames. These middle bits are used to distinguish true control frames from fill frames, which always have the middle bits set to either 00, 11, or 10. Similarly, there are 2^{14} control words provided in 16 bit mode.

HDMP-1002 (Tx), HDMP-1004 (Rx)

Control Frame Structure
M20SEL Not Asserted (16 bit mode)

D-Field				C-Field			
D0 - D6	D7	D8	D9 - D15	C0	C1	C2	C3
$D_0 - D_6$	0	1	$D_7 - D_{13}$	0	0	1	1
$\overline{D_0 - D_6}$	1	0	$\overline{D_7 - D_{13}}$	1	1	0	0

HDMP-1002 (Tx), HDMP-1004 (Rx)

Control Frame Structure
M20SEL Asserted (20 bit mode)

D-Field				C-Field			
D0 - D8	D9	D10	D11 - D19	C0	C1	C2	C3
$D_0 - D_8$	0	1	$D_9 - D_{17}$	0	0	1	1
$\overline{D_0 - D_8}$	1	0	$\overline{D_9 - D_{17}}$	1	1	0	0

Fill Frame Codes

Two logical fill frames are provided: FF0 and FF1. FF0 is physically a 50% duty cycle wave form with its sole rising edge occurring between C1 and C2. Logical FF1 toggles between two different physical codes, the first of which advances the falling edge of FF0 by one bit, the second of which retards the falling edge of FF0 by one bit. Two logical fill frame types are required for link start up in duplex mode.

HDMP-1002 (Tx), HDMP-1004 (Rx)

Fill Frame Structure
M20SEL Not Asserted (16 bit mode)

Fill Frame	D-Field			C-Field
0	1111111	10	0000000	0011
1a	1111111	11	0000000	0011
1b	1111111	00	0000000	0011

HDMP-1002 (Tx), HDMP-1004 (Rx)

Fill Frame Structure
M20SEL Asserted (20 bit mode)

Fill Frame	D-Field			C-Field
0	111111111	10	000000000	0011
1a	111111111	11	000000000	0011
1b	111111111	00	000000000	0011

HDMP-1004 (Rx)

Detectable Error States
M20SEL Not Asserted (16 bit mode)

D-Field			C-Field
xxxxxxx	xx	xxxxxxx	x00x
xxxxxxx	xx	xxxxxxx	x11x
xxxxxxx	0x	xxxxxxx	1100
xxxxxxx	11	xxxxxxx	1100
xxxxxxx	xx	xxxxxxx	1010
xxxxxxx	xx	xxxxxxx	0101

HDMP-1004 (Rx)

Detectable Error States
M20SEL Asserted (20 bit mode)

D-Field			C-Field
xxxxxxxxx	xx	xxxxxxxxx	x00x
xxxxxxxxx	xx	xxxxxxxxx	x11x
xxxxxxxxx	0x	xxxxxxxxx	1100
xxxxxxxxx	11	xxxxxxxxx	1100
xxxxxxxxx	xx	xxxxxxxxx	1010
xxxxxxxxx	xx	xxxxxxxxx	0101

Tx Operation Principles

The HDMP-1002 (Tx) is implemented in a high performance silicon bipolar process. The Tx performs the following functions for link operation:

- Phase lock to frame rate clock
- Clock multiplication
- Frame Encoding
- Multiplexing

In normal operation, the Tx phase locks to a user supplied frame rate clock and multiplies the frequency to produce the high speed serial clock. When locked, the Tx indicates that it is locked by asserting the LOCKED output. When the ED input is asserted, the Tx asserts the RFD signal indicating that it is now ready to transmit data or control frames.

The Tx can accept either 16 or 17 bit data and produce a 20 bit frame. It also can accept 20 or 21 bit data and produce a 24 bit frame. Similarly, either 14 bit or 18 bit control words can be transmitted in a 20 bit or 24 bit frame respectively.

Tx Encoding

A simplified block diagram of the transmitter is shown in Figure 4. The PLL/Clock Generator Block locks onto the incoming frame rate (or one-half frame rate) clock and multiplies it up to the serial clock rate. It also generates all the internal clock signals required on the Tx chip.

The data inputs, D0-D19, as well as the control signals; ED, FF, DAV*, CAV*, and FLAG are latched in on the rising edge of the frame rate clock. The data field is then encoded depending on the state of the control signals. At the same time, the coding field is generated. At this point, the entire frame has been constructed in parallel form and its sign is determined. This frame sign is compared with the accumulated sign of previously transmitted bits to decide whether to invert the frame. If the sign of the current frame is the same as the sign of the previously transmitted bits, then the frame is inverted. If the signs are opposite, the frame is not inverted. No inversion is performed if the frame is a fill frame.

The Output Select block allows the user to select between two sets of differential high speed serial outputs. This is useful for loop back testing. If LOOPEN is high, LOUT is enabled and DOUT is disabled. If LOOPEN is low, DOUT is enabled and LOUT is disabled.

The active-low RST* input resets the internal registers to a balanced state. This pin should be held low for at least five frame rate clock cycles to ensure a complete reset.

The Data Field and Control Field are encoded depending on ED, FF, DAV*, CAV*, FLAG, FLAGSEL, M20SEL as well as two internally generated signals, O/E and ACCMSB.

When FLAGSEL is high, O/E is equivalent to FLAG. This is equivalent to adding an additional bit to the data field. When FLAGSEL is low, O/E alternates between high and low for data frames. This allows the link to perform more extensive error detection when the extra bit is unused.

ACCMSB is the sign of the previously transmitted data. This is used to determine which type of FF1 should be sent. When ACCMSB is low, FF1a is sent and when ACCMSB is high, FF1b is sent. This effectively drives the accumulated offset of transmitted bits back toward the balanced state.

Tx Phase-Locked Loop

The block diagram of the transmitter phase-locked loop is shown in Figure 11. It consists of a sequential frequency detector, loop filter, VCO, clock generation circuitry and a lock indicator. The outputs of the frequency detector pass through a charge pump filter that controls the center frequency of the VCO. These outputs also go to the VCO directly to effectively add a zero in the loop response. An external high-speed clock can be used instead of the VCO clock. This is accomplished by applying a high signal to EHCLKSEL and a differential clock to STRBIN.

One of four frequency bands may be selected by applying appropriate inputs to DIV0 and DIV1. The VCO or STRBIN frequency is divided by N, where N is 1, 2, 4 or 8 corresponding to the binary number represented by DIV1, DIV0. This divided version of the VCO clock or STRBIN is used as the serial rate clock and is available as a differential signal at the HCLK output.

A clock generator block creates all the clock signals required for the chip. Depending on M20SEL, STRBOUT is either HCLK/20 or HCLK/24. If MDFSEL is low, then

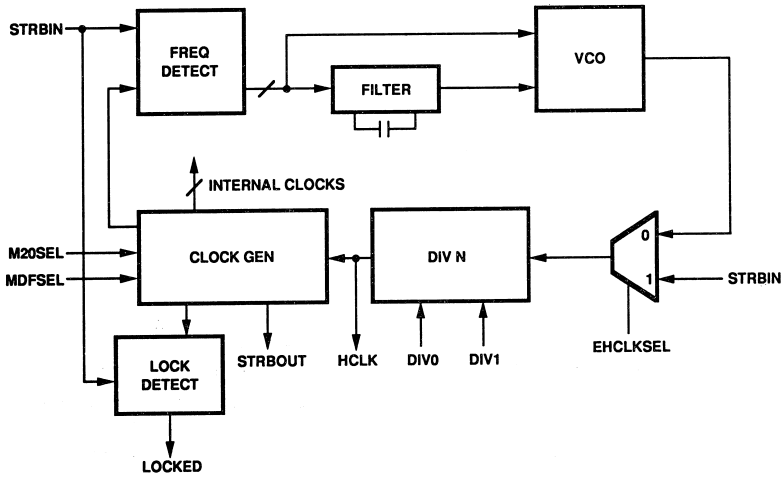


Figure 11. HDMP-1002 (Tx) Phase-Locked Loop.

STRBOUT is a phase-locked version of STRBIN. If MDFSEL is high, STRBOUT is twice the frequency of STRBIN.

The lock detect circuit samples STRBIN with phase shifted versions of STRBOUT. If the samples are not the proper values, the LOCKED signal goes low and stays low for at least two frames.

Rx Operation Principles

The HDMP-1004 (Rx) is monolithically implemented in a high performance 25 GHz f_t bipolar process. When properly configured, the Rx can accept 20B/24B CIMT line code frames, and then output parallel 16B/17B/20B/21B Data Words or 14B/18B Control Words. The Rx provides the following functions for link operation:

- Clock recovery
- Frame synchronization
- Data recovery
- Demultiplexing
- Frame decoding
- Frame error detection
- Link state control

Rx Encoding

Figure 6 shows a simplified block diagram of the receiver. The data path consists of an Input Select, an Input Sampler, a Frame Demultiplexer, a Coding Field (C-Field) Decoder, and a Data Field (D-Field) Decoder. An on-chip phase-locked loop (PLL) is used to extract timing reference from the serial input (DIN or LIN). The PLL includes a Phase-Frequency Detector, a Loop Filter, and a variable-frequency oscillator (VCO). All the Rx internal clock signals are generated from a Clock Generator. The Clock Generator can be driven either by the internal VCO or an external signal, TCLK, depending on the Clock Select configuration.

Integrated on the chip is a Link-Control State Machine for link status monitoring and link startup. Figure 12 shows the details of the Input Selector. The Input Selector chooses either the nominal serial data (DIN) or the loop back (LIN) signal for the Input Sampler's input. If loop back enable (LOOPEN) is asserted, the LIN input is selected. Included in the Input Selector is cable equalization circuitry. When coaxial cable is used as the transmission media, by setting EQEN=1 (enable equalization), the equalization circuitry is in the DIN signal path and provides fixed compensation for high-frequency cable loss.

The Data Field of the CIMT line code can be either 16-bits or 20-bits wide. The width selection for the Rx is made by setting the input pin M20SEL (Figure 6). If M20SEL = 1, then the Rx is configured to accept serial input with 20-bit data field (24 bits per frame). When M20SEL = 0, 16-bit data field is selected.

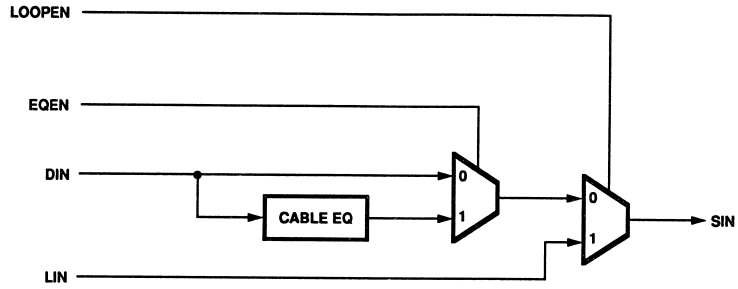


Figure 12. HDMP-1004 (Rx) Input Selector.

HDMP-1004 (Rx) Phase-Locked Loop

A more detailed block diagram for the Rx phase-locked loop (PLL) is shown in Figure 13. In the PLL, the phase of the serial input, SIN, is compared with synchronizing signals from the internal clock generator, using either a phase detector or a frequency detector. The frequency detector disable signal, FDIS, selects which detector to use. If synchronization in a link has yet to be established, the HDMP-1002 (Tx) should send out Fill Frame 0 (FF0) or Fill Frame 1 (FF1) to the remote Rx. By setting FDIS=0, the Rx uses the frequency detector to align its internal clock with the rising edge of FF0/FF1. Once this is accomplished, FDIS can be set to 1, then the PLL uses only the phase detector for synchronization adjustment and the Rx is ready to accept data. Due to the narrow frequency acquisition range of the phase detector, the frequency detector is used for internal frequency acquisition. The frequency detector, however, can only work with FF0 and FF1 and it then is necessary for the PLL to select the phase detector (by setting FDIS=1) before receiving any random data.

The output of the phase-frequency detector is externally available through pin PHI. An external clock source can also be used (through pin TCLK) by setting TCLKSEL=1. To broaden the usable frequency range of the chip, there is a programmable divider before the clock generator. The VCO or TCLK frequency can be divided by 1, 2, 4, 8 by setting DIV1, DIV0 = 00, 01, 10, 11 (see Operating Rate Tables).

HDMP-1004 (Rx) Decoding

In Figure 6, the frame demultiplexer de-serializes the recovered serial data from the Input Sampler, and outputs the resulting parallel data one frame at a time. Every frame is composed of a 16-bit or 20-bit

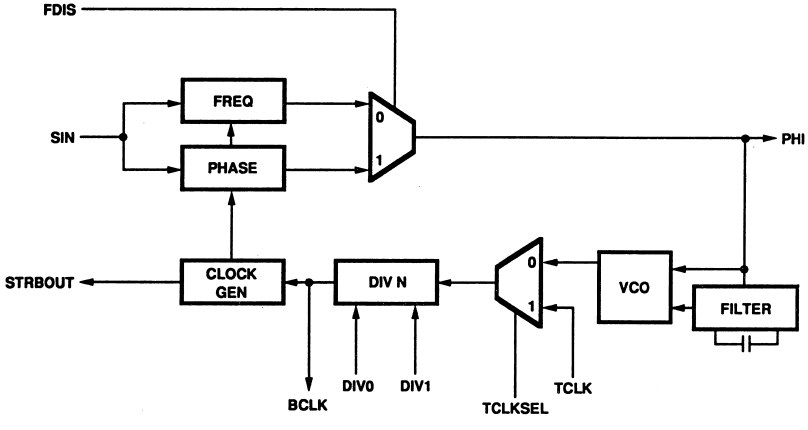


Figure 13. HDMP-1004 (Rx) Phase-Locked Loop.

Data Field (D-Field) and a 4-bit Coding Field (C-Field). The C-Field, C0-C3, together with the two center bits of the D-Field (D9 and D10 for 20 bit mode, D7 and D8 for 16 bit mode) are then decoded by the C-Field decoder to determine the content of the frame. The D-Field decoder is controlled by the outputs of the C-Field decoder. If an inverted Data Frame or Control Frame is detected, the D-Field decoder will automatically invert the D-Field data. If a Control Frame is detected, the D-Field decoder will shift the bottom half of the D-Field so that the outputs are at pin D_0 - D_{17} (if M20SEL = 1) or at pin D_0 - D_{13} (if M20SEL = 0). A data Frame is detected by the receiver when DAV = 1. A control Frame is detected by the receiver if CAV = 1. A Fill Frame is detected by the receiver if DAV = 0 and CAV = 0.

The C-Field decoder will set iERR = 1 when it detects an error. The internal error bit (iERR) is combined with the internal flag bit (iFLAG) and the flag-bit mode-select signal (FLAGSEL) to produce the externally available error (ERROR) and flag (FLAG) bits. If FLAGSEL = 1, the FLAG bit can be used as an extra data bit.

- ERROR=iERR.
- FLAG=iFLAG.
- If a Fill Frame is detected, then FLAG=0.
- If a Control Frame is detected, FLAG should be ignored.

If FLAGSEL = 0, the serial input is assumed to consist of alternating even frames (iFLAG = 0) and odd frames (iFLAG = 1).

- If iERR=1, then ERROR=1.
- If a Fill Frame is detected, then FLAG=0.
- If a Data Frame is detected, then FLAG=iFLAG, and iFLAG should alternate between 0 and 1, starting with 0 and ending with 1; otherwise, ERROR=1.
- If a Control Frame is detected, then FLAG automatically alternates between 0 and 1, starting with 0.

The even or odd feature allows a 32/40-bit wide data word to be transmitted through the link. A 2:1 multiplexer and a 1:2 demultiplexer are required. FLAG is used to synchronize the even and odd frames. Note, both Data and Control Frames can be transmitted as even/odd pairs, but only Data Frames can be detected for out of order errors.

HDMP-1004 (Rx) Link-Control State Machine Operation Principle

The link-control state machine (SMC) on the Rx chip provides a link handshake protocol enabling the duplex link to transition from frequency acquisition and training mode into data mode.

The HDMP-1000 Tx/Rx link uses an explicit frequency acquisition mode at startup that operates on a square-wave training sequence. This makes it possible to use a VCO with a very wide tuning range yet avoid the harmonic false lock problems associated with other circuits of this type.

Using the SMC, a full duplex data channel can be implemented without additional controller or hardware.

The State Machine Handshake Protocol

Figure 1 shows a simplified block diagram of the HDMP-1000 data channel configured for full duplex operation. Two HDMP-1000 chipsets are required to perform the handshake in parallel. There are three states that the link must go through to complete the link startup process:

State 0: Frequency Acquisition

State 1: Waiting for Peer

State 2: Sending Data

Each side of the link decides which of the three states that it should be in. The decision is based on its own memory and the type of frame that it is currently receiving from the other side of the link.

Considering only the local port of the link, we have a transmitter (Tx), a receiver (Rx), and a state machine controller (SMC). In practice, the SMC entity, although logically distinct, is implemented on the same die as the Rx chip. The SMC monitors the data frame status indicators (ERROR, DAV, CAV, FF) from the Rx, and is able to force (or

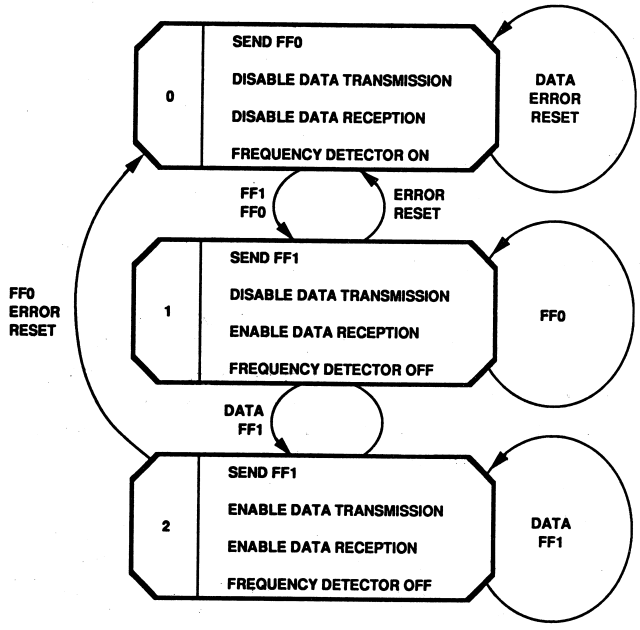


Figure 14. HDMP-1004 (Rx) State Machine State Diagram.

control) various characteristics of the Tx and the Rx chips. The Tx chip has the following controllable features:

- It can be forced to send a Fill Frame using the ED input.
- The type of Fill Frame sent can be controlled using the FF input.

The Rx Chip has the following controllable features:

- It can be in Frequency acquisition or Phase-lock/Data reception mode depending on the state of the FDIS input.
- It can be enabled for data reception or set in a mode in which data frames are ignored depending on the ACTIVE input.

The Rx chip can distinguish between the various types of frames. It can communicate the frame type to the SMC. The various frame types are:

- Fill Frame 0, (FF0)
- Fill Frame 1 a/b, (FF1)
- Data/Control frames (Data)
- Error frames (ERROR)

The SMC can be reset by either the SMCRST0* or SMCRST1* inputs. Usually one of these inputs is used for power-on reset, and the other is connected to the Tx LOCKED output.

This holds the SMC in state 0 until the transmitter PLL has locked.

Figure 14 shows the state diagram of the SMC. The SMC is debounced by allowing state transitions to be made only after at least 2 consecutive frames give the same indication. This prevents single bit errors from causing false state transitions. In addition to this debouncing mechanism, when two consecutive ERROR or Resets occur, a timer is enabled forcing the SMC into state zero for 128 frames. Any transition out of this initial state can only occur after the link has been error-free for 128 frames. This prevents false transitions from being made during the bit-slipping that occurs in the initial frequency acquisition of both the Tx and Rx PLLs.

When the local port is in State 0, it is in the reset state. Both local Tx and Rx parallel interfaces are disabled. The local Tx transmits FF0 continuously, and the Rx PLL is in the frequency detection mode. When the local Rx is phase-locked to the remote Tx it transitions to State 1. The local Tx transmits FF1 to acknowledge the phase-locked condition (its parallel input is still disabled). The local Rx PLL is in the phase detection mode and its parallel output is enabled. When in State 2, the two-way synchronization between the local port and the remote port is established. Both the local Tx and Rx parallel interfaces are enabled, and the local Rx PLL is in the phase detection mode. Parallel data can be sent by the local Tx, and at the same time, received by the local Rx.

The Rx chip has the state machine logic built in. The SMC has two status outputs, STAT0 and STAT1, that control the various features of the two chips depending on the current state.

SMC Output (STAT0 and STAT1) at Current Link State

State	STAT0	STAT1
0	0	0
1	0	1
2	1	1

The Tx inputs that need to be controlled are FF and ED. The Rx inputs that need to be controlled are FDIS and ACTIVE. To control the chips as shown in the state diagram of Figure 14, these inputs need to be driven as follows:

State	Tx FF	Tx ED	Rx FDIS	Rx ACTIVE
0	0	0	0	0
1	1	0	1	1
2	1	1	1	1

To control the link as shown above the following interchip connections must be made (Figure 15):

- Tx FF is driven by STAT1
- Tx ED is driven by STAT0
- Rx FDIS is driven by STAT1
- Rx ACTIVE is driven by STAT1
- Tx RST and Rx SMCRST0 are driven by a power-on, or user, reset circuit.

Link Configuration Examples

This section shows some application examples using the HDMP-1000 chipset. Refer to Section 2 (I/O Definition) for detailed circuit-level interconnection. For example, the chipset's ECL output drivers have weak driving power; hence, external buffers are required for large loading.

Figure 15 is the schematic for a full-duplex port. The network start-up protocol is provided by the Rx internal state-machine controller, and is transparent to the host. The handshaking between the host and the chipset is provided by the RFD and LINKRDY* signals. The host interface registers are clocked by the falling edges of the STRBOUT from the Tx and the Rx. The user has to make sure that M20SEL, FLAGSEL, DIV0, and DIV1 have the same setting on both the Tx and Rx. The word width of the parallel data from the host can be either 16 bits if M20SEL = 0, or 20 bits if M20SEL=1. Also, the FLAG bit can be used as an additional bit by setting FLAGSEL = 1. In the last case, the parallel data word width is either 17 bits or 21 bits. The local loopback test can be enabled by setting LOOPEN high.

Figure 16 shows how to use the FLAG bit and MDFSEL to transfer parallel data with 36-bit or 40-bit word width. Each data word is multiplexed and carried by two consecutive CIMT frames called even and odd frames. The FLAGSEL is set to high, and the FLAG bit is used to designate the even/odd frame. For the Tx, the MDFSEL is set to high so that the frequency of STRBOUT is twice that of STRBIN. The flag signal to the Tx is generated from STRBIN and STRBOUT. The Tx interface registers are clocked by the Tx FLAG signal. On the Rx side, the FLAG output is retimed by STRBOUT to generate RCLK, which is used to demultiplex the data output. Note that the Rx interface registers for LINKRDY*, ERROR, DAV*, CAV*, and FF are clocked by STRBOUT instead of RCLK; this is due to the fact that the FLAG is reset to "0" when receiving FF0.

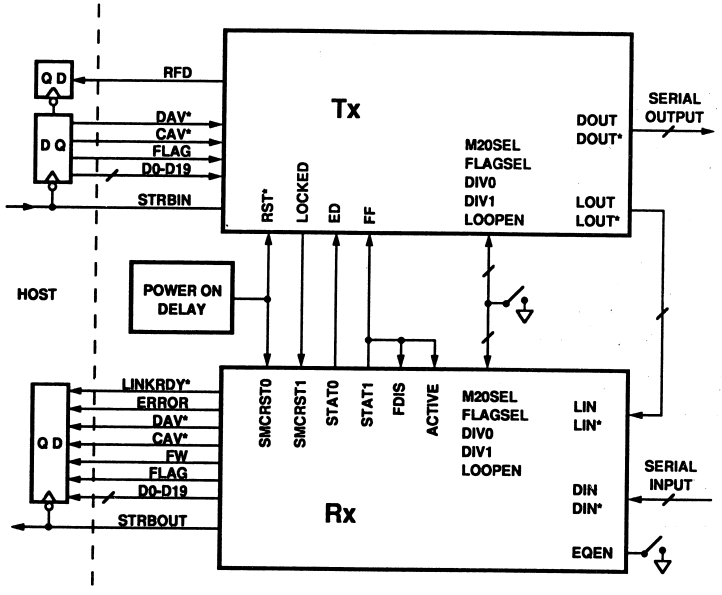


Figure 15. A Full-Duplex Port.

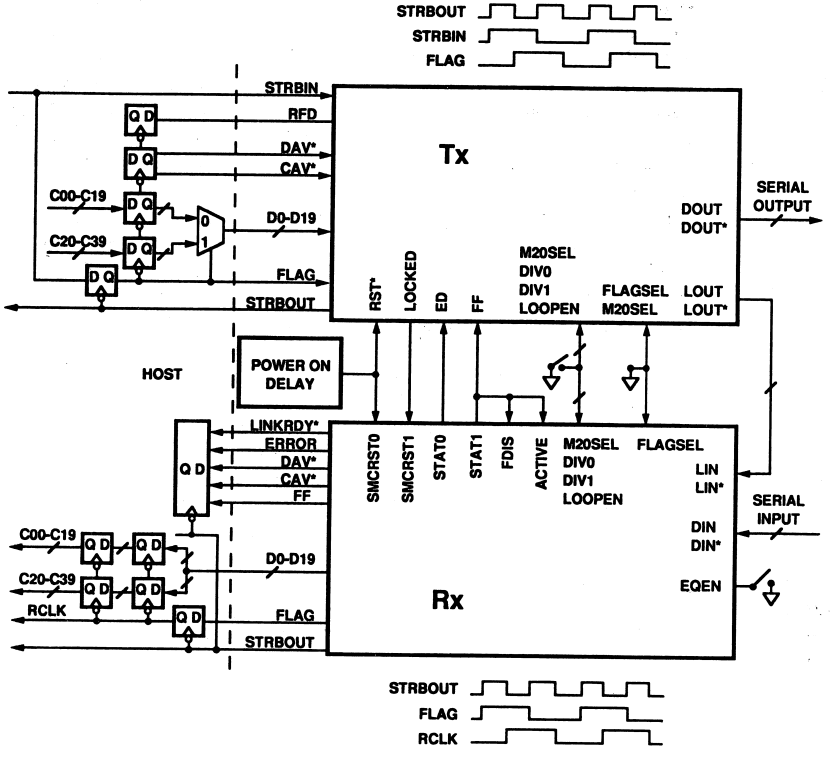


Figure 16. A Full-Duplex Double-Frame Port.

Although the HDMP-1000 chipset is designed for full-duplex applications, it is possible to configure the chipset for simplex applications as shown in Figure 17. Although the Tx has no knowledge of the status of the remote Rx, the Tx host can periodically allocate a time slot to transmit FF1. This is shown as a negative pulse to the Tx ED input in Figure 17. If the remote Rx is unlocked, it can wait for the next sequence of FF1 to regain synchronization.

The length of each FF1 sequence must be longer than the Rx frequency acquisition time (approximately 2 msec). Note that the Rx internal state-machine controller can also be used in this simplex application; no additional controller is necessary.

Surface Mount Assembly Recommendations

The package is designed to be surface mounted with the lid facing the board (lid acts as bottom of the package or pin view facing the board). It is recommended that the leads be formed into a "Gull-Wing" configuration prior to surface mounting. The recommended package stand-off (distance between "bottom" of package to the board surface) is 30 mils. It is also recommended that the leads be solder (Sn/Pb) coated prior to surface mounting. The lead material is Alloy 42. Note: Packages are shipped with unformed leads in carriers.

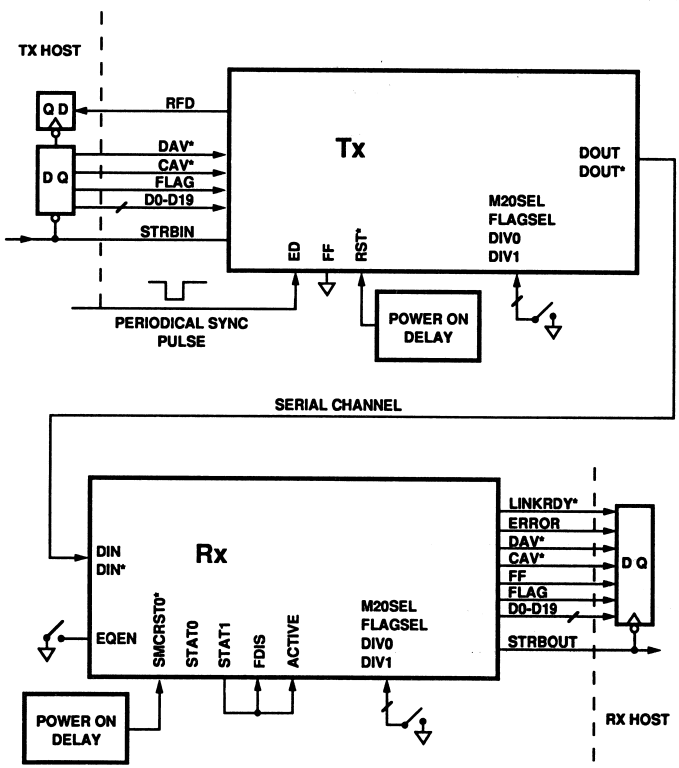
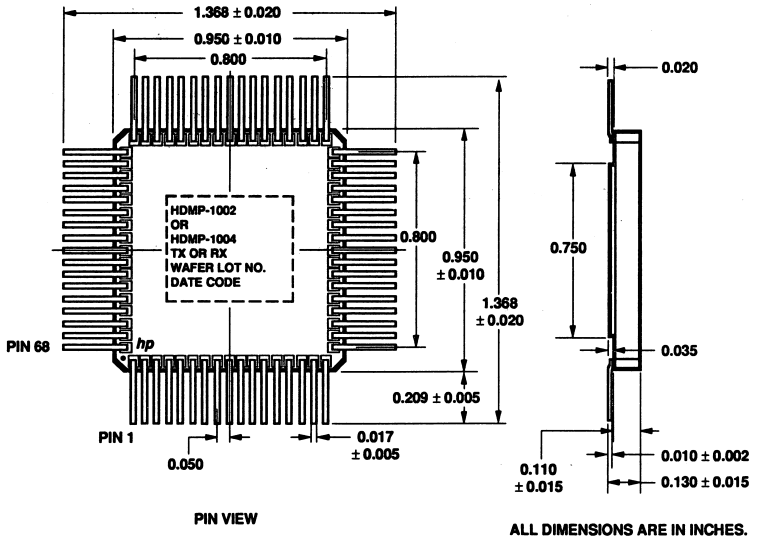


Figure 17. Simplex Configuration.

Outline

68 Lead Ceramic Quad Flatpack



Evaluation Board Ordering Information

A Gigabit Rate Transmit Receive Chipset Evaluation Board may be ordered through your local HP Components Representative or authorized HP Components distributor.

Designer Kit

Part Number	Kit Description
HDMP-100K	Evaluation board for the Gigabit Rate Transmit Receive Chipset, and literature

HEWLETT PACKARD

Decision Circuit (Comparator/D-FF)

Technical Data

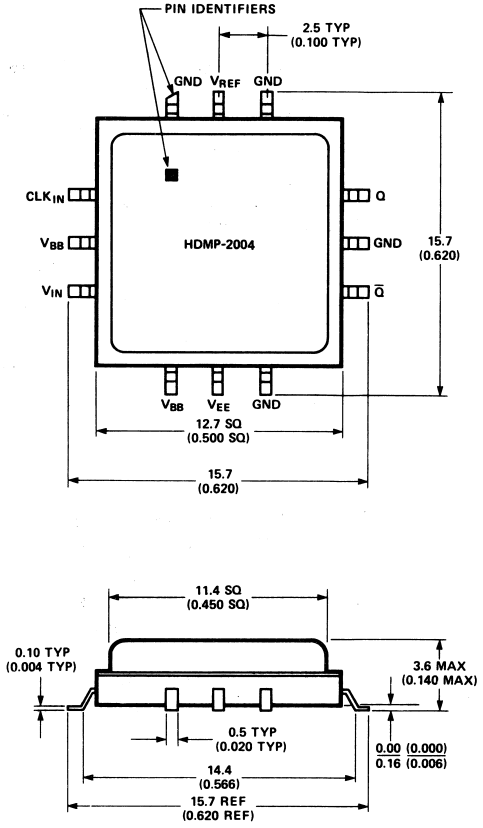
HDMP-2003
HDMP-2004

Features

- **Silicon Bipolar Technology**
- **ECL Levels**
- **Operational to 1.5 GBit Input Rates**
- **Single -5.2 V Power Supply**
- **Operational over Full Temperature Range -55°C to +125°C**
- **Highly Reliable HBIC Hermetic Surface Mount Package**
- **Low Power Dissipation ≤0.5 W**

Description/Applications

The HDMP-2003, and -2004 Decision Circuits are high speed/high sensitivity digital waveform regeneration modules consisting of a comparator, an edge-triggered D-flip-flop, and a 50 ohm output driver. They sample GBit data in both time and amplitude, and decide whether a "1" or a "0" exists relative to an internal V_{BB} or external DC reference voltage, thus regenerating a retimed, less noisy digital waveform. They are recommended for use as the data regeneration circuits in high speed fiber optics communication receivers. Other applications include Digital Radio communications systems, High Speed Computer Interconnect Systems, Instrumentation, and other Data Recovery Systems.



NOTE: BOTTOM OF PACKAGE IS PRIMARY GROUND CONTACT.
ALL DIMENSIONS IN MILLIMETERS (INCHES).

OUTLINE HBIC-0512
WEIGHT (TYPICAL): 1.15 GRAMS
(HDMP-2003, HDMP-2004)

Absolute Maximum Ratings

Symbols	Parameters	Units	Ratings
V_{EE}	Supply Voltage	V	-6.0
T_{STG}	Storage Temperature	°C	-60 to +150
T_C	Operating Case Temperature	°C	-55 to +125
V_{IN}	Input Voltage	V	+2 pk-pk

Operation in excess of these conditions may result in permanent damage to the device.

Operating Specifications

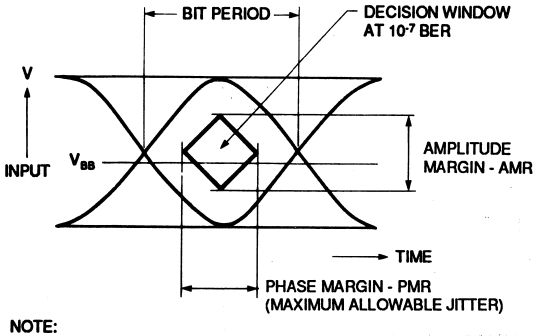
Symbols	Parameters	Units	HDMP-2003		HDMP-2004	
			Min.	Typ.	Min.	Typ.
DR	Input Data Rate	GBits/sec	2.0	2.4	2.8	
AMR[1]	Amplitude Margin	mV	100	120	70	130
PMR[1]	Phase Margin	psec	250	300	170	240
VTM	Threshold Margin	mV		40		40
t_r[2]	Rise Time	psec		110		120
t_f[2]	Fall Time	psec		110		90
V_O	pk-pk Output Voltage	Volts		0.6		0.6
I_{EE}	Supply Current	mA		70		60

Test Conditions:
V_{EE} = -5.2 V
CLK: HDMP-2003 = 2.0 GHz, 400 mV pk-pk
HDMP-2004 = 2.8 GHz, 400 mV pk-pk

V_{IN} : HDMP-2003 = 2.0 GHz, 200 mV pk-pk
HDMP-2004 = 2.8 GHz, 200 mV pk-pk

2^{15}-1 Pseudo Random Bit Sequence (PRBS)
CLK, V_{IN}, and Output are at 50 Ohms AC coupled
T_A = 25°C

Notes:
1. See Figure 1A.
2. 10% to 90% (see Figure B).



NOTE:
VTM = THE MINIMUM DIFFERENCE BETWEEN THE INTERNAL REFERENCE VOLTAGE AND THE NEAREST EDGE OF THE AMPLITUDE MARGIN WINDOW.

Figure 1a. Decision Window Definition.

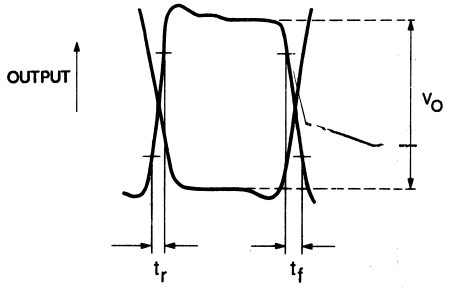


Figure 1b. Output Waveform Definition.

TYPICAL RETURN LOSS AT T = 25°C FOR HDMP-2003

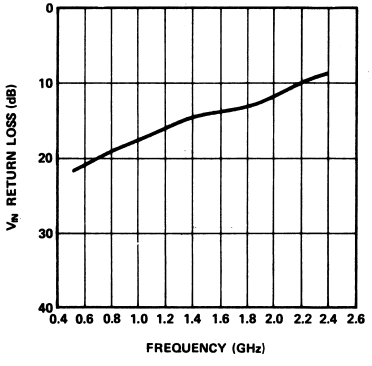


Figure 2a.

TYPICAL CASE TEMPERATURE PERFORMANCE FOR HDMP-2003

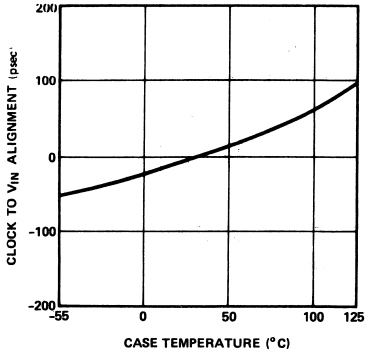


Figure 2b.

TYPICAL RETURN LOSS AT T = 25°C FOR HDMP-2003

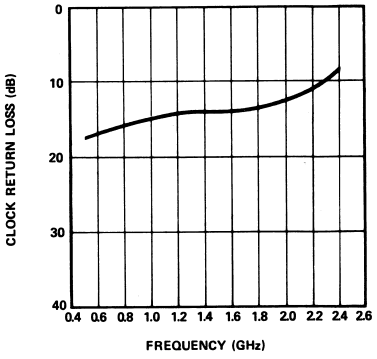


Figure 2c.

TYPICAL CASE TEMPERATURE PERFORMANCE FOR HDMP-2003

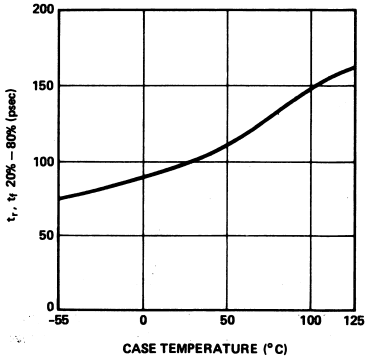


Figure 2d.

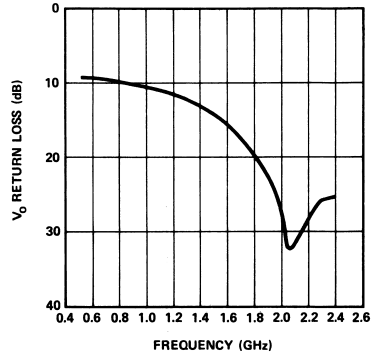


Figure 2e.

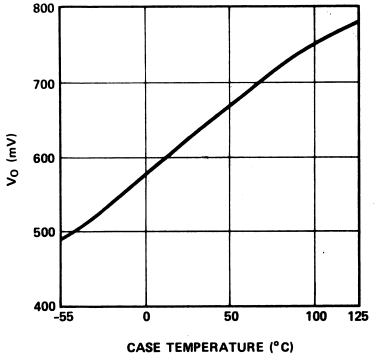


Figure 2f.

TYPICAL RETURN LOSS AT T = 25°C
FOR HDMP-2004

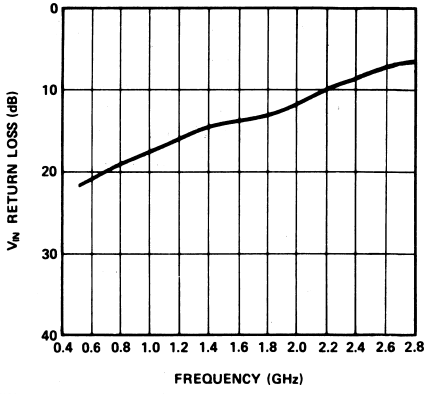


Figure 3a.

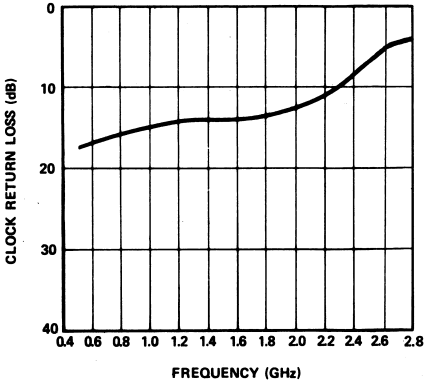


Figure 3b.

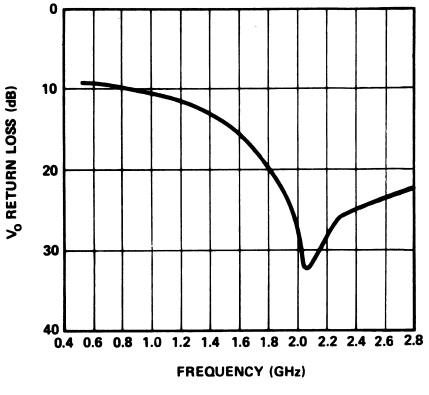


Figure 3c.

TYPICAL CASE TEMPERATURE PERFORMANCE
FOR HDMP-2004

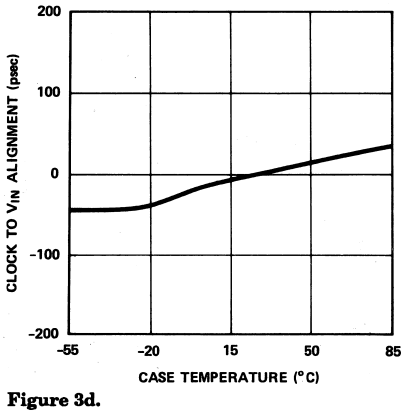


Figure 3d.

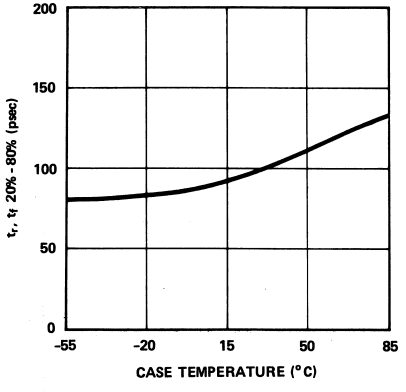


Figure 3e.

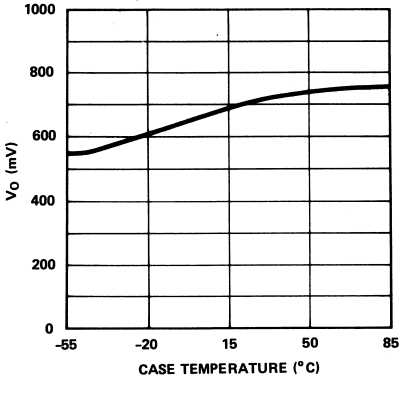


Figure 3f.

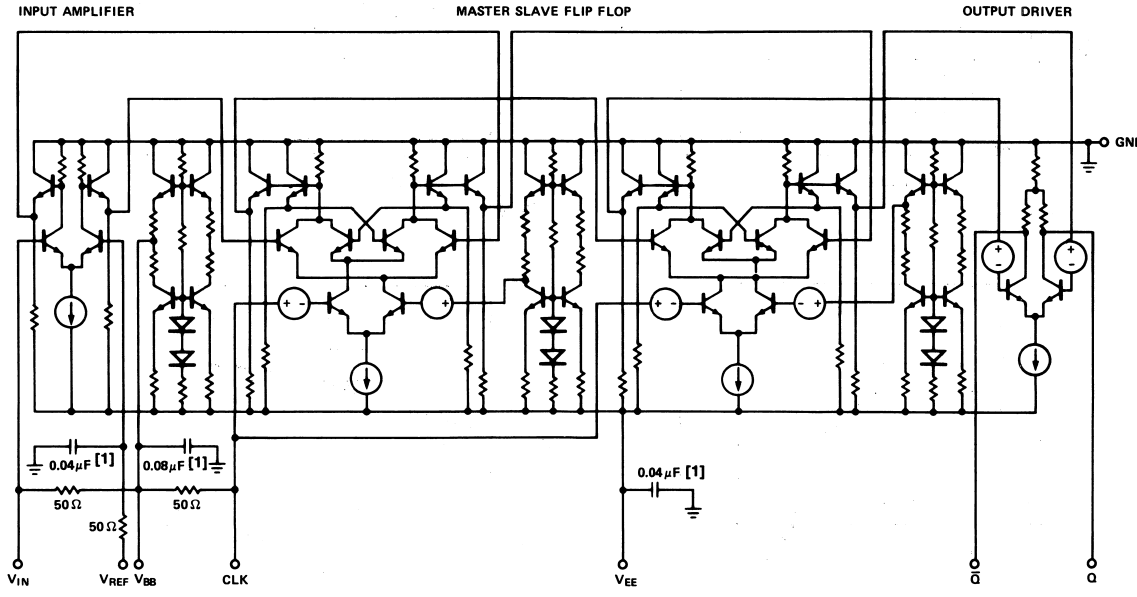
Theory of Operation

The HDMP-2003 and -2004 consist of three major sections – an input comparator amplifier, a master-slave flip-flop, and an output driver (see Figure 4). During operations, a distorted waveform enters the comparator via V_{IN}, and is compared to a reference DC voltage supplied at V_{REF}. The output of the D-flip-flop is next fed into the D-flip-flop section where a clock input triggers the master/slave action that synchronizes the signal with the rising edge of the clock. The amplified and retimed signal then exits the module through the driver section.

Under normal operating conditions, V_{REF} is connected to V_{BB}, and V_{IN} and CLK are externally capacitively coupled (see Figure 4). The internal termination resistors also form a biasing network which eliminate the need for additional external biasing. The integrity of the input amplifier is determined by the Amplitude Margin (AMR), which is defined by the range of V_{REF} at which the Bit Error Rate (BER) is less than 10^{-7}. For values inside this range, the BER falls sharply to produce virtually error free operation (see Figures 6 and 8).

The performance of the retiming flip-flop is determined by the Phase Margin (PMR) which is defined by the range of deviation of clock alignment relative to the input signal at a BER less than 10^{-7}. Again, the BER falls sharply inside this range (see Figure 7 and 9). Once the clock to data alignment is set, the internal compensation circuitry will track this alignment over temperature (see Figures 2d and 3d).

The output driver section is characterized by the peak-to-peak output voltage and the 10% to 90% rise and fall times relative to the levels at the center of the output bit. This driver also has the advantage of driving directly into 50 ohms with or without a coupling capacitor, or directly into ECL (see Figure 10). The excellent line matching also dampens pulse reflections typical for many high frequency circuit interconnections.



[1]HDMP-2004 only.

Figure 4. Circuit Schematic, HDMP-2003 and HDMP-2004.

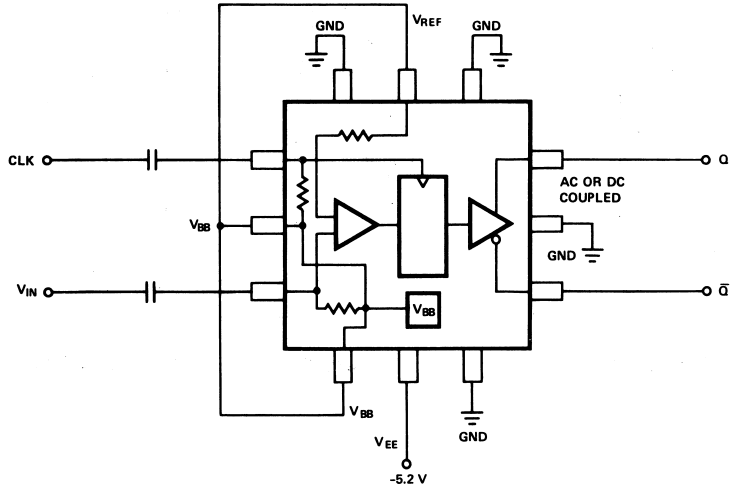


Figure 5. Typical Interfacing Diagram (Top View); HDMP-2003, HDMP-2004.

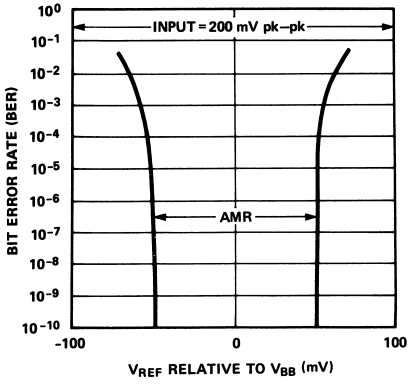


Figure 6. Amplitude Margin (AMR), HDMP-2003.

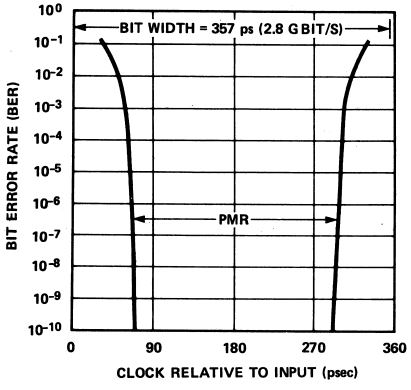


Figure 7. Phase Margin (PMR), HDMP-2003.

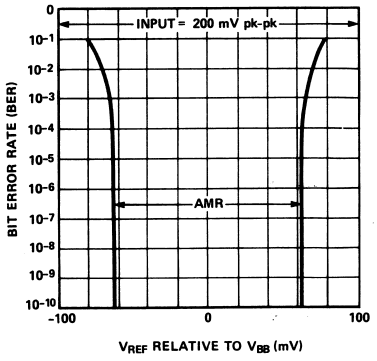


Figure 8. Amplitude Margin (AMR), HDMP-2004.

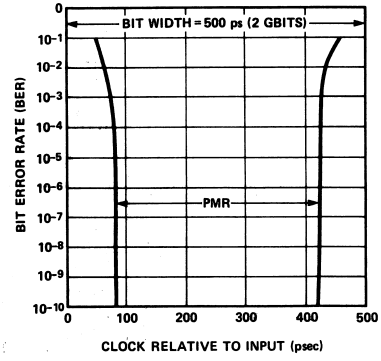


Figure 9. Phase Margin (PMR), HDMP-2004.

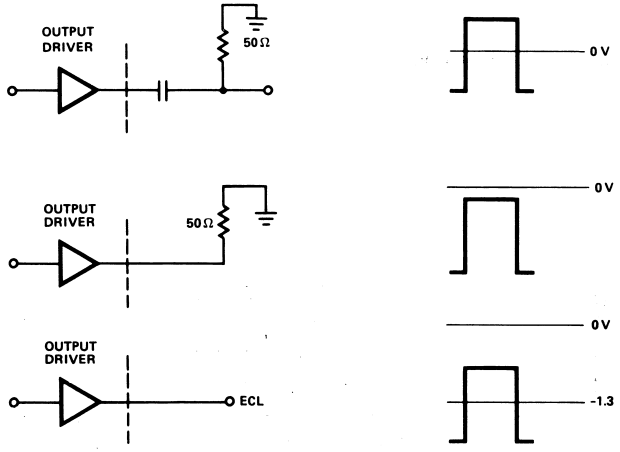


Figure 10. Output with Various Loading Conditions, HDMP-2003, HDMP-2004.

Testing

The characterization test set-up for the HDMP-2003 and -2004 is shown in Figure 11. The input signal is provided by a pseudo random bit sequence (PRBS) generator set at the operating frequency. To insure that the DUT is correctly evaluated, the square wave output from the generator (A) is fed into a high performance AGC amplifier (HAMP-5001), which emulates a typical system. The AGC amplifier output (B), and the sinusoidal clock signals (C) are applied to the DUT. The outputs Q and $\overline{Q}$ are measured with the BER receiver and a sampling scope (D).

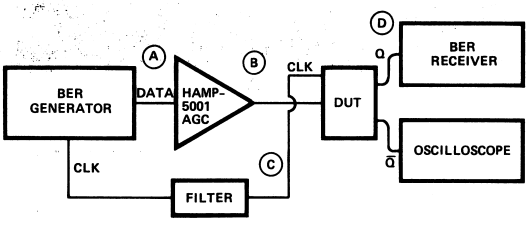
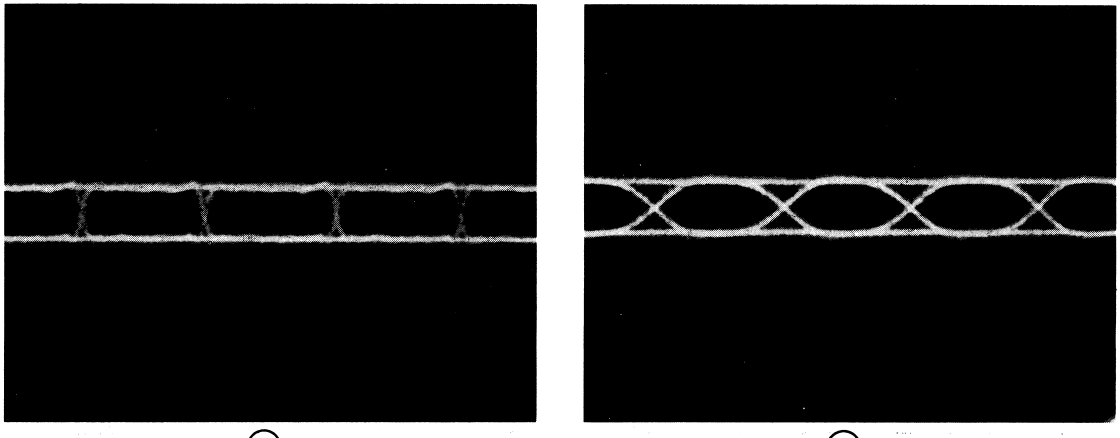
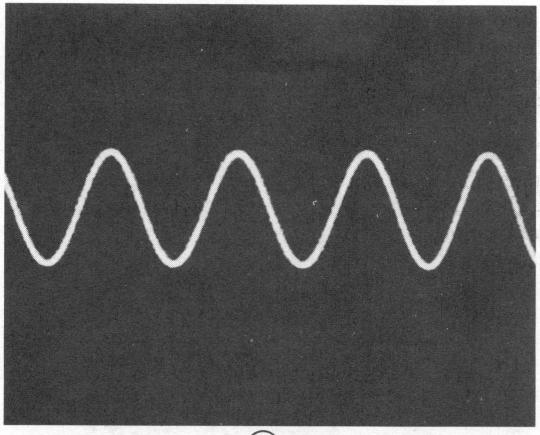


Figure 11. Test Setup

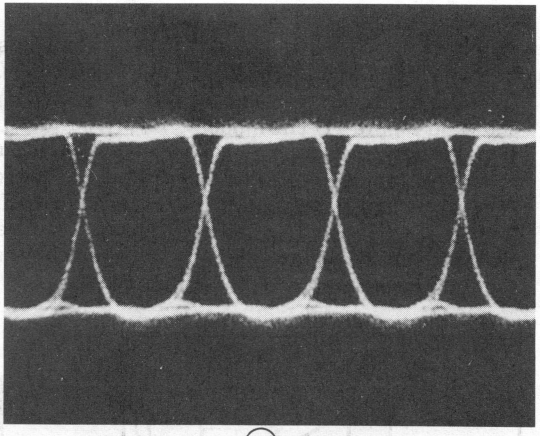
HDMP-2003



HDMP-2003 continued

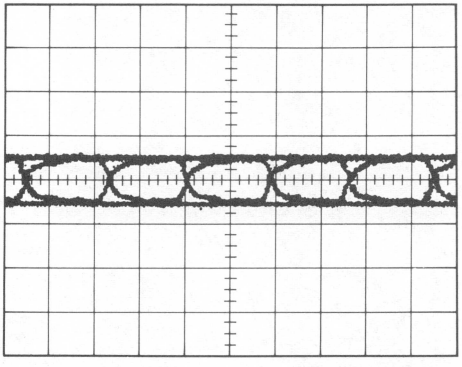


C

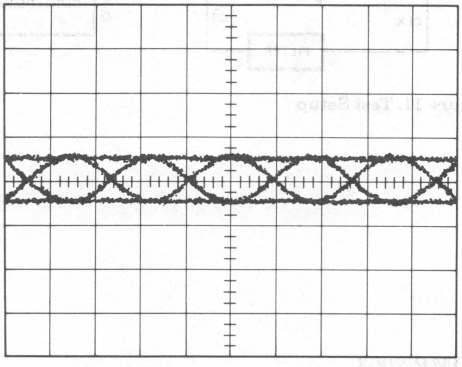


D

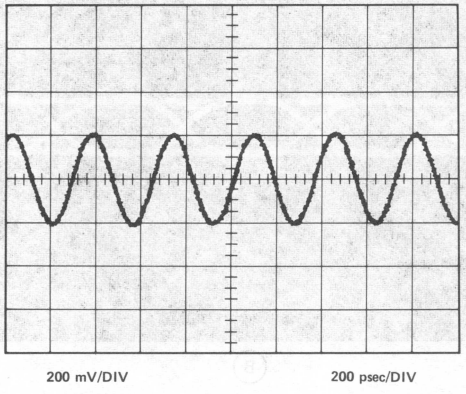
HDMP-2004



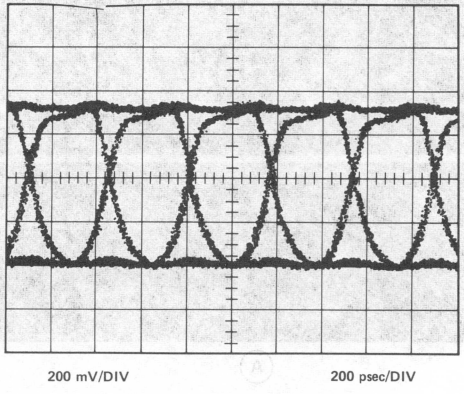
A



B



C



D

Figure 12. Characterization Test Set-up.

Handling and Mounting Procedures for Hermetic, Base is Circuit (HBIC-0512 Packages

1. Storage

Under normal circumstances, storage of the HBIC packages in HP supplied containers is sufficient. However, in particularly dusty or chemically hazardous environments, storage in a clean, inert atmosphere is advised to maintain solderability.

2. Handling

As with any multi-leaded surface mount package, care must be taken during handling of the HBIC package not to cause deformation of the leads. The planarity of the leads to each other and to the bottom of the package must be maintained for successful mounting. The HBIC package can be handled with tweezers or other tools by clamping the package around the lid, or with vacuum systems on the top of the lid.

3. Grounding

The prime ground contact of the HBIC package is its bottom (with unused leads and the lid as secondary ground points). For optimum circuit performance, the bottom of the package must be soldered to a ground pad on the substrate (PC board or ceramic). This ground pad should be the size of the package bottom and have several plated thru holes to the substrate's ground plane, giving the package a low inductance contact to system ground.

4. Mounting

Solder reflow is the suggested method of attaching HBIC packages onto substrates. The recommended solder is 62% Sn, 36% Pb, 2% Ag, with an RMA flux. This solder paste can be dispensed (for packages with wide lead spacing) or screen printed onto the substrate. The use of a solder mask on the substrate is also recommended. Solder reflow can then be achieved by infrared heating or vapor-phase heating. The packages must not be exposed to more than 260°C for 20 seconds.

Conductive epoxy could be used for mounting the HBIC packages, however, care must be taken due to the potential problem of silver migration between the leads and the ground pad under the package.

Wave soldering is not recommended due to the metal lid and the need for solder under the package base.

HEWLETT PACKARD

Silicon Bipolar High Speed Decision Circuit with 1.5 GBit Operation (Comparator/D-FF)

Technical Data

HDMP-2006

Features

- **High Performance Low Bit Error Rate (BER)**
- **Operational to >1.5 Gbit Data Rates**
- **ECL Compatible I/O**
- **Requires only a 100 mV Minimum Input Signal**
- **Single -5.2 V Power Supply**
- **Hermetic Glass Metal SOIC Package**
- **Low Power Dissipation < 0.5W**

Applications

- **SONET Fiber Optic Systems**
- **Provides Excellent 622 Mb OC-12 Performance**
- **High Speed Digital Telecom Systems**
- **High Speed Datacomm and Computer Interconnect to 1.5 Gb**
- **Digital Television Studio Systems**
- **Instrumentation-- Comparator, DFF**

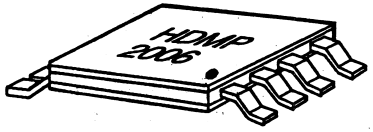
Description

The HDMP-2006 Decision Circuit is a high speed/ high sensitivity digital waveform regenerator IC consisting of a comparator, an edge triggered D-type flip-flop, and a 50 Ohm output driver. The device is fabricated on Hewlett-Packard's >13 GHz f_T silicon bipolar IC process. The HDMP-2006 samples input data at rates up to 1.5 Gb/sec in both time and amplitude, and decides whether data is a "1" or "0" relative to the sampling level V_{REF} which can be tied to the internally generated V_{BB} or externally supplied .

The HDMP-2006 is ideally suited for data regeneration applications in high speed fiber optic communication systems such as SONET standard systems.

The HDMP-2006 is supplied in an 8 lead hermetic package with gold plated Kovar (ASTM F-15 alloy) cover, base, and leads.

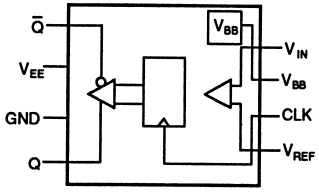
SOIC8 Package Outline



PIN #1

Functional Block Diagram

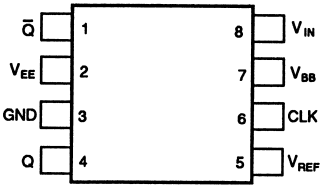
Top View



NOTE:
BOTTOM OF PACKAGE IS AT V_{EE} POTENTIAL (-5.2 V NOMINAL). TOP OF PACKAGE IS ISOLATED AND MAY BE GROUNDED BY USER.

Package Lead Code Identification

Top View



Absolute Maximum Ratings, T_A = 25 °C*

Symbol	Parameter	Units	Max.
V_{EE}	Supply Voltage	Volts	-6.0
V_{IN}	Signal Input Voltage	Volts DC Pk to Pk	2
T_{op}	Ambient Operating Temperature	°C	+100
T_{stg}	Storage Temperature	°C	-60 to +150
T_{max}	Maximum Assembly Temperature (for 60 seconds maximum)	°C	+300

* Operation in excess of any of these conditions may result in permanent damage to this device.

ESD Sensitivity
These high performance devices are ESD sensitive (Class 2).
Proper precautions should be used when handling these devices

DC Electrical Specifications, T_A = 25 °C

Symbol	Parameter	Units	HDMP-2006		
			Min.	Typ.	Max.
V_{EE}	Supply Voltage	V	-5.46	-5.2	-4.94
I_{EE}	Supply Current	mA		70	90
V_{BB}	Reference Voltage	V		-1.3	
θ_{JC}	Thermal Resistance (Die to Case)	°C/W		50	

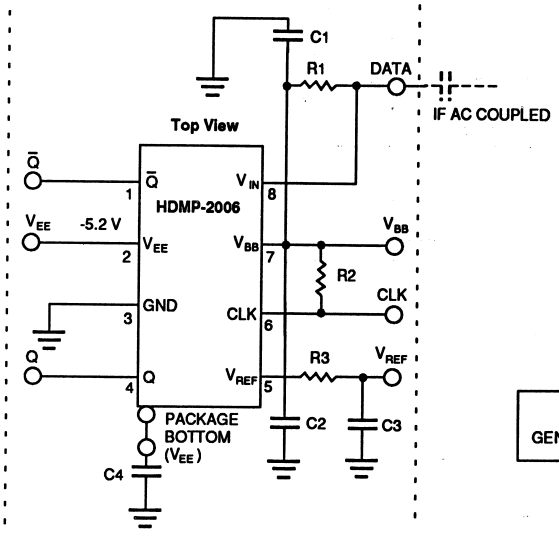
AC Electrical Specifications, T_A = 25 °C

CLK = 1 GHz 400 mV p-p, V_{IN} = 200 mV p-p @ 1 GHz @ V_{EE} = -5.2V
Input data test sequence = PRBS @ 2^{23}-1
When tested per Test Circuit (Figures 1 and 2) in test board per layout of Figure 3.

Symbol	Parameter	Units	HDMP-2006		
			Min.	Typ.	Max.
AMR	Amplitude Margin [1]	mV	100	130	
PMR	Phase Margin [1]	ps	700	800	
V_{TM}	Threshold Voltage	mV		55	
t_r	Rise time (10% to 90%) [2]	ps			200
t_f	Fall time (90% to 10%) [2]	ps			200
V_{OUT}	Output Voltage Swing (pk to pk)	V	0.6	0.8	

Notes: 1 AMR is measured by varying V_{REF} relative to V_{IN}. PMR is measured similarly by varying the clock phase relative to the data. AMR and PMR are defined in Figure 6.
2. t_r and t_f are defined in Figure 7.

Test Circuits



ALL CAPACITORS ARE 39000 pF
ALL RESISTORS ARE 50 Ohms

Figure 1. DUT Interface Circuitry

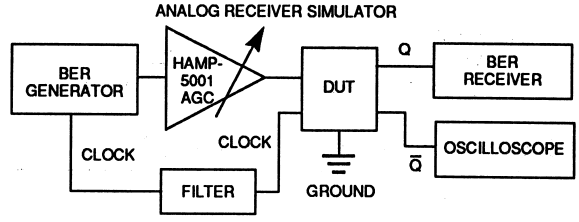
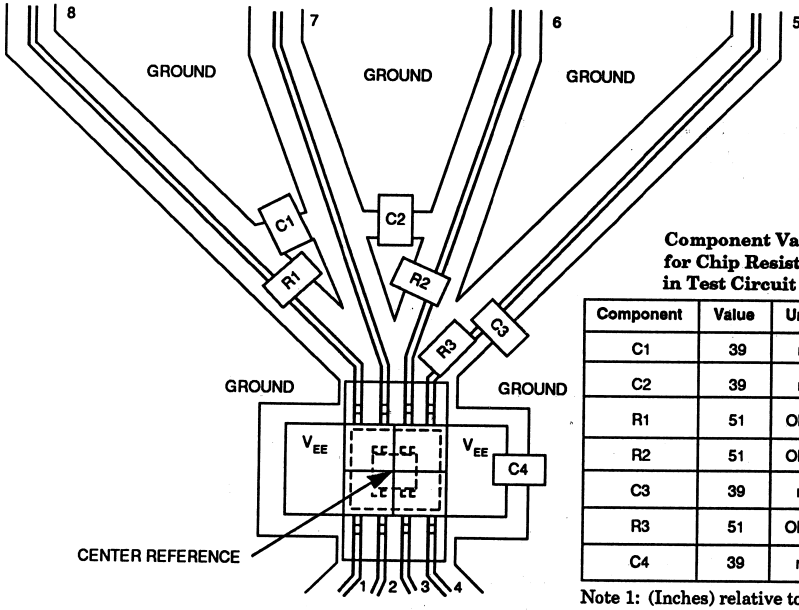


Figure 2. Device Test Setup



Component Values and Relative Positions for Chip Resistors and Capacitors in Test Circuit of Figure 3.

Component	Value	Units	Relative X [1]	Relative Y[1]
C1	39	nF	-0.22	0.49
C2	39	nF	-0.01	0.48
R1	51	Ohms	-0.20	0.33
R2	51	Ohms	0.04	0.35
C3	39	nF	0.18	0.31
R3	51	Ohms	0.07	0.22
C4	39	nF	0.22	0.00

Note 1: (Inches) relative to device center

Figure 3. Physical Test Circuit Layout and Component Information

Performance Curves

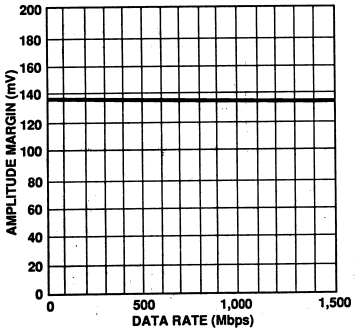


Figure 4. Input Eye Amplitude Margin

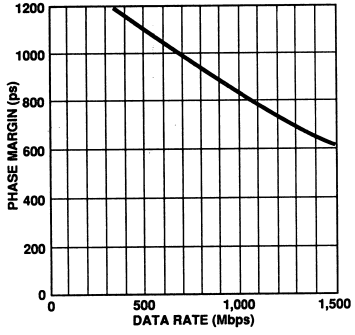
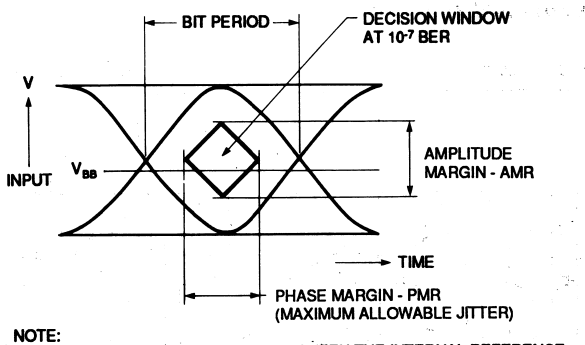


Figure 5. Input Eye Phase Margin



NOTE:
VTM = THE MINIMUM DIFFERENCE BETWEEN THE INTERNAL REFERENCE VOLTAGE AND THE NEAREST EDGE OF THE AMPLITUDE MARGIN WINDOW.

Figure 6. Eye Diagram Performance Measures

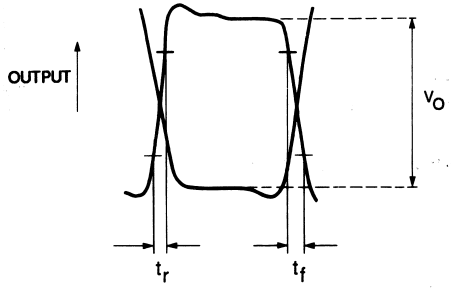


Figure 7. Output Waveform Definitions

Eye Performance Measures

HP specifies the performance of this decision circuit by measuring the input Amplitude Margin (AMR) and input Phase Margin (PMR) which will produce a Bit Error Rate (BER) of 1E-07 or less.This is accomplished (see Figure 2) by setting the input psuedorandom signal amplitude from the BER Test Set (BERT)at a constant level and varying the reference signal V_{REF} (externallly connected). In a similar manner the clock to data phase is varied. The input signal from the BERT is band limited by the HAMP-5001 which is an AGC circuit simulating the analog performance of a fiber optic receiver. The measurements are made independently; first by varying phase and second amplitude. In this way the center useable portion of the eye (Figure 6) is determined. The vertices of the diamond pattern are the values of amplitude and phase at which the BER exceeds 1E-07. This measurement simulates typical system conditions and provides both the amplitude and phase (timing) limits. The measurement provides an accurate determination of Gaussian noise superimposed on the data signal and is minimally effected by switching noise.

Ambiguity level can also be used to accurately measure the amplitude window of the eye diagram for this class of devices. A full ambiguity level test uses the PRBS output signal of the BERT with a precision attenuator (or AGC) in series with the input of the device. This requires a precision attenuator which has a constant level of noise independent of attenuation level and bandwidth.

Because of the difficulty in accurately doing the ambiguity test and since the AMR and PMR tests provide more operationally relevant data, HP does not specify ambiguity level.

Circuit Schematic

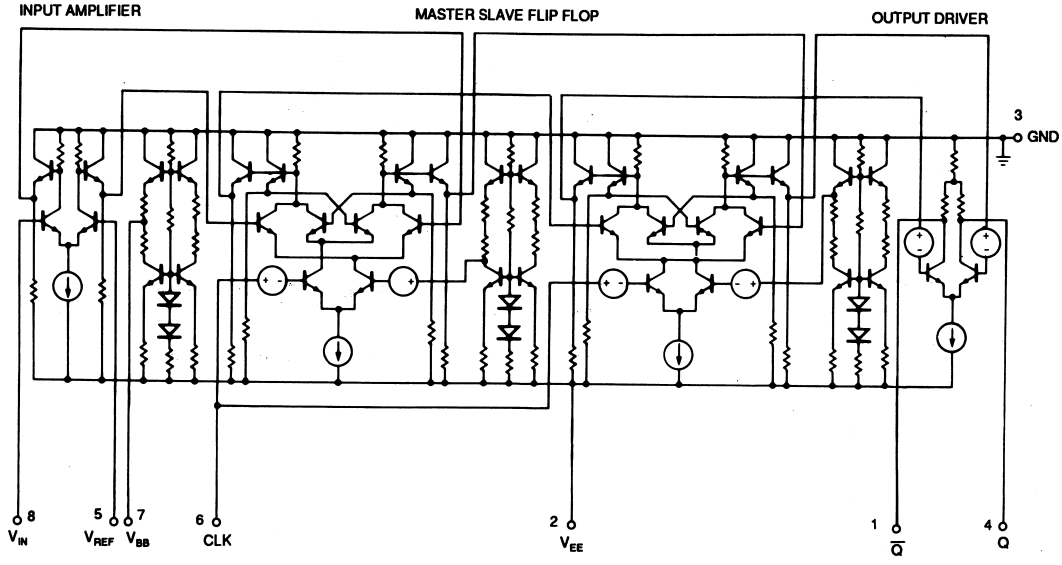


Figure 8. HDMP-2006 Circuit Schematic

Theory of Operation

The HDMP-2006 consists of three major sections - an input comparator amplifier, a master slave flip-flop, and an output driver (see Figure 8). During operation, a distorted waveform enters the comparator via V_{IN}, and is compared to a reference voltage V_{REF}. The output of the comparator is next fed to a D-type flip-flop section where the clock input triggers the master-slave action that synchronizes the signal with the rising edge of the clock. The amplified and retimed signal then exits the module through the driver section. Direct coupled inputs will work with ECL levels.

The output driver section provides the peak-to-peak voltage with the 10 to 90 % rise and fall times relative to the levels at the center of the output waveform (Figure 7). Typical interface circuit diagrams for the HDMP-2006 are given in Figure 9 and 10 which show both AC and DC input and output options.

The HDMP-2006 can interface the output directly into a 50 Ohm load with or without a coupling capacitor, or directly into an ECL gate (see Figure 10). The excellent line matching, when terminated externally, also dampens the pulse reflections that typically occur in high frequency applications.

Application Interface Circuits

There are three recommended application configurations for the HDMP-2006, wherein the user either AC or DC couples the DATA and/or supplies the V_{IN} and V_{REF} DC bias. In addition, there is a possible but non-recommended case where the user also supplies the DC clock bias externally, or DC couples the clock.

For AC coupled applications, the configuration shown in Figures 9a and 10a is recommended. Here, both the clock and data, as well as the V_{REF}, utilize the internal V_{BB} generator. This is suitable for inputs with 50% average mark ratio such as PRBS.

AC coupled applications can also employ an externally supplied DC bias for V_{IN} and V_{REF} as shown in Figure 9b. The bias level should be close to -1.3 V. For temperature compensation reasons, the V_{IN} and V_{REF} biasing should be supplied from the same source as indicated in Figure 9b. If separate biasing is used for V_{IN} and V_{REF}, care should be taken to ensure that the biasing from the different sources tracks identically as possible over temperature excursions.

For DC coupled applications, the configuration shown in Figures 9c and 10b is recommended. Here the clock is biased from V_{BB}; V_{IN} and V_{REF} are directly DC coupled externally. For temperature compensation reasons, the quiescent DC level of the DATA and $\overline{\text{DATA}}$ should temperature track and be set to approximately -1.3V as in standard ECL levels. For single-ended DC coupling, V_{REF} can be tied to an external -1.3V or a voltage (near -1.3 V) that matches and tracks the data quiescent voltage (see Figure 9c). This configuration is necessary for data with mark ratios much different than 50%.

For all three recommended configurations above, the bias of the clock by the internal V_{BB} is necessary for temperature compensation of the sampling of the decision circuit relative to the input data.

The user can separately bias the clock input if desired (Figure 9d). In this case the relative levels and temperature tracking of the DC bias signals need to be carefully considered. Experimental testing by user is strongly recommended.

Interfacing Cases

Case	Figure	Data In	V_{REF} DC Bias	V_{IN} DC Bias	Clock Bias
1	9a	AC	$=V_{BB}$	$=V_{BB}$	$=V_{BB}$
2	9b	AC	External	External	$=V_{BB}$
3	9c	DC	External	External	$=V_{BB}$
4	9d	AC or DC	External or $= V_{BB}$	External or $= V_{BB}$	External

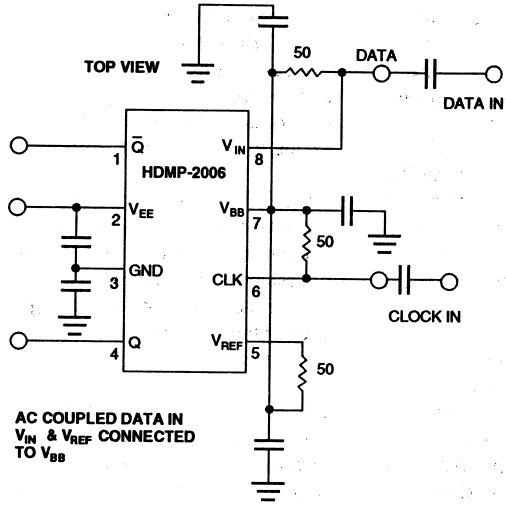


Figure 9a. AC Interface Circuit

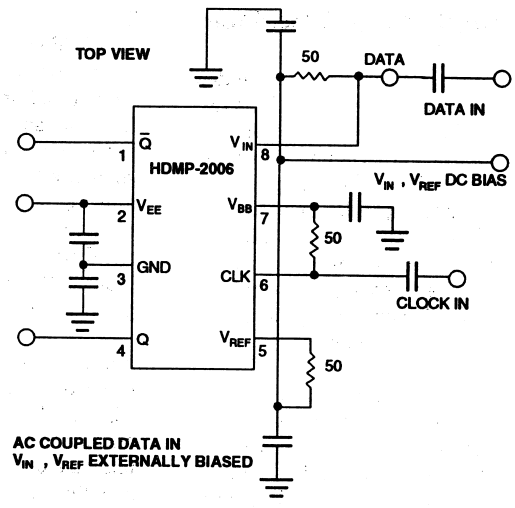


Figure 9b. AC Interface with DC V_{IN} and V_{REF} Bias

ALL CAPACITORS ARE 39000 pF
ALL RESISTORS ARE 50 Ohms

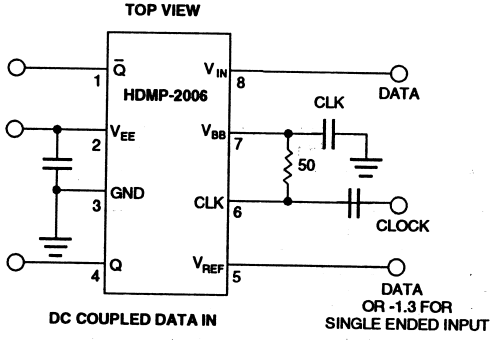


Figure 9c. DC Interface Circuit

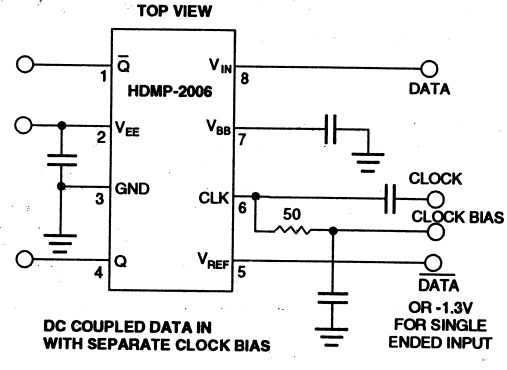


Figure 9d. DC Interface with External CLOCK Bias

Output Drive Level

The output driver is designed to deliver 0.8 V into 50 Ohms AC, or DC coupled, as shown in Figures 10a and 10b.

The V_{OH} and V_{OL} levels of the driver are such that the peak-to-peak voltage is approximately 1.2 V unloaded centered around V_{BB} = -1.3 V. For driving ECL, the line can be terminated with a parallel combination of resistors as shown in Figure 10c. The equivalent termination of 50 Ω shrinks the pk- to-pk voltage down to approximately 0.8 V centered about -1.3V. The output impedance of the driver is matched to 50 Ω. The amplitude can be increased with larger termination resistance with minimal VSWR penalty. Nominal values for a 50 Ω interface are: R_1 = 140 Ω; R_2= 77 Ω.

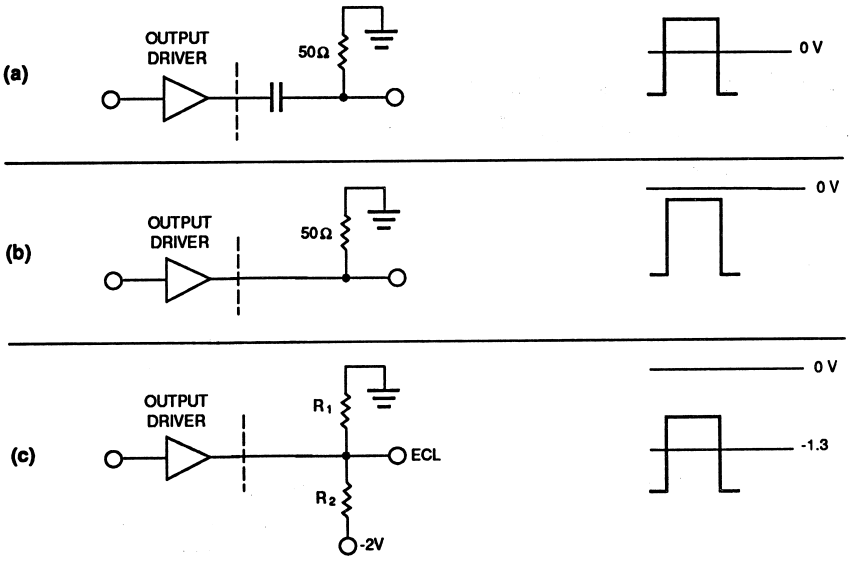
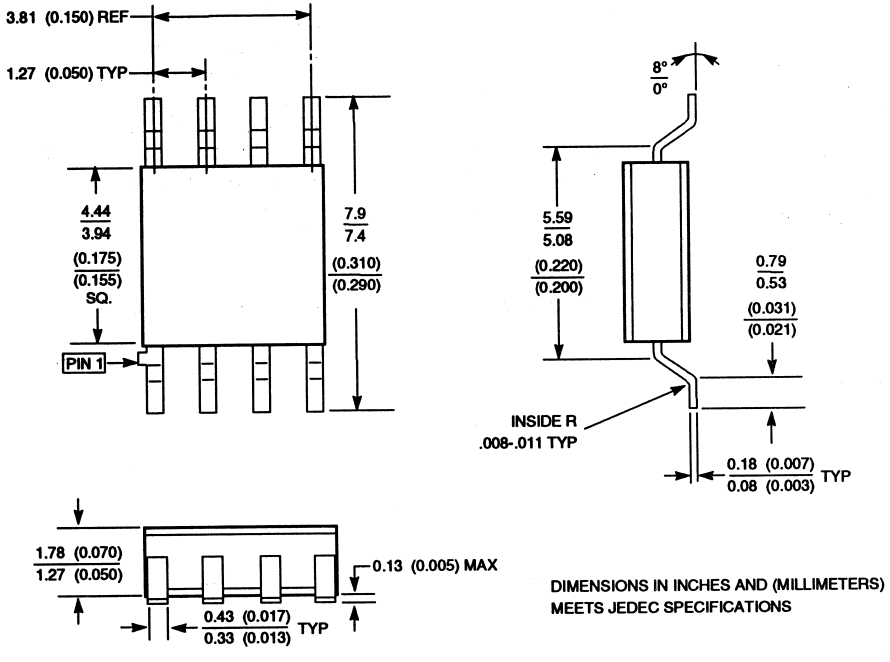


Figure 10. Output with Various Loading Conditions



NOTE: MAXIMUM STATIC PRESSURE ON PACKAGE <30 PSI (MIL-STD-883, METHOD 1014). CARE SHOULD BE TAKEN IN HANDLING AND MOUNTING SO THE PRESSURE LIMIT IS NOT EXCEEDED.

Figure 11. Package Outline Dimensions

HEWLETT PACKARD

High Speed Silicon Bipolar 622 Mb/s Serial Data and Clock Recovery Circuit

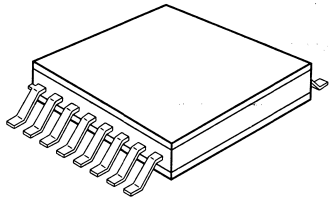
Technical Data

HDMP-2501

Features

- **Single Chip Clock Extraction and Data Retiming**
- **Designed for 622 Mb/s Applications**
- **Easy to Apply, Cost Effective**
- **Operational with Data Patterns Pseudorandom to 2^{23}-1**
- **Lock Time < 2.5 ms**
- **Low Jitter Generation < 1.7 Degrees at 622 Mb/s**
- **Auto Adjusting – No Board Level Adjustment Needed**
- **Autotracks Temperature and Voltage Changes**
- **0 to 65°C Case Temperature Range**
- **ECL Compatible I/O**
- **50 mV Minimum Signal Input Required**
- **Standard ECL -5.2V & -2.0V Power Supply**
- **Low Power Dissipation (1.4W)**
- **Hermetic Glass Metal Surface Mount Package**

HDMP-2501



Applications

- **Telecom and Datacom Switching Systems**
- **Computer Back Plane Interconnect**
- **Board to Board High Speed Data Links**

Description

The HDMP-2501 is a 622 Mb/s serial data and clock recovery circuit which is based on a Phase Locked Loop (PLL) approach for clock extraction. This chip includes a phase/frequency detector, integrator (external capacitor required), and a voltage controlled oscillator (VCO), see Figure 1. A self contained decision circuit automatically aligns the data relative to the recovered clock. Both recovered clock and retimed data outputs are available.

The digital phase detector generates a correction to the VCO ramp after each transition of the input serial data stream.

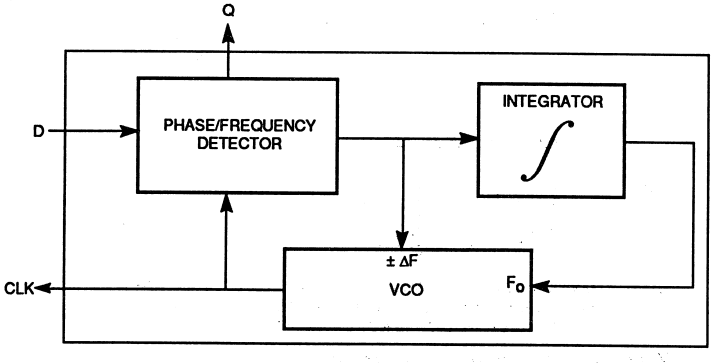
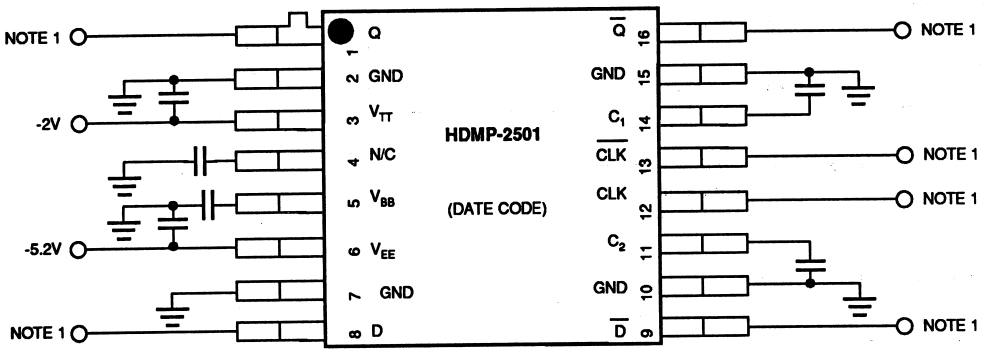


Figure 1. Functional Block Diagram

The design insures clock capture over the entire range of the VCO, and provides for fast lock-up and autotracking of the recovered clock over temperature and supply voltage changes. No external adjustment is required.

The PLL approach integrated in this design eliminates the temperature and phase variation conditions normally found with multiple device and diverse technology approaches such as surface acoustic wave devices.



NOTES:
1. PINS 1 AND 16 (Q AND $\overline{Q}$); 8 AND 9 (D AND $\overline{D}$); 12 AND 13 (CLK AND $\overline{CLK}$) MUST BE TERMINATED TO AC OR DC 50 Ω (SEE FIGURE 11).
2. CAPACITORS SHOWN ARE 0.1 μF CERAMIC CHIP TYPE AND ARE REQUIRED FOR ALL OPERATING CONDITIONS.

Figure 2. Package Connection

Table 1. HDMP-2501 Pin Connections Description

Label	Pin	Description
C_1	14	Charge pump capacitor connection. 0.1 μF typical, ground other end.
C_2	11	Charge pump capacitor connection. 0.1 μF typical, ground other end.
CLK	12	Retimed clock output AC or DC couple to 50 ohms, or DC couple to ECL.
$\overline{CLK}$	13	Retimed clock output (complimentary) AC or DC couple to 50 ohms, or DC couple to ECL.
D	8	Serial data input. ECL bias or AC couple with 0.1 μF.
$\overline{D}$	9	Serial data input (complimentary). ECL bias or AC couple with 0.1 μF
GND	2, 7, 10, 15	Ground
N/C	4	No connection to chip
Q	1	Retimed data output.
$\overline{Q}$	16	Retimed data output (compliment) AC or DC couple to 50 ohms, or DC couple to ECL.
V_{BB}	5	Internally generated bias reference voltage, typically -1.3 volts. Use bypass capacitor.
V_{EE}	6	Main power supply pin, typically -5.2 volts. Use bypass capacitor.
V_{TT}	3	Secondary power supply pin, typically -2.0 volts. Use bypass capacitor.

Absolute Maximum Ratings

T_C = 25°C, except as specified. Operation in excess of these may result in permanent damage to this device.

Symbol	Parameter	Units	Min.	Max.
V_{EE}	Supply Voltage	Volts	-6.0	
V_D	Data Input Voltage	Volts Pk to Pk		2.0
T_{op}	Case Operating Temperature	°C		+105
T_{stg}	Storage Temperature	°C	-60	+150
T_{max}	Maximum Assembly Temperature (for 60 seconds maximum)	°C		+300

Thermal Specifications

Symbol	Parameters	Units	Typical
θjc	Thermal Resistance (Die to Case)	°C/W	10
P_D	Power Dissipation at V_{EE} = -5.2V	Watts	1.4

DC Electrical Specifications

Symbol	Parameters	Units	Min	Typ.	Max.
V_{EE}	Supply Voltage	V	-5.46	-5.2	-4.94
I_{EE}	Supply Current	mA		230	
V_{TT}	Second Supply Voltage	V	-2.05	-2	-1.95
I_{TT}	Second Supply Current	mA		75	

AC Electrical Specifications

T_C = 25°C; V_{in} = 200 mV p-p @ 622 Mbp/s @ V_{EE} = -5.2V; V_{TT} = -2 V
Input data test sequence = PRBS @ 2^{23}-1; D and $\overline{D}$ are AC coupled (0.1 µF), 50Ω termination.
Integrating capacitors C_1 and C_2 are 0.1 µF (refer to Figure 2).

Symbol	Parameters	Units	Min.	Typ.
V_D	Minimum Data Input Voltage (pk - pk) (Ambiguity @ 10^{-7} BER)	mV		50
t_{acq}	Acquisition Lock Time	ms		2.3
t_r, t_f	Rise Time, Fall Time; Data and Clock See Figures 7 and 8	ps		200
J_g	Jitter Generation	ps (rms)		7.5
V_{CLK}	Recovered Clock Output (pk to pk)	V	0.6	0.7
V_Q	Output Voltage Swing (pk to pk) See Figure 7	V	0.6	0.7
VSWR	Data In and Out; Clock out	—		< 2:1

Theory of Operation

The retiming circuit is based on a PLL approach to timing extraction[1]. The functional block diagram is shown in Figure 1. A phase/frequency detector samples the incoming data, and generates an error signal which controls a dual input VCO. the VCO is realized as a ring oscillator in order to be integrated on the same chip.

The VCO frequency, F_0, is adjusted by feedback to a frequency approximately equal to the incoming data bit rate. The fine adjustment $\pm\Delta F$, is made by a bang-bang delay element as shown in Figure 3. The bang-bang element tracks the small variations of the incoming bit rate. The ring oscillator has a nominal delay of 800 ps with a typical usable range of ± 10%. The bang-bang fine control delay time is approximately 3 ps. The response time of the bang-bang element is about 700 ps for a full VCO update or much less than one clock cycle at 622 Mb/s.

The integrator (Figure 1) is achieved by a balanced charge-pump configuration with two off chip capacitors (pins 11 and 14).

[1]B. Lai and R. Walker, "A Monolithic 622 Mb/s Clock Extraction and Retiming Circuit", ISSCC91 Paper TPM 8.7.

Phase/Frequency Detector

The phase/frequency detector is shown in Figure 4. In the sampling pattern of Figure 4, the input data is sampled at three points: the bit prior to the transition, in the vicinity of the transition, and the bit following the transition. At each transition encountered, the clock can be deduced as either fast or slow compared to the incoming data. This information is used to generate a pulse train which updates the integrator and drives the bang-bang delay element.

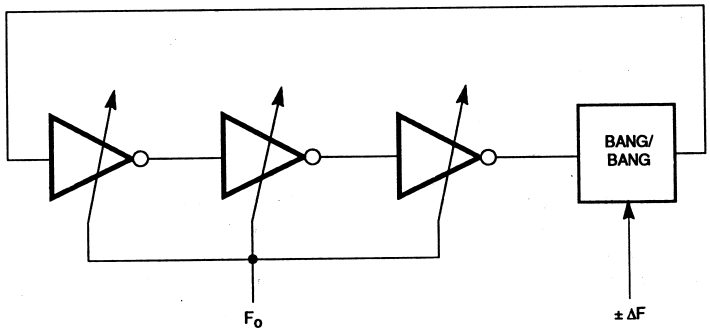
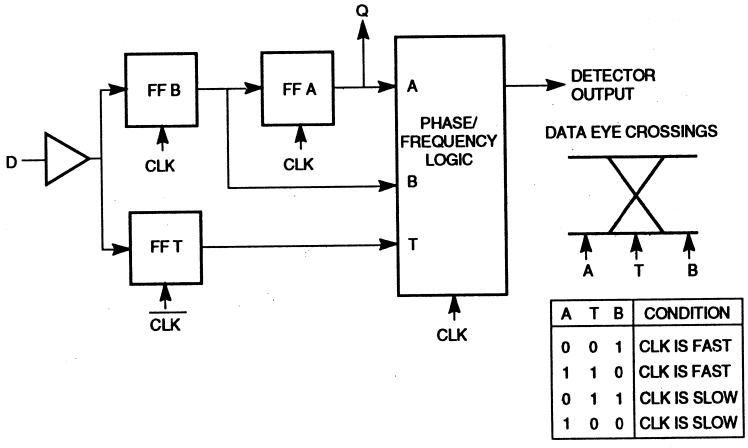


Figure 3. Ring Oscillator and Control Elements



A	T	B	CONDITION
0	0	1	CLK IS FAST
1	1	0	CLK IS FAST
0	1	1	CLK IS SLOW
1	0	0	CLK IS SLOW

Figure 4. Block Diagram of the Phase/Frequency Detector.

The phase tracking of clock to data behaves as shown in Figure 5. Each correction in the faster direction (clock phase increasing with respect to data phase) has slope $+\Delta F$, and each correction in the slower direction has slope $-\Delta F$. Over time, the VCO phase tracks the phase changes in the incoming data. Flip-flop A (Figure 4) samples at the center of the data eye and provides the decision circuit function.

Lock Capture

Initial lock acquisition behavior is highly complex and works best with high transition densities typical of pseudorandom bit patterns. Due to the phase frequency detector architecture, the acquisition behavior is different from a typical PLL.

Lock capture of repetitive data patterns becomes increasingly difficult as transition density decreases. This can cause lock acquisition times to be

significantly longer than expected or sub-harmonic false locks to occur.

The fact that false lock is weaker than true lock is essential to eliminating it. When both true and false phase locks occur, a slight displacement of the data phase relative to clock phase produces an error signal in the bang-bang detector which tends to restore it back to the original lock condition. This restoring force is represented at the integrating capacitor by a change in capacitor voltage which is in turn applied to the VCO to adjust the frequency. A simple idea to eliminate false lock is to connect a current source to the integrating capacitor (Figure 6). Its immediate effect is to ramp the capacitor voltage,

$$I_{CS} = \frac{dQ}{dt} = C\frac{dV}{dt},$$

which causes the VCO to sweep. If the capacitor charging rate is high enough to cancel out the "restoring force" current due to false lock, then false lock will be suppressed. However, the ramp current must not be so large it will suppress true lock. An estimate of true lock current can be obtained through acquisition lock time t_{acq}. For example, the HDMP-2501 with 0.1 µF integrating capacitors has a t_{acq} of approximately 2.3 mS. During this time the VCO control voltage changes about 1 Volt. Thus

$$I = C\frac{dV}{dt}(0.1\ \mu F)(\frac{1\ Volt}{2.3\ mS}) = 43\ \mu A$$

is an estimate of the ramp current.

A simple and inexpensive lock enhancement circuit is shown in Figure 7. The circuit consists of a very low frequency oscillator built from an inexpensive 555 timer chip, 3 resistors and 1 capacitor (plus a supply bypass capacitor). The time output is a 100 Hz TTL square wave applied via a large (15 kΩ) resistor to one side of the balanced HDMP-2501 integrator. Since the balanced integrator circuit uses differential pairs, the signal can be applied to only one side while the other side responds by symmetry.

To assist correct lock capture, the VCO can be forced to its center frequency by momentarily equalizing the two integration capacitor voltages (pins 11 and 14) as shown in Figure 6. The VCO then begins its lock capture from the center frequency which, by design, is close to the data frequency.

Input/Output Impedance Match

The input and output are closely matched to 50 ohms impedance. This allows easy interconnection to other circuits with minimum reflection of signals. The return loss performance is shown in Figures 10 and 11.

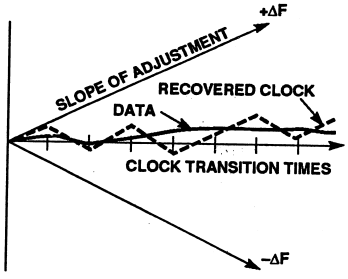


Figure 5. Clock Tracking of Data Phase.

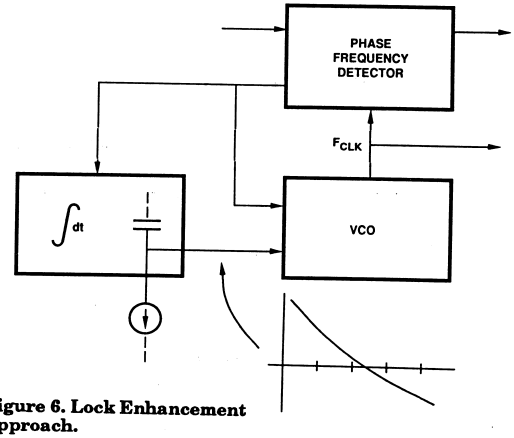


Figure 6. Lock Enhancement Approach.

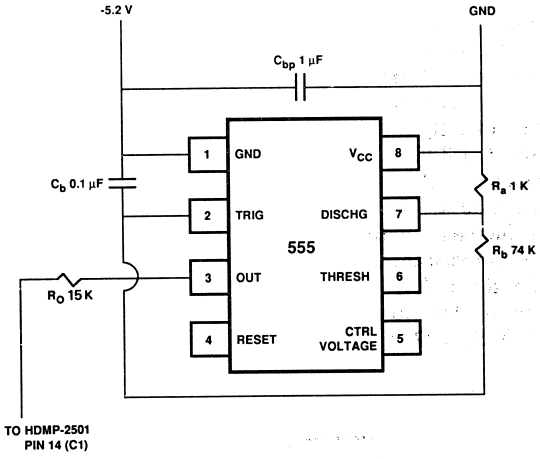


Figure 7. Practical Lock Enhancement Circuit.

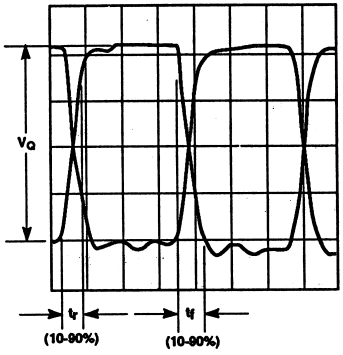


Figure 8. Typical Data Output Waveform.

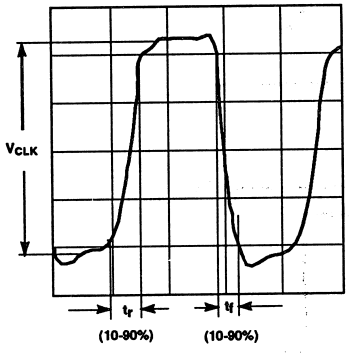


Figure 9. Typical Clock Output Waveform.

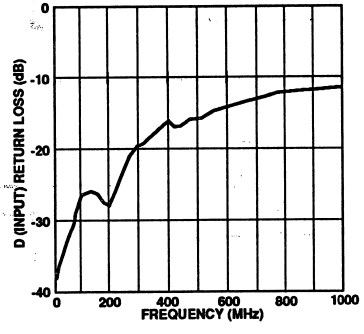


Figure 10. Typical Input Return Loss vs. Frequency.

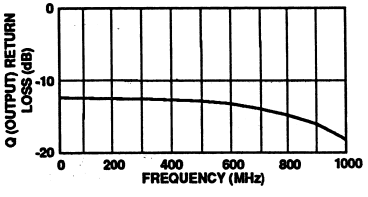


Figure 11. Typical Output Return Loss vs. Frequency.

Output Drive Level

The output driver is designed to deliver 0.8 V into 50 ohms, AC or DC coupled, as shown in Figures 12a and 12b.

The V_{OH} and V_{OL} levels of the driver are such that the peak-to-peak voltage is approximately 1.2 V unloaded centered around -1.3 V.

For driving ECL, the line can be terminated with a parallel combination of resistors as shown in Figure 12c. The equivalent termination of 50 Ω shrinks the peak-to-peak voltage down to approximately 0.8 V centered about -1.3 V. The output impedance of the driver is matched to 50 Ω. The amplitude can be increased with a larger termination resistance with minimal VSWR penalty. Nominal values for a 50 Ω interface are R_1 = 140 Ω, R_2 = 77 Ω.

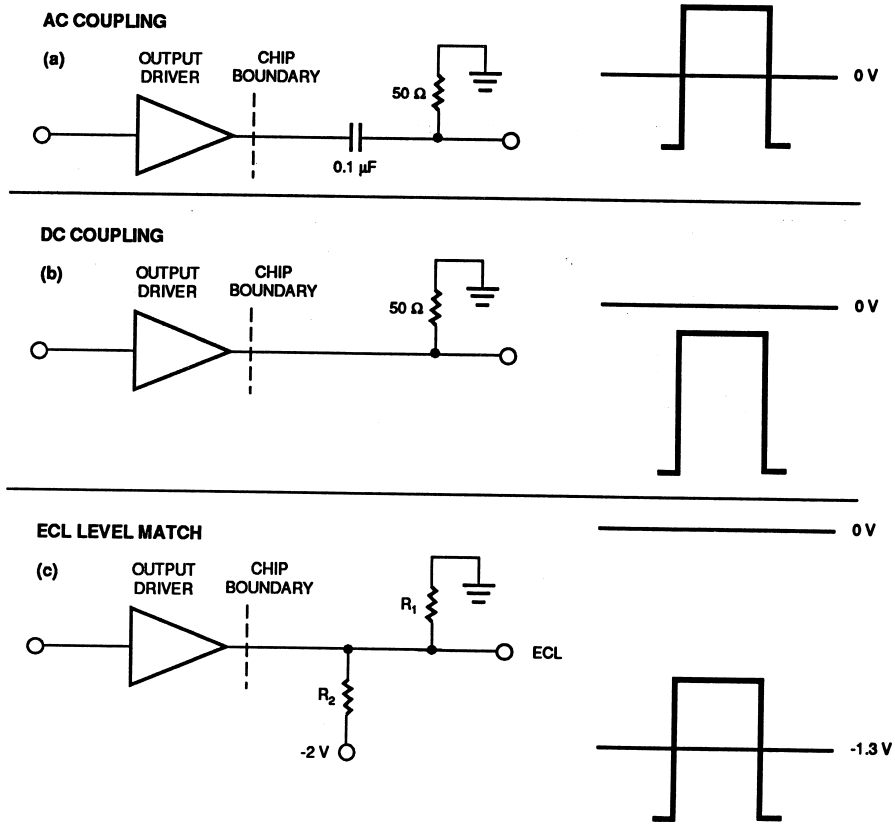


Figure 12. Output with Various Loading Conditions.

Performance vs. Supply Voltage V_{EE} Variation

The performance of the output voltage is shown in Figure 13. A 600 mV level for ECL compatibility is maintained.

VCO lock range is relatively insensitive to V_{EE} changes. The typical behavior is shown in Figure 14.

Temperature Performance

The VCO range of the HDMP-2501 is designed to accommodate variation over temperature. Figures 15 through 19 show typical performance over temperature.

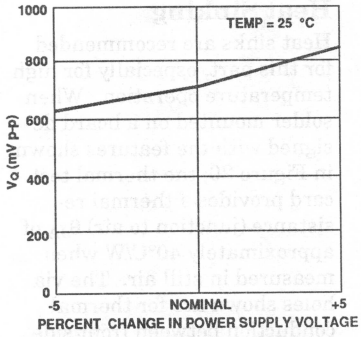


Figure 13. Output Voltage, V_Q vs. Power Supply, V_{EE}, Change.

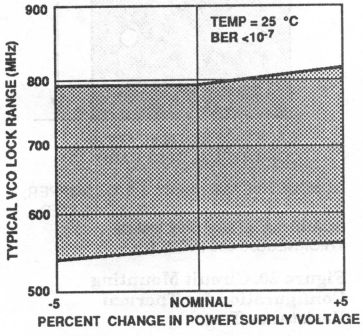


Figure 14. VCO Lock Range Variation vs. Supply Voltage, V_{EE}.

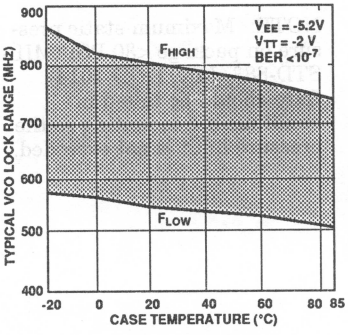


Figure 15. Typical VCO Lock Range Variation vs. Temperature.

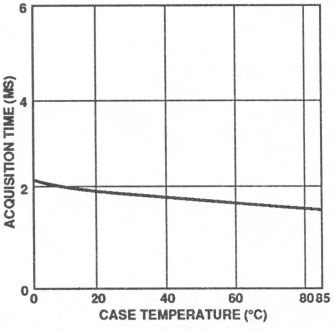


Figure 16. Typical Acquisition Time Variation vs. Temperature.

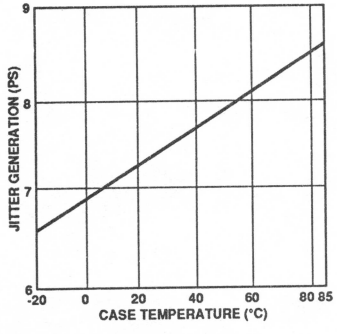


Figure 17. Typical RMS Value Jitter Generation Variation vs. Temperature with 3.5 ps Test Set Jitter.

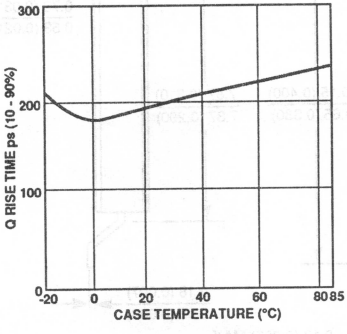


Figure 18. Typical Output Rise Time Variation vs. Temperature.

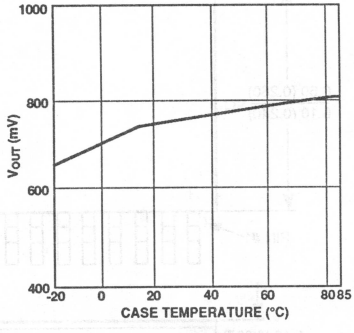


Figure 19. Typical Output Voltage Variation vs. Temperature.

Heat Sinking

Heat sinks are recommended for this part, especially for high temperature operation. When solder mounted on a board designed with the features shown in Figure 20, the thermal test card provides a thermal resistance (junction to air) θ_{JA} of approximately 40°C/W when measured in still air. The via holes shown are for thermal conduction between front side and back side metallization.

Package and Mechanical Considerations

The package is a glass metal construction designed for excellent high frequency electrical performance. The cover, base, and leads are gold plated Kovar (ASTM F-15 alloy). The mechanical outline is shown in Figure 21.

The base and cover of the package are electrically isolated and may be grounded. The base may be soldered to a printed circuit board.

NOTE: Maximum static pressure on package <30 PSI (MIL-STD-883, METHOD 1014). Care should be taken in handling and mounting so the pressure limit is not exceeded.

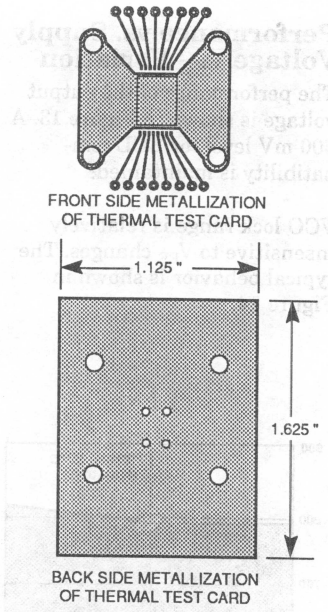


Figure 20. Circuit Mounting Configuration for Thermal Resistance Test.

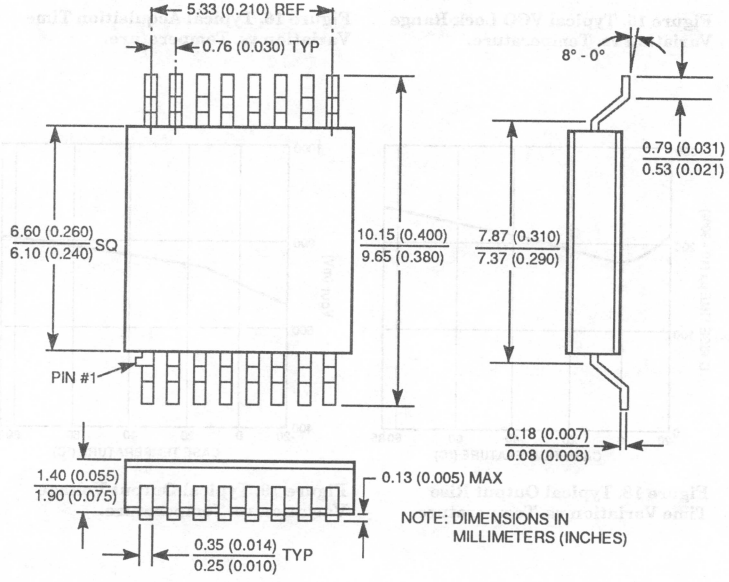


Figure 21. Outline F6.

HEWLETT PACKARD

Fiber Channel 266 MBaud Optical Link Card

Technical Data

HOLC-0266

Features

- **Conforms to ANSI X3T9.3 Fiber Channel Standard (25-M5-SL-I) (FC-0 Layer)**
- **Supports Link Lengths to 2 km at 266 MBaud**
- **Multi-Sourced Package/ Footprint**
- **Highly Reliable Multi-Mode Laser for High Performance at Low Cost**
- **Certified for Worldwide Class 1 Laser Safety Standards**
- **Industry Standard SC Connectors**
- **Highly Integrated Surface Mount Construction**
- **Industry Standard TTL Level Interface**

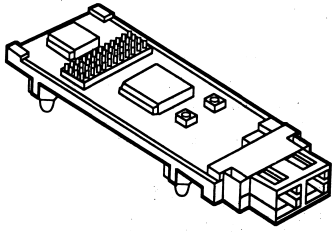
Applications

- **CPU to CPU**
- **CPU to Disk/Disk Array**
- **CPU to Peripheral**
- **Backplane Extender**
- **High Speed Data Switching**
- **Proprietary Point-to-Point Links**

Description

The HOLC-0266 optical link card (OLC) is a highly integrated fiber optic transmitter and receiver that provides a high speed serial link operating at a signaling rate of 265.625 MBaud implementing the fiber channel FC-0 specification for Short Wavelength (SWL) operation. This compact, double-sided, surface mount card conforms to Fiber Channel (25-M5-SL-I), a task group of the ANSI X3T9.3, Version 2.2 Standards Committee. The optical link card is designed to connect to a user's system card and communicates through a 10-bit wide encoded data (8B/10B) interface at industry standard TTL levels.

The OLC uses self-pulsating, SWL multimode lasers which are produced in high volumes, with proven high reliability, and low cost, for data transmission at low bit error rate (BER) levels. The OLC has on board all the functions necessary for sending 10-bit wide encoded data serially. These functions include the serializer, deserializer, clock recovery, laser driver, and automatic power control. All of these functions are implemented in silicon bipolar technology. In addition, the OLC uses an innovative open loop fiber control scheme that certifies the OLC for Class 1 laser safety limits. The OLC conforms to U.S. regulation DHHS 21 CFR(J), and internationally to IEC 825.



SIZE:
HEIGHT: 0.547 INCHES (13.9 mm)
WIDTH: 1.559 INCHES (39.6 mm)
LENGTH: 4.508 INCHES (114.5 mm)

The optical portion of the OLC interfaces to multimode optical fiber, (recommended 50/125 µm, 62.5 µm can also be used), through low loss, easy to use, push-pull SC connectors.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Reference
Storage Temperature	T_S	-40		+75	°C	Still Air
Relative Humidity - Storage	RH_S	5		95	%	
Ambient Operating Temperature	T_{OP}	0		60	°C	
Relative Humidity Operating	RH_{OP}	8		80	%	
Supply Voltage	V_{CC}	4.0	5.0	6.0	V	
Data Input Voltage	V_I	0		V_{CC}	V	

Caution: It is advised that normal static precautions be taken in handling and assembly of the OLC to prevent damage and/or degradation which may be induced by electrostatic discharge (ESD).
(ESD to 48 pin connector: 1000 V maximum per MIL-STD-883C HBM) (see Figure 1).

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Reference
Ambient Operating Temperature	T_{OP}	10		50	°C	Still Air
Supply Voltage	V_{CC}	4.75	5.0	5.5	V	
Low Data Input Voltage	V_{IL}	0		0.4	V	
High Data Input Voltage	V_{IH}	2.4		5.5	V	
Signaling Rate*	f_S	262.969	265.625	268.281	MBaud	

*For fiber channel compatibility, must be within ±0.01% of 265.625 MBaud.

Physical and Mechanical Description

The layout of the HOLC-0266 is shown in Figure 1. The transmit and receive circuits are mounted on opposite sides of a multi-layer, surface mount card. The card has a top and bottom signal plane and four internal power planes with the transmitter and receiver sides of the card electrically isolated. A 48-pin connector with 100-mil pin spacing is mounted on the receiver side of the OLC for connection to the user's system card. The laser is mounted in a receptacle with a graded index lens and an SC fiber optic connector. The receiver is a PIN photodiode also mounted in a receptable and an SC fiber optic connector, with a transimpedance amplifier mounted in an SOIC package under a metal shield. The connector ports are keyed and color coded to prevent misplugging. The receiver port is colored yellow, the transmitter port is black.

Electrical connection to the users system card is through the 48-pin connector (see note 17 on page 16). The OLC also uses a molded plastic frame with J-clips for precisely and securely mounting the OLC to the user's system card. A detailed outline drawing showing the dimensions of the card and mounting bracket is given in Figure 2.

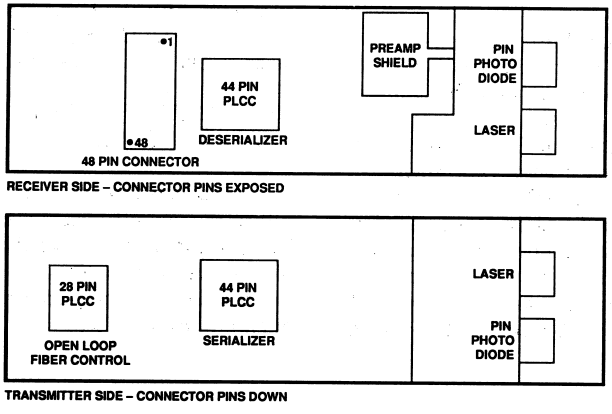


Figure 1. OLC Layout.

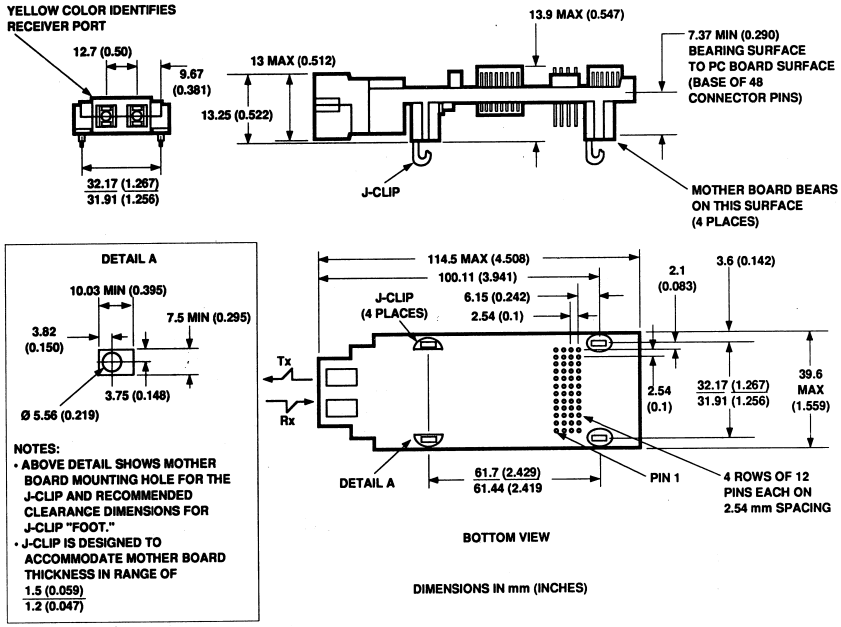


Figure 2. Optical Link Card Dimensions and Recommended Mounting Dimensions.

Electrical Description

Figure 3 is a block diagram of the transmitter, receiver and open loop fiber control portions of the HOLC-0266.

Transmitter:

10-bit wide encoded TTL level transmit data enters the shift register portion of the 44-pin PLCC serializer chip. This data is shifted out using an internal VCO at 265.625 Mb/s to the AC drive. A phase locked loop (PLL) generates the 265.625 MHz clock for the shift register, and the clock is phase locked to the user supplied 26.5625 MHz transmit clock. The AC drive modulates the 780 nm semiconductor laser with the serialized data. The DC section of the serializer controls the laser bias, keeping the laser at a correct preset power level. The DC drive also includes safety circuits that will disable the laser if an on-card fault occurs that could produce an unsafe laser power level. A multiplexer is used to provide the serialized data to the deserializer for operation of the OLC in the loopback mode.

Receiver:

The incoming laser light is received by a silicon PIN photodiode. This signal is amplified by the transimpedance amplifier which is contained in a 14-pin SOIC under the preamplifier shield. The PLL phase locks a 265.625 MHz clock to the incoming data and sends the data and the clock to the shift register of the 44-pin deserializer chip to be deserialized. The shift register uses a byte sync detector that detects the first seven bits of one polarity of the K28.5 character to enable complete bytes to be unloaded from the shift register without being fragmented. The deserializer recovers the clock and drives the 10-bit wide receive encoded data on the bus at TTL levels. Low speed Receive Clock 0 and Receive Clock 1 are output for use (see Figure 7).

Open Loop Fiber Control (OFC):

Two complementary phases of the 265.625 MHz clock are generated. The transition detector and the DC detector detect a minimum AC and DC level entering the PIN photodiode. These redundant signals are used by the open fiber control chip, a 28-pin PLCC module, as a safety interlock to shut down the link in the event of an open optical fiber. If the fiber is open, the OFC module pulses the laser at a low duty cycle. This produces Class 1 optical power in the open fiber. When the fibers are reconnected, the OFC returns the laser to continuous power. See the "Open Loop Fiber Control" section of this data sheet (page 10) for further information.

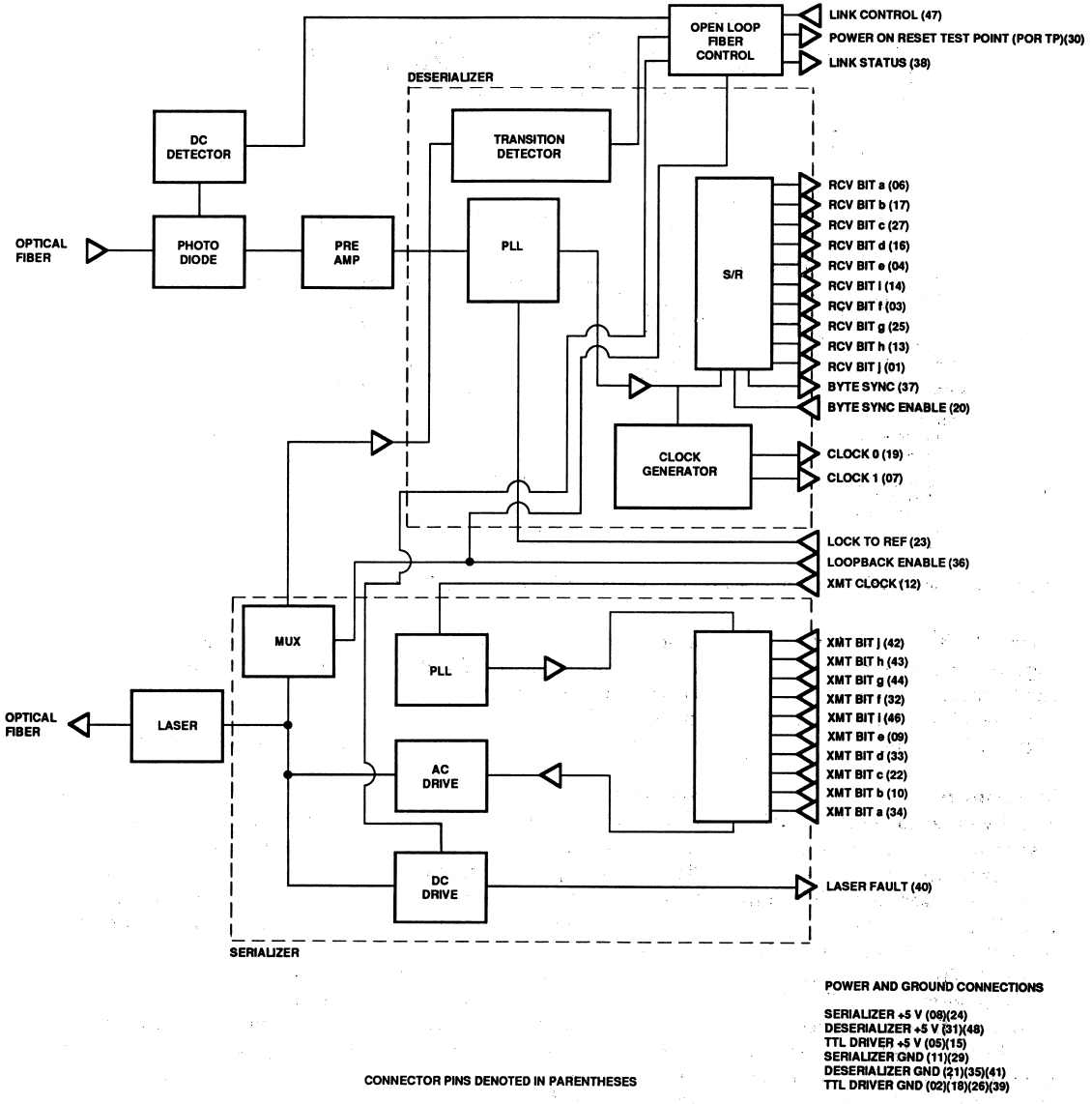


Figure 3. HOLC-0266 Functional Block Diagram.

Electrical Interface

Figure 4 defines the functions of the 48 connector pins. The pin functions and pin numbers are as viewed on the HOLC-0266 with the connector pins pointing up toward the viewer. These functions will be discussed in detail in the "OLC Input Definitions" (page 6) and "OLC Output Definitions" (page 6) sections of this specification.

Figure 5 represents the interface between the OLC and the user's system. The OLC interfaces directly with the encode/decode logic of the user's system.

37 • Byte Sync	25 • RCV bit g	13 • RCV bit h	1 • RCV bit j
38 • Link Status	26 • TTL Gnd	14 • RCV bit i	2 • TTL Gnd
39 • TTL Gnd	27 • RCV bit c	15 • TTL +5V	3 • RCV bit f
40 • Laser Fault	28 • No Connect	16 • RCV bit d	4 • RCV bit e
41 • Deserializer Gnd	29 • Serializer Gnd	17 • RCV bit b	5 • TTL +5V
42 • Xmt bit j	30 • POR TP	18 • TTL Gnd	6 • RCV bit a
43 • Xmt bit h	31 • Deserializer +5V	19 • RCV Clock 0	7 • RCV Clock 1
44 • Xmt bit g	32 • Xmt bit f	20 • Byte Sync Enable	8 • Serializer +5V
45 • No Connect	33 • Xmt bit d	21 • Deserializer Gnd	9 • Xmt bit e
46 • Xmt bit i	34 • Xmt bit a	22 • Xmt bit c	10 • Xmt bit b
47 • Link Control	35 • Deserializer Gnd	23 • Lock to Reference	11 • Serializer Gnd
48 • Deserializer +5V	36 • Loopback Enable	24 • Serializer +5V	12 • Xmt Clock

Figure 4. Connector Pin Definition (Pins Up)

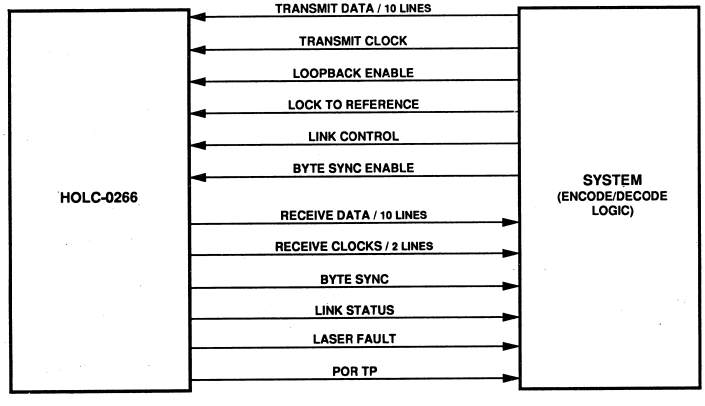


Figure 5. OLC/System Interface Signals.

OLC Input Definitions

Transmit Data:
Ten transmission lines carry 10-bit wide encoded data from the systems encode logic to the OLC to be received by the shift register of the serializer. The data will be serialized and launched onto the fiber starting with bit "a" and ending with bit "j" (see Note 8).

Transmit Clock:
The serializer uses the Transmit Clock to synthesize the 265.625 MHz clock (see Note 9). Figure 8 shows the relationship between the Transmit Clock and the Transmit Data. A minimum duty cycle of 40% is required for this clock to operate properly. A maximum of 10 ns jitter (peak to peak) is allowed on the rising edge of this clock.

Loopback Enable:
This active high signal wraps the Transmit Data from the Serializer to the Deserializer (see Note 10). The laser is disabled while Loopback Enable is active. Once Loopback Enable is deactivated one of two events will occur. If the link was active and operating prior to Loopback Enable being activated, the laser will be activated and will stabilize within 1.8 µs. If the link was not active prior to Loopback Enable being activated, the laser will pulse after 10.1 seconds and continue to pulse until the fiber is connected. See the section entitled "Open Loop Fiber Control" (page 10) for a complete description of the safety interlock.

Lock to Reference:
This is an active low signal that synchronizes the Deserializer phase locked loop to the Transmit Clock (see Note 11). This signal should stay on for approximately 8 µs. The Deserializer will be locked to the incoming serial data in less than 8 µs after Lock to Reference is deactivated. The 8 µs time period is approximate and is intended to represent the correct order of magnitude.

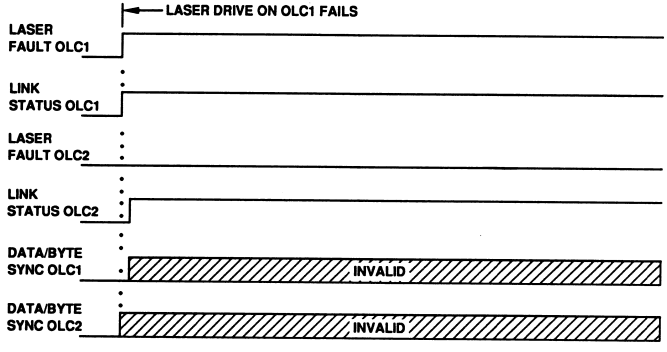


Figure 6. Laser Fault Sequence.

Link Control:
This active high signal turns the laser off (see Note 12). When this line is deactivated, the Open Loop Fiber Control Module will connect the link within 10.1 seconds.

Byte Sync Enable:
Asserting the active high signal makes the Deserializer reset the Receive Clocks when a comma character (see Byte Sync) is detected (see Note 11). When this signal is low, the comma character is treated as normal data.

OLC Output Definitions

Receive Data:
Ten lines are used by the Deserializer to send 10-bit wide encoded data to the system's decode logic (see Note 6). These signals are clocked by the systems receive clocks inside the decode logic. The relationship between Receive Clocks and Receive Data is shown in Figure 7. If no light is received by the PIN photodiode, or the PLL is out of lock for some other reason, the Receive Data lines will be random. A Loopback Enable mode initiated on an upstream OLC will cause the Open Loop Fiber Control module on that OLC to turn its laser off. Under these conditions, data at the output of the downstream deserializer will be invalid. In addition, if the Deserializer is in the Lock to Reference mode, the Receive Data will be invalid.

Receive Clocks:
The Deserializer generates two complementary clocks for use by the system's decode logic to clock the Receive Data into an elastic buffer (see Note 6). These

clocks will be reset anytime a Byte Sync word is received. If a Byte Sync word is received asynchronously (see Figure 7), the Receive Clocks will immediately be reset. The worst case duty cycle of the Receive Clocks is 30%. If no light is received by the PIN photodiode, or the PLL is out of lock for some other reason, the Receive Clocks will be operating at a frequency between 17 MHz and 33 MHz.

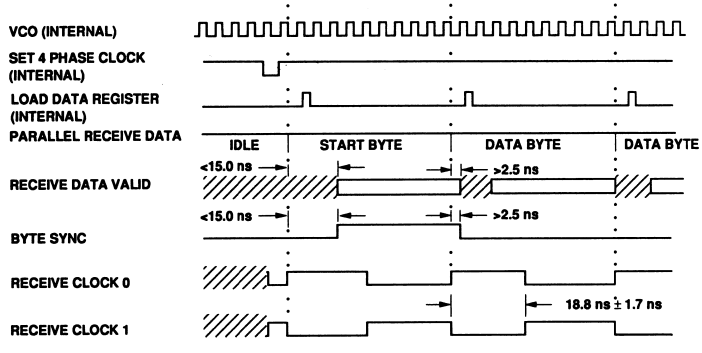
Byte Sync:
This active high signal is driven by the Deserializer (see Note 6). When the Deserializer detects a comma character, it sets the Byte Sync high for one cycle indicating the start of a frame. The Receive Clocks are reset according to Figure 7. The comma detect function detects the first seven bits of one polarity of the K28.5 character (0011111010) as defined in the IBM Journal of Research and Development, Vol. 25, No. 5, September 1983, 8B/10B Transmission Code. Bit a is launched on the fiber first, bit j is last. If no light is detected by the PIN photodiode, or the PLL is out of lock for some other reason, the Byte Sync line will pulse randomly.

a	b	c	d	e	i	f	g	h	j
0	0	1	1	1	1	1	X	X	X

Link Status:
This active high signal is driven by the Open Loop Fiber Control circuitry (see Note 7). Link Status high indicates an open fiber connection. In this mode, the Open Loop Fiber Control will be pulsing the laser at a low power level, meeting Class 1 safety requirements. Once the fiber is reconnected, the link will be re-established in less than 10.1 seconds. It takes several milliseconds for Link Status to go high after the fiber is disconnected. Invalid Receive Data and Byte Sync will occur prior to the Link Status being activated high.

Laser Fault:
This active high signal is driven by the Serializer (see Note 7). Once an improper power level in the laser driver is detected, the Serializer activates the Laser Fault and the laser is turned off in approximately 1 ms. During power up, the laser control loop will stabilize in less than 100 ms after the supply reaches 4.0 V. When the Laser Fault is activated, the Open Loop Fiber Control shuts down the laser through two independent paths so a single malfunction cannot prevent the laser from being turned off. The OLC receiver connected to this laser will detect a loss of light (no light at the PIN photodiode), and Link Status will be activated. Figure 6 shows the sequence of events during a laser driver hardware malfunction.

Power On Reset Test Point (POR TP):
This signal is used to test the OLC (see Note 7). POR TP is at an undetermined level when the +5 V supply is below 3.6 V. POR TP is low when the supply is between 3.6 V and 4.75 V, and it is high when the supply is greater than 4.75 V.



NOTE: ALL CRITICAL TIMINGS ARE REFERENCED TO THE POSITIVE EDGE OF THE CLOCKS, ASSUMING 30 pF OUTPUT LOADS ON CLOCK AND DATA LINES.

Figure 7. Deserializer Interface Receive Timings.

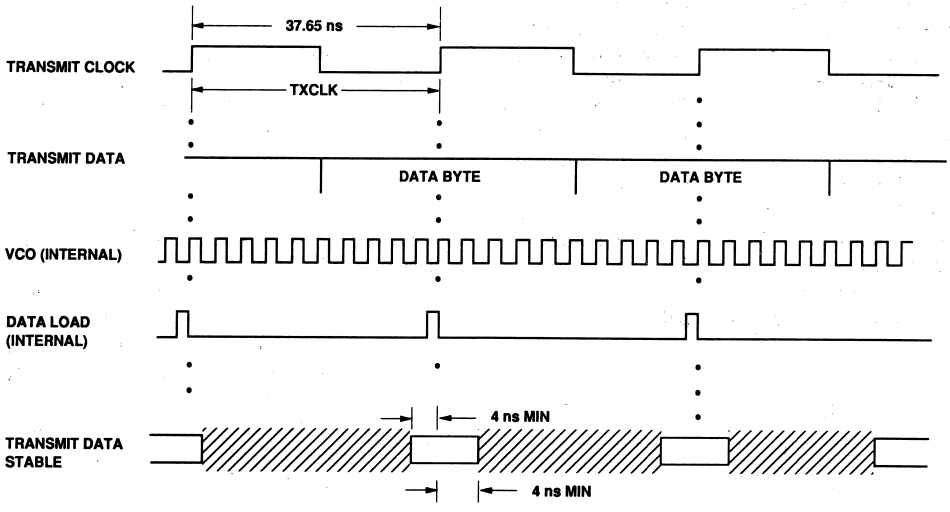
Link Operation

Serial Link Receive Operation: The Deserializer generates two complementary clocks for use in clocking the parallel data coming from the Deserializer. Each of the Receive Clocks has a nominal 37.65 ns period. Figure 7 shows the relationship of the Start Byte, the Receive Data, the Byte Sync Pulse, and the two Receive Clocks generated by the Deserializer.

Serial Link Transmit Operation:
The Serializer uses a single-phase 37.65 ns Transmit Clock for transmit operations. Figure 8 shows the timing relationship of the Transmit Clock and the Transmit Data.

Link Acquisition Sequence:
The following sequence and conditions are required for proper OLC operation. The receive PLL will not self-lock to the incoming data stream. For example, when the card is powered up or the fiber is connected, the receive PLL will be out of bit sync. Random data will be on the 10 receive data lines, the Byte Sync line will pulse randomly, and the Receive Clocks will not be at 26.5625 MHz. To acquire bit sync, the link acquisition sequence must be followed. This has no effect on the transmit data.

- Bring Lock to Reference low for at least 8 µs after the Link Status line is low.
- The upstream station should transmit valid 8B/10B encoded data. The transmitting station clock and the receiving station clock frequencies must be within 0.5% of each other for phase lock to be assured.
- Bring Lock to Reference high (wait at least 8 µs).
- The OLC will now be in bit sync. The data on the receive lines will be correct.



NOTE: ALL CRITICAL TIMINGS ARE REFERENCED TO THE POSITIVE EDGE OF THE TRANSMIT CLOCK. JITTER OF THE POSITIVE EDGE MUST BE LESS THAN 1.0 ns.

Figure 8. Serializer/Deserializer Interface Transmit Timings.

Electrical/Optical Characteristics (T_A = 10°C to 50°C, V_{CC} = 4.75 V to 5.50 V)

Transmitter Section

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Voltage	V_{CC}	4.75	5.0	5.50	V	
Supply Current	I_{CC}	190		320	mA	
Power Dissipation	P_D	0.9		1.80	W	
Data Input Voltage - Low	V_{IL}	0		0.4	V	Note 6
Data Input Voltage - High	V_{IH}	2.4		4.0	V	Note 6
Spectral Center Wavelength	λ	770	780	850	nm	
Spectral Width	FWHM			4	nm	RMS value
Launched Optical Power	P_T	-5.0		0	dBm (avg.)	Note 1
Optical Extinction Ratio		6			dB	Note 2
Relative Intensity Noise	RIN_{12}			-112	dB/Hz	Note 3
Eye Opening		61			% (pk-pk)	Note 4
Random Jitter @ ±7 sigma limit points	RJ		19		% (pk-pk)	Note 5
Numerical Aperture	NA		0.20			

Receiver Section

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Voltage	V_{CC}	4.75	5.0	5.5	V	
Supply Current	I_{CC}	200		240	mA	
Power Dissipation	P_D	0.95		1.32	W	
Data Output Voltage - Low	V_{OL}	0		0.8	V	Note 8
Data Output Voltage - High	V_{OH}	2.0		V_{cc}	V	Note 8
Return Loss of Receiver	RL	12			dB	
Receiver Sensitivity		-17		0	dBm (avg.)	Note 13
Numerical Aperture	NA		0.20			

Optical System Performance

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Signaling Rate*	f_S	262.969	265.625	268.281	MBaud	
Link Length 50/125 µm NA = 0.20		0.002		2.0	km	Note 14
Link Length 62.5/125 µm NA = 0.275		0.002		0.70	km	Note 15
Optical Power Budget	OPB			12	dB	Notes 14,15
Bit Error Rate	BER			10^{-12}		
SC Optical Connector Attenuation			0.25		dB	Note 16
Attenuation (EOL)				0.5	dB	Note 16
Connects/Disconnects				250		Note 16

*For fiber channel compatibility, must be within ±0.01% of 265.625 MBaud.

Open Loop Fiber Control

A safety interlock is provided by the Optical Fiber Control (OFC) module on the OLC. When the OLCs are connected as in Figure 9 (below), the OFC module detects when a fiber is opened. This sequence is shown in Figure 10. If Path A is opened, the OFC on OLC2 detects it and pulses its laser at a low duty cycle. The OFC on OLC1 detects this pulse signal and also pulses its laser at a low duty cycle. This provides Class 1 optical power in Path A, the open path. OLC1 launches a pulse synchronously with the pulse it receives on Path B. OLC2, however, receives no pulse and continues in inactive mode, launching pulses. When Path A is restored, OLC2 receives pulses synchronously with its transmit pulses. OLC2 then turns off its laser and confirms that its receive pulse disappears in 1.23 ms. If it does, OLC2 then turns on the laser and confirms that it receives light in 671 µs. If it does, it keeps the laser on. This confirms that the first synchronous pulse actually came from another OLC. The OFC goes to Active Mode and the laser is on continuously. Continuous power is now restored to both paths. The longest time that this reconnect sequence will take is 10.1 seconds. Note that the term synchronous used in the above discussion is valid since the delays on the OLC and the time of flight on the fiber are insignificant compared to 617 µs.

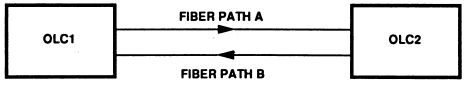


Figure 9. OLC Fiber Connection.

Laser Safety Compliance Requirements

This product is designed and certified as Class 1. It is to be used only with another Hewlett-Packard HOLC-0266 or a certified equivalent OLC to ensure Class 1 performance. This equivalent OLC must contain the Open Fiber Control system as described in the "Open Loop Fiber Control" section (above) of this specification. This is a requirement for proper operation of the HOLC-0266. Figure 10 contains a description of the open loop fiber control sequence.

The functional power supply range is specified at 4.75 V to 5.5 V. Operation outside this range may degrade performance and lifetime of the OLC. The system using the OLC must provide power supply protection that guarantees a voltage of 5.0 V ± 20% to maintain Class 1 operation.

Connection of an OLC to a non-approved optical source or operating the power supply below 4.0 V or above 6.0 V may result in hazardous radiation exposure, and may be considered an act of modifying or new manufacturing of a laser product under US regulations contained in 21 CFR(J) or CENELEC regulations contained in HD 482 S1. The person(s) performing such an act are required by law to re-certify and re-identify the product in accordance with the provisions of 21 CFR(J) for distribution within the U.S.A., and in accordance with provisions of CENELEC HD 482 S1 (or successive regulations) for distribution within the CENELEC countries or countries using the IEC 825 standard per VDE Reg. Nr. 3642.

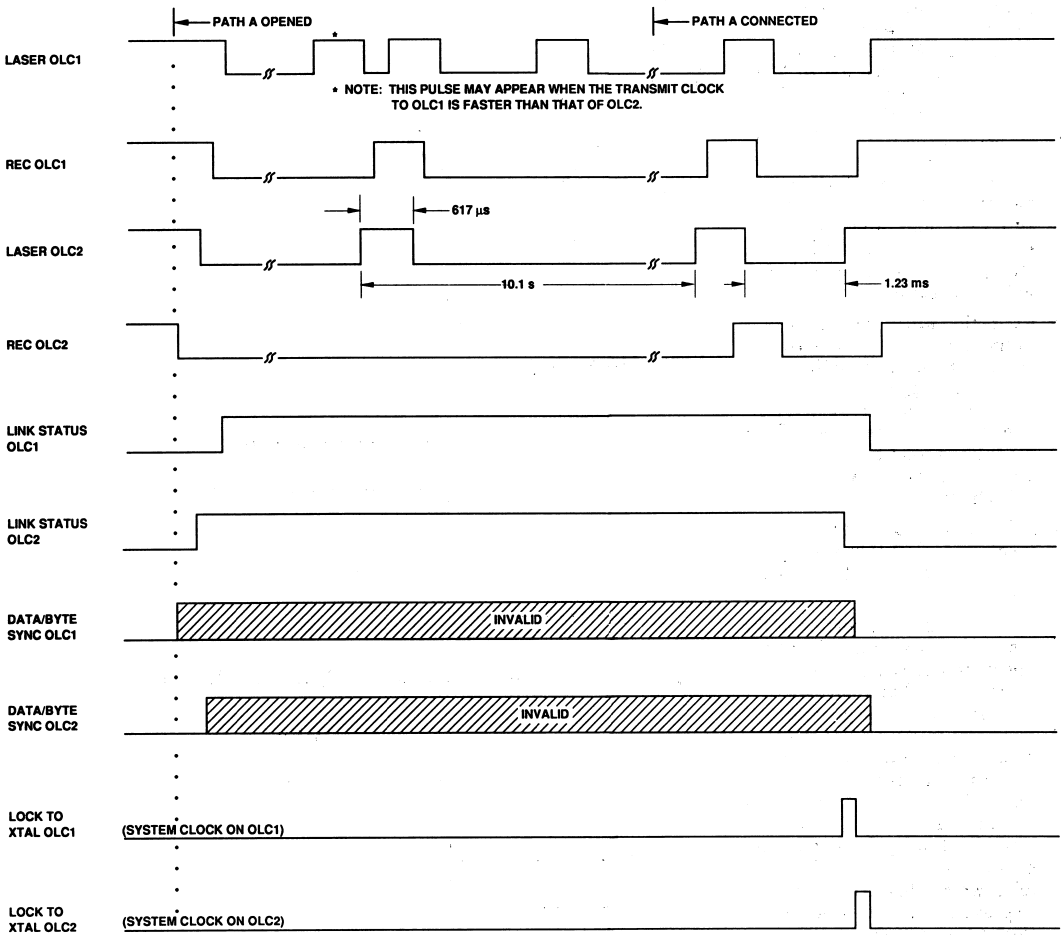


Figure 10. Open Loop Fiber Control Sequence.

Notes:

1. Launched optical power is measured at the end of a 2 m section of a 50/125 µm fiber with a nominal NA = 0.20. The maximum and minimum of the allowed range of average transmitter power coupled into the fiber are worst case values to account for manufacturing variances, drift due to temperature variations, and aging effects; and operation within the specified minimum value of extinction ratio.
2. Extinction Ratio is the minimum acceptable value of the ratio of the average optical energy in a logic level one to the average optical energy in a log level zero measured under fully modulated conditions in the presence of worst case reflections.
3. RIN_{12} is the laser noise measured relative to average optical power with 12 dB return loss.
4. Eye opening is the portion of the bit time which is error free for a given bit error rate (BER). The Fiber Channel standard for BER is < 10^{-12}. The general laser transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram. These characteristics include rise time, fall time, pulse overshoot, pulse undershoot, and ringing, all of which should be controlled to prevent excessive degradation of the receiver sensitivity. For the purpose of an assessment of the transmit signal, it is important to consider not only the eye opening, but also the overshoot and undershoot limitations. The parameters specifying the mask of the transmitter eye diagram are shown in Figure 11.
5. Random Jitter (RJ) is due to thermal noise which may be modeled as a Gaussian process. The peak-to-peak value of RJ is of a probabilistic nature and thus any specific value requires an associated probability.

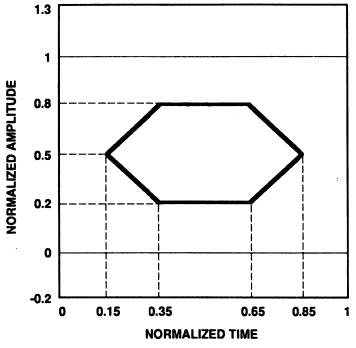


Figure 11. Eye Diagram.

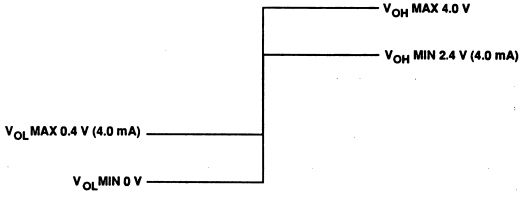


Figure 12. Receive Clock, Data and Byte Sync Driver Levels.

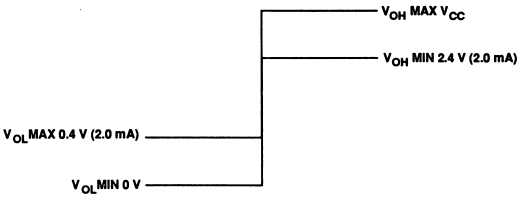


Figure 13. Link Status, Laser Fault and POR TP Driver Levels.

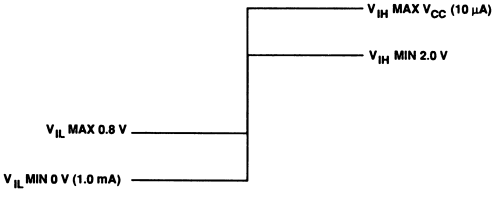


Figure 14. Transmit Data Receiver Levels.

6. The drive levels given are appropriate for Receive Data, Receiver Clock, and Byte Sync signals. The Receive Data, Receive Clock, and Byte Sync TTL drivers are push-pull totem pole drivers with a 25 Ω series resistor to dampen transmission line reflections (see Figure 12).
7. The Link Status, Laser Fault, and POR TP lines are control signals that should be treated as asynchronous lines. The drive levels for Link Status, Laser Fault, and POR TP are shown in Figure 13.
8. Figure 14 shows the receive levels for the Transmit Data lines.
9. Figure 15 shows the receive levels for the Transmit Clock.
10. Figure 16 shows the receive levels for the Loopback Enable.
11. Figure 17 shows the receive levels for the Lock to Reference and Byte Sync Enable lines.
12. Figure 18 shows the receive levels for the Link Control line.
13. The minimum and maximum values of the average received power in dBm give the input power range to maintain a BER < 10^{-12}. These values take into account power penalities caused by the use of a transmitter with worst-case combination of transmitter spectral, extinction ratio and pulse shape characteristics.
14. Optical Fiber with core diameter of 50 µm and cladding diameter of 125 µm, and a nominal Numerical Aperture of 0.20 is recommended. The modal bandwidth (-3 dB optical minimum) of the 50/125 µm fiber should be 500 MHz * km at a wavelength of 850 nm. This allows for a modal bandwidth of 400 MHz * km at 780 nm. Fiber attenuation should be 3.0 dB/km maximum at 850 nm. This allows for a fiber attenuation of 4.0 dB/km maximum at 780 nm.
15. Optical fiber with a core diameter of 62.5 µm, and a nominal Numerical Aperture of 0.275 can also be used with the HOLC-0266 OLCs. The modal

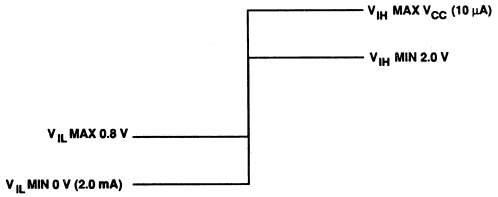


Figure 15. Transmit Clock Receiver Levels.

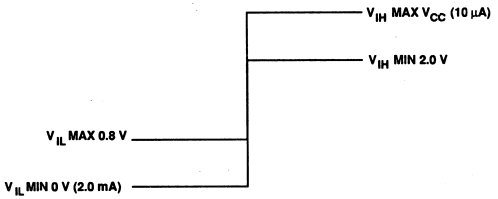


Figure 16. Loopback Enable Receiver Levels.

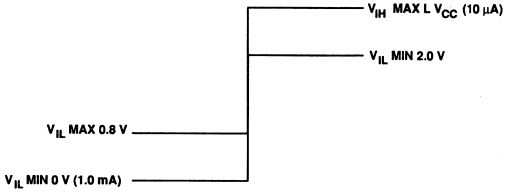


Figure 17. Lock to Reference and Byte Sync Enable Receiver Levels.

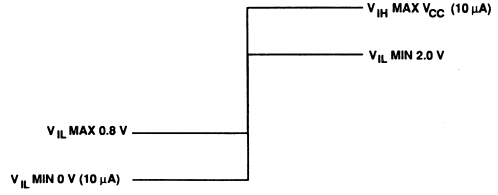


Figure 18. Link Control Receiver Levels.

bandwidth (-3dB optical minimum) should be 160 MHz • km at a wavelength of 850 nm. The length limit of 0.70 km is due to the restricted fiber bandwidth.

16. The optical interface connector dimensionally conforms to the industry standard SC type connector documented in JIS-5973. A dual keyed SC receptacle serves to align the optical transmission fiber mechanically to the OLC. The transmit side of the receptacle is color coded black, the receiver side of the receptacle is color coded yellow. See Figure 19 for a drawing of the duplex SC receptacle that is part of the OLC.

17. A possible source of the SC Duplex Cable Assembly is:
    Alcoa Fujikara Ltd.
    Telecommunications Division
    P.O. Box 5831
    Spartanburg, South Carolina 29304
    Phone# (803) 439-5160
    Fax# (803) 433-5353
    Product: SC Duplex Cable Assembly with HP Clip
    P/N: C020818

A possible source of the 48 pin connector product is:
    3M Company
    Electronics Product Division
    P.O. Box 2963
    Austin, TX 78763
    Phone#: (800) 225-5373
    Fax#: (800) 325-5329
    Product: 48 Position, 4 Row, 100 mil Spaced Board Mount Socket Connector P/N: 962456-01-12-30

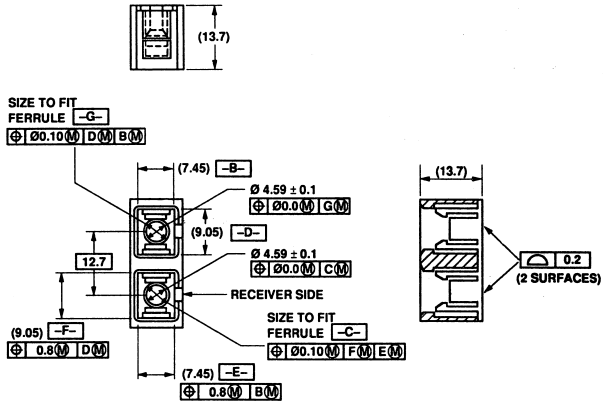


Figure 19. Duplex SC Receptacle.

Designer Kit Ordering Information

Fiber Channel 266 MBaud Optical Link Card Designer's Kits may be ordered through your local HP Components Representative or authorized HP Components distributor.

Designer Kit

Part Number	Kit Description
HOLC-K266	Two HOLC-0266 cards, 4m SC Duplex Cable Assembly, Two 48-pin electrical connectors, and literature

HEWLETT PACKARD

Silicon Bipolar Monolithic Variable Gain Amplifier

Technical Data

HPVA-0180

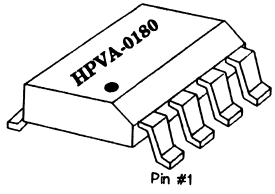
Features

- **3 dB Bandwidth: DC to 2.5 GHz**
- **Temperature Compensated Bias**
- **Single Ended or Differential Operation**
- **Low Cost Plastic Surface Mount Package**
- **Linearized Gain Control (S_{21} Magnitude)**

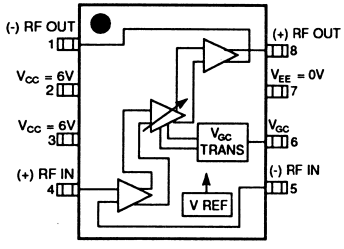
Applications

- **VHF/UHF Transceivers**
- **RF Data Links**
- **Broadband LAN's**

Plastic SO-8 Package



Functional Block Diagram and Pin Configuration



Description

The HPVA-0180 is a silicon monolithic variable gain amplifier in a plastic surface mount SO-8 package. It is designed for wide or narrow bandwidth applications from DC to 2.5 GHz. The amplifier provides 20 dB gain (26 dB in differential operation) with 20 dB gain control over its entire DC to 2.5 GHz bandwidth, and dissipates only 250 mW from a single 6 volt power supply. The device may be operated in any combination of single-ended or differential input/output configurations.

The internal signal path of the amplifier is fully differential to achieve the highest possible immunity against transition noise. The HPVA-0180 also features a band-gap voltage reference to stabilize the bias against temperature variations and a gain control linearizer for linear gain change with gain control voltage variation.

The device is manufactured using Hewlett-Packard's 13 GHz F_t, 25 GHz F_{max} silicon bipolar integrated circuit process.

HPVA-0180
Absolute Maximum Ratings, T_A = 25°C*

Device Voltage, V_{CC} ..... 7 Volts
RF Input Power, P_{in} ..... +10 dBm
Gain Control Voltage, V_{GC} ..... 0 Volts to V_{CC}
Junction Temperature, T_j ..... +150°C
Storage Temperature, T_{stg} ..... -55° to +150°C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

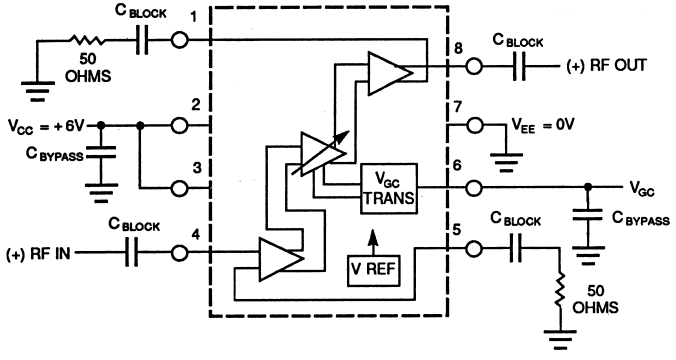
Care should be taken to prevent Electro Static Discharge (ESD) that could permanently damage the device. (Class II sensitivity)

Notes:

1. A θ_{JA} of 200°C/W should be used for derating and junction temperature calculations: $T_J = (P_D \times \theta_{JA}) + T_A$
2. Maximum soldering temperature is 260°C for 5 seconds.

Electrical Specifications, T_A = 25°C

Symbol	Parameters / Test Conditions: V_{CC} = 6 V, Z_o = 50 Ohms, Single Ended Operation, Gain Set = +20 dB	Units	Min.	Typ.	Max.
G	Small Signal Gain $\|S_{21}\|^2$, V_{GC} = 5 Volts, f = 300 MHz	dB		21	
F_{3dB}	3 dB Bandwidth	GHz		2.5	
V_{GC}	Gain Control Range f = 300 MHz, V_{GC} = 3 to 5 Volts	dB		20	
P_{1dB}	Output Power at 1 dB Gain Comp. f = 300 MHz	dBm		-3	
IP_3	Output 3rd Order Intercept Point, F1 = 300 MHz, F2 = 305 MHz	dBm		7	
NF	50 Ohm Noise Figure f = 300 MHz	dB		16	
VSWR	Input VSWR V_{GC} = 3 to 5 Volts, f = 10 MHz to 2,000 MHz			1.8	
	Output VSWR V_{GC} = 3 to 5 Volts, f = 10 MHz to 2,000 MHz			1.8	
$\|S_{12}\|^2$	Isolation, $\|S_{12}\|^2$, f = 300 MHz	dB		32	
ΔG	Gain Flatness f = 10 MHz to 2,000 MHz	dB		±0.8	
I_{CC}	Supply Current	mA	30	41	60
I_{GC}	Gain Control Supply Current	mA		0.1	



Transmission lines (50 ohms) are recommended for all RF input and output connections.
The use of chip capacitors and chip resistors will minimize unwanted parasitics.

Typical Biasing Configuration

HPVA-0180 Typical S-Parameters

Z_O = 50 Ohms, T_A = 25° C, V_{CC} = 6 V, V_{GC} Set for Nominal +20 dB Gain.

Frequency	S_{11}		S_{21}			S_{12}			S_{22}	
MHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
10	0.23	0	20.3	10.38	-2	-44.3	0.007	-34	0.09	2
50	0.24	-4	20.2	10.23	-9	-39.3	0.011	-113	0.10	7
100	0.21	-3	20.3	10.31	-17	-40.9	0.009	68	0.12	29
200	0.23	-3	20.2	10.25	-35	-33.7	0.021	56	0.16	26
300	0.19	-9	20.1	10.05	-53	-32.0	0.025	38	0.20	23
400	0.14	-1	19.8	9.75	-70	-27.0	0.045	23	0.20	17
500	0.15	18	19.4	9.32	-87	-27.7	0.041	15	0.24	16
600	0.18	29	19.0	8.94	-102	-26.5	0.047	3	0.29	0
700	0.25	31	18.7	8.65	-116	-27.7	0.041	-30	0.28	-21
800	0.28	23	18.8	8.66	-130	-29.2	0.035	-31	0.27	-43
900	0.30	11	19.0	9.88	-145	-31.8	0.026	-61	0.24	-66
1,000	0.28	-3	19.0	8.91	-161	-30.7	0.029	-76	0.21	-90
1,100	0.27	-15	19.3	9.24	-178	-40.9	0.009	-47	0.16	-109
1,200	0.23	-25	19.4	9.33	166	-37.3	0.014	-21	0.14	-110
1,300	0.20	-32	19.4	9.35	149	-36.3	0.015	3	0.15	-125
1,400	0.14	-34	19.6	9.59	132	-31.1	0.028	10	0.16	-142
1,500	0.12	-42	19.5	9.45	115	-30.1	0.031	-13	0.15	-156
1,600	0.09	-37	19.5	9.40	97	-28.3	0.039	0	0.15	-168
1,700	0.10	-10	19.3	9.21	79	-28.2	0.039	-16	0.14	-168
1,800	0.10	-14	19.5	9.45	62	-25.9	0.051	-32	0.11	-179
1,900	0.11	-21	19.4	9.29	45	-24.7	0.058	-46	0.16	174
2,000	0.12	-54	19.6	9.58	28	-24.1	0.062	-62	0.17	167
2,100	0.10	-68	19.9	9.85	9	-25.6	0.053	-49	0.21	159
2,200	0.10	-83	20.0	10.00	-12	-24.3	0.061	-60	0.28	139
2,300	0.06	-163	19.8	9.79	-33	-22.7	0.073	-71	0.34	122
2,400	0.08	158	19.5	9.43	-56	-23.6	0.066	-84	0.40	105
2,500	0.11	126	18.7	8.57	-76	-25.1	0.055	-90	0.43	90
2,600	0.17	103	17.7	7.89	-95	-24.6	0.059	-101	0.44	80
2,700	0.20	84	16.7	6.80	-115	-22.8	0.072	-99	0.46	66
2,800	0.24	69	15.6	6.00	-134	-23.7	0.065	-101	0.48	61
2,900	0.29	48	14.8	5.50	-153	-21.6	0.083	-115	0.45	56
3,000	0.36	45	14.0	5.03	-169	-23.0	0.071	-125	0.42	52
3,100	0.35	27	13.1	4.50	178	-23.7	0.065	-115	0.44	52
3,200	0.38	31	12.0	4.00	162	-21.0	0.089	-119	0.39	48
3,300	0.43	27	11.3	3.67	147	-20.9	0.091	-135	0.33	47
3,400	0.48	24	10.3	3.28	130	-20.6	0.094	-144	0.32	42
3,500	0.47	23	9.2	2.88	115	-20.2	0.098	155	0.24	43
4,000	0.40	15	5.1	1.81	44	-19.0	0.112	-166	0.18	90

HPVA-0180 Typical Performance Parameters

Z_O = 50 Ohms, T_A = 25° C, V_{CC} = 6 V, V_{GC} Set for Nominal +20 dB Gain.

Frequency MHz	Linear Phase Deviation (Deg.)	Relative Phase (Deg.)	Gain Deviation (dB)	Group Delay (ns)	Input VSWR	Output VSWR
10	-0.3	0.0	0.0	0.52	1.6	1.2
50	-0.7	-10.7	-0.01	0.46	1.6	1.2
100	-1.1	-19.5	0.00	0.49	1.6	1.3
200	-2.2	-37.0	-0.01	0.49	1.6	1.4
300	-3.0	-50.9	-0.02	0.48	1.5	1.5
400	-4.0	-72.1	-0.54	0.49	1.4	1.5
500	-4.0	-88.5	-0.93	0.46	1.4	1.7
600	-2.4	-103.5	-1.30	0.42	1.5	1.8
700	0.1	-117.6	-1.58	0.39	1.7	1.8
800	2.4	-131.7	-1.57	0.39	1.8	1.7
900	3.6	-147.1	-1.35	0.43	1.8	1.6
1,000	4.0	-163.1	-1.32	0.45	1.8	1.5
1,100	3.8	-180.0	-1.00	0.47	1.8	1.4
1,200	4.3	-196.1	-0.92	0.44	1.5	1.4
1,300	4.5	-212.4	-0.91	0.46	1.5	1.4
1,400	3.6	-229.7	-0.68	0.48	1.3	1.4
1,500	2.9	-247.1	-0.82	0.48	1.3	1.4
1,600	1.8	-264.7	0.85	0.49	1.2	1.4
1,700	0.6	-282.4	-1.04	0.50	1.3	1.3
1,800	0.1	-299.4	-0.82	0.48	1.2	1.3
1,900	-0.8	-317.0	-0.96	0.48	1.2	1.4
2,000	-1.2	-334.0	-0.69	0.47	1.3	1.4
2,100	-3.8	-353.0	-0.45	0.53	1.2	1.6
2,200	-7.5	-373.4	-0.29	0.56	1.2	1.8
2,300	-13.0	-395.2	-0.51	0.61	1.1	2.1
2,400	-18.8	-417.6	-0.83	0.62	1.2	2.4
2,500	-22.0	-437.4	-1.66	0.55	1.3	2.6
2,600	-24.8	-456.7	-2.46	0.53	1.4	2.5
2,700	-27.9	-476.5	-3.67	0.55	1.5	2.8
2,800	-31.0	-495.9	-4.75	0.55	1.7	2.8
2,900	-33.5	-514.9	-5.51	0.52	1.8	2.6
3,000	-32.4	-530.5	-6.29	0.43	2.2	2.4
3,100	-29.1	543.9	-7.26	0.37	2.1	2.5
3,200	-28.6	-559.9	-8.29	0.44	2.3	2.2
3,300	-26.7	-574.8	-9.29	0.43	2.6	2.1
3,400	-27.9	-591.8	-10.01	0.46	2.8	1.8
3,500	-25.5	-606.4	-11.12	0.42	3.0	1.7
4,000	-14.0	-677.5	-15.18	0.37	2.3	1.4

HPVA-0180 Typical Parameters

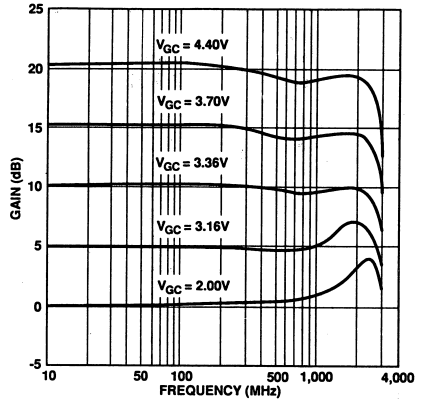


Figure 1. Typical Gain vs. Frequency over Gain Control Range at 25° C

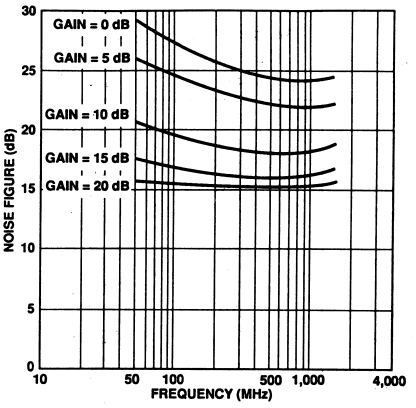


Figure 2. Typical Noise Figure vs. Frequency over Gain Control Range at 25° C

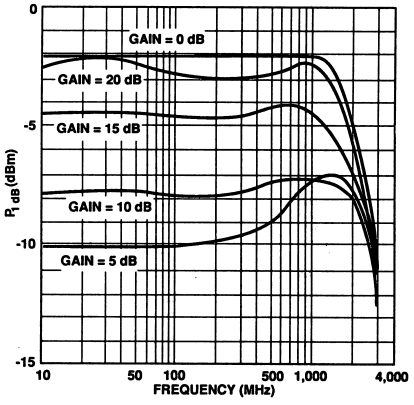


Figure 3. Typical $P_{1\,dB}$ vs. Frequency over Gain Control Range at 25° C

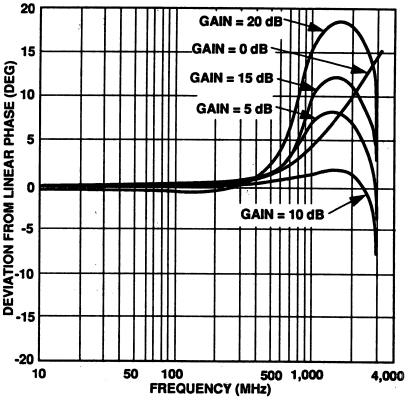


Figure 4. Typical Linear Phase vs. Frequency over Gain Control Range at 25° C

(continued)

HPVA-0180 Typical Parameters

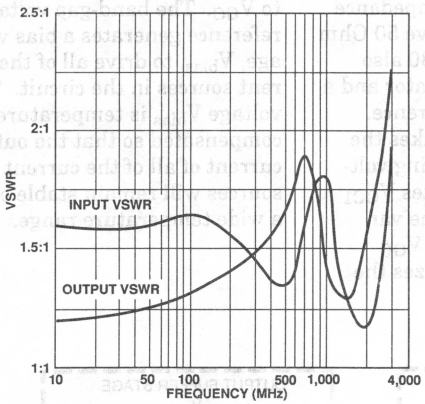


Figure 5. Typical Input and Output VSWR vs. Frequency Gain = 20 dB at 25° C

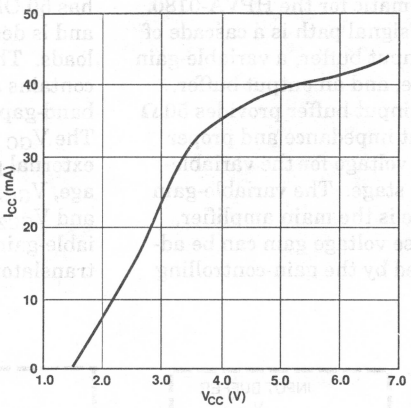


Figure 6. Typical I_{CC} vs. V_{CC} at 25°C

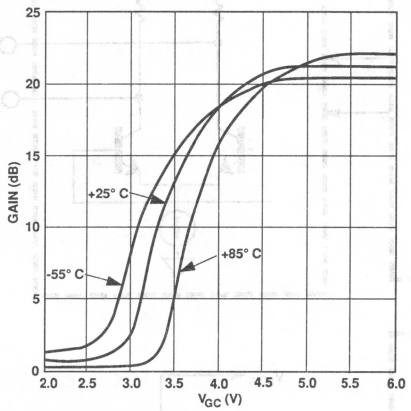


Figure 7. Typical Gain vs. V_{GC} at 300 MHz at Three Temperatures

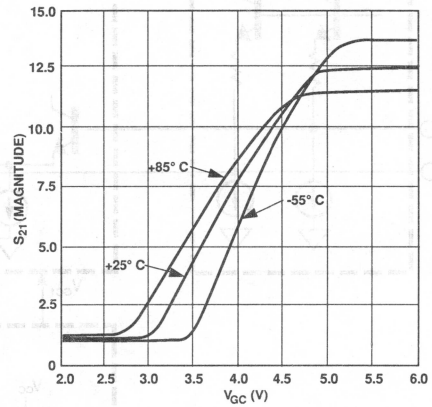


Figure 8. Typical S_{21} vs. V_{GC} at 300 MHz at Three Temperatures

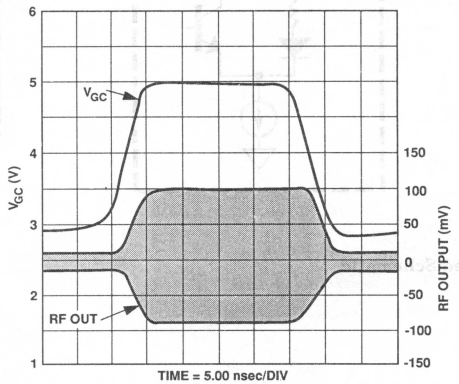


Figure 9. Typical Pulsed V_{GC} Response with RF Frequency of 100 MHz at 25°C

Theory of Operation

Figure 10 shows the simplified schematic for the HPVA-0180. The signal path is a cascade of an input buffer, a variable-gain stage, and an output buffer. The input buffer provides 50 Ω input impedance and proper bias voltage for the variable-gain stage. The variable-gain stage is the main amplifier, whose voltage gain can be adjusted by the gain-controlling voltage, V_{GC}. The output buffer has 50 Ohm output impedance and is designed to drive 50 Ohm loads. The HPVA-0180 also contains a V_{GC} translator and a band-gap voltage reference. The V_{GC} translator takes the external gain-controlling voltage, V_{GC}, and generates V_{GC1} and V_{GC2} to control the variable-gain stage. The V_{GC} translator also linearizes the HPVA-0180's gain with respect to V_{GC}. The band-gap voltage reference generates a bias voltage, V_{bias}, to drive all of the current sources in the circuit. The voltage V_{bias} is temperature compensated so that the output current of all of the current sources will remain stable over a wide temperature range.

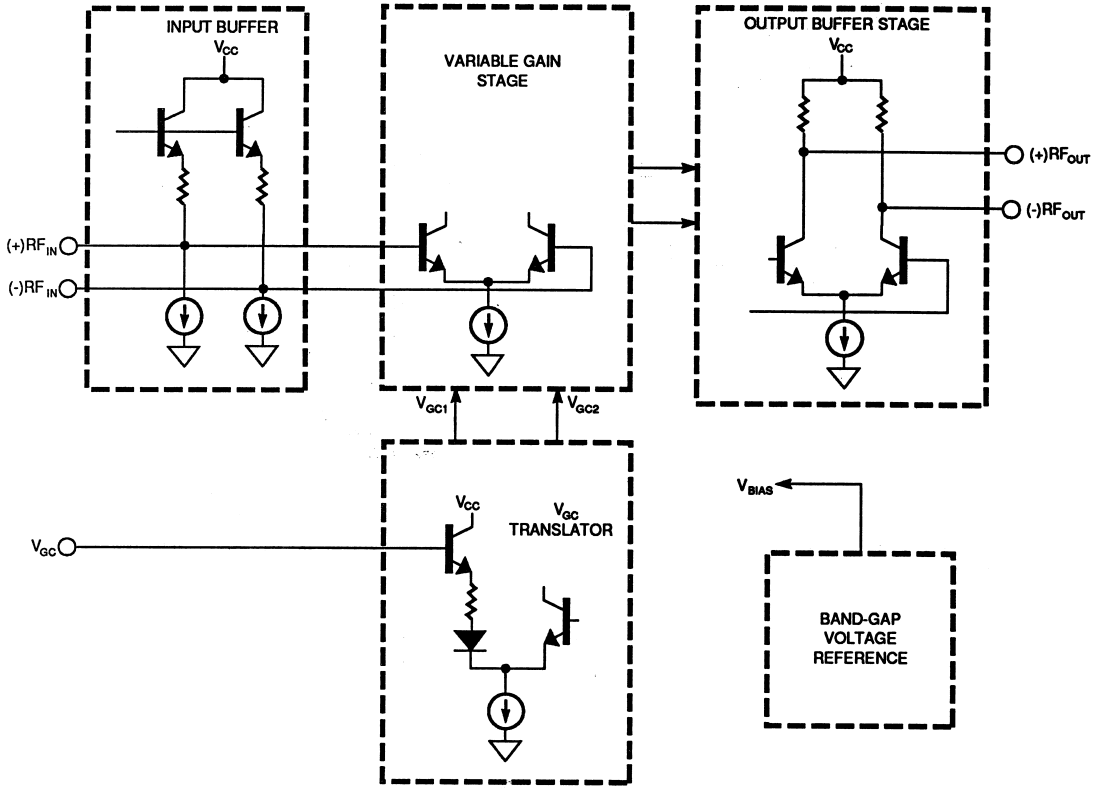
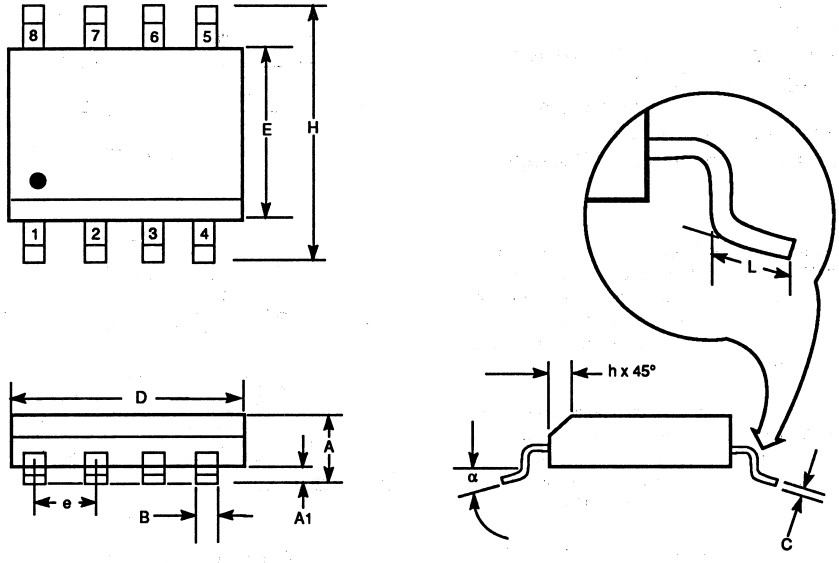


Figure 10. HPVA-0180 Simplified Schematic

Package Dimensions

Plastic SO-8 Package



Symbol	Dimensions	
	Min.	Max.
A	1.35 (0.053)	1.75 (0.068)
A1	0.10 (0.004)	0.25 (0.0098)
B	0.35 (0.0138)	0.49 (0.0192)
C	0.19 (0.007)	0.25 (0.0098)
D	4.80 (0.189)	5.00 (0.197)
E	3.80 (0.150)	4.00 (0.157)
e	1.27 BSC (0.050)	
H	5.80 (0.228)	6.20 (0.244)
h	0.25 (0.010)	0.50 (0.020)
L	0.40 (0.016)	1.27 (0.050)
α	0°	8°

Meets JEDEC outline dimensions.
Dimensions are in millimeters (inches)

HEWLETT PACKARD

IDA-07318
MagIC™ Silicon Bipolar MMIC
1.5 Gb/s Laser Diode Driver

Features

- **High Data Rates: 1.5 Gb/s NRZ**
- **High Modulation Current: 50 mA**
- **High Prebias Current: 50 mA**
- **Low VSWR 50 Ω Input, ECL Level Compatible**
- **Differential or Single-ended Inputs**
- **Separate Modulation and Prebias Controls**
- **Single Power Supply: +5 V or -5.2 V**
- **Hermetic Glass-metal Surface Mount Package**

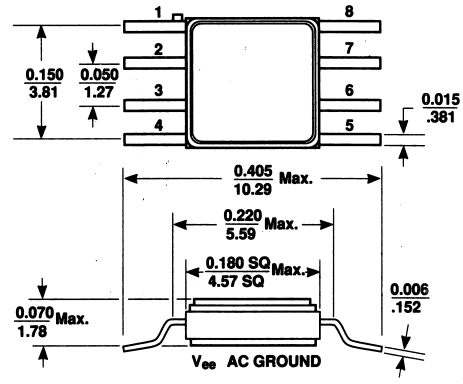
Description

The IDA-07318 is a wideband silicon bipolar Monolithic Microwave Integrated Circuit (MMIC), Laser Diode (LD) driver, housed in a miniature glass-metal hermetic surface mount package. It is designed to provide high speed current drive for laser diodes or light emitting diodes (LEDs). On-chip termination resistors and flexible prebias and modulation control inputs simplify your design.

Typical applications include fiber optic data communications (e.g., FDDI, serial HIPPI) and telecommunications (e.g., SONET) systems where high speed laser diodes are used with data rates up to 1.5 Gb/s. In addition, instrumentation and communication circuits can use the high speed current modulation feature of the IDA-07138.

The IDA series of laser diode drivers is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX} ISOSAT™-1 silicon bipolar process that uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metalization, and polyimide inter-metal dielectric and scratch protection to achieve excellent performance uniformity, and reliability.

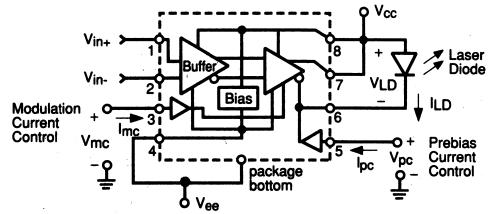
180 mil Package

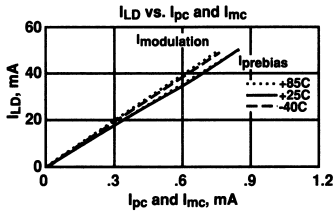


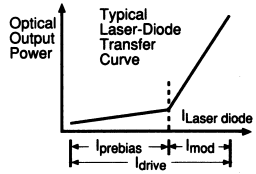
PIN DESCRIPTION	
1 V_{in+}	8 V_{cc}
2 V_{in-}	7 Output Current-
3 Mod, Input	6 Output Current+ (to LD)
4 V_{ee}	5 Prebias Input
Bottom of Package is V_{ee}	

Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
in .xxx = ±.005
mm .xx = ±.13

Functional Block Diagram







Guaranteed Electrical Specifications, T_A = 25°C, V_{cc} = 0 V, V_{ee} = -5.2 V, Z Load = 12 Ω (see Test Configuration)

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
t_r	Output Rise Time, 20% to 80% (Pin 6)	I_{mod} = 25 mA, I_{pb} = 50 mA	ps		220	300
t_f	Output Fall Time, 20% to 80% (Pin 6)	I_{mod} = 25 mA, I_{pb} = 50 mA	ps		240	320
I_{pb}	Laser Diode Prebias Current Set Range		mA	0-50		
I_{mod}	Laser Diode Modulation Current Set Range[1]		mA	5-50		
I_d	Device Current	V_{cc} - V_{cc} = 5 V, I_{mod} = 0 mA, I_{pb} = 0 mA		30	40	50

Notes: 1. Recommended operating range for Modulation Current Set is 10 to 50 mA.

Design Information, T_A = 25°C, V_{cc} = 0 V, V_{ee} = -5.2 V, Z Load = 12 Ω (see Test Configuration)

Symbol	Parameters and Test Conditions		Units	Typ.
τ_p	Propagation Delay Time, Input to Output	I_{mod} = 25 mA	ps	300
BW	Small Signal -3 dB Bandwidth	I_{mod} = 25 mA	GHz	1.0
VSWR	V_{in+}, V_{in-} VSWR	f = 0.1 to 2 GHz		2:1
$t_{r\,pb}$, $t_{r\,mod}$	Modulation or Prebias Current Output Rise Time (Inputs Pin 3 or 5)		ns	6

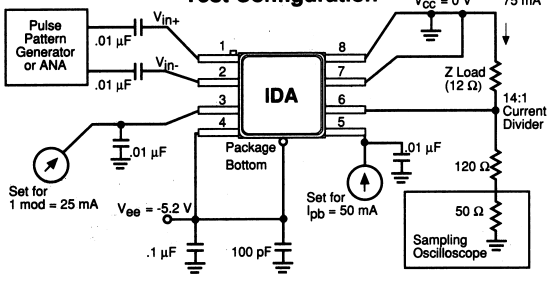
Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	10 V
Power Dissipation[2, 3]	2.5 W
I_{mod} or I_{pb}	150 mA rms
Junction Temperature	200°C
Storage Temperature	-65 to 200°C

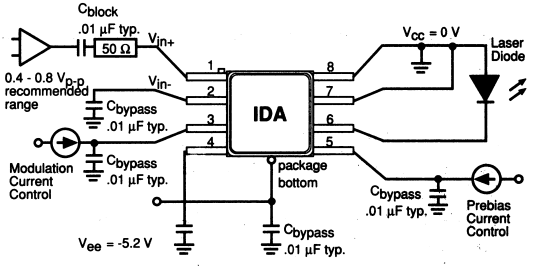
Thermal Resistance[2]: θ_{jc} = 50°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{case} = 25°C
3. Derate at 20 mW/°C for T_C > 75°C

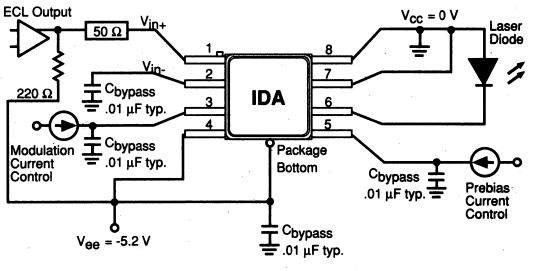
Test Configuration



Typical Use: AC Coupled, Single-ended 50Ω Input

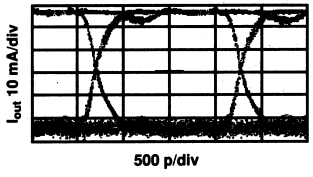


Typical Use: DC Coupled, Single-ended ECL Input

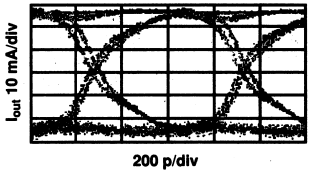


Typical Performance, T_A = 25°C
V_{cc} = 0 V, V_{ee} = 5.2 V, R_L = 12 Ω
(unless otherwise noted)

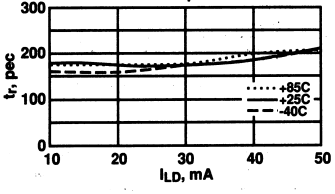
Eye Diagram, 622 Mb/s



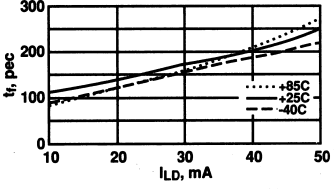
Eye Diagram, 1.5 Gb/s



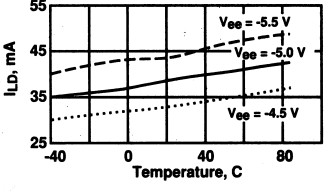
Rise Time vs. I_{LD} and Temperature



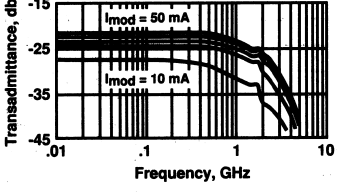
Fall Time vs. I_{LD} and Temperature



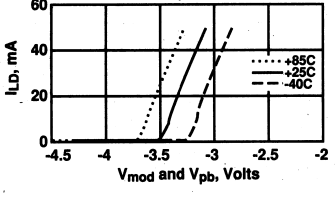
I_{device} vs. Power Supply and Temperature



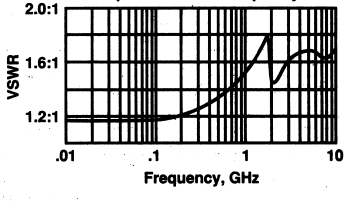
Frequency Response



I_{LD} vs. V_{pc} and V_{mc}



Input VSWR vs. Frequency



HEWLETT PACKARD

IDC-51418
MagIC™ Silicon Bipolar MMIC
1.5 Gb/s Decision Circuit

Features

- **High Data Rates: 1.5 Gb/s NRZ**
- **Input Sensitivity < 20 mVpp Typical**
- **ECL Voltage Swing Compatible C-Input and Q-Outputs**
- **Single Ended or Differential C and D Inputs**
- **Single Power Supply: +5 V or -5.2 V**
- **Low Power: 450 mW Typical Dissipation**
- **Hermetic Glass-metal Surface Mount Package**

Description

The IDC-51418 is a high speed silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) decision circuit, housed in a miniature glass-metal hermetic, surface mount package. It is designed for data communications and LAN applications. Other uses include wide bandwidth communications and digital circuits, such as comparators and D type flip-flops. The IDC-51418 is a master-slave D type flip-flop with a high gain data preamplifier for increased sensitivity. Both the data and clock inputs can be driven differentially or single ended. The bias and input matching circuits are included on-chip.

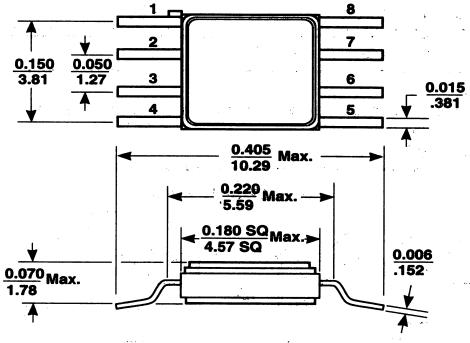
The IDC series of high speed decision circuits is fabricated using HP's 10 GHz, f_T, 25 GHz f_{MAX} ISOSAT™-1 silicon bipolar process that uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization, and polyimide inter-metal dielectric and scratch protection to achieve excellent performance uniformity, and reliability.

Truth Table

Input		Output	
Cn	Dn	Qn +1	$\overline{Qn+1}$
⌐⌐	x	Qn	$\overline{Qn}$
⌐⌐	0	0	1
⌐⌐	1	1	0

Cn: Clock State at t = n
Dn: Data State at t = n
Qn: Output state at t = n
Qn +1: Output state at t = n +1

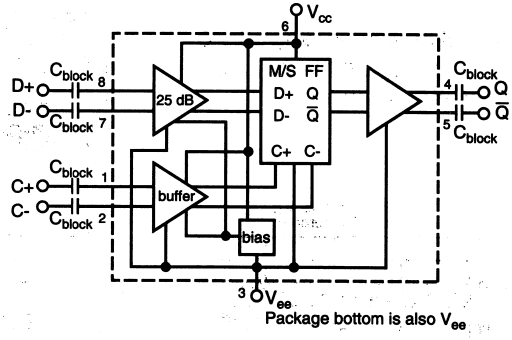
180 mil Package



PIN DESCRIPTION	
1 C+	8 D+
2 C-	7 D-
3 V_{ee}	6 V_{cc}
4 Q	5 $\overline{Q}$
Bottom of Package is V_{ee}	

Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
in .xxx = ±.005
mm .xx = ±.13

Functional Block Diagram



Package bottom is also V_{ee}

Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions: V_{cc} = 5 V, V_{ee} = 0 V, R_L = 50 Ω		Units	Min.	Typ.	Max.
t_r	Q Output Rise Time, 10% to 90%	1.5 Gb/s	ps		200	
t_f	Q Output Fall Time, 90% to 10%	1.5 Gb/s	ps		190	
V_{in} (D+,D-)	Minimum Data Input Amplitude (single ended), BER = 10^{-9}	1.5 Gb/s	mVpp		20	40
CPM	Clock Phase Margin	1.5 Gb/s	deg		335	
F_b max	Maximum Data Rate (NRZ Operation)	V_{in} = 40 mV_{pp}	Gb/s	1.2	1.5	
V_{ck}(C+,C-)	Clock Input Amplitude (single ended)		mVpp		600	
V_o(Q, $\overline{Q}$)	Output Voltage		mVpp	650	800	
t_{pd}	Propagation Delay Time, Falling Clock Edge to Q Output		ps		500	
t_{setup}	Setup Time (see Timing Diagram)		ps		-25	
t_{hold}	Hold TIme (see Timing Diagram)		ps		60	
VSWR	Clock and Data Input VSWR	f = .01-1.5 GHz			1.3:1	
VSWR	Q, $\overline{Q}$ Output VSWR	f = .01-1.5 GHz			2.0:1	
I_d	Quiescent Device Current		mA	75	95	115

The recommended Power Supply Voltage range ($V_{cc} - V_{ee}$) for this device is 4.5 to 5.5 V.

Absolute Maximum Ratings

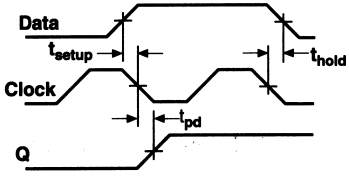
Parameter	Absolute Maximum[1]
Device Voltage	8 V
Power Dissipation[2, 3]	800 mW
C or D Input	2 Vpp
Junction Temperature	200°C
Storage Temperature	-65 to 200°C

Thermal Resistance[2]: θ_{jc} = 55°C/W

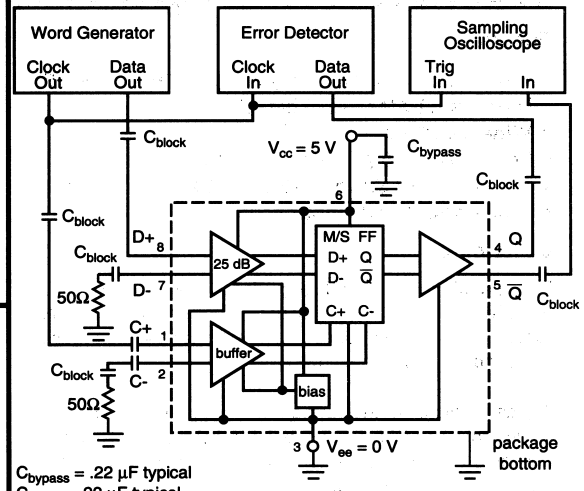
Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. Derate at 18 mW/°C for T_{case} > 156°C

Typical Performance, T_A = 25°C, V_{cc} = 5 V, V_{ee} = 0 V, R_L = 50 Ω
(unless otherwise noted)

Timing Diagram



Test Configuration
Single Ended Input/Single Ended Output

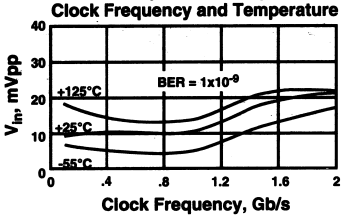


C_{bypass} = .22 µF typical
C_{block} = .22 µF typical

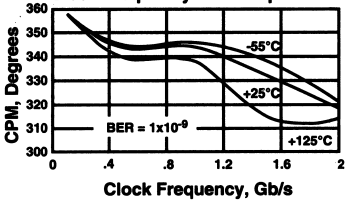
Notes: For transparent (non-latched comparator) operation, AC couple pins 1, 2 (C+, C-) to ground.

Good RF ground of Pin 3 and package bottom is critical for proper operation and good VSWR performance of this part.

Data Input Sensitivity vs. Clock Frequency and Temperature



Input Clock Phase Margin vs. Clock Frequency and Temperature



Quiescent Input/Output Voltages
(Inputs terminated, offset voltages = 0 V)

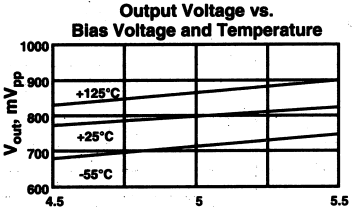
$V_{cc} - V_{ee}$	D	C	Q
5.0 V	5.0 V	3.8 V	3.4 V
-5.2 V	0.0 V	-1.2 V	-1.6 V

Note: Small offset voltages between D+ and D- will cause Q ($\overline{Q}$) to go to a high (Vcc -.2 V) or low (Vcc -1.2 V) state.

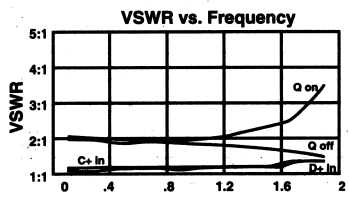
Output Voltages in the Latched (on/off) State

$V_{cc} - V_{ee}$	Q (V_{OH})	$\overline{Q}$ (V_{OL})
5.0 V	4.8 V	3.8 V
-5.2 V	-.2 V	-1.2 V

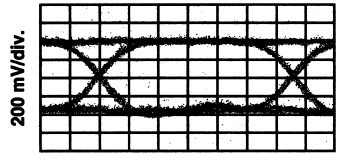
Output Voltage vs. Bias Voltage and Temperature



VSWR vs. Frequency



Output Eye Diagram at 1.5 Gb/s (Pseudorandom pattern = 2^{23} -1)



HEWLETT PACKARD

ITA-06300
MagIC™ Silicon Bipolar MMIC
1.5 Gb/s Transimpedance Amplifier Chip

Features

- **High Transimpedance Gain: A_Z = 2800 Ω (69 dB)**
- **High Data Rates: 1.5 Gb/s NRZ**
- **Wide Bandwidth: 1.5 GHz**
- **Low Noise: 3.5 pA/√Hz at 100 MHz**
- **Single Power Supply: +5 V or -5.2 V**
- **Low Power Consumption: 170 mW**

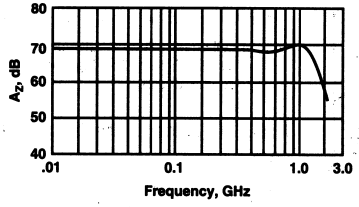
Description

The ITA-06300 series of high-performance transimpedance amplifier chip. It is designed for use in fiber-optic receivers that require high transimpedance gain, wide bandwidth, reduced power consumption, and low noise.

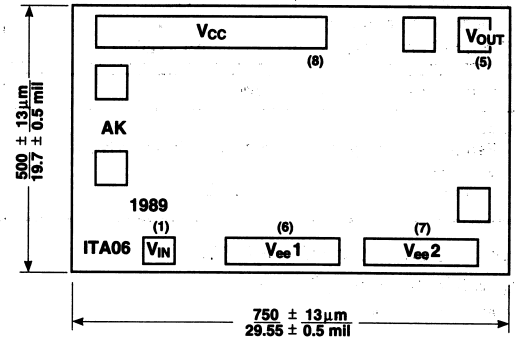
Typical applications include fiber-optic systems such as high-speed data communications, point to point (Fiber Channel), networks (LAN, MAN), and telecommunications (SONET) with data rates up to 1.8 Gb/s.

The ITA series of transimpedance amplifiers is fabricated using HP's 10 GHz f_T, 25 GHz f_{max} ISOSAT™-1 silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metalization and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability. The recommended assembly procedure is gold eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil. gold wire.[1]

Typical Transimpedance Gain vs. Frequency
T_A = 25°C, V_{CC} = 5 V

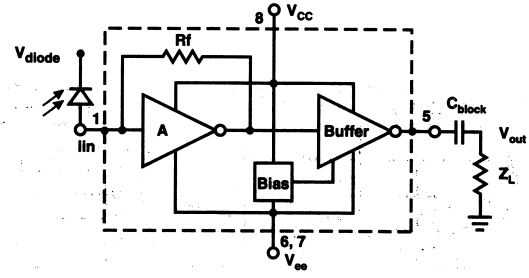


Chip Outline



Chip Thickness is 140 µm / 5.5 mil.
Bond Pads are 50µm / 1.97 mil.

Typical Biasing Configuration[8]



Electrical Specifications[2,3], T_A = 25°C

Symbol	Parameters and Test Conditions[4]: V_{cc} = 5 V, V_{ee} = 0 V, Z_L = 50 Ω		Units	Min.	Typ.	Max.
A_Z	Transimpedance Gain	f = 100 MHz	ohms		2800	
F_{3dB}	Small Signal -3 dB Bandwidth[5, 6]		GHz		1.5	
ΔA_Z	Frequency Response Gain Peak[5, 6]		dB	0.0	1.0	
I_n	Input Current Noise Spectral Density[5]	f = 100 MHz	pA/√Hz		3.5	
V_{op-p}	Output V_o Swing (peak to peak)	f = 50 MHz	V_{p-p}		0.95	
VSWR	Output VSWR	f = 100 MHz			2.2:1	
I_{MAX}	Maximum Input Current Before Input Overload[7]	f = 50 MHz	μA_{p-p}		450	
I_d	Device Quiescent Current		mA		34	
V_{in}	Input Quiescent Voltage		Vdc		1.5	
V_{OUT}	Output Quiescent Voltage		Vdc		2.5	

Notes:
1. See Application Note, "AN-005: Transistor Chip Use" for additional information.
2. The recommended operating voltage range for this device is 4.5 to 5.5 V.
3. Tested in HP 180 mil package.
4. RF performance of chip is determined by packaging and testing 10 devices per wafer.
5. Assumes photodiode capacitance, C_{PD}, <0.3 pF.
6. Referenced from 100 MHz.
7. Output duty cycle distortion ≤ ±10%.
8. See Data Sheet, "ITA-06318, MagIC™ Silicon Bipolar MMIC"

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	8 V
Power Dissipation[2, 3]	700 mW
V_{in}-V_{ee}	2.0 V
Junction Temperature	200°C
Storage Temperature	-65 to 200°C

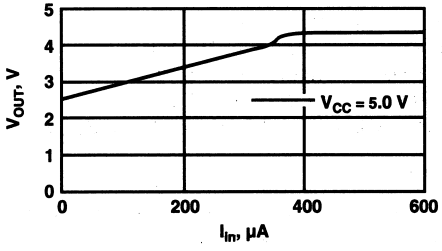
Thermal Resistance: θ_{jc} = 25°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{mounting\ surface}$ (T_{ms}) = 25°C.
3. Derate at 40 mW/°C for T_{ms} > 182°C.

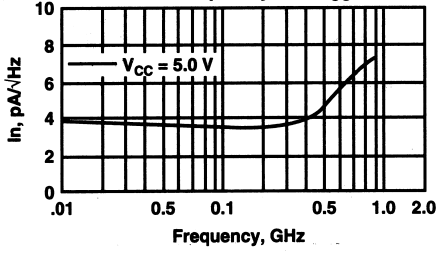
Typical Performance, T_A = 25°C, V_{cc} = 5 V, V_{ee} = 0 V, Z_L = 50 Ω, C_{PD} < 0.3 pF

(Unless otherwise noted)

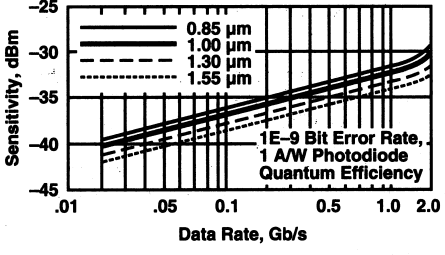
DC Input/Output Characteristics No Load



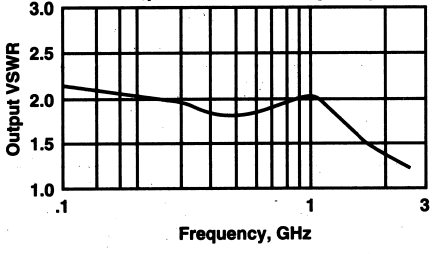
Equivalent Input Current Noise vs. Frequency and V_{CC}



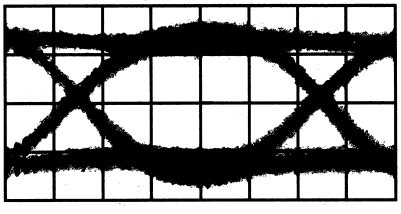
Calculated Sensitivity vs. Frequency and Optical Wavelength



Output VSWR vs. Frequency



Eye Diagram 1.0 Gb/s



HEWLETT PACKARD

ITA-06318
MagIC™ Silicon Bipolar MMIC
1.5 Gb/s Transimpedance Amplifier

Features

- **High Transimpedance Gain: A_Z = 2800 Ω (69 dB)**
- **High Data Rates: 1.5 Gb/s NRZ**
- **Wide Bandwidth: 1.3 GHz**
- **Low Noise: 3.5 pA/√Hz at 100 MHz**
- **Single Power Supply: +5 V or -5.2 V**
- **Low Power Consumption: 170 mW**
- **Hermetic Glass Metal Surface Mount Package**

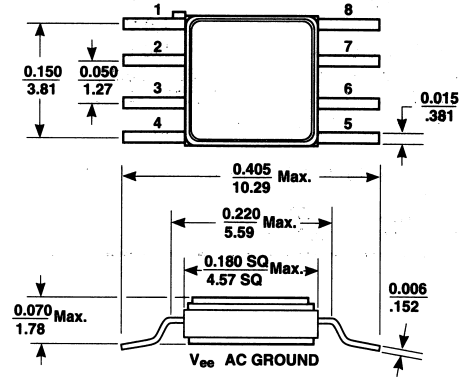
Description

The ITA-06318 is a high-performance transimpedance amplifier housed in a minature glass-metal hermetic surface- mount package. It is designed for use in fiber-optic receivers that require high transimpedance gain, wide bandwidth, reduced power consumption, and low noise.

Typical applications include fiber-optic systems such as high-speed data communications, point to point (Fiber Channel), networks (LAN, MAN), and telecommunications (SONET) with data rates up to 1.8 Gb/s.

The ITA series of transimpedance amplifiers is fabricated using HP's 10 GHz f_T, 25 GHz f_{max} ISOSAT™-1 silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metalization and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

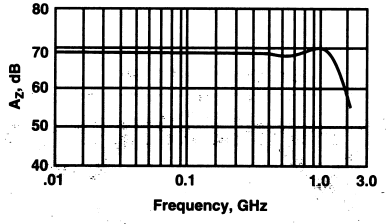
180 mil Package



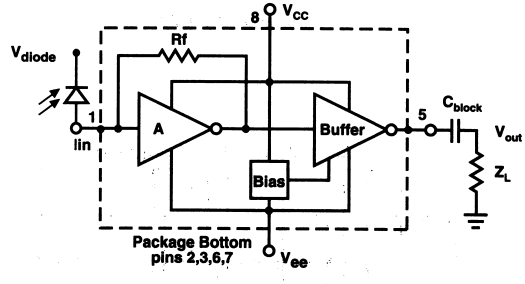
PIN DESCRIPTION	
1 Input	8 V_{cc}
2 V_{ee}, AC Ground	7 V_{ee}
3 V_{ee}, AC Ground	6 V_{ee}
4 NC	5 V_{out}
Bottom of Package is V_{ee} (AC Ground)	

Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
   in .xxx = ±.005
   mm .xx = ±.13

Typical Transimpedance Gain vs. Frequency
T_A = 25°C, V_{CC} = 5 V



Typical Biasing Configuration[8]



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: V_{cc} = 5 V, V_{ee} = 0 V, Z_L = 50 Ω		Units	Min.	Typ.	Max.
A_Z	Transimpedance Gain	f = 100 MHz	ohms	2200	2800	
F_{3dB}	Small Signal -3 dB Bandwidth[2, 4]		GHz	0.9	1.3	
ΔA_Z	Frequency Response Gain Peak[2, 4]		dB	0.0	1.1	2.0
I_n	Input Current Noise Spectral Density[2]	f = 100 MHz	pA/√Hz		3.5	
V_{op-p}	Output Vo Swing (peak to peak)	f = 50 MHz	V_{p-p}		0.95	
VSWR	Output VSWR	f = 100 MHz			1.5:1	
I_{MAX}	Maximum Input Current Before Input Overload[3]	f = 50 MHz	μA_{p-p}		450	
I_d	Device Quiescent Current		mA		34	
V_{in}	Input Quiescent Voltage		Vdc		1.5	
V_{OUT}	Output Quiescent Voltage		Vdc		2.5	

Notes: 1. The recommended operating voltage range for this device is 4.5 to 5.5 V.
2. Assumes photodiode capacitance, C_{PD},<0.3 pF.
3. Output duty cycle distortion ≤ ±10%.
4. Referenced from 100 MHz.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	8 V
Power Dissipation[2, 3]	700 mW
V_{in}-V_{ee}	2.0 V
Junction Temperature	200°C
Storage Temperature	-65 to 200°C

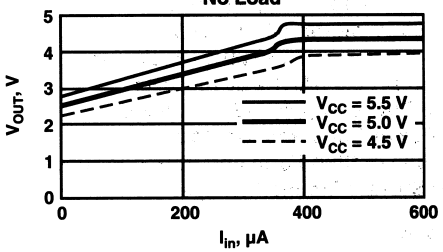
Thermal Resistance: θ_{jc} = 50°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{case} = 25°C.
3. Derate at 20 mW/°C for T_{case} > 165°C.

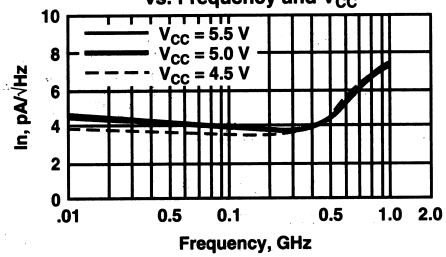
Typical Performance, T_A = 25°C, V_{cc} = 5 V, V_{ee} = 0 V, Z_L = 50 Ω, C_{PD} < 0.3 pF

(Unless otherwise noted)

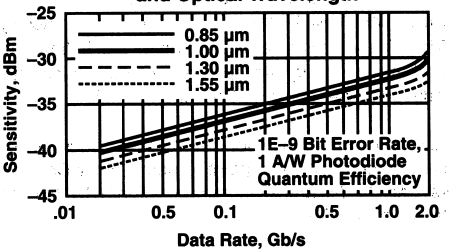
DC Input/Output Characteristics
No Load



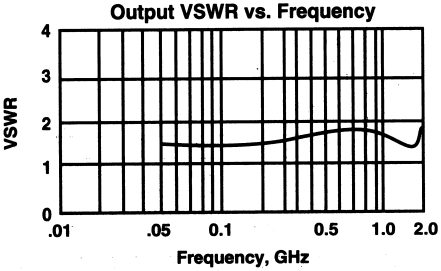
Equivalent Input Current Noise vs. Frequency and V_{CC}



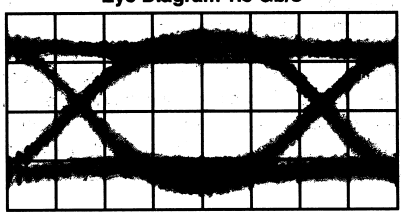
Calculated Sensitivity vs. Frequency and Optical Wavelength



Output VSWR vs. Frequency



Eye Diagram 1.0 Gb/s



ITA-06318 Scattering Parameters: VCC - Vee = 5V

Freq.	S_{11}		S_{21}		S_{12}		S_{22}	
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
0.05	.10	-24	62.0	-6	.002	-104	.38	168
0.10	.07	-21	63.3	-14	.003	-86	.35	166
0.20	.04	39	64.3	-30	.003	-75	.33	165
0.30	.08	90	66.1	-45	.003	-63	.33	161
0.40	.17	92	67.4	-67	.003	-57	.33	155
0.50	.28	84	67.0	-86	.003	-44	.32	147
0.60	.38	74	64.1	-107	.002	-30	.32	139
0.70	.48	61	58.6	-128	.002	-14	.29	129
0.80	.55	50	51.8	-147	.002	0	.28	122
0.90	.60	39	44.7	-165	.002	16	.26	110
1.00	.64	31	38.3	179	.002	27	.25	103
1.25	.69	16	25.6	146	.003	61	.21	86
1.50	.71	6	17.9	118	.004	93	.21	73
1.75	.71	-2	12.9	94	.006	141	.21	66
2.00	.71	-9	9.8	70	.007	164	.20	63
2.50	.69	-25	6.3	28	.015	178	.14	69

HEWLETT PACKARD

ITA-12300, ITA-12318
MagIC™ Silicon Bipolar MMIC
0.8 Gb/s Transimpedance Amplifier

Features

- **High Transimpedance Gain: A_Z = 4200 Ω (72.5 dB)**
- **High Data Rates: 0.8 Gb/s NRZ**
- **Wide Band width: 900 MHz (Chip)**
  750 MHz (Packaged)
- **Low Noise: 2.8 pA/√Hz at 100 MHz**
- **Single Power Supply: +5 V or -5.2 V**
- **Low Power Consumption: 210 mW**
- **Available in Chip Form and Hermetic Glass–Metal Surface Mount Package**

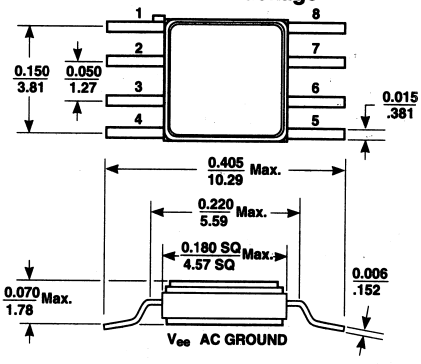
Description

The ITA-123 series of high-performance transimpedance amplifiers is available in either chip form, ITA-12300 or housed in a miniature glass-metal hermetic surface-mount package, ITA-12318. These devices are designed for use in fiber-optic receivers that require high transimpedance gain, wide bandwidth, reduced power consumption, and low noise.

Typical applications include fiber-optic systems such as high-speed data communications, point to point (Fiber Channel), networks (LAN, MAN), and telecommunications (SONET) with data rates up to 0.8 Gb/s.

The ITA series of transimpedance amplifiers is fabricated using HP's 10 GHz f_T, 25 GHz f_{max} ISOSAT™-1 silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metalization and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability. The recommended assembly procedure for the ITA-12300 chip is gold eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil. gold wire.[1]

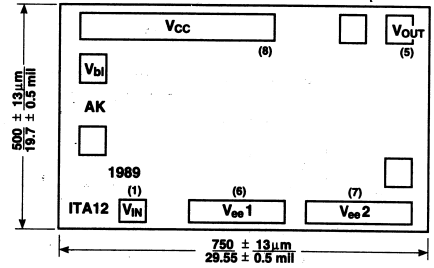
180 mil Package



PIN DESCRIPTION			
1	Input	8	V_{CC}
2	V_{ee}, AC Ground	7	V_{ee}
3	V_{ee}, AC Ground	6	V_{ee}
4	NC	5	V_{out}
Bottom of Package is V_{ee} (AC Ground)			

Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
in .xxx = ±.005
mm .xx = ±.13

ITA-12300 Chip Outline



Chip Thickness is 140 µm / 5.5 mil. (nominal)
Bond Pads are 50 µm / 1.97 mil. (nominal)

Electrical Specifications[2], T_A = 25°C

Symbol	Parameters and Test Conditions: V_{cc} = 5V, V_{ee} = 0V, Z_L = 50 Ω		Units	ITA-12318 180 mil.			ITA-12300[3] 00 (Chip)		
				Min.	Typ.	Max.	Min.	Typ.	Max.
A_Z	Transimpedance Gain	f = 100 MHz	ohms	3800	4200			4200	
F_{3dB}	Small Signal -3 dB Bandwidth[4, 5]		MHz	600	750			900	
ΔA_Z	Frequency Response Gain Peak[4, 5]		dB		0.2	0.7		0.2	
I_n	Input Current Noise Spectral Density[4]	f = 100 MHz	pA/√Hz		2.8			2.8	
V_{op-p}	Output Voltage Swing (peak to peak)	f = 50 MHz	V_{p-p}		1.2			1.2	
VSWR	Output VSWR	f = 50 to 1000 MHz			2:1			2:1	
I_{MAX}	Maximum Input Current Before Input Overload[6]	f = 50 MHz	μA_{p-p}		400			400	
I_d	Device Quiescent Current		mA	30	43	55	30	43	55
V_{in}	Input Quiescent Voltage (Pin 1)		Vdc		2.2			2.2	
V_{OUT}	Output Quiescent Voltage (Pin 5)		Vdc		2.2			2.2	

Notes:
1. See Application Note, "AN-A005: Transistor Chip Use" for additional information.
2. The recommended operating voltage range for this device is 4.75 to 5.5 V.
3. RF performance of chip is determined by testing 10 devices per wafer in a 180 mil package.
4. Assumes photodiode capacitance, C_{PD},<0.5 pF.
5. Referenced from 100 MHz.
6. Input overload is defined as output duty cycle distortion ≥ ±10%.

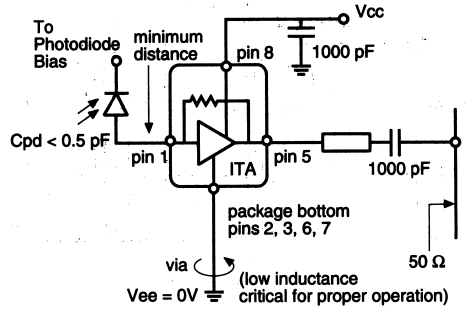
Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	8 V
Power Dissipation[2, 3]	700 mW
V_{in}-V_{ee}	3.0 V
Junction Temperature	200°C
Storage Temperature	-65 to 200°C

Thermal Resistance: θ_{jc} = 50°C/W (ITA-12318)
θ_{jc} = 25°C/W (ITA-12300)

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{case} = 25°C (ITA-12318), $T_{mounting\ surface}$ = 25°C (ITA-12300)
3. Derate at 20 mW/°C for T_{case} > 165°C (ITA-12318)
   Derate at 40 mW/°C for $T_{mounting\ surface}$ > 182°C (ITA-12300)

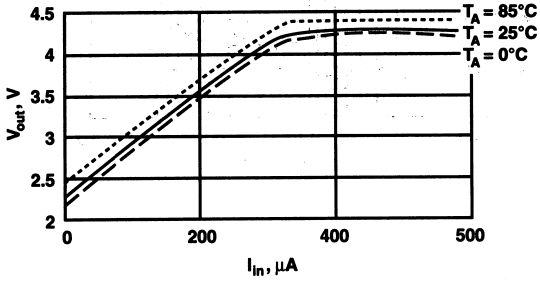
ITA-12318 Typical Biasing Configuration and Functional Block Diagram



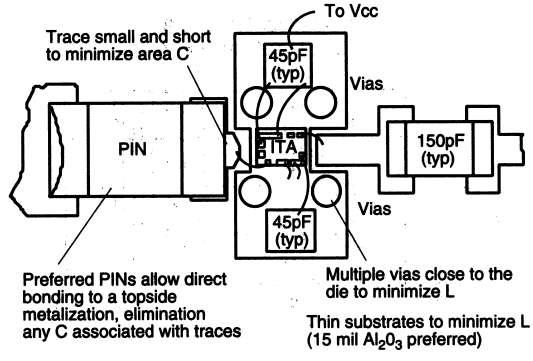
Typical Performance, T_A = 25°C, V_{CC} = 5V, V_{ee} = 0V, Z_L = 50 Ω, C_{PD} < 0.5 pF

(Unless otherwise noted)

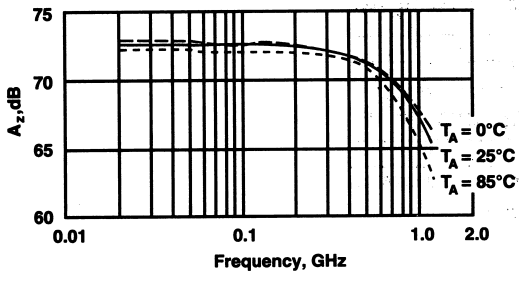
ITA-12300/ITA-12318 DC Input/Output Characteristics No Load



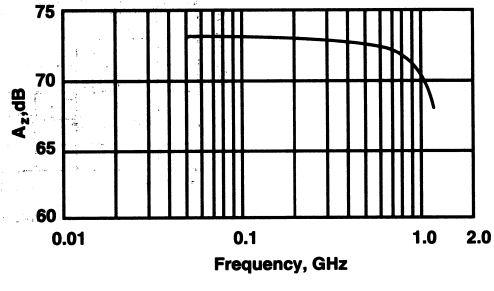
ITA-12300 Circuit Layout



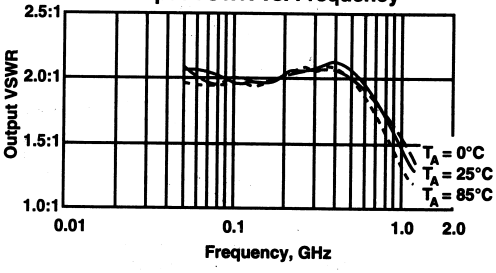
ITA-12318 Typical Transimpedance Gain vs. Frequency



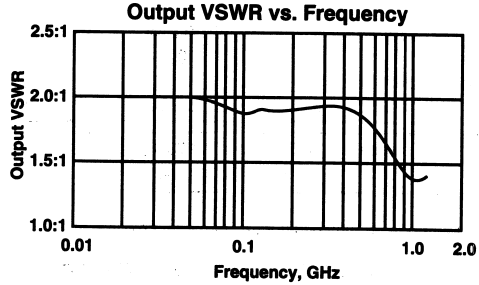
ITA-12300 Typical Transimpedance Gain vs. Frequency



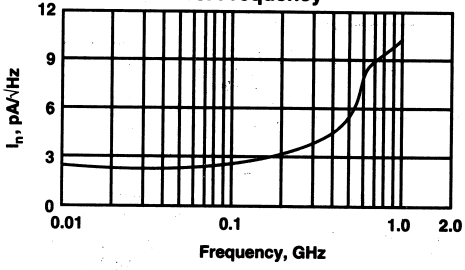
ITA-12318
Output VSWR vs. Frequency



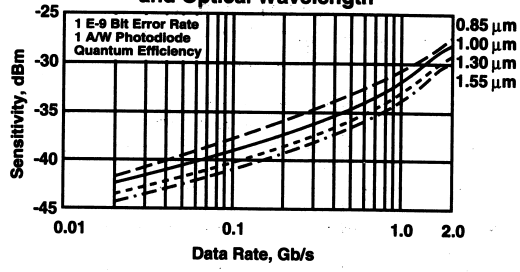
ITA-12300
Output VSWR vs. Frequency



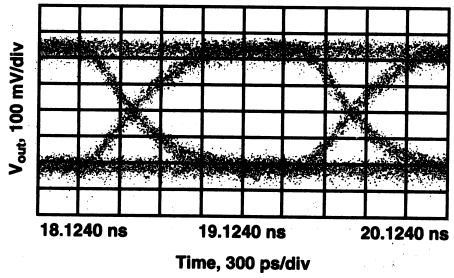
ITA-12300/ITA-12318
Equivalent Input Current Noise vs. Frequency



ITA-12300/ITA-12318
Calculated Sensitivity vs. Data Rate and Optical Wavelength



ITA-12318
Eye Diagram, 622 Mb/s
Photo current = 100 µA P-P, PRBS = 2^{31} - 1



Typical ITA-12318 Scattering Parameters: $Z_O = 50\ \Omega$

$T_A = 25°C$, Vcc = 5 V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
MHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
50	.57	-1.0	31.70	38.57	-10.0	-49.50	.003	-131.0	.36	164.0	2.23
100	.57	1.0	31.50	37.60	-22.0	-49.60	.003	18.0	.33	160.0	2.65
150	.59	2.0	31.20	36.14	-32.0	-55.00	.002	-59.0	.33	157.0	4.68
200	.60	2.0	30.70	34.32	-41.0	-64.00	.001	148.0	.34	151.0	12.92
250	.62	1.0	30.40	32.91	-50.0	-55.50	.002	-32.0	.34	144.0	5.15
300	.63	0.0	30.00	31.58	-59.0	-56.80	.002	-83.0	.35	137.0	5.37
350	.63	-2.0	29.60	30.29	-66.0	-55.80	.002	-26.0	.35	129.0	5.55
400	.64	-3.0	29.30	29.21	-74.0	-57.10	.001	74.0	.35	122.0	6.47
450	.65	-4.0	29.00	28.25	-81.0	-54.80	.002	-135.0	.35	115.0	4.84
500	.65	-5.0	28.80	27.52	-89.0	-66.60	0.000	145.0	.35	106.0	9.06
550	.65	-7.0	28.60	26.85	-96.0	-57.50	.001	20.0	.35	98.0	7.30
600	.65	-8.0	28.40	26.26	-104.0	-52.40	.002	114.0	.33	90.0	4.03
650	.65	-9.0	28.20	25.52	-112.0	-61.30	.001	-56.0	.33	83.0	11.82
700	.65	-10.0	27.90	24.91	-120.0	-53.40	.002	-169.0	.31	72.0	4.73
750	.65	-11.0	27.70	24.17	-128.0	-62.70	.001	-117.0	.29	63.0	15.10
800	.65	-12.0	27.50	23.57	-136.0	-54.90	.002	155.0	.27	52.0	6.21
850	.65	-13.0	27.20	22.78	-144.0	-47.40	.004	177.0	.25	40.0	2.69
900	.65	-14.0	26.90	22.05	-153.0	-64.50	.001	-168.0	.23	28.0	20.61
950	.65	-15.0	26.40	20.86	-161.0	-49.60	.003	131.0	.21	15.0	3.96
1000	.65	-15.0	26.10	20.15	-169.0	-61.40	.001	-167.0	.18	4.0	16.16
1050	.65	-16.0	25.60	19.07	-177.0	-55.40	.002	-176.0	.17	-12.0	8.57
1100	.65	-16.0	25.10	18.04	175.0	-50.10	.003	144.0	.15	-24.0	4.96
1150	.65	-17.0	24.60	17.06	168.0	-44.80	.006	157.0	.14	-41.0	2.82
1200	.65	-18.0	24.10	16.05	160.0	-47.20	.004	163.0	.12	-58.0	4.01

Typical ITA-12300 Scattering Parameters: $Z_O = 50\ \Omega$

$T_A = 25°C$, Vcc = 5 V

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
MHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
50	.52	-2.0	32.40	41.51	-9.0	-48.00	.004	1.0	.35	171.0	2.20
100	.53	2.0	32.20	40.62	-19.0	-69.80	0.000	-159.0	.34	169.0	7.67
150	.54	4.0	31.90	39.43	-28.0	-52.20	.002	-97.0	.35	166.0	3.19
200	.55	4.0	31.60	38.21	-37.0	-57.60	.001	86.0	.35	162.0	6.18
250	.56	4.0	31.30	36.65	-45.0	-62.20	.001	29.0	.35	157.0	10.77
300	.58	4.0	31.00	35.31	-52.0	-54.60	.002	48.0	.35	151.0	4.65
350	.58	4.0	31.00	34.26	-60.0	-53.20	.002	43.0	.35	145.0	4.10
400	.59	3.0	30.40	33.17	-67.0	-67.00	0.000	95.0	.34	138.0	8.79
450	.60	2.0	30.20	32.16	-74.0	-60.90	.001	-96.0	.33	132.0	9.69
500	.61	2.0	29.90	31.31	-81.0	-53.70	.002	164.0	.32	125.0	4.28
550	.61	2.0	29.70	30.57	-88.0	-58.70	.001	-175.0	.31	117.0	7.82
600	.62	1.0	29.50	29.77	-95.0	-58.90	.001	-7.0	.29	110.0	8.54
650	.62	0.0	29.20	28.93	-103.0	-48.10	.004	-139.0	.27	101.0	2.37
700	.63	0.0	29.00	28.20	-110.0	-49.70	.003	159.0	.25	92.0	3.02
750	.63	-1.0	28.70	27.36	-117.0	-55.00	.002	41.0	.23	82.0	5.99
800	.63	-1.0	28.40	26.30	-125.0	-46.40	.005	136.0	.20	72.0	2.27
850	.64	-2.0	28.10	25.26	-133.0	-47.30	.004	164.0	.18	59.0	2.60
900	.64	-3.0	27.70	24.21	-140.0	-52.20	.002	179.0	.15	47.0	4.76
950	.64	-3.0	27.30	23.20	-147.0	-45.60	.005	161.0	.13	31.0	2.37
1000	.64	-4.0	26.80	21.81	-155.0	-45.50	.005	-178.0	.11	12.0	2.48
1050	.65	-4.0	26.40	20.85	-161.0	-43.20	.007	125.0	.10	-6.0	2.01
1100	.65	-5.0	25.90	19.64	-169.0	-45.20	.006	157.0	.10	-32.0	2.64
1150	.65	-5.0	25.30	18.45	-175.0	-45.60	.005	166.0	.10	-52.0	2.96
1200	.65	-6.0	24.80	17.30	178.0	-44.50	.006	153.0	.11	-65.0	2.75

HEWLETT PACKARD

IVA-05118
Silicon Bipolar MMIC
1.5 GHz Variable Gain Amplifier

Features

- **50 MHz to 1.5 GHz Bandwidth**
- **Data Rates up to 2.0 Gbit/s**
- **High Gain: 26 dB typical**
- **Wide Gain Control Range: 30 dB typical**
- **Differential Output Capability**
- **Bias V_{cc}-V_{ee} = 5 V**
- **5 V TTL Compatible V_{gc} Control Voltage, I_{gc} < 3 mA**
- **Hermetic Glass-Metal Surface Mount Package**

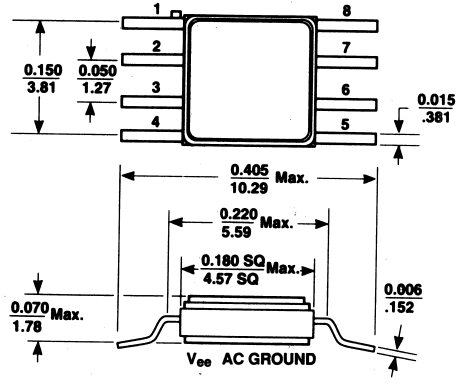
Description

The IVA-05118 is a variable gain amplifier housed in a miniature glass-metal hermetic surface mount package. It is designed for narrow or wide bandwidth commercial, industrial and military applications that require high gain and wide gain control range. The amplifier can be used in a single-ended or differential output configuration. For low frequency applications (<50 MHz) a bypass capacitor and series resistor are connected to pin 4, the AC Input Ground lead.

Typical applications include variable gain amplification for fiber-optic systems at data rates in excess of the 1.24 Gb/s SONET standard, mobile radio and satellite receivers, millimeter wave receiver IF amplifiers and communications receivers.

The IVA series of variable gain amplifiers is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX} ISOSAT™-I silicon bipolar process. This process uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

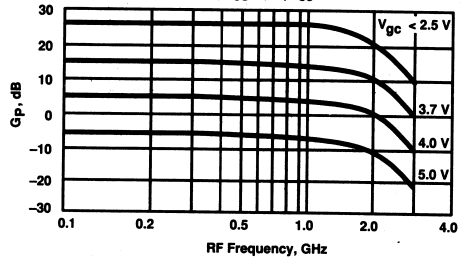
180 mil Package



PIN DESCRIPTION			
1	INPUT +	8	V_{gc}
2	V_{EE}	7	OUT –
3	V_{EE}	6	OUT +
4	INPUT –	5	V_{CC}
BOTTOM OF PACKAGE IS V_{EE} (AC GROUND)			

Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
   in .xxx = ±.005
   mm .xx = ±.13

TYPICAL VARIABLE GAIN vs. FREQUENCY
T_A = 25°C, V_{CC} = 5 V, V_{ee} = 0 V



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions[2]: V_{CC} = 5 V, V_{ee} = 0 V, V_{gc} = 0 V, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain $\|S_{21}\|^2$	f = 0.5 GHz	dB	20	26	
ΔG_P	Gain Flatness	f = 0.05 to 1.0 GHz	dB		±0.3	
$f_{3\,dB}$	3 dB Bandwidth[3]		GHz	1.0	1.5	
GCR	Gain Control Range[4]	f = 0.5 GHz, V_{gc} = 0 to 5 V	dB	25	30	
ISO	Reverse Isolation ($\|S_{12}\|^2$)	f = 0.5 GHz, V_{gc} = 0 to 5 V	dB		45	
VSWR	Input VSWR	f = 0.05 to 1.5 GHz, V_{gc} = 0 to 5 V			1.7:1	
	Output VSWR	f = 0.05 to 1.5 GHz, V_{gc} = 0 to 5 V			1.5:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		9	
$P_{1\,dB}$	Output Power @ 1 dB Compression	f = 0.5 GHz	dBm		–2	
IP_3	Output Third Order Intercept Point	f = 0.5 GHz	dBm		8	
t_D	Group Delay	f = 0.5 GHz	psec		400	
I_{CC}	Supply Current		mA	25	35	45

Notes:
1. The recommended operating voltage range for this device is 4 to 6 V. Typical performance as a function of voltage is on the following page.
2. As measured using Input Pin 1 and Output Pin 6; with Output Pin 7 terminated into 50 ohms.
3. Referenced from 50 MHz Gain.
4. The recommended gain control range for these devices for dynamic control is 0 to 4.2 V. Operation at gain control settings above 4.2 V may result in gain increase rather than gain decrease.

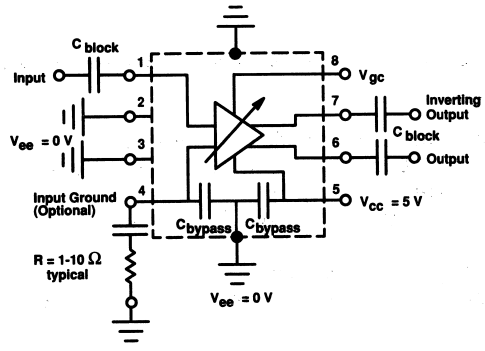
Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	8 V
Power Dissipation[2,3]	600 mW
Input Power	+14 dBm
Vgc–Vee	7 V
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C

Thermal Resistance[2,4]: θ_{jc} = 50°C/W

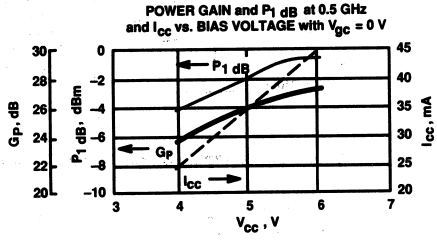
Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 20 mW/°C for T_C >170°C.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

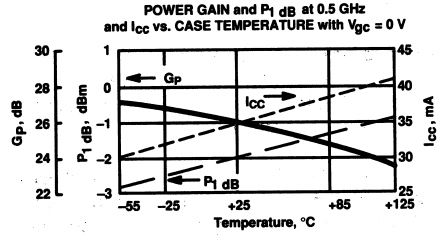
Typical Biasing Configuration and Functional Block Diagram

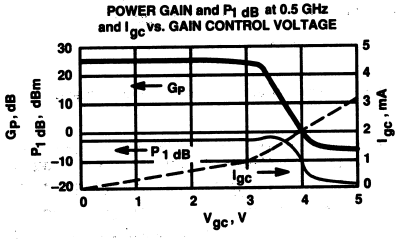


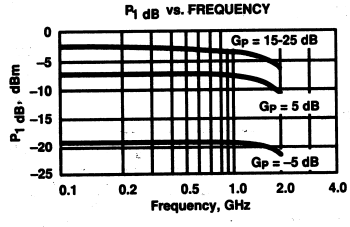
Typical Performance, T_A = 25°C, V_{cc} = 5 V, V_{ee} = 0 V

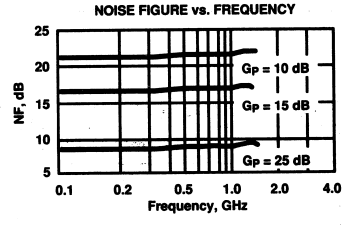
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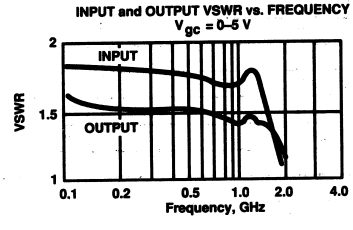


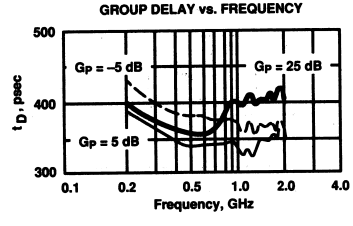












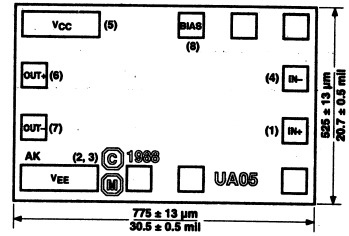
HEWLETT PACKARD

IVA-05200
MagIC™ Silicon Bipolar MMIC
1.5 GHz Variable Gain Amplifier Chip

Features

- **Differential Input and Output Capability**
- **DC to 1.5 GHz Bandwidth; 2.0 Gb/s Data Rates**
- **High Gain: 30 dB typical**
- **Wide Gain Control Range: 30 dB typical**
- **5 V Bias**
- **5 V V_{gc} Control Voltage, I_{gc} < 3 mA**
- **Fast Gain Control Response: <10 nsec typical**

IVA-05200 Chip Outline



Description

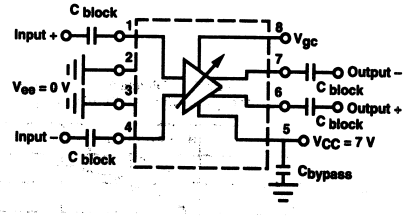
The IVA-05200 is a variable gain amplifier chip. This device can be used in any combination of single-ended or differential inputs or outputs (see Functional Block Diagram). The lowest frequency of operation is limited only by values of user selected blocking capacitors.

Typical applications include variable gain amplifiers for fiber-optic systems (e.g. SONET) with data rates up to 2.0 Gb/s, mobile radio and satellite receivers, millimeter wave receiver IF amplifiers and communications receivers.

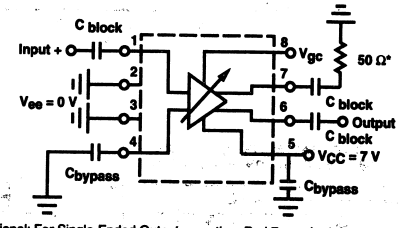
The IVA series of variable gain amplifiers is fabricated using HP's 10 GHz f_T, 25 GHz f_{max} ISOSAT™-1 silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metalization and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability. The recommended assembly procedure is gold eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil. gold wire.[1]

Typical Biasing Configuration and Functional Block Diagram:

Differential Input / Differential Output



Single Ended Input / Single Ended Output



*Optional: For Single-Ended Output operation, Pad 7 may be left unterminated (no C_{block} or 50 Ω).

Electrical Specifications[2,3], T_A = 25°C

Symbol	Parameters and Test Conditions[4,5]: V_{cc} = 5 V, V_{ee} = 0 V, V_{gc} = 0 V, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain $\|S_{21}\|^2$	f = 0.5 GHz	dB	25	30	
ΔG_P	Gain Flatness	f = 0.05 to 1.0 GHz	dB		±0.5	
f_{3dB}	3 dB Bandwidth[6]		GHz	1.0	1.5	
GCR	Gain Control Range[7]	f = 0.5 GHz, Vgc = 0 to 5 V	dB	25	30	
ISO	Reverse Isolation ($\|S_{12}\|^2$)	f = 0.5 GHz, Vgc = 0 to 5 V	dB		45	
VSWR	Input VSWR	f = 0.05 to 1.5 GHz, Vgc = 0 to 5 V			1.7:1	
	Output VSWR	f = 0.05 to 1.5 GHz, Vgc = 0 to 5 V			1.5:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		9	
$P_{1\,dB}$	Output Power @ 1 dB Compression	f = 0.5 GHz	dBm		-3	
V_{OUT}	Peak-to-Peak Single-Ended Output Voltage	f = 0.5 GHz	mVpp		450	
IP_3	Output Third Order Intercept Point	f = 0.5 GHz	dBm		7	
t_D	Group Delay	f = 0.5 GHz	psec		400	
I_{cc}	Supply Current		mA	25	35	45

Notes:
1. See Application Note, "AN-A005 Transistor Chip Use" for additional information.
2. The recommended operating voltage range for this device is 4 to 6 V. Typical performance as a function of voltage is on the following page.
3. Tested in 180 mil package.
4. As measured using Input Pin 1 and Output Pin 6; with Output Pin 7 terminated into 50 Ω and Input Pin 4 at AC ground.
5. RF performance of chip is determined by packaging and testing 10 devices per wafer.
6. Referenced from 50 MHz gain.
7. The recommended gain control range for these devices for dynamic control is 0 to 4.2 V. Operation at gain control settings above 4.2 V may result in gain increase rather than gain decrease.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage (V_{cc}-V_{ee})	8 V
Power Dissipation[2, 3]	600 mW
Input Power	+14 dBm
V_{gc}-V_{ee}	7 V
Junction Temperature	200°C
Storage Temperature	-65 to 200°C

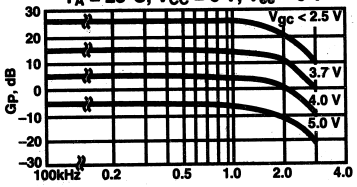
Thermal Resistance[2]: θ_{jc} = 25°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{mounting\ surface}$ (T_{ms}) = 25°C
3. Derate at 40 mW/°C for T_{ms} > 182°C.

Typical Performance, T_A = 25°C, V_{cc} = 5 V, V_{ee} = 0 V

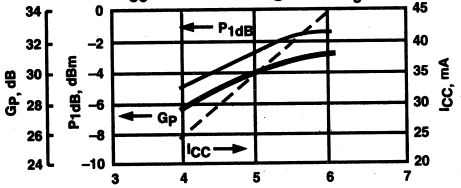
(Unless otherwise noted)

Typical Variable Gain vs. Frequency
T_A = 25°C, V_{CC} = 5 V, V_{ee} = 0 V



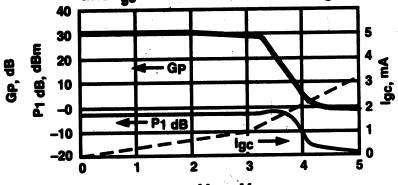
RF Frequency, GHz

Power Gain and P_{1dB} at 0.5 GHz and I_{CC} vs. Bias Voltage with V_{gc} = 0 V



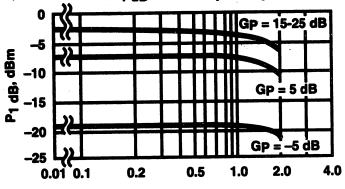
V_{CC}, V

Power Gain and P_{1dB} at 0.5 GHz and I_{gc} vs. Gain Control Voltage



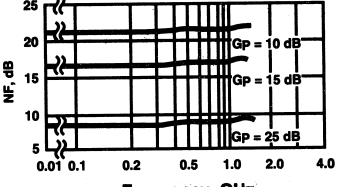
V_{gc}, V

$P_{1\ dB}$ vs. Frequency



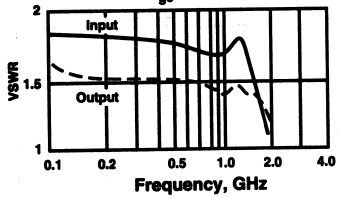
Frequency, GHz

Noise Figure vs. Frequency



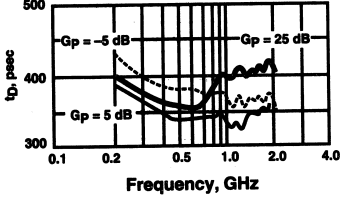
Frequency, GHz

Input and Output VSWR vs. Frequency
V_{gc} = 0-5 V



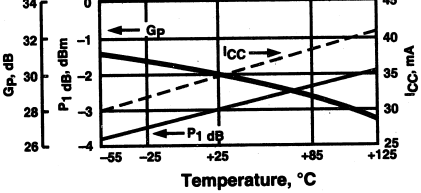
Frequency, GHz

Group Delay vs. Frequency



Frequency, GHz

Power Gain and $P_{1\ dB}$ at 0.5 GHz and I_{cc} vs. Case Temperature with V_{gc} = 0 V



Temperature, °C

HEWLETT PACKARD

IVA-05208
MagIC™ Silicon Bipolar MMIC
1.5 GHz Variable Gain Amplifier

Features

- **Differential Input and Output Capability**
- **DC - 1.5 GHz Bandwidth; 2.0 Gb/s Data Rates**
- **High Gain: 30 dB typical**
- **Wide Gain Control Range: 30 dB Typical**
- **5 V Bias**
- **5 V V_{gc} Control Voltage, I_{gc} < 3 mA**
- **Fast Gain Control Response: < 10 nsec Typical**
- **Low Cost Plastic Surface Mount Package**

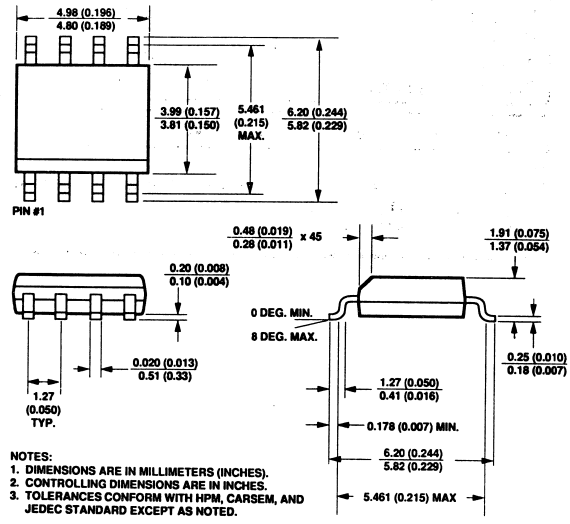
Description

The IVA-05208 is a variable gain amplifier housed in a miniature low cost plastic surface mount package. This device can be used in any combination of single-ended or differential inputs or outputs (see Functional Block Diagram). The lowest frequency of operation is limited only by the values of user selected blocking and bypass capacitors.

Typical applications include variable gain amplification for fiber optic systems (e.g., SONET) with data rates up to 2.0 Gb/s, mobile radio and satellite receivers, millimeter wave receiver IF amplifiers and communication receivers.

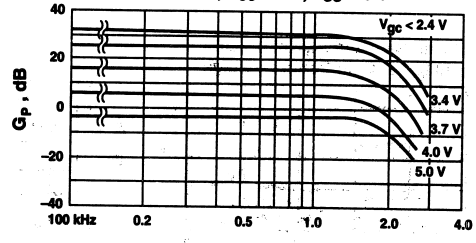
The IVA series of variable gain amplifiers is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX} |SOSAT™| silicon bipolar process. This process uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

SO-8 Package



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSIONS ARE IN INCHES.
3. TOLERANCES CONFORM WITH HPM, CARSEM, AND JEDEC STANDARD EXCEPT AS NOTED.

Typical Variable Gain vs. Frequency
T_a = 25°C, V_{CC} = 5 V, V_{ee} = 0 V



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: [2] V_{CC}=5 V, V_{ee} = 0 V, V_{gc}=0 V, Z_O=50 Ω		Units	Min.	Typ.	Max.
G_p	Power Gain ($\|S_{21}\|^2$)	f = 0.5 GHz	dB	25	30	
ΔG_p	Gain Flatness	f = 0.05 to 1.0 GHz	dB		±0.8	
$f_{3\,dB}$	3 dB Bandwidth[3]		GHz	1.2	1.8	
GCR	Gain Control Range[4]	f = 0.5 GHz, V_{gc} = 0 to 5 V	dB	25	30	
ISO	Reverse Isolation ($\|S_{12}\|^2$)	f = 0.5 GHz, V_{gc} = 0 to 5 V	dB		45	
VSWR	Input VSWR	f = 0.05 to 1.5 GHz, V_{gc} = 0 to 5 V			2.0:1	
	Output VSWR	f = 0.05 to 1.5 GHz, V_{gc} = 0 to 5 V			2.5:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		9	
$P_{1\,dB}$	Output Power at 1 dB Compression	f = 0.5 GHz	dBm		-3	
V_{out}	Peak-to-Peak Single-Ended Output Voltage	f = 0.5 GHz	mVpp		450	
IP_3	Output Third Order Intercept Point	f = 0.5 GHz	dBm		7	
t_D	Group Delay		psec.		400	
I_{CC}	Supply Current		mA	25	35	50

Notes:
1. The recommended operating voltage range for this device is 4 to 6 V. Typical performance as a function of voltage is on the following page.
2. As measured using Input Pin 1 and Output Pin 6, with Output Pin 7 terminated into 50 Ω and input Pin 4 at AC ground.
3. Referenced from 50 MHz Gain.
4. The recommended gain control range for these devices for dynamic control is 0 to 4.2 V. Operation at gain control settings above 4.2 V may result in gain increase rather than gain decrease.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage (V_{cc}-V_{ee})	8 V
Power Dissipation[2,3]	600 mW
Input Power	+14 dBm
$V_{gc} - V_{ee}$	7 V
Junction Temperature	150°C
Storage Temperature	-65 to 150°C

Thermal Resistance: $\theta_{jc} = 150°C/W$[2]

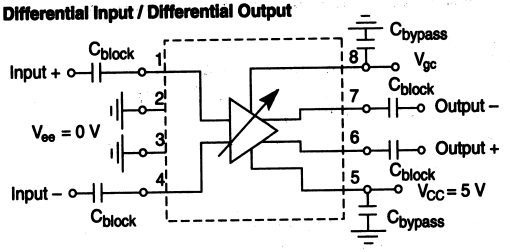
Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE} = 25°C$.
3. Derate at 6.67 mW/°C for $T_C > 60°C$.

Part Number Ordering Information

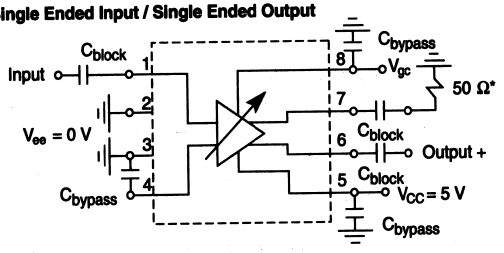
Part Number	Devices Per Reel	Reel Size
IVA-05208-TR1	1000	7"
IVA-05208-TR2	4000	13"

Typical Biasing Configuration and Functional Block Diagram

Differential Input / Differential Output



Single Ended Input / Single Ended Output



* Optional: For Single-Ended Output operation, Pin 7 may be left unterminated (no C_{block} or 50 Ω)

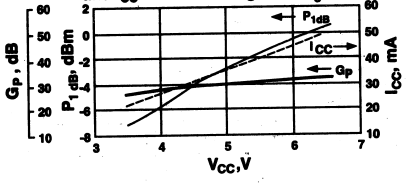
Cbypass = 1000 pF typical

Good grounding of Pins 2, 3 is critical for proper operation and good VSWR performance of this part.

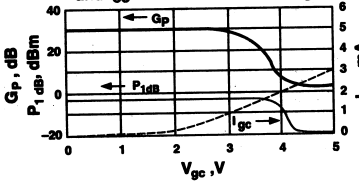
Typical Performance, $T_A = 25°C$, $V_{cc} = 5$ V, $V_{ee} = 0$ V

(Unless otherwise noted)

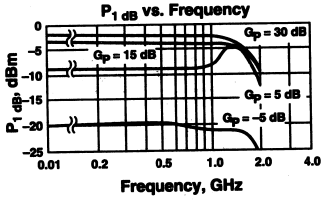
Power Gain and $P_{1\,dB}$ at 0.5 GHz, and I_{CC} vs. Bias Voltage with $V_{gc} = 0$ V



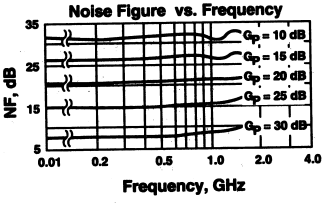
Power Gain and $P_{1\,dB}$ at 0.5 GHz and I_{CC} vs. Gain Control Voltage



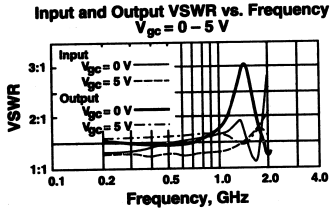
$P_{1\,dB}$ vs. Frequency



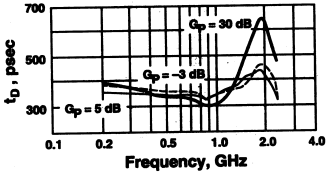
Noise Figure vs. Frequency



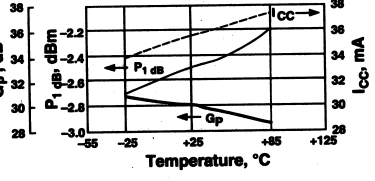
Input and Output VSWR vs. Frequency $V_{gc} = 0 - 5$ V



Group Delay vs. Frequency



Power Gain and $P_{1\,dB}$ at 0.5 GHz, and I_{CC} vs. Case Temperature with $V_{gc} = 0$ V



HEWLETT PACKARD

IVA-05218
MagIC™ Silicon Bipolar MMIC
1.5 GHz Variable Gain Amplifier
Differential Input Option

Features

- **Differential Input and Output Capability**
- **DC to 1.5 GHz Bandwidth; 2.0 Gb/s Data Rates**
- **High Gain: 30 dB typical**
- **Wide Gain Control Range: 30 dB typical**
- **5 V Bias**
- **5 V V_{gc} Control Voltage, I_{gc} < 3 mA**
- **Fast Gain Control Response: < 10 ns typical**
- **Hermetic Glass Ceramic Package**

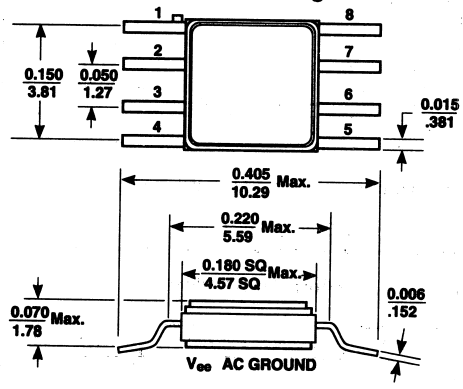
Description

The IVA-05218 is a variable gain amplifier housed in a miniature glass-metal hermetic surface mount package. This device can be used in any combination of single-ended or differential inputs or outputs (see Functional Block Diagram). The lowest frequency of operation is limited only by the values of user selected blocking and bypass capacitors.

Typical applications include variable gain amplification for fiber optic systems (e.g., SONET) with data rates up to 2.0 Gb/s, mobile radio and satellite receivers, millimeter wave receiver IF amplifiers and communication receivers.

The IVA series of variable gain amplifiers is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX} |SOSAT™| silicon bipolar process. This process uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

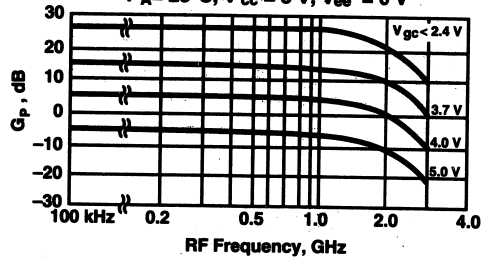
180 mil Package



PIN DESCRIPTION			
1	Input +	8	Gain Control Voltage
2	V_{ee}, AC Ground	7	Output -
3	V_{ee}, AC Ground	6	Output +
4	Input -	5	V_{cc}
Bottom of Package is V_{ee} (AC Ground)			

Notes:
(unless otherwise specified)
1. Dimensions are in / mm
2. Tolerances
in .xxx = ±.005
mm .xx = ±.13

Typical Variable Gain vs. Frequency
T_A= 25°C, V_{cc} = 5 V, V_{ee} = 0 V



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: [2] V_{cc}=5 V, V_{ee} = 0 V, V_{gc} = 0 V, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain (|S21|²)	f = 0.5 GHz	dB	25	30	
ΔG_P	Gain Flatness	f = 0.05 to 1.0 GHz	dB		±0.5	
f_{3dB}	3 dB Bandwidth[3]		GHz	1.0	1.5	
GCR	Gain Control Range[4]	f = 0.5 GHz. V_{gc}= 0 to 5 V	dB	25	30	
ISO	Reverse Isolation (|S12|²)	f = 0.5 GHz. V_{gc} = 0 to 5 V	dB		45	
VSWR	Input VSWR	f = 0.05 to 1.5 GHz. V_{gc} = 0 to 5 V			1.7:1	
	Output VSWR	f = 0.05 to 1.5 GHz. V_{gc} = 0 to 5 V			1.5:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		9	
P_{1dB}	Output Power at 1 dB Compression	f = 0.5 GHz	dBm		–3	
V_{OUT}	Peak-to-Peak Single-Ended Output Voltage	f = 0.5 GHz	mVpp		450	
IP_3	Output Third Order Intercept Point	f = 0.5 GHz	dBm		7	
t_D	Group Delay	f = 0.5 GHz	psec		400	
I_{CC}	Supply Current		mA	25	35	45

Notes:
1. The recommended operating voltage range for this device is 4 to 6 V. Typical performance as a function of voltage is on the following page.
2. As measured using Input Pin 1 and Output Pin 6, with Output Pin 7 terminated into 50 ohms and Input Pin 4 at AC ground.
3. Referenced from 50 MHz Gain.
4. The recommended gain control range for these devices for dynamic control is 0 to 4.2 V. Operation at gain control settings above 4.2 V may result in gain increase rather than gain decrease.

Absolute Maximum Ratings

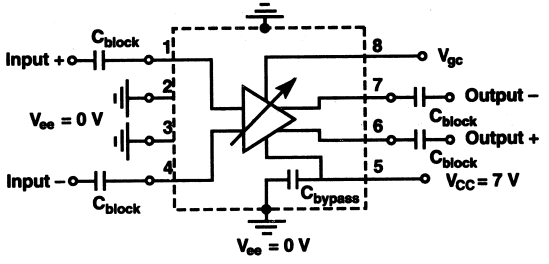
Parameter	Absolute Maximum[1]
Device Voltage (V_{cc}-V_{ee})	8 V
Power Dissipation[2,3]	600mW
Input Power	+14 dBm
V_{gc} - V_{ee}	7 V
Junction Temperature	200°C
Storage Temperature	-65 to 200°C

Thermal Resistance: θ_{jc} = 50°C/W

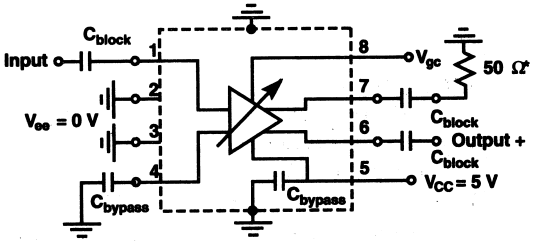
Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C.
3. Derate at 20mW/°C for T_C > 170°C.

Typical Biasing Configuration and Functional Block Diagram

Differential Input / Differential Output



Single Ended Input / Single Ended Output

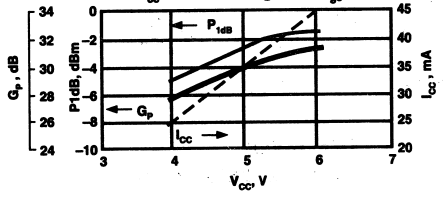


* Optional: For Single-Ended Output operation, Pin 7 may be left unterminated (no C_{block} or 50 Ω)

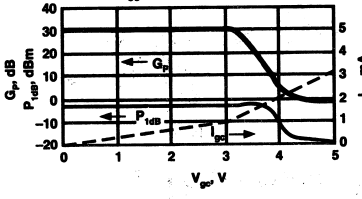
Typical Performance, T_A = 25°C, V_{CC} = 5 V, V_{ee} = 0 V

(Unless otherwise noted)

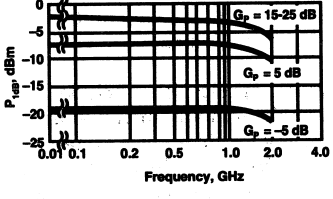
Power Gain and P_{1dB} at 0.5 GHz, and I_{cc} vs. Bias Voltage with V_{gc} = 0 V



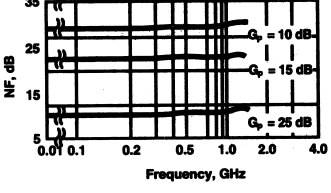
Power Gain and P_{1dB} at 0.5 GHz and I_{cc} vs. Gain Control Voltage



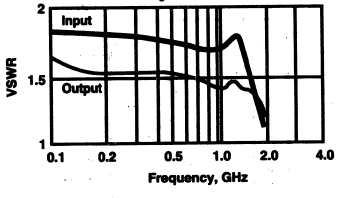
P_{1dB} vs. Frequency



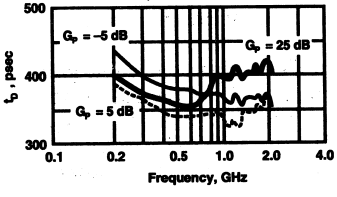
Noise Figure vs. Frequency



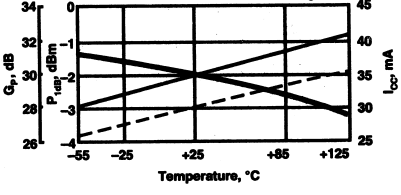
Input and Output VSWR vs. Frequency V_{gc} = 0 – 5 V



Group Delay vs. Frequency



Power Gain and P_{1dB} at 0.5 GHz, and I_{cc} vs. Case Temperature with V_{gc} = 0 V



HEWLETT PACKARD

Silicon Bipolar MMIC 2.5 GHz Variable Gain Amplifier

Technical Data

IVA-14208
IVA-14228

Features

- **Differential Input and Output Capability**
- **DC to 2.5 GHz Bandwidth; 3.4 Gbits/s Data Rates**
- **High Gain: 24 dB Typical**
- **Wide Gain Control Range: 34 dB Typical**
- **6 V Bias**
- **5 V V_{GC} Control Range, I_{GC} <3 mA**
- **Fast Gain Response: <10 nsec Typical**
- **IVA-14208: Low Cost Plastic Surface Mount Package**
- **IVA-14228: Hermetic Ceramic Surface Mount Package**

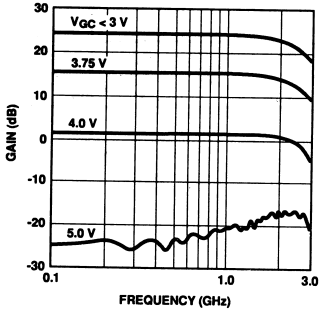


Figure 1. IVA-14228 Typical Variable Gain vs. Frequency and V_{GC} at V_{CC} = 6 V, T_{case} = 25°C.

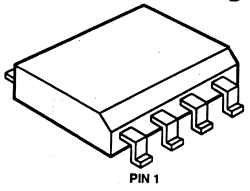
Description

The IVA-14 series MMICs are variable gain amplifiers. The IVA-14208 is housed in a miniature low cost plastic surface mount package. The IVA-14228 is housed in a miniature hermetic ceramic surface mount package. Both devices can be used in any combination of single-ended or differential inputs or outputs (see Functional Block Diagram). The lowest frequency of operation is limited only by the values of user selected blocking and bypass capacitors.

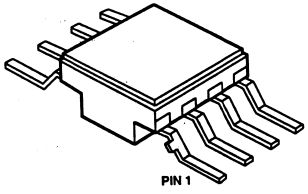
Typical applications include variable gain amplification or limiting for fiber optic systems (e.g. SONET) with data rates up to 3.4 Gbits/s, mobile radio and satellite receivers, millimeter wave receiver IF amplifiers and communications receivers.

The IVA series of variable gain amplifiers is fabricated using Hewlett-Packard's 10 GHz f_T, 25 GHz f_{MAX} ISOSAT™-1 silicon bipolar process. This process uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

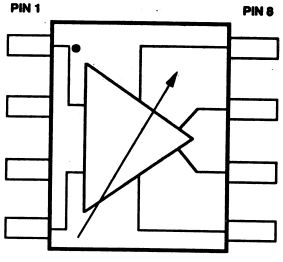
IVA-14208
Plastic SO-8 Package



IVA-14228
Ceramic '28' Package



Functional Block Diagram and Pin Configuration



PIN DESCRIPTION	
1. INPUT +	8. V_{GC}
2. V_{EE}, AC GROUND	7. OUTPUT -
3. V_{EE}, AC GROUND	6. OUTPUT +
4. INPUT -	5. V_{CC}

IVA-14228 PACKAGE BOTTOM IS V_{EE} AC GROUND.

Absolute Maximum Ratings[1]

Symbol	Parameter	Units	IVA-14208	IVA-14228
V_{CC}-V_{EE}	Device Voltage, T_{case} = 25°C	Volts	12	12
P_{in}	Input Power, T_{case} = 25°C	dBm	13	13
V_{GC}-V_{EE}	Control Voltage, T_{case} = 25°C	Volts	10	10
T_j	Junction Temperature+	°C	150	200
T_{stg}	Storage Temperature	°C	-65 to +150	-65 to +200
P_t	Total Device Dissipation	mW	1000[2]	1000[3]

Thermal Resistance:

IVA-14208 Thermal Resistance Junction to Case[4]: Θ_{jc} = 68°C/W
IVA-14228 Thermal Resistance Junction to Case[4]: Θ_{jc} = 63°C/W

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. T_{case} = 25°C. Derate at 14.7 mW/°C for T_{case} > 82°C.
3. T_{case} = 25°C. Derate at 15.9 mW/°C for T_{case} > 137°C.
4. T_j = 150°C.

Guaranteed Electrical Specifications All measurements reflect single-ended (unbalanced) performance. T_{case} = 25°C. V_{CC} = 6 V, V_{EE} = 0 V, V_{GC} = 0 V, Z_L = 50 Ω

Symbol	Parameter	Units	IVA-14208			IVA-14228		
			Min.	Typ.	Max.	Min.	Typ.	Max.
GP	Power Gain ($\|S_{21}\|^2$), f = 1 GHz	dB	20	24		22	24	
ΔGP	Gain Flatness, f = 0.05 to 2 GHz	dB		±1.2			±0.7	
f_{3dB}	3 dB Bandwidth	GHz	2.0	2.5		2.2	2.5	
GCR	Gain Control Range[2], f = 1 GHz, V_{GC} = 0 to 5 V	dB	30	34		30	34	
ISO	Reverse Isolation ($\|S_{12}\|^2$), f = 1 GHz, V_{GC} = 0 to 5 V	dB		37			40	
VSWR	Input VSWR, f = 0.05 to 2.0 GHz, V_{GC} = 0 to 5 V			2:1			2:1	
	Output VSWR, f = 0.05 to 2.0 GHz, V_{GC} = 0 to 5 V			2:1			2.5:1	
NF	50 Ω Noise Figure, f = 1 GHz	dB		9.0			9.0	
P_{1dB}	Output Power at 1 dB Gain, Compression f = 1 GHz	dBm		-2.0			-2.0	
V_{OUT}	Pk-Pk Single-ended Output Voltage, f = 1 GHz	mVpp		450			450	
IP_3	Third Order Intercept Point, f = 1 GHz	dBm		8			8	
t_D	Group Delay, f = 1 GHz	psec		450			450	
I_{cc}	Supply Current	mA	28	38	48	28	38	48

Note:
1. The recommended operating voltage range for these devices is 5 to 8 V. Typical performance as a function of voltage is shown in the graphs on the following pages.
2. The recommended gain control range for these devices for dynamic control is 0 to 4.2 V. Operation at gain control settings above 4.2 V may result in gain increase rather than gain decrease. See figures 4 and 19.

IVA-14228 Typical Performance Curves

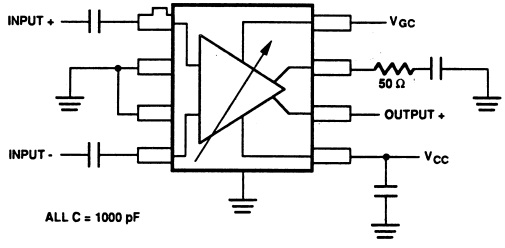


Figure 2. IVA-142X8 Connection Diagram Showing Balanced Inputs and Unbalanced Outputs. Inputs and Outputs May Be Either Balanced or Unbalanced.

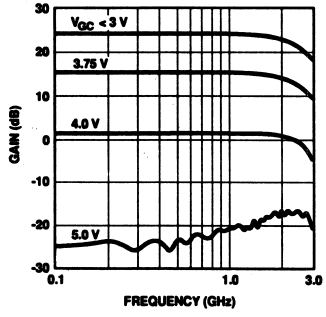


Figure 3. IVA-14228 Gain vs. Frequency and V_{GC}; V_{CC} = 6 V, T_{case} = 25°C.

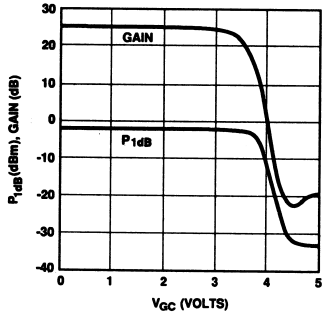


Figure 4. IVA-14228 P_{1dB} and Gain vs. V_{GC}; V_{CC} = 6 V, T_{case} = 25°C.

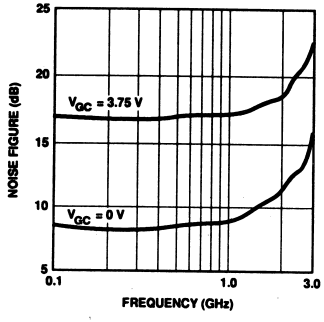


Figure 5. IVA-14228 Noise Figure vs. Frequency and V_{GC}; V_{CC} = 6 V, T_{case} = 25°C.

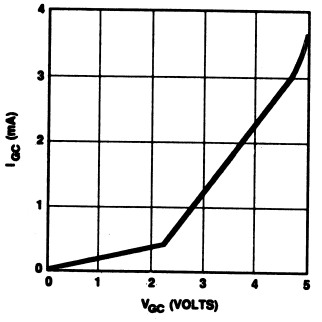


Figure 6. IVA-14228 I_{GC} vs. V_{GC}; V_{CC} = 6 V, T_{case} = 25°C.

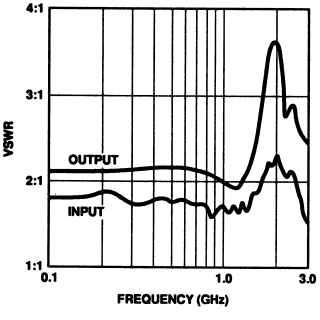


Figure 7. IVA-14228 VSWR vs. Frequency; V_{CC} = 6 V, V_{GC} = 0 V, T_{case} = 25°C.

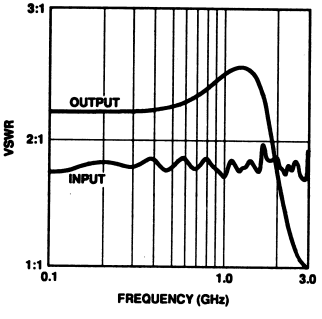


Figure 8. IVA-14228 VSWR vs. Frequency; V_{CC} = 6 V, V_{GC} = 5 V, T_{case} = 25°C.

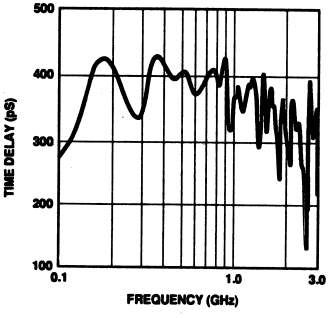


Figure 9. IVA-14228 Group Delay vs. Frequency; V_{GC} = 0 V, V_{CC} = 6 V, T_{case} = 25°C.

IVA-14228 Typical Performance Curves (cont.)

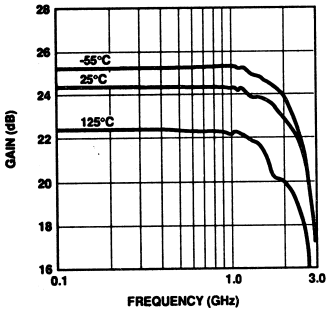


Figure 10. IVA-14228 Gain vs. Frequency and Temperature; V_{CC} = 6 V, V_{GC} = 0 V.

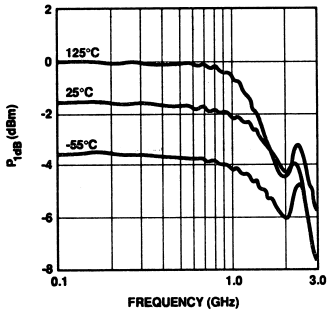


Figure 11: IVA-14228 P_{1dB} vs. Frequency and Temperature; V_{CC} = 6 V, V_{GC} = 0 V.

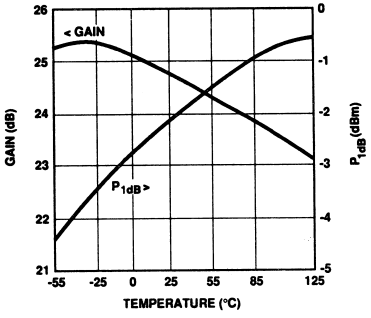


Figure 12. IVA-14228 Gain and P_{1dB} vs. Temperature; V_{CC} = 6 V, V_{GC} = 0 V, Frequency = 1 GHz.

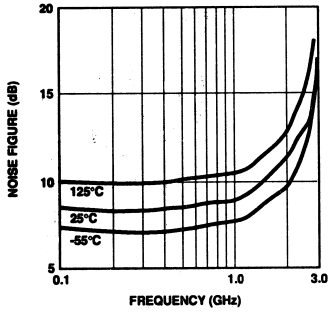


Figure 13. IVA-14228 Noise Figure vs. Frequency and Temperature; V_{CC} = 6 V, V_{GC} = 0 V.

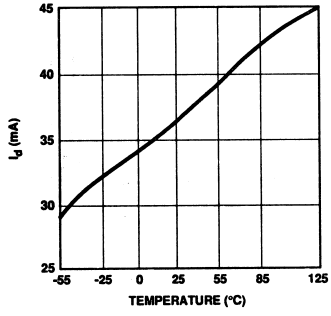


Figure 14. IVA-14228 I_{CC} vs. Temperature; V_{CC} = 6 V, V_{GC} = 0 V, Frequency = 1 GHz.

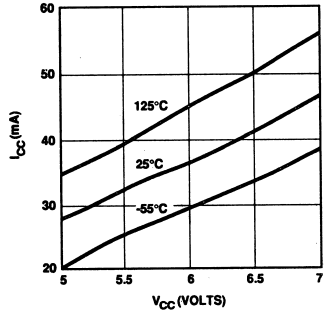


Figure 15. IVA-14228 I_{CC} vs. V_{CC} and Temperature; V_{GC} = 0 V.

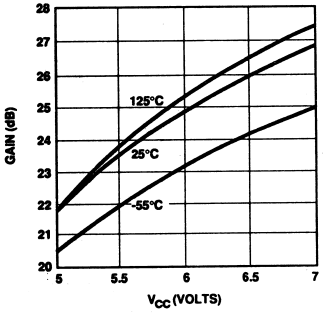


Figure 16. IVA-14228 Gain vs. V_{CC} and Temperature; V_{GC} = 0 V, Frequency = 1 GHz.

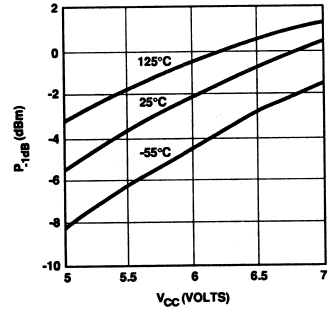


Figure 17. IVA-14228 P_{1dB} vs. V_{CC} and Temperature; V_{GC} = 0 V, Frequency = 1 GHz.

IVA-14208 Typical Performance Curves

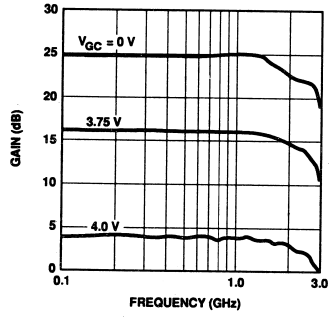


Figure 18. IVA-14208 Gain vs. Frequency and V_{GC}; V_{CC} = 6 V, T_{case} = 25°C.

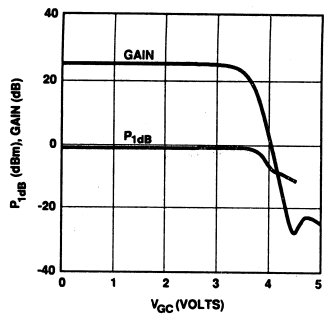


Figure 19. IVA-14208 Gain and P_{1dB} vs. V_{GC}; V_{CC} = 6 V, Frequency = 1 GHz, T_{case} = 25°C.

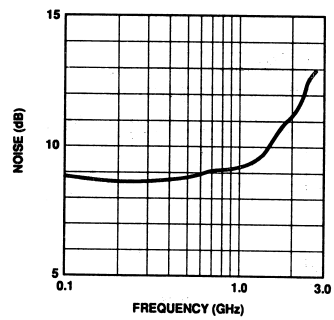


Figure 20. IVA-14208 Noise Figure vs. Frequency; V_{CC} = 6 V, V_{GC} = 0 V, T_{case} = 25°C.

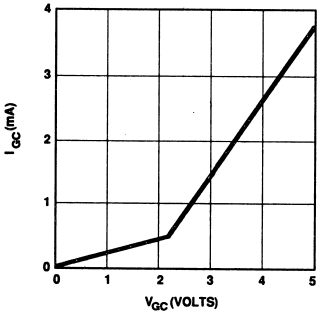


Figure 21. IVA-14208 I_{GC} vs. V_{GC}; V_{CC} = 6 V, T_{case} = 25°C.

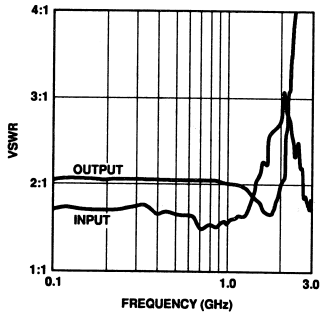


Figure 22. IVA-14208 VSWR vs. Frequency; V_{CC} = 6 V, V_{GC} = 0 V, T_{case} = 25°C.

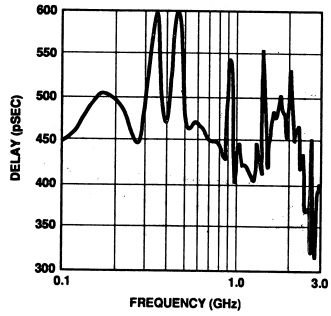


Figure 23. IVA-14208 Group Delay vs. Frequency; V_{CC} = 6 V, V_{GC} = 0 V, T_{case} = 25°C.

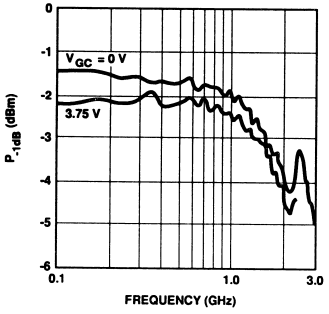


Figure 24. IVA-14208 P_{1dB} vs. Frequency and V_{GC}; V_{CC} = 6 V, Frequency = 1 GHz, T_{case} = 25°C.

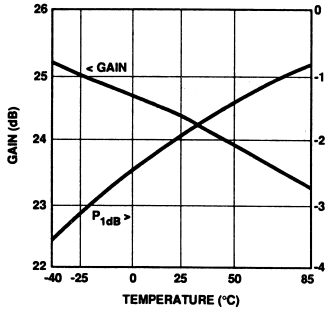


Figure 25. IVA-14208 Gain and P_{1dB} vs. Temperature; V_{CC} = 6 V, V_{GC} = 0 V, Frequency = 1 GHz.

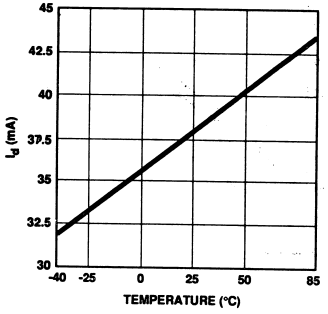


Figure 26. IVA-14208 I_{CC} vs. Temperature; V_{CC} = 6 V, V_{GC} = 0 V.

IVA-14208 Typical Performance Curves (cont.)

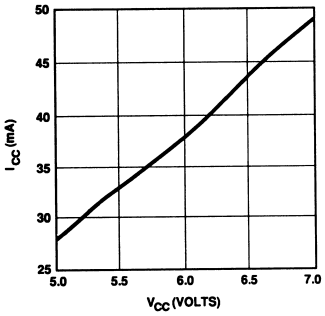


Figure 27. IVA-14208 I_{CC} vs. V_{CC}; V_{GC} = 0 V, T_{case} = 25°C.

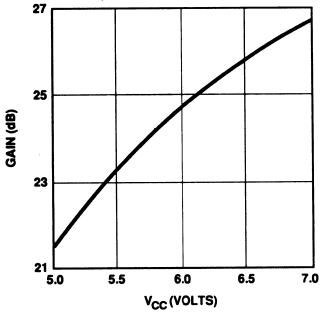


Figure 28. IVA-14208 Gain vs. V_{CC}; V_{GC} = 0 V, Frequency = 1 GHz, T_{case} = 25°C.

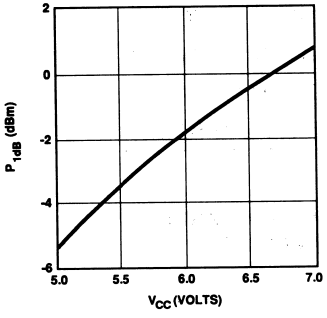


Figure 29. IVA-14208 P_{1dB} vs. V_{CC}; V_{GC} = 0 V, Frequency = 1 GHz, T_{case} = 25°C.

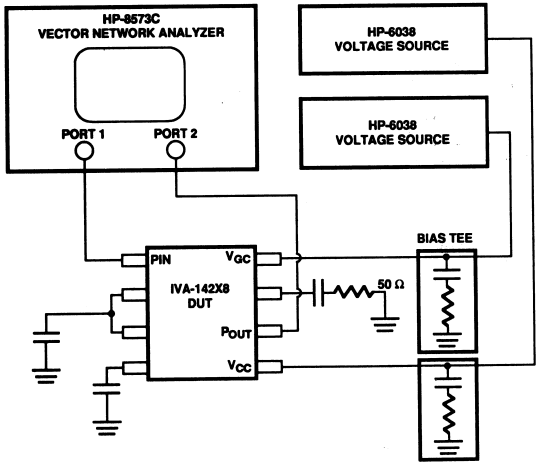
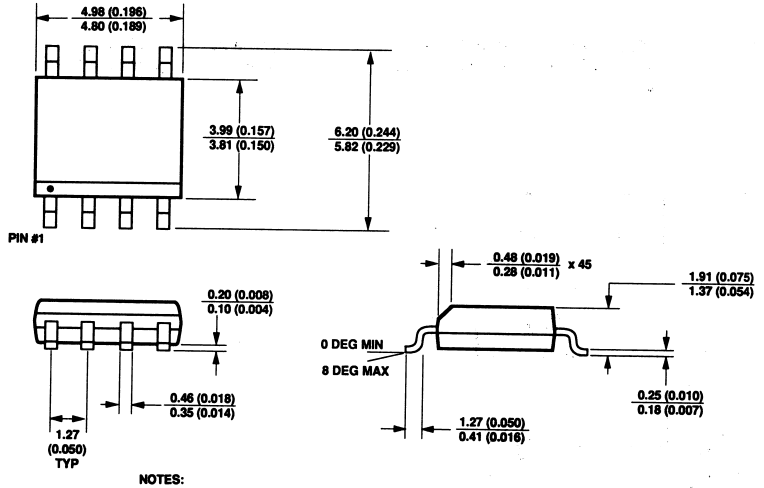


Figure 30. Test Equipment Setup for Measuring Performance of the IVA-142X8.

Part Number Ordering Information

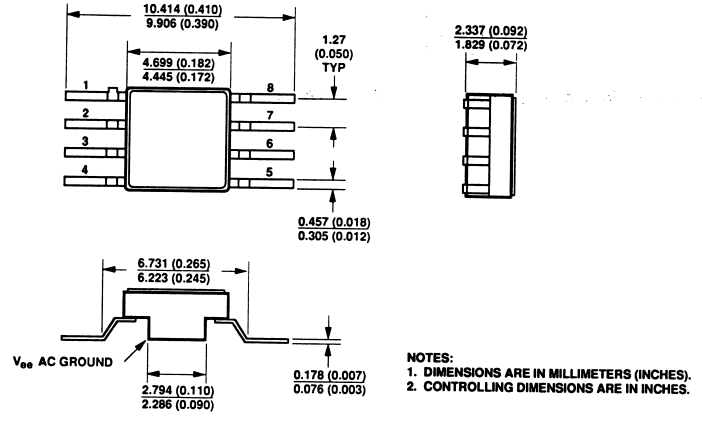
Part Number	Container Type	Qty. per Container
IVA-14208-STR	BIP Strip	1
IVA-14208-TR1	7" Reel	1000
IVA-14208-TR2	13" Reel	4000
IVA-14228-STR	BIP Strip	1

Package Dimensions
IVA-14208



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSIONS ARE IN INCHES.

Package Dimensions
IVA-14228



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSIONS ARE IN INCHES.

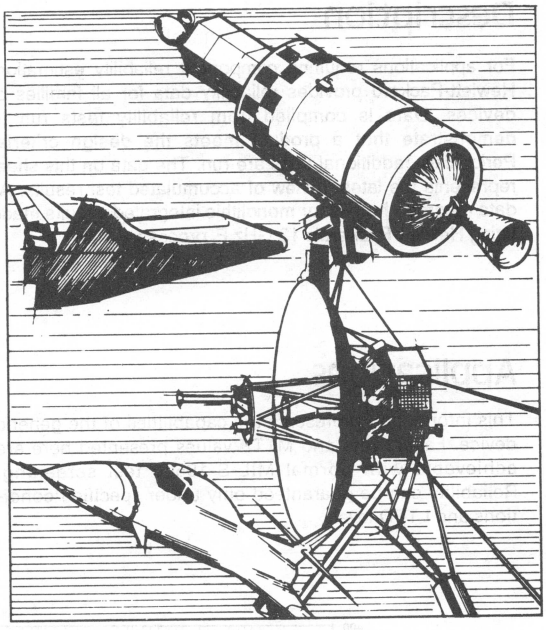
HEWLETT PACKARD

Decision Circuit Products

Reliability Data

Description

For applications requiring component reliability estimation Hewlett-Packard provides reliability data for the Interface devices. Data is complied from reliability tests to demonstrate that a product meets design criteria. The data on this sheet represents the latest review of accumulated test results.



Reliability

Each design is tested for performance under varying conditions of temperature, humidity, vibration and mechanical shock. Sample production units undergo life testing to demonstrate predicted MTTF for selected product designs.

The following MTTF (Mean Time To Failure) hours have been calculated from the failure rate predictions found in MIL-HDBK-217D, Reliability Prediction of Electronic Equipment. The Hybrid Microcircuit failure rate model was used:

$$\lambda_p = \left\{ \Sigma N_C \lambda_C \Pi_G + [N_R \lambda_R + \Sigma N_I \lambda_I + \lambda_S] \Pi_F \Pi_E \right\} \Pi_Q \Pi_D$$

(failures/10^6 hour)

where:

$MTTF = 1/\lambda_p$

$\Sigma N_C \lambda_C \Pi_G$ is the sum of the adjusted failure rates for the active components, packaged resistors, and capacitors in the hybrid

N_C is the number of each particular component

λ_C is the component failure rate

Π_G is the die correction factor

$N_R \lambda_R$ is the number of (N_R) and failure rate contribution (λ_R) of the chip or substrate resistors

$\Sigma N_I \lambda_I$ is the sum of the failure rate contributions of the interconnections (λ_I)

λ_S is the failure rate contribution of the hybrid package

Π_E is the environmental factor for the film resistors, interconnections and package

Π_Q is the quality factor

Π_D is the density factor

Π_F is the circuit function factor

MTTF Summary

Product	Part Number	Package	Case Temp. °C	MTTF Hours
Interface	HDMP-2003	HBIC-0512	85	$3x10^7$
	HDMP-2004	HBIC-0512	85	$3x10^7$

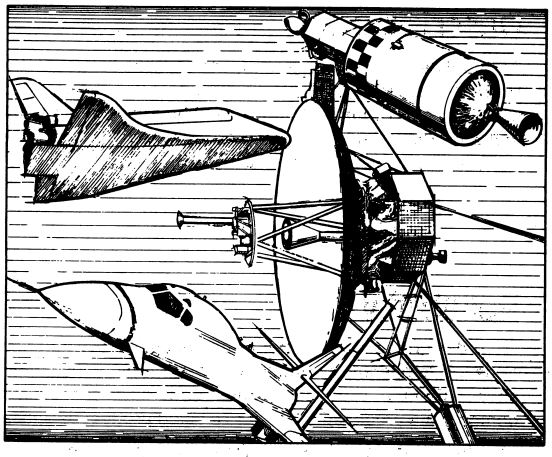
HEWLETT PACKARD

Decision Circuit Products

Reliability Data

Description

For applications requiring component reliability estimation, Hewlett-Packard provides reliability data for all families of devices. Data is compiled from reliability tests run to demonstrate that a product meets the design criteria. Periodically, additional tests are run. The data on this sheet represents the latest review of accumulated test results. All data recorded here is for monolithic integrated circuits made using Hewlett-Packard's 13 GHz F_t process.

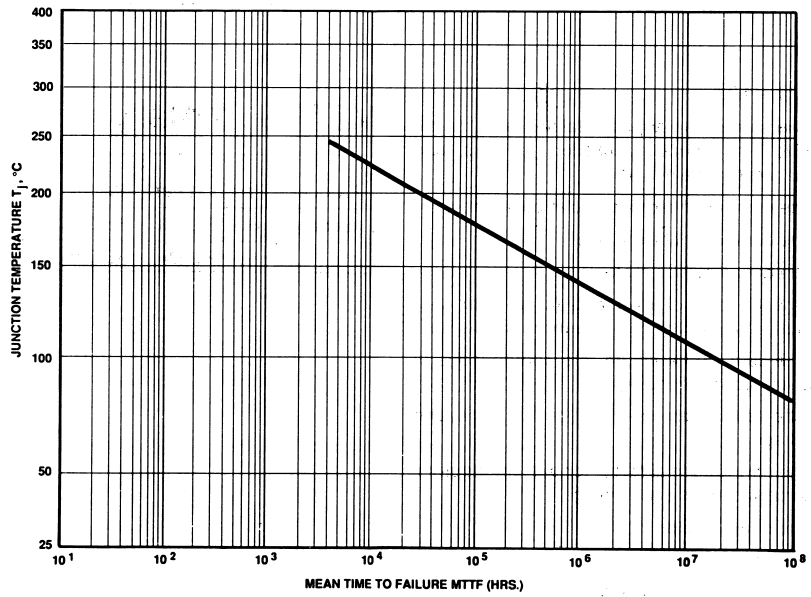


Applications

This information represents the capabilities of the generic device. Failure rate and MTTF values presented here are achievable with normal MIL-S-19500 test screening. Reliability can be guaranteed only under specified conditions and LTPD levels.

Applicable Part Numbers

HDMP-2006



Integrated Assemblies



Silicon Comb Generator Modules

Part Number	Minimum P_{out} at 12.4 GHz (dBm)	Typical P_{out} at 18 GHz (dBm)	Package	Page
33002A/B[a,b]	-30	-35	A/B	11-4
33003A/B[a,b]	-20	-30	A/B	11-4
33004A/B[a,b]	-15	-15	A/B	11-4
33005C/D[a,b]	-10	-5	C/D	11-4

Switches and Attenuators

General Purpose Microwave SPST Switches and Attenuators DC-18 GHz

Part Number	Parameter	Conditions	0.1-1.0	1.0-2.0	4.0-8.0	8.0-12.0	12.0-18.0	Page
33102A	Max. Isolation (dB)	I_C = -100 mA	33	35	43	43	43	11-12
	Min. Insertion Loss (dB)	I_C = 0	1.0	1.0	2.0	2.0	2.5	
	Max. SWR		1.7	1.7	2.0	2.0	2.5	
33104A	Max. Isolation (dB)	I_C = -100 mA	42	65	80	80	–	11-12
	Min. Insertion Loss (dB)	I_C = 0	1.0	1.0	2.1	2.2	–	
	Max. SWR		1.7	1.8	2.0	2.0	–	

Low Loss Microwave SPST Switches and Attenuators DC-18 GHz

Part Number	Parameter	Conditions	0.1-1.0	1.0-2.0	4.0-8.0	8.0-12.0	12.0-18.0	Page
33132A	Max. Isolation (dB)	I_C = 30 mA	28	33	43	43	43	11-18
	Min. Insertion Loss (dB)	V_C = -10 V	1.0	1.0	1.2	1.4	2.0	
	Max. SWR		1.7	1.7	1.9	1.9	2.2	
33134A	Max. Isolation (dB)	I_C = -100 mA	40	60	80	80	80	11-18
	Min. Insertion Loss (dB)	I_C = 0	1.0	1.0	1.6	1.8	2.5	
	Max. SWR		1.7	1.7	2.0	2.0	2.2	

Fast Microwave SPST Switches and Attenuators DC-18 GHz

Part Number	Parameter	Conditions	0.1-1.0	1.0-2.0	4.0-8.0	8.0-12.0	12.0-18.0	Page
33142A	Max. Isolation (dB)	I_C = 20 mA	25	30	45	45	45	11-22
	Min. Insertion Loss (dB)	V_C = -10 V	1.0	1.0	1.5	1.5	2.5	
	Max. SWR		1.7	1.9	1.9	1.9	2.2	
33144A	Max. Isolation (dB)	I_C = 40 mA	35	60	80	80	80	11-22
	Min. Insertion Loss (dB)	V_C = -10 V	1.0	1.1	1.7	2.0	3.0	
	Max. SWR		1.7	2.0	2.0	2.0	2.5	

Notes:
[a] A/C are complete comb generators with DC return and require no external bias.
[b] B/D (no connectors) can be biased from either end using a bias tee.

Switches and Attenuators (cont.)

Microwave Switch – SPDT 0.1-18 GHz

Part Number	Parameter	Frequency Range, GHz				Page
		0.1-1.0	1.0-2.0	2.0-4.0	12.0-18.0	
33016C	Min. Isolation, Common to OFF Arm Max.Insertion Loss, ON Arm (dB) Max. SWR, ON Arm	70 1.5 1.5	70 2.0 1.5	70 2.0 1.8	55 3.0 3.0	11-9

Switch Driver for Fast PIN Diode Switches

		Driver Input Controls			Steady State Output Levels			
Part Number	Switch Mode	Logic State	Input Voltage	Max. Input Current	Logic State	Typ. Open Circuit Voltage	Min. Available Output Current	Page
33190B	Min. Insertion Loss Isolation	0 1	0-0.8 V 2.5 V min.	4 mA Sink 50 µA (2) Source	0 1	-10 V +3 V	40 mA 40 mA	11-28

Note:
[2] Increases for V_{IN} greater than 2.5 V. Input impedance appx. 1 KΩ for V_{IN} greater than 2.5 V.

Microwave Bias Network – 0.1-18 GHz

Part Number	Parameter	Frequency Range, GHz				Page
		0.1-3.5	3.5-11	11-18	18-26 Option 002	
33150A	Min. Insertion Loss Max. VSWR Max. DC Bias Resistance (Ω)	0.4 1.5:1	0.6 1.5:1	1.1 1.8:1 4.0	1.5 2.8:1	11-26

Notes:
For reliability data see page 11-31 – 11-35.

HEWLETT PACKARD

Coaxial Step Recovery Diode Modules (Impulse Train Generators)

Technical Data

33002A/B
33003A/B
33004A/B
33005C/D

Features

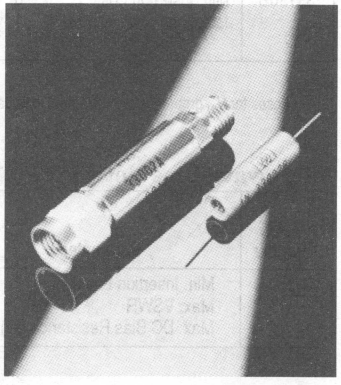
- **Various Drive Frequencies Available**
  100, 250, 500,1000 MHz
- **Narrow Output Pulses**
  130 Picosecond Pulse Width with 10 Volt Amplitude
- **Broadband Output Comb**
  Useful Power at Each Harmonic through 18 GHz
- **Input Matched to 50 Ω**
- **Self-Biased**
  No External Bias Required
- **Reliable**
  Rugged, Reliable Solid State Hybrid Integrated Design

Description

These units are integrated step recovery diode "impulse train" generating circuits matched to 50 Ω at the input frequency. All circuit elements necessary to produce the impulse train are integrated into the hermetically sealed cylindrical module. All internal joints are welded or thermocompression bonded for high reliability. Modules are also available mounted in a 3 mm connector housing containing a DC return which self-biases the diode.

Applications

When driven at the appropriate input frequency, the output of these devices is a train of narrow, high amplitude pulses at a repetition rate equal to the input frequency. The resulting "comb" spectrum consists of lines at all multiples of f_{IN} up to and beyond 18 GHz. The outputs are useful in many applications such as: measurement of the spectral behavior of various linear components (filters and slow wave structures); frequency and amplitude calibration of receivers, systems, and antennas; frequency marking systems; reference frequency generation for phase locked systems; sampling phase-lock systems; local oscillator drivers for coherent receiving techniques; multipliers; and pulse circuit applications.



In addition to drive frequencies of 100 MHz, 250 MHz, 500 MHz, and 1000 MHz, other drive frequencies (any frequency between 50 MHz and 3000 MHz) are available on special order.

Specifications at T_{CASE} = 25°C

Maximum Ratings

Maximum Power at Input Frequency[1]	1.0 W
Maximum Operating Temperature	125°C

Note:
1. Derate to 0.5 W at 125°C.

Specifications at T_{CASE} = 25°C (cont.)

Input Specifications

Model Number	Input Frequency
33002A/B	100 ± 5 MHz (useful at slightly reduced performance 100 ± 10 MHz)
33003A/B	250 ± 12.5 MHz (useful at slightly reduced performance 250 ± 25 MHz)
33004A/B	500 ± 25 MHz (useful at slightly reduced performance 500 ± 50 MHz)
33005C/D	1000 ± 50 MHz (useful at slightly reduced performance 1000 ± 100 MHz)
Input SWR for all Models	Less than 2:1 at center frequency

Typical Output Pulse Characteristics, 0.5 W Drive

Model Number (Drive Frequency)	Pulse Height (V) Typ.	Pulse Width(ps) Typ.
33002A/B (100 MHz)	15	130
33003A/B (250 MHz)	15	130
33004A/B (500 MHz)	15	130
33005C/D (1000 MHz)	10	130

Line Spectra, 0.5 W Drive

Model Number	Power Output per Line (dBm)							
	f_{IN}* to 4 GHz		4-8 GHz		8-12.4 GHz		12.4-18 GHz	
	Min.	Typ.†	Min.	Typ.†	Min.	Typ.†	Min.	Typ.†
33002A/B (100 MHz)	-15	-5	-25	-15	-30	-25	-	-35
33003A/B (250 MHz)	-5	0	-15	-5	-20	-15	-	-30
33004A/B (500 MHz)	+5	+10	-5	+5	-15	-5	-	-15
33005C/D (1000 MHz)	+5	+10	0	+5	-10	0	-15	-5

*Fundamental line excluded.
†Midband, see Figures 7-10.

Mechanical Characteristics

Size ..... See outline drawing
Weight ..... 10 grams
Materials
B and D versions ..... outer case and leads - Kovar
A and C versions ..... outer case and connections - stainless steel
Finish
B and D versions ..... Gold plated, 50 microinch minimum
A and C versions ..... Stainless steel

Temperature Effects

The comb generator is designed to operate over wide ambient temperatures (-55°C to +125°C). The SWR remains below 2:1 and typical spectral line power variation is about ±2 dB over this temperature range.

Bias

The circuit diagrams are shown in Figure 1. The "A" and "C" versions are complete comb generators with DC return and require no external bias. The module ("B" and "D" versions, no connectors) can be biased from either end by using a bias tee.

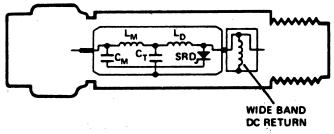


Figure 1a. Electrical Schematic of "A" and "C" Versions.

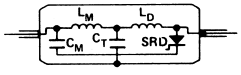


Figure 1b. Electrical Schematic of "B" and "D" Versions.

Environmental Characteristics

Temperature Storage	-55°C to +125°C
Temperature Operating	-55°C to +125°C
Temperature Cycling	MIL-STD-750, Method 1051
	Test Condition A
Temperature Shock	MIL-STD-750, Method 1056
	Test Condition A ("B" and "D" versions only)
Moisture Resistance	MIL-STD-750, Method 1021
Shock (nonoperating)	MIL-STD-750, Method 2016
	5 blows each X_1, Y_1, Y_2 orientations
	0.5 ms, 1500 g's
Vibration Fatigue	MIL-STD-750, Method 2046

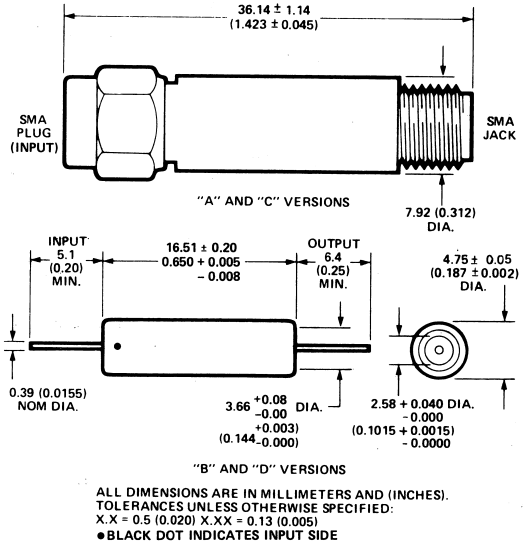


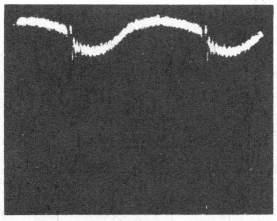
Figure 2. Mechanical Outlines.

The output of these devices consists of a train of very short pulses periodic with the input frequency.

In the time domain, the output is characterized by the pulse height, pulse width and the excess feed-through of the fundamental frequency component to the output.

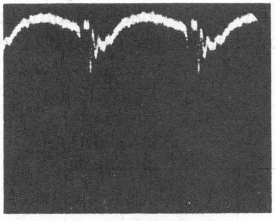
In the frequency domain the output consists of power at all frequencies which are integral multiples of f_{IN} up to and beyond 18 GHz. All specifications are for 0.5 watt drive at 25°C case temperature.

Time Domain



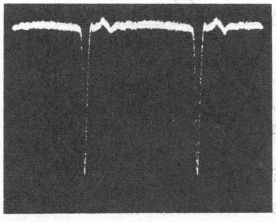
2 VOLTS/cm
2 ns/cm

Figure 3. Impulse Waveform 33002A/B (100 MHz).



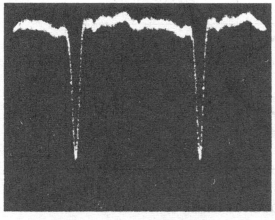
2 VOLTS/cm
1 ns/cm

Figure 4. Impulse Waveform 33003A/B (250 MHz).



3 VOLTS/cm
500 ps/cm

Figure 5. Impulse Waveform 33004A/B (500 MHz).



2 VOLTS/cm
200 ps/cm

Figure 6. Impulse Waveform 33005C/D (1000 MHz).

Frequency Domain

In the frequency domain the output is characterized by a line spectrum. The spacing of the lines is equal to the input frequency. Fundamental frequency feed-through is approximately 15 dBm with 27 dBm input power.

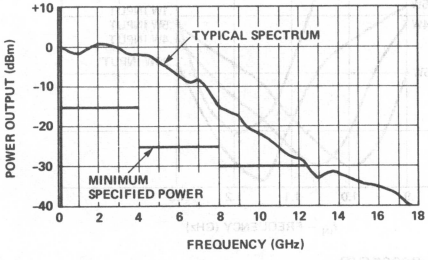


Figure 7. Spectrum Envelope of 33002A/B (100 MHz).

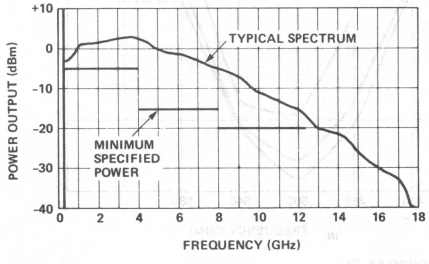


Figure 8. Spectrum Envelope of 33003A/B (250 MHz).

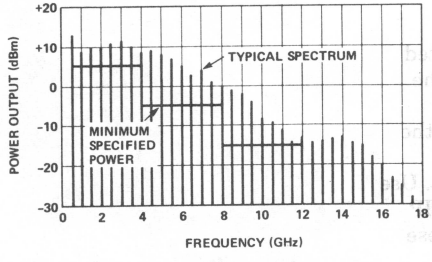


Figure 9. Spectrum Envelope of 33004A/B (500 MHz).

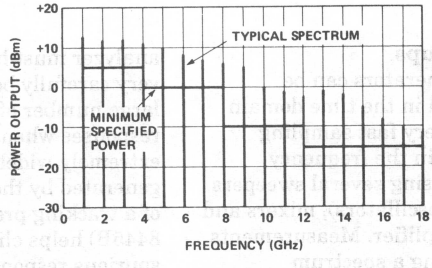


Figure 10. Spectrum Envelope of 33005C/D (1000 MHz).

Input SWR

The input SWR is a function of the input power. The devices have all been optimized for minimum SWR at the nominal center frequency with 0.5 watt drive. Below 0.5 watts, the SWR begins increasing. The point of minimum SWR may be adjusted if external bias is applied to the diode ("B" and "D" versions only, which have no DC return).

SWR Characteristics

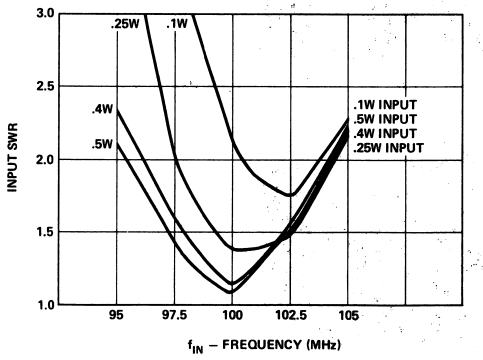


Figure 11. 33002A/B

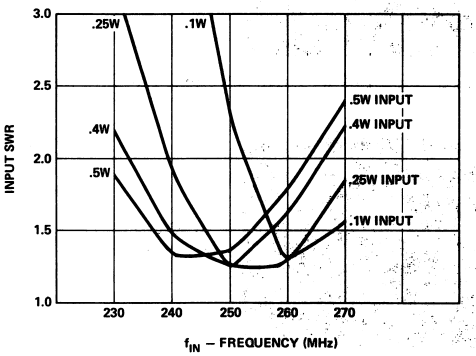


Figure 12. 33003A/B.

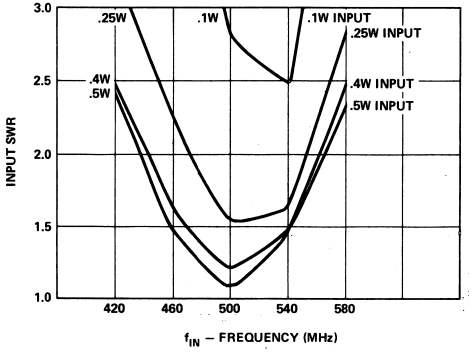


Figure 13. 33004A/B.

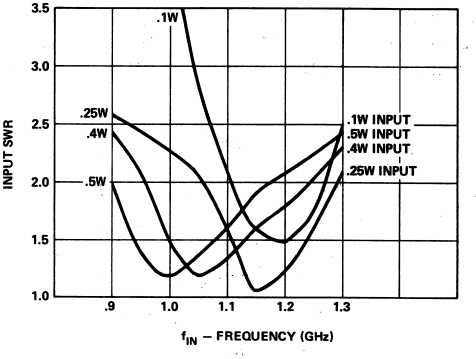


Figure 14. 33005C/D.

Test Setups

Comb generators can be measured in the time domain using a very fast sampling scope, or in the frequency domain using several sweepers (as local oscillators), mixers and an IF amplifier. Measurements made using a spectrum analyzer must be interpreted very carefully because of the large number of spurious responses when driven by the extremely wideband comb generated by these devices. Use of a tracking preselector (HP 8445B) helps eliminate these spurious responses.

HEWLETT PACKARD

Microwave Switch-SPDT 0.1-18 GHz

Technical Data

33016C

Features

- **Wideband 0.1 to 18 GHz**
- **Hermetic Diode Module**
- **High Isolation**

Description/ Applications

This single-pole, double-throw switch takes advantage of HP's low capacitance Beam Lead PIN diodes as a series element and HP's chip PIN diodes as shunt elements to provide high performance over a broad bandwidth.

This microwave switch is operable from 0.1 to 18 GHz, in both broadband and narrowband applications. Specified isolation is 60 dB up to 18 GHz. This switch is a reliable general purpose device usable in test instrumentation, ECM systems, communications, and other applications where high performance is desirable.

Driver Considerations

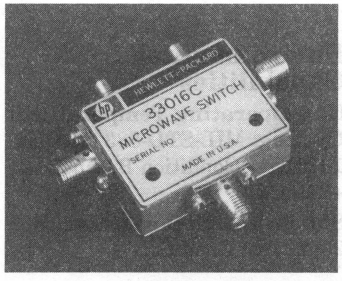
The recommended bias currents for the 33016C are 50 mA for the ON arm and -50 mA for the OFF arm. Driver requirements are dictated by the specific application. Using suitable driver circuits typical 10 to 90% switching speeds of 100 ns may be achieved. See Application Note AN 932 for additional details.

RF to DC Isolation

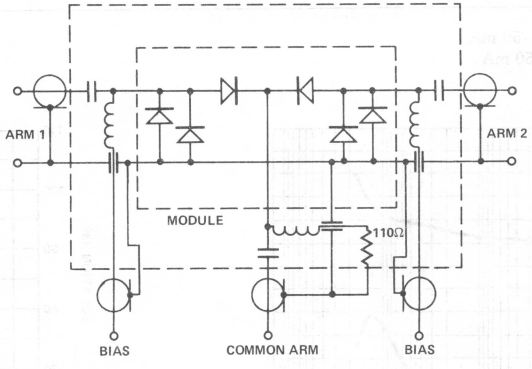
Isolation of the RF from the control circuit is typically 30 dB.

RF Power Handling

CW RF power handling is limited by the maximum power dissipation of the ON series diode. Pulse RF power handling is limited by the voltage breakdown of the shunt diodes.



Schematic Diagram



Maximum Ratings

Parameter	Limits
Operating Temperature	-65°C to +95°C
Storage Temperature	-65°C to +125°C
CW RF Power at T_C = 25°C	1 W (Derate linearly to 0.4 W at 95°C)
Pulse RF Power at T_C = 25°C (1 µs, 0.001 duty cycle)	75 W (Derate linearly to 33 W at 95°C)
Control Current ON Arm OFF Arm	 +100 mA -100 mA
Control Voltage	-1 V, +12.0 V

Environmental Capabilities

Non-Operating Temperature Cycling: MIL-STD-883. Method 1010 Test Condition B (-55°C to +125°C).

Shock: MIL-STD-883, Method 2002, Test Condition B.

Moisture Resistance: MIL-STD-883. Method 1004.

Salt Atmosphere: (corrosion) MIL-STD-883, Method 1009, Test Condition A.

Mechanical Specifications

Size: See Outline Drawing.

Body Finish: painted.

Electrical Specifications at T_{CASE} = 25°C

Parameter*	Frequency Range (GHz)				
	0.1-1	1-2	2-4	4-12	12-18
Minimum Isolation, Common to OFF Arm (dB)	70	70	70	60	55
Maximum Insertion Loss, ON Arm (dB)	1.5	2.0	2.0	2.0	3.0
Maximum SWR, ON Arm	1.5	1.5	1.8	2.2	3.0

*I_C (OFF) = -50 mA
I_C (ON) = +50 mA

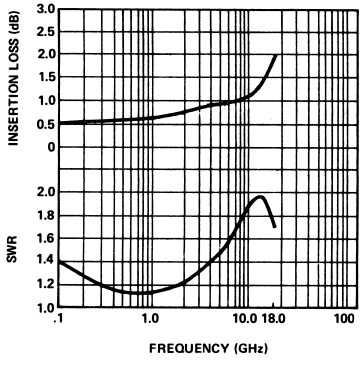


Figure 1. Typical Insertion Loss and SWR (ON Arm).

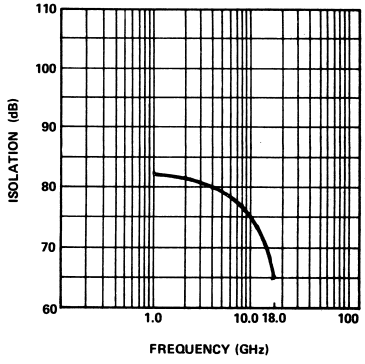
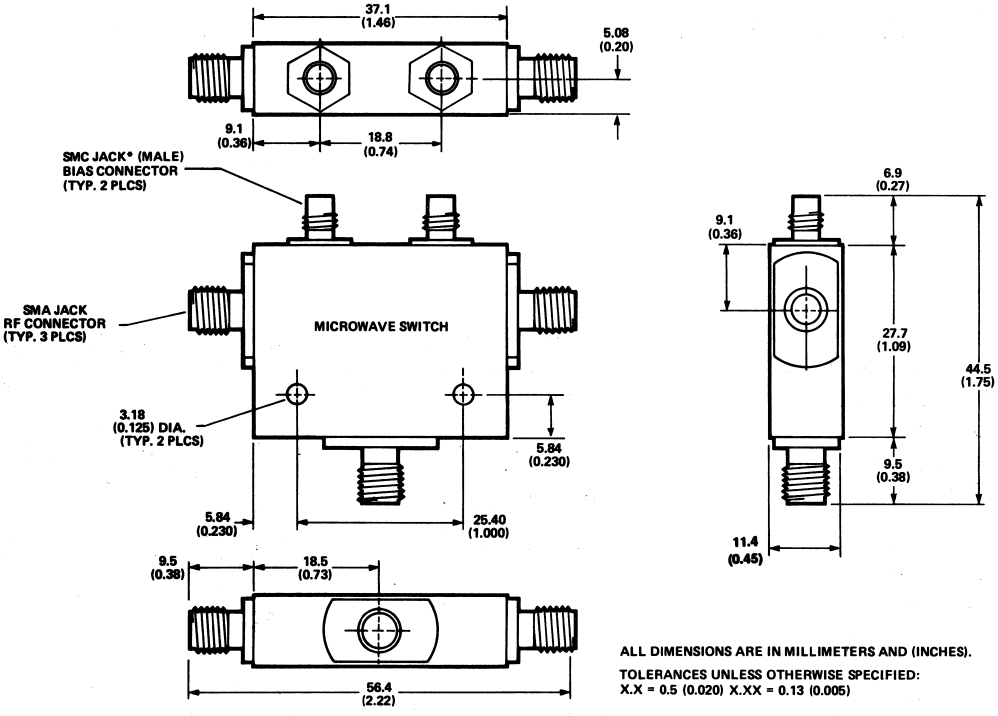


Figure 2. Typical Isolation (OFF Arm).

Outline Drawing



*SMA JACK AVAILABLE AS OPTION 001

ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES).

TOLERANCES UNLESS OTHERWISE SPECIFIED:
X.X = 0.5 (0.020) X.XX = 0.13 (0.005)

HEWLETT PACKARD

General Purpose Microwave SPST Switches and Attenuators DC-18 GHz

Technical Data

33102A
33104A

Features

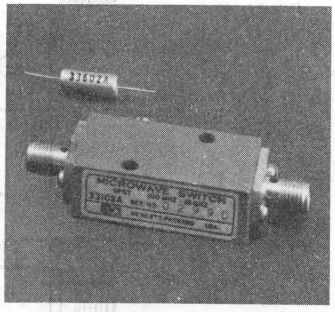
- **Low Insertion Loss**
- **High Isolation**
- **Low SWR**
- **Package and Connector Variety**

Description

HP SPST switches utilize PIN diodes in shunt across a 50 ohm transmission line. At microwave frequencies the PIN diode presents a high impedance at zero bias. With the diode in shunt, the switch is "on" at zero bias (well matched and passing all the incident RF power). Approximately 50 mA of DC current per diode reduces the diode impedance to much less than 50 ohms. Thus the switch is "off" when the diode is heavily forward biased (high mismatch reflecting most of the power back to the source). When switching from the "on" to "off" state, the switch can be set at any attenuation level between these two extremes. The PIN diode allows a smooth and repeatable variation of attenuation with change in bias level. Typical switching speed is 50 ns.

The HP 33100 is a complete switch, with RF connector, bias circuit, and built in DC return. Ordering information is given on the following page.

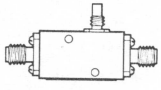
For further technical details, see HP Application Note 922, "Application of PIN Diodes."



Ordering Information

The HP 33100 series switch is a broadband general purpose switch. The standard unit is supplied with SMA jack (female) RF connectors and SMC jack bias connector. An SMA jack bias connector is available as Option 001.

Selection Guide

Description/Configuration	Standard (2-diode)	High Isolation (4-diode)	Connector Options	DC Bias Circuit
Broadband 33100 Series 	33102A	33104A	SMA Only	Built-In

Electrical Specifications

Maximum Ratings

Parameter	33100 Series
Operating Temperature	-55°C to +95°C
Storage Temperature	-55°C to +125°C
CW RF Power at T_{CASE} = 25°C	2 W (Derate to 0.85 Watt at 95°C)
Pulse RF Power at T_{CASE} = 25°C (1 µs 0.001 duty cycle)	75 W (Derate to 33 Watt at 95°C)
Control Current/Voltage	See following table

Maximum Control Current/Voltage

Model	Current (mA)	Voltage (V)
33102	-200	+100 to -1.0
33104	-400	+100 to -1.0

Noise Figure
Equal to attenuation.

Distortion
Internally generated harmonics in the General Purpose Series are typically 40 dB below the fundamental at input power levels up to 2 watts.

RF to DC Isolation
Isolation of the RF from the control circuit is typically 30 dB.

Driver Considerations
Driver requirements are dictated by the specific application. When the switch is used as a modulator or attenuator, a current amplifier is required. Suitable integrated circuits can be obtained for either laboratory or OEM applications. For example, an HP 33190B is suitable as a driver.

Switch Schematics



Figure 1. Module Schematic.

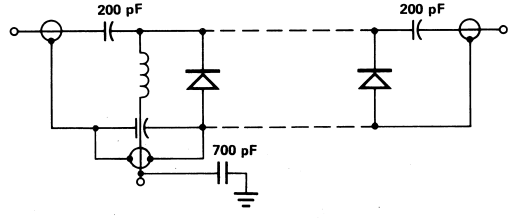


Figure 2. Switch Assembly Schematic.

Typical Switching Speed (10%-90%)	General Purpose 33102A, 33104A
Off-On	50 ns
On-Off	50 ns

Model	Diode Polarity	Number of Diodes
33102	As Shown	2
33104	As Shown	4

Electrical Specifications at T_{CASE} = 25°C

33100 Series Broadband

Model	Parameter	Conditions	Frequency Range (GHz)					
			0.1-1.0	1.0-2.0	2.0-4.0	4.0-8.0	8.0-12.0	12.0-18.0
33102A	Min. Isolation (dB)	I_C = -100 mA	33	35	40	43	43	43
	Max. Insertion Loss (dB)	I_C = 0	1.0	1.0	1.3	2.0	2.0	2.5
	Max. SWR		1.7	1.7	1.8	2.0	2.0	2.5
33104A	Min. Isolation (dB)	I_C = -200 mA	42	65	80	80	80	-
	Max. Insertion Loss (dB)	I_C = 0	1.0	1.0	1.5	2.1	2.2	-
	Max. SWR		1.7	1.8	2.0	2.0	2.0	-

Typical Attenuation Characteristics

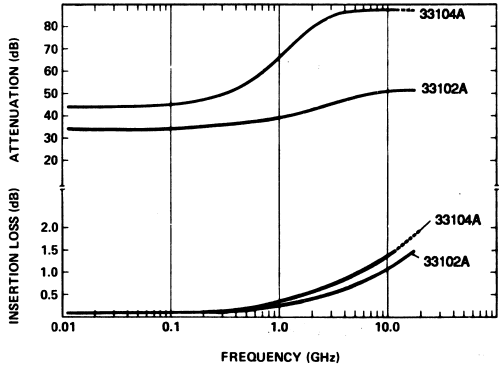


Figure 3. Attenuation and Insertion Loss vs. Frequency, 33100 Series.

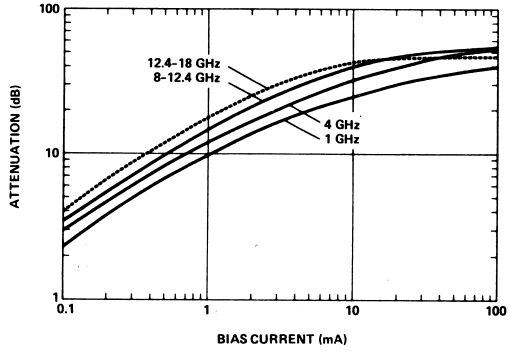


Figure 4. Attenuation vs. Bias with Frequency as a Parameter, 33102A.

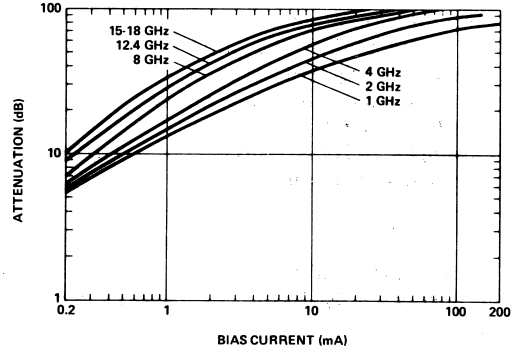


Figure 5. Attenuation vs. Bias with Frequency as a Parameter, 33104A.

RF Power Handling

The breakdown voltage of the diode, the maximum diode power dissipation, the bias state, and the frequency of the RF signal all determine the maximum RF power a switch can handle. Under full isolation conditions, the limiting factor which defines power handling capability is energy storage capacity of the diodes. Under insertion loss conditions the limiting factor which defines power handling capability is diode breakdown voltage.

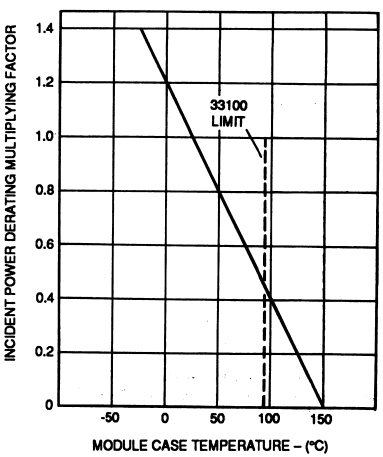


Figure 6. Temperature Derating of Incident Power.

RF Power Handling at T_{CASE} = 25°C

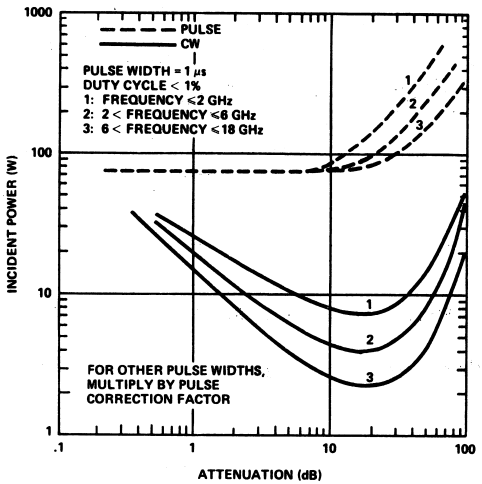


Figure 7. Incident Pulse and CW Power Ratings vs. Attenuation, General Purpose 4-Diode Switches. See Table for Pulse Correction Factor.

Pulse Width Correction Factor

Apply to Incident Power Ratings of Figure 7.

Pulse Width	Correction Factor
0.5 μs	1 .55
2.0 μs	0.62

Typical Phase Shift Characteristics

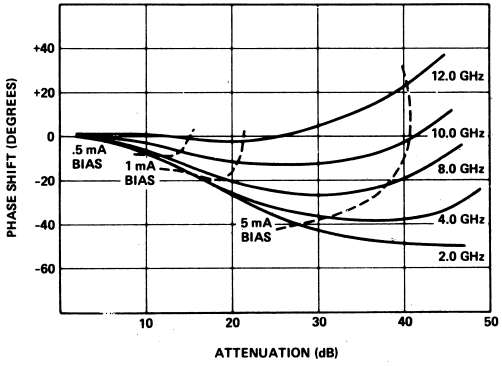


Figure 8. Phase Shift vs. Attenuation, 33102A.

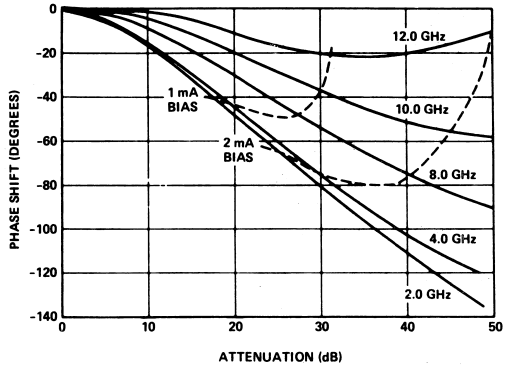


Figure 9. Phase Shift vs. Attenuation, 33104A.

Typical Temperature Effects

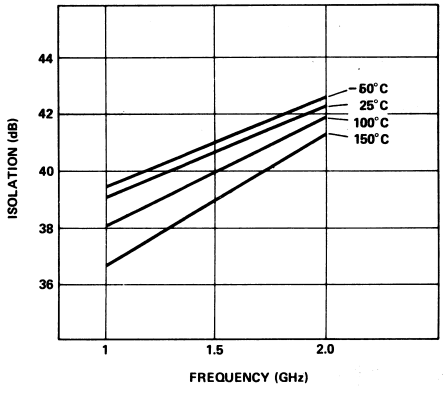


Figure 10. Typical Isolation vs. Frequency with Temperature as a Parameter of Recommended Bias, General Purpose 2-Diode Switches.

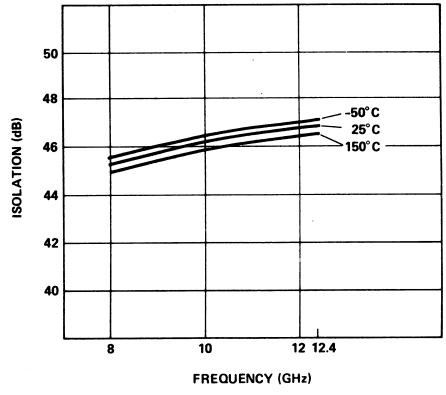


Figure 11. Typical Isolation vs. Frequency with Temperature as a Parameter at Recommended Bias, General Purpose 2-Diode Switches.

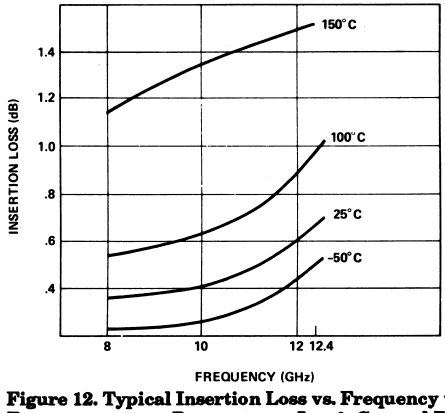


Figure 12. Typical Insertion Loss vs. Frequency with Temperature as a Parameter at $I_C = 0$, General Purpose 2-Diode Switches.

Environmental Capabilities

33100 Series:

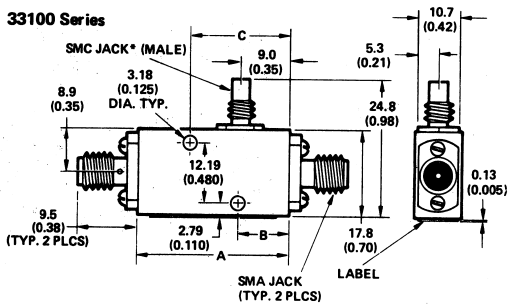
Non-Operating Temperature Cycling: MIL-STD-883, Method 1010, Test Condition B (-55°C to +125°C).

Shock: MIL-STD-883, Method 2002, Test Condition B.

Moisture Resistance: MIL-STD-883, Method 1004.

Salt Atmosphere: (corrosion) MIL-STD-883, Method 1009, Test Condition A.

Outline Drawing



Model	A	B	C
33102	31.8 (1.25)	9.7 ± 0.25 (0.383 ± 0.010)	21.9 ± 0.25 (0.863 ± 0.010)
33104	37.3 (1.47)	12.5 ± 0.25 (0.493 ± 0.010)	24.7 ± 0.25 (0.973 ± 0.010)

*SMA Jack available as Option 001.

Mechanical Specifications

Size: See Outline Drawing

Finish: 33100 Series - Body: painted

Maximum Weight	33100 Series	
	33102A	33104A
Ounces	0.8	1.0
Grams	23	29

HEWLETT PACKARD

Low Loss Microwave SPST Switches and Attenuators DC-18 GHz

Technical Data

33132A
33134A

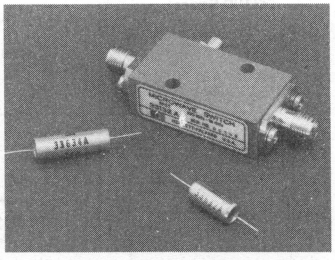
Features

- **Low Insertion Loss**
- **High Isolation**
- **Low SWR**

Description

HP SPST switches utilize PIN diodes in shunt across a 50 ohm transmission line. At microwave frequencies the PIN diode presents a very high impedance at zero bias. With the diode in shunt, the switch is "on" at zero bias (well matched and passing all the incident RF power). Approximately 15 mA of DC current per diode reduces the diode impedance to much less than 50 ohms. Thus the switch is "off" when the diode is heavily forward biased (high mismatch reflecting most of the power back to the source). When switching from the "on" to "off" state, the switch can be set at any attenuation level between those two extremes. The PIN diode allows a smooth and repeatable variation of attenuation with change in bias level.

The HP 33130 series are complete switches with RF connectors, bias circuits, and built in DC returns.



Switch Schematics

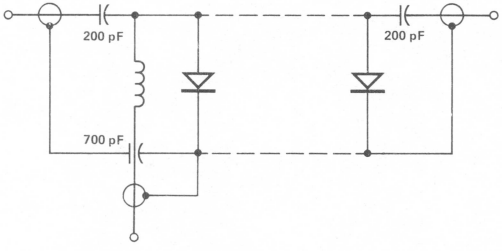


Figure 1. Switch Assembly Schematic. 33130 Series.

Model	Diode Polarity	Number of Diodes
33132A	As Shown	2
33134A	As Shown	4

For further technical details, see HP Application Note 922, "Applications of PIN Diodes."

Electrical Specifications

Maximum Ratings

Parameter	33130 Series
Operating Temperature	-55°C to +95°C
Storage Temperature	-55°C to +125°C
CW RF Power at T_{CASE} = 25°C	2 W (Derate to 0.85 Watt at 95°C)
Pulse RF Power at T_{CASE} = 25°C (1 µs, 0.001 duty cycle)	75 W (Derate to 33 Watt at 95°C)
Control Current/Voltage	See following table

Maximum Control Current/Voltage

Model	Current (mA)	Voltage (V)
33132A	+200	-100 to +1.0
33134A	+400	-100 to +1.0

RF Power Handling

The breakdown voltage of the diode, the maximum diode power dissipation, the bias state, and the frequency of the RF signal all determine the maximum RF power a switch can handle.

Pulse Width Correction Factor

Apply to Incidental Power Ratings of Figure 2.

Pulse Width	Correction Factor
0.5 µs	1 .55
2.0 µs	0.62

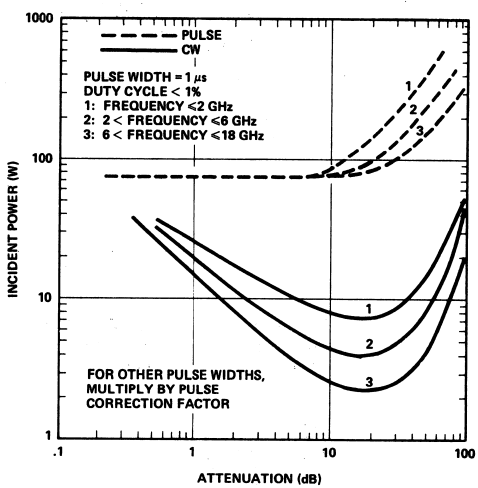


Figure 2. Incident Pulse and CW Power Ratings vs. Attenuation. See Table for Pulse Correction Factor (T_C = 25°C).

Driver Considerations

Driver requirements are dictated by the specific application. When the switch is used as a modulator or attenuator, a current amplifier is required. Suitable integrated circuits can be obtained for either laboratory or OEM applications. The HP 33190B is also suitable as a driver. Typical 10%-90% switching speed is 50 to 100 ns in either off-on or on-off switching.

Noise Figure

Equal to attenuation.

Distortion

Internally generated harmonics are typically 40 dB below the fundamental at input power levels up to 2 watts.

RF to DC Isolation

Isolation of the RF from the control circuit is typically 30 dB.

Electrical Specifications at T_{CASE} = 25°C

33130 Series Switches

Model	Parameter	Conditions	Frequency Range (GHz)					
			0.1-1.0	1.0-2.0	2.0-4.0	4.0-8.0	8.0-12.0	12.0-18.0
33132A	Min. Isolation (dB)[1]	I_C = 30 mA	28	33	37	43	43	43
	Max. Insertion Loss (dB)	V_C = -10 V	1.0	1.0	1.0	1.2	1.4	2.0
	Max. SWR		1.7	1.7	1.7	1.9	1.9	2.2
33134A	Min. Isolation (dB)	I_C = 200 mA	40	60	80	80	80	80
	Max. Insertion Loss (dB)	V_C = -10 V	1.0	1.0	1.4	1.6	1.8	2.5
	Max. SWR		1.7	1.7	2.0	2.0	2.0	2.2

Note:
1. 3-6 dB improvement in isolation in the frequency range 0.1-12 GHz can be realized by increasing bias current to 100 mA.

Typical Characteristics

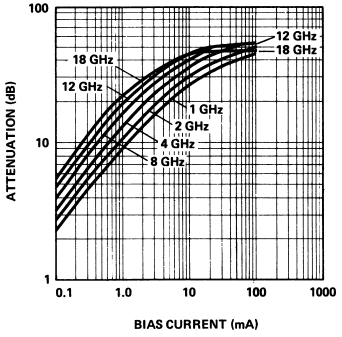


Figure 3. Attenuation of the 33132A as a Function of Bias Current with Frequency as a Parameter.

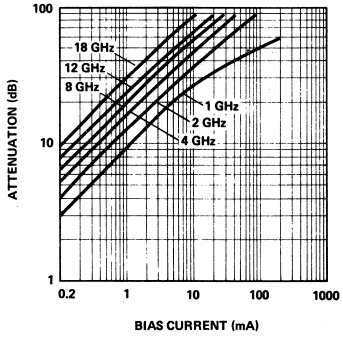


Figure 4. Attenuation of the 33134A as a Function of Bias Current with Frequency as a Parameter.

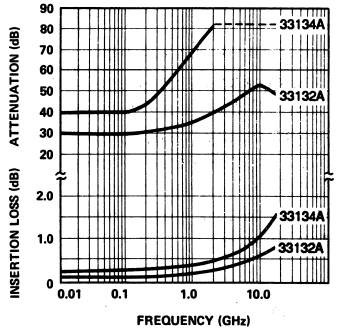


Figure 5. Typical Attenuation and Insertion Loss vs. Frequency.

Ordering Information

33130 Series General Purpose Switches

The HP 33130 series switch is a broadband general purpose switch. The standard unit is supplied with SMA jack (female) RF connectors and SMC jack bias connector. An SMA jack bias connector is available as Option 001.

Mechanical Specifications

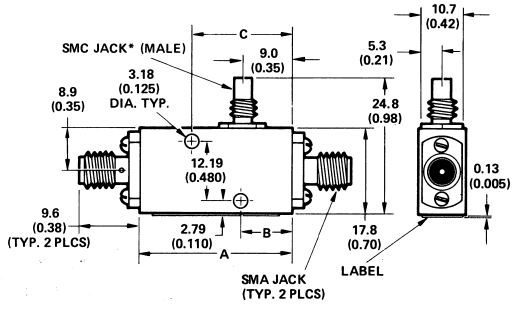
Size: See Outline Drawing.

Finish: 33130 Series - Body: painted.

Maximum Weight	33130 Series	
	33132A	33134A
Ounces	0.8	1.0
Grams	23	29

Outline Drawing

33130 Series



Model	A	B	C
33132A	31.8 (1.25)	9.7 ± 0.25 (0.383 ± 0.010)	21.9 ± 0.25 (0.863 ± 0.010)
33134A	37.3 (1.47)	12.5 ± 0.25 (0.493 ± 0.010)	24.7 ± 0.25 (0.973 ± 0.010)

*SMA Jack available as Option 001.

Environmental Capabilities

33130 Series:

Non-Operating Temperature Cycling: MIL-STD-883, Method 1010, Test Condition B (-55°C to +125°C).

Operating Temperature: MIL-E-5400 Table I, Class 2 (-55°C to +95°C continuous).

Shock: MIL-STD-883 Method 2002, Test Condition B.

Moisture Resistance: MIL-STD-883, Method 1004.

Salt Atmosphere: (corrosion) MIL-STD-883, Method 1009, Test Condition A.

HEWLETT PACKARD

Fast Microwave SPST Switches and Attenuators DC-18 GHz

Technical Data

33142A
33144A

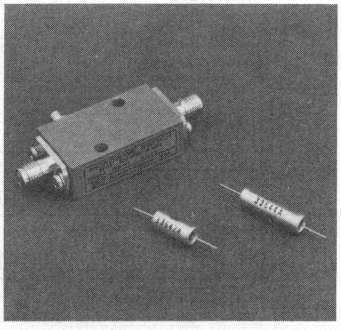
Features

- **5 ns Switching**
- **TTL Compatible Driver**
- **Hermetic**
- **Low Insertion Loss**
- **High Isolation**
- **Low Bias Current**

Description

The HP 33140 Series switches utilize HP's fastest PIN diodes in shunt across a 50 ohm transmission line. The PIN diode presents a very high impedance with reverse bias. With the diode in shunt, the switch is "on" with reverse bias (well matched and passing all the incident RF power). Approximately 10 mA of DC current per diode reduces this impedance to much less than 50 ohms. Thus the switch is "off" when the diode is forward biased (high mismatch reflecting most of the power back to the source). The PIN diode allows a smooth and repeatable variation of attenuation with change in bias level.

The HP 33140 series are complete switches with RF connectors, bias circuit, and built in DC returns. The HP



33190B TTL compatible driver is recommended for use with this switch series.

Switch Schematics

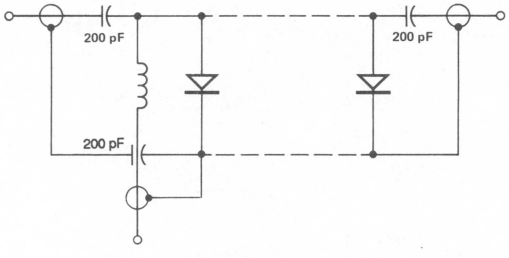


Figure 1. Switch Assembly Schematic. 33140 Series.

Model	Diode Polarity	Number of Diodes
33142A	As Shown	2
33144A	As Shown	4

For further technical details, see HP Application Note 922, "Applications of PIN Diodes."

Maximum Ratings

Parameter	33142A	33144A
Operating Temperature	-55°C to +95°C	
Storage Temperature	-55°C to +125°C	
CW RF Power at T_{CASE} = 25°C	2 W (Derate to 0.85 Watt at 95°C)	
Pulse RF Power at T_{CASE} = 25°C (1 µs 0.001 duty cycle)	75 W (Derate to 7 Watt at 95°C)	
Control Current	+200 mA	+400 mA
Control Voltage	-60 V to +1 V	

Electrical Specifications

RF Power Handling

The breakdown voltage of the diode, the maximum diode power dissipation, the bias state and the frequency of the RF signal all determine the maximum RF power a switch can handle.

Pulse Width Correction Factor

Apply to Incidental Power Ratings of Figure 2.

Pulse Width	Correction Factor
0.5 µs	1 .5
2.0 µs	0.7

Driver Considerations

The recommended driver for the HP 33142A/33144A switch is the HP 33190B Add-on switch Driver. The 33190B requires +5 volts and -12 volts bias power supplies and has TTL compatible input. The 33190B output port connects directly to the SMC control port of the 33142A/33144A switch.

Due to the broad RF bandwidth of the 33142A and 33144A, Video switching spikes from the switch driver will appear at the RF input and output connectors. Depending on the application, video filtering or attenuators may be required to minimize video feed-through and/or ringing on RF pulses due to multiple reflections of video spikes down the RF lines.

Noise Figure

Equal to attenuation.

Distortion

Internally generated harmonics are 20 dB below the fundamental from 1 to 4 GHz at either full isolation or insertion loss for input power levels up to 1/2 watt. Above 4 GHz harmonics are down 40 dB.

RF to DC Isolation

Isolation of the RF from the control circuit is typically 30 dB.

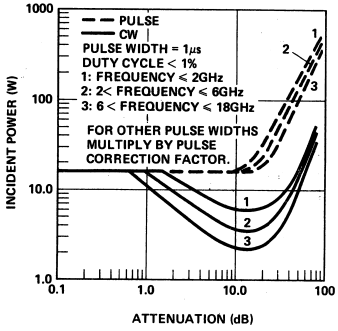
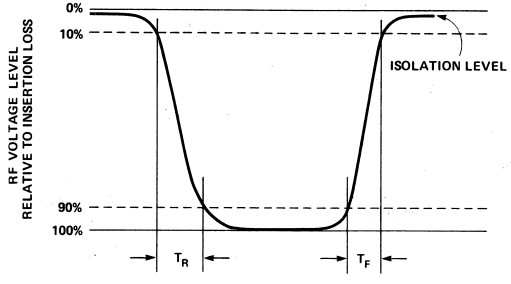


Figure 2. Incident Pulse and CW Power Ratings vs. Attenuation. See Table for Pulse Correction Factor (T_C = 25°C).

Switching Speed at 25°C:

T_R (10% - 90% RF Voltage) = 5 ns Max.

T_F (90% - 10% RF Voltage) = 7 ns Max.



Test Conditions at 10 GHz:

33142A I_C (Off) = 20 mA, V_C (On) = -10 V

33144A I_C (Off = 40 mA, V_C (On) = -10 V

Electrical Specifications at T_{CASE} = 25°C

33140 Series Switches

Model	Parameter	Conditions	Frequency Range (GHz)					
			0.1-1.0	1.0-2.0	2.0-4.0	4.0-8.0	8.0-12.0	12.0-18.0
33142A	Min. Isolation (dB)	I_C = 20 mA	25	30	40	45	45	45
	Max. Insertion Loss (dB)	V_C = -10 V	1.0	1.0	1.0	1.5	1.5	2.5
	Max. SWR		1.7	1.9	1.9	1.9	1.9	2.2
33144A	Min. Isolation (dB)	I_C = 40 mA	35	60	80	80	80	80
	Max. Insertion Loss (dB)	V_C = -10 V	1.0	1.1	1.4	1.7	2.0	3.0
	Max. SWR		1.7	2.0	2.0	2.0	2.0	2.5

Typical Characteristics

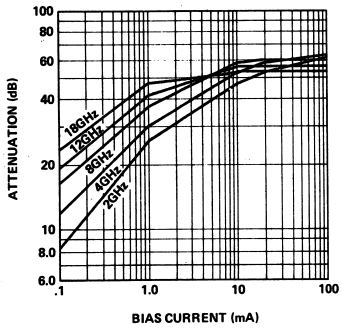


Figure 3. Attenuation of the 33142A as a Function of Bias Current with Frequency as a Parameter.

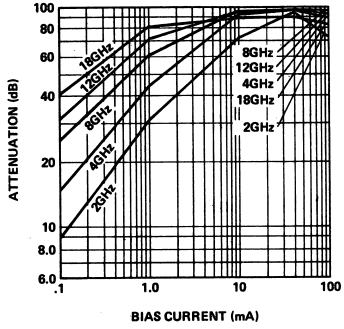


Figure 4. Attenuation of the 33144A as a Function of Bias Current with Frequency as a Parameter.

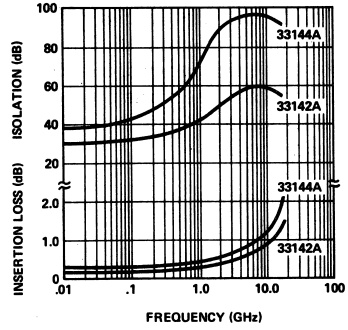


Figure 5. Attenuation and Insertion Loss vs. Frequency.

Ordering Information

The HP 33140 series switch is a broadband fast switch. The standard unit is supplied with SMA jack (female) RF connectors and SMC jack bias connector. An SMA jack bias connector is available as Option 001. An add-on Driver 33190B is also available.

Mechanical Specifications

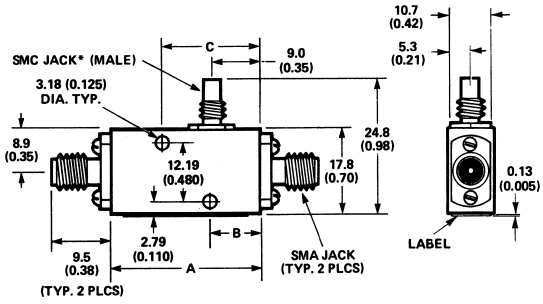
Size: See Outline Drawing.

Finish: 33140 Series - Body: painted.

Maximum Weight	33140 Series	
	33142A	33144A
Ounces	0.8	1.0
Grams	23	29

Outline Drawing

33140 Series



Model	A	B	C
33132A	31.8 (1.25)	9.7 ± 0.25 (0.383 ± 0.010)	21.9 ± 0.25 (0.863 ± 0.010)
33134A	37.3 (1.47)	12.5 ± 0.25 (0.493 ± 0.010)	24.7 ± 0.25 (0.973 ± 0.010)

*SMA Jack available as Option 001.

Environmental Capabilities

33140 Series:

Non-Operating Temperature: MIL-STD-883, Method 1010, Test Condition B (-55°C to +125°C).

Operating Temperature: MIL-E-5400R Table I, Class 2 (-55°C to +95°C continuous).

Shock: MIL-STD-883, Method 2002, Test Condition B.

Moisture Resistance: MIL-STD-883, Method 1004.

Salt Atmosphere: (corrosion) MIL-STD-883, Method 1009 Test Condition A.

HEWLETT PACKARD

Microwave Bias Network 0.1-18 GHz

Technical Data

33150A

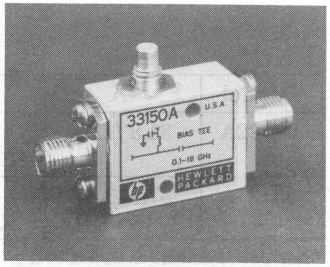
Features

- **Wideband**
- **Low Insertion Loss**
- **High RF to DC Isolation**

Description

The broadband DC return is designed for use as a bias tee or DC return in microwave laboratory and systems applications.

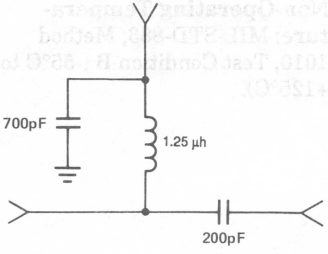
Examples of microwave bias applications include FET or Bipolar transistor amplifiers, SRD multipliers, mixers and detectors, and limiters. This device is ideal for use in device and circuit test setups in the laboratory, where minimum disturbance of the RF circuit is desired.



Maximum Ratings

Parameter	Total
Operating Temperature	-65°C to +95°C
Storage Temperature	-65°C to +125°C
Bias Voltage	100 V
Bias Current	200 mA

Schematic Diagram



Electrical Specifications at T_{CASE} = 25°C

Parameter	Frequency Range (GHz)			
	0.1-3.5	3.5-11	11-18	18-26 Option 002
Maximum Insertion Loss (dB)	0.4	0.6	1.1	1.5
Maximum SWR	1.5:1	1.5:1	1.8:1	2.8:1
Maximum DC Bias Resistance (Ω)	4.0			

Ordering Information

The 33150 is a broadband bias network. The standard unit is supplied with SMA jack (female), RF connectors, and SMC jack (male) bias connector. An SMA jack bias connector is available as Option 001.

Mechanical Specifications

Body: Alodined aluminum MIL-C-5541.
Maximum Weight: 23 grams (0.8 ounces)

Environmental Ratings

Non-Operating Temperature Cycling: MIL-STD-883, Method 1010, Test Condition B (-55°C to +125°C).
Shock: MIL-STD-883. Method 2002, Test Condition B, (0.5 ms, 1500 G).
Moisture Resistance: MIL-STD-883, Method 1004.

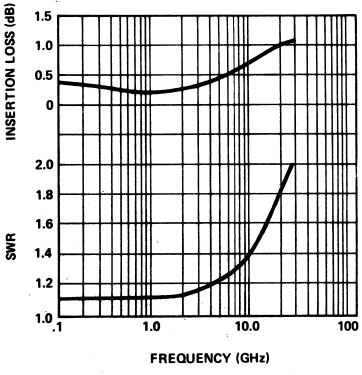


Figure 1. Typical Insertion Loss and SWR.

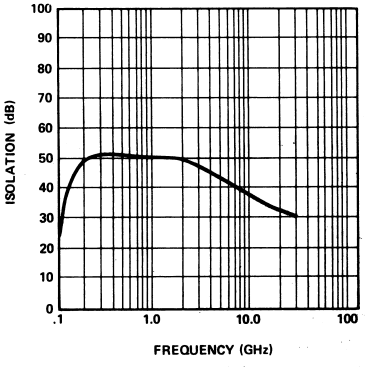
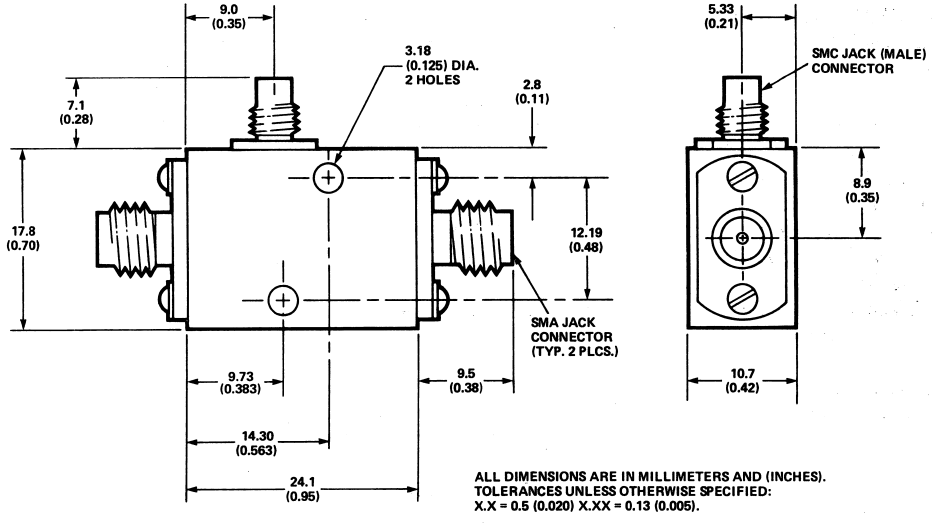


Figure 2. Typical RF to DC Isolation

Outline Drawing



HEWLETT PACKARD

Switch Driver for Fast SPST PIN Diode Switches

Technical Data

33190B

Features

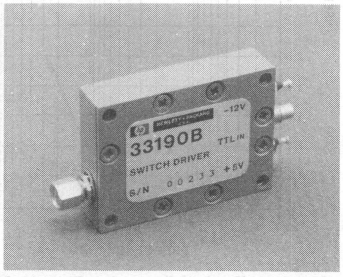
- **TTL Compatible Input**
- **High Speed**

Description

The HP 33190B is a driver designed for the HP 33140 Fast SPST switch series. The fully TTL compatible driver simplifies high speed switching by converting the TTL inputs to the required switching bias levels. The HP 33190B requires +5 V and -12 V bias supplies. Its output connector mates directly with the SMC control port connector on the HP 33140 series switches.

Applications

To achieve nanosecond switching times with diode switches, a specially shaped switching impulse is required to compensate for PIN diode minority carrier lifetime. Since minority carrier lifetime is a diode parameter and varies greatly for different classes of diodes, drivers are designed to optimize switching time for a specific diode/switch. The HP 33190B is designed specifically for the HP 33142A and 33144A model switches, but can be used to improve switching time of any SPST diode switch.



Maximum Ratings

Operating Temperature ..... -55°C to 95°C
Storage Temperature .....-55°C to 125°C

Electrical Specifications at T_{CASE} = 25°C

Driver Input Control Levels

Switch Mode[1]	Logic State	Input Voltage	Max. Input Current
Minimum Insertion Loss	0	0-0.8 V	4 mA Sink
Isolation	1	2.5 V- Min.	50 µA Source[2]

Notes:
1. Inverted for 33102A/33104A.
2. Increases for V_{IN} greater than 2.5 V. Input impedance approximately 1 KΩ for V_{IN} greater than 2.5 V.

Bias Supply Voltages:

+5 V ± 5%
-12 V ±5%

Bias Supply Currents (Maximum)

HP Switch Type	+5 V	-12 V
33142A/33144A 33132A/33134A	80 mA	10 mA
33102A/33104A	10 mA	80 mA

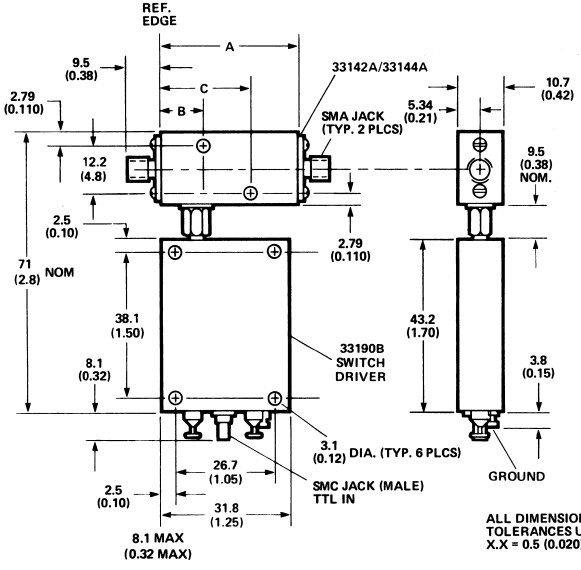
Steady State Output Levels

Logic State	Typical Open Circuit Voltage	Minimum Available Output Current
0	-10 V	40 mA
1	+3 V	40 mA

Switching Considerations

Switch Being Driven	T_R (ns)	T_F (ns)	T_{DR} (ns)	T_{DF} (ns)
33142A/33144A (Max.)	5	7	26 (Typ.)	30 (Typ.)
33102A/33104A (Typ.)	100	20	-	-
33132A/33134A (Typ.)	150	50	-	-

Outline Drawing



33142A	33144A
A 31.8 (1.25)	37.3 (1.47)
B 9.7 (0.38)	12.5 (0.49)
C 21.9 (0.86)	24.7 (0.97)

ALL DIMENSIONS IN MILLIMETERS AND (INCHES).
TOLERANCES UNLESS OTHERWISE SPECIFIED:
X.X = 0.5 (0.020) X.XX = 0.13 (0.005)

Environmental Capabilities

Non-Operating Temperature Cycling: MIL-STD-883, Method 1010, Test Condition B (-65°C to +125°C).

Operating Temperature: MIL-E-5400, Table 1, Class 2 (-65°C to +95°C continuous).

Shock: MIL-STD-883, Method 2002, Test Condition B.

Moisture Resistance: MIL-STD-883, Method 1004.

Salt Atmosphere: (corrosion) MIL-STD-883, Method 1009, Test Condition A.

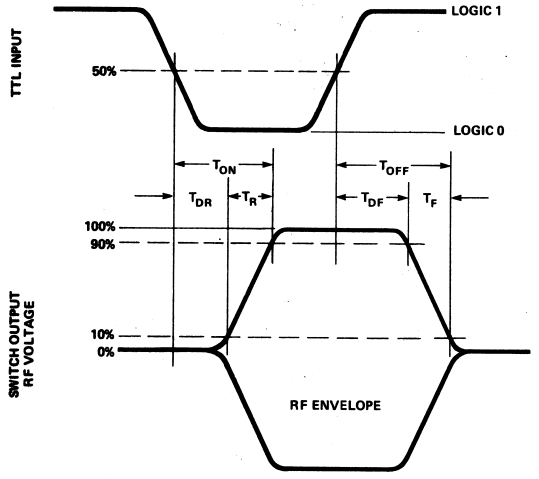


Figure 1. Switching Definitions.

Definitions (Figure 1.)

T_R = 10% to 90% Switch RF voltage.

T_F = 90% to 10% Switch RF voltage.

T_{DR} = Time delay from 50% driver input voltage to 10% switch RF output voltage.

T_{DF} = Time delay from 50% driver input voltage to 90% switch RF output voltage.

$T_{ON} = T_{DR} + T_R$

$T_{OFF} = T_{DF} + T_F$

HEWLETT PACKARD

Comb Generators

Reliability Data

Description

For applications requiring component reliability estimation, Hewlett-Packard provides reliability data for all families of devices. Data is compiled from reliability tests to demonstrate that a product meets design criteria. The data on this sheet represents the latest review of accumulated test results.

Reliability

Each design is tested for performance under varying conditions of temperature, humidity, vibration, and mechanical shock. Sample production units undergo life testing to demonstrate predicted MTTF for selected product designs.

The following MTTF (Mean Time To Failure) hours have been calculated from the failure rate predictions found in MIL-HDBK-217D, Reliability Prediction of Electronic Equipment. The Hybrid Microcircuit failure rate model was used:

$$\lambda_P = \{\Sigma N_C \lambda_C \Pi_G + (N_R \lambda_R + \Sigma N_I \lambda_I + \lambda_S) \Pi_F \Pi_E\} \Pi_Q \Pi_D \text{ (failures/}10^6\text{ hour)}$$

where:

$MTTF = 1/\lambda_P$

$\Sigma N_C \lambda_C \Pi_G$ is the sum of the adjusted failure rates for the active components, packaged resistors, and capacitors in the hybrid

N_C is the number of each particular component

λ_C is the component failure rate

Π_G is the die correction factor

$N_R \lambda_R$ is the number of (N_R) and failure rate contribution (λ_R) of the chip or substrate resistors

$\Sigma N_I \lambda_I$ is the sum of the failure rate contributions of the interconnections (λ_I)

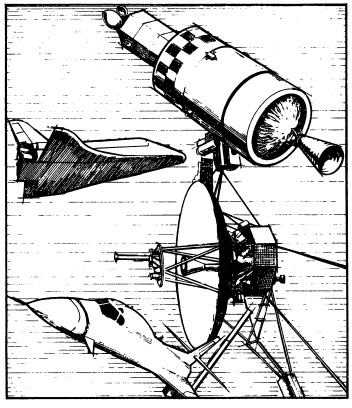
λ_S is the failure rate contribution of the hybrid package

Π_E is the environmental factor for the film resistors, interconnections and package

Π_Q is the quality factor

Π_D is the density factor

Π_F is the circuit function factor



Environmental

Two common environments were chosen for the following MTTF predictions:

Ground, Benign (GB) at 25°C ambient temperature

—Nonmobile, laboratory environment readily accessible to maintenance; includes laboratory instruments and test equipment, medical electronic equipment, business and scientific computer complexes.

Ground Fixed (GF) at 40°C ambient temperature

—Conditions less than ideal such as installation in permanent racks with adequate cooling air and possible installation in unheated buildings; includes permanent installation of air traffic control, radar and communications facilities, and missile silo ground support equipment.

MTTF Summary

Part Number	Environment	Ambient Temperature	MTTF Hours
33002A	G_F	50°C	4×10^6
33002B	G_B	25°C	14×10^6
33002B	G_F	50°C	5×10^6
33003A	G_F	50°C	4×10^6
33003B	G_B	25°C	14×10^6
33003B	G_F	50°C	5×10^6
33004A	G_F	50°C	4×10^6
33004B	G_B	25°C	14×10^6
33004B	G_F	50°C	5×10^6
33005C	G_F	50°C	4×10^6
33005D	G_B	25°C	14×10^6
33005D	G_F	50°C	5×10^6

HEWLETT PACKARD

Switches, Switch Drivers

Reliability Data

Description

For applications requiring component reliability estimation, Hewlett-Packard provides reliability data for the High Speed Circuit devices. Data is compiled from reliability tests to demonstrate that a product meets design criteria. The data on this sheet represents the latest review of accumulated test results.

Reliability

Each design is tested for performance under varying conditions of temperature, humidity, vibration, and mechanical shock. Sample production units undergo life testing to demonstrate predicted MTTF for selected product designs.

The following MTTF (Mean Time To Failure) hours have been calculated from the failure rate predictions found in MIL-HDBK-217D. Reliability Prediction of Electronic Equipment. The Hybrid Microcircuit failure rate model was used:

$$\lambda_P = \{\Sigma N_C \lambda_C \Pi_G + (N_R \lambda_R + \Sigma N_I \lambda_I + \lambda_S) \Pi_F \Pi_E\} \Pi_Q \Pi_D \text{ (failures/}10^6\text{ hour)}$$

where:

$MTTF = 1/\lambda_P$

$\Sigma N_C \lambda_C \Pi_G$ is the sum of the adjusted failure rates for the active components, packaged resistors, and capacitors in the hybrid

N_C is the number of each particular component

λ_C is the component failure rate

Π_G is the die correction factor

$N_R \lambda_R$ is the number of (N_R) and failure rate contribution (λ_R) of the chip or substrate resistors

$\Sigma N_I \lambda_I$ is the sum of the failure rate contributions of the interconnections (λ_I)

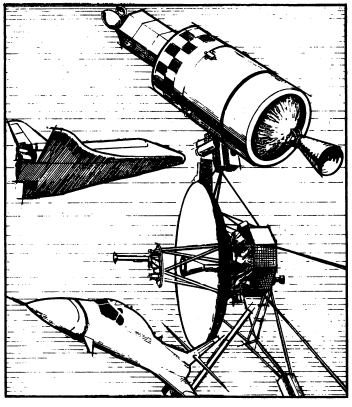
λ_S is the failure rate contribution of the hybrid package

Π_E is the environmental factor for the film resistors, interconnections and package

Π_Q is the quality factor

Π_D is the density factor

Π_F is the circuit function factor



Environmental

Two common environments were chosen for the following MTTF predictions:

Ground, Benign (GB) at 25°C temperature

—Nonmobile, laboratory environment readily accessible to maintenance, includes laboratory instruments and test equipment, medical electronic equipment, business and scientific computer complexes.

Ground Fixed (GF) at 40°C ambient temperature

—Conditions less than ideal such as installation in permanent racks with adequate cooling air and possible installation in unheated buildings, includes permanent installation of air traffic control, radar and communications facilities, and missile silo ground support equipment.

Product Family	Part Number	Environment	Ambient Temperature °C	MTTF Hours x 10^6
General Purpose Microwave Switch	33016C	GB	25	16
	33016C	GF	40	4
	33102A	GB	25	23
	33102A	GF	40	6
	33104A	GB	25	14
	33104A	GF	40	3
SPST Low Loss Microwave Switch	33132A	GB	25	23
	33132A	GF	40	6
	33134A	GB	25	14
	33134A	GF	40	3
SPST Fast Microwave Switch	33142A	GB	25	23
	33142A	GF	40	6
	33144A	GB	25	14
	33144A	GF	40	3
Switch Driver	33190B	GB	25	40
		GF	40	9

HEWLETT PACKARD

Broadband DC Return

Reliability Data

Description

For applications requiring component reliability estimation, Hewlett-Packard provides reliability data for all families of devices. Data is compiled from reliability tests to demonstrate that a product meets design criteria. The data on this sheet represents the latest review of accumulated test results.

Reliability

Each design is tested for performance under varying conditions of temperature, humidity, vibration, and mechanical shock. Sample production units undergo life testing to demonstrate predicted MTTF for selected product designs.

The following MTTF (Mean Time To Failure) hours have been calculated from the failure rate predictions found in MIL-HDBK-217D, Reliability Prediction of Electronic Equipment.

The Hybrid Microcircuit failure rate model was used:

$$\lambda_P = \{\Sigma N_C \lambda_C \Pi_G + (N_R \lambda_R + \Sigma N_I \lambda_I + \lambda_S) \Pi_F \Pi_E\} \Pi_Q \Pi_D \text{ (failures/}10^6\text{ hour)}$$

where:

$MTTF = 1/\lambda_P$

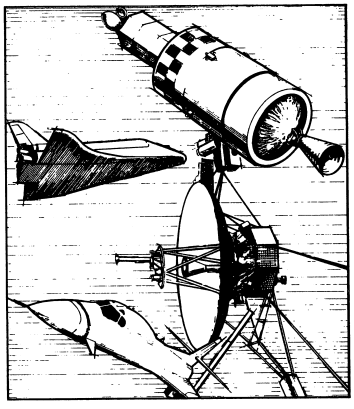
$\Sigma N_C \lambda_C \Pi_G$ is the sum of the adjusted failure rates for the active components, packaged resistors, and capacitors in the hybrid

N_C is the number of each particular component

λ_C is the component failure rate

Π_G is the die correction factor

$N_R \lambda_R$ is the number of (N_R) and failure rate contribution (λ_R) of the chip or substrate resistors



$\Sigma N_I \lambda_I$ is the sum of the failure rate contributions of the interconnections (λ_I)

λ_S is the failure rate contribution of the hybrid package

Π_E is the environmental factor for the film resistors, interconnections, and package

Π_Q is the quality factor

Π_D is the density factor

Π_F is the circuit function factor

MTTF Summary

Product Family	Part Number	Environment	Ambient Temperature, °C	MTTF Hours x 10^6
Microwave Bias Network	33150A	GB	25	54
	33150A	GF	40	22

Communications Amplifier Products



Communications Amplifier Products

Cellular Base Station Amplifiers

Analog: Hewlett-Packard offers a line of Cellular Analog Base Station amplifiers with output power up to 45 Watts and covering both North American and International frequency bands (869-894 & 917-950 MHz). The most popular model includes computer-controlled dynamic power output.

Digital: HP also offers advanced linear power amplifiers for Digital Cellular Base Stations and for DCS-1800 and GSM applications. Intermod performance of minus 30-dBc at power levels of 45 Watts are typical at 900 and 1800 MHz.

Cellular base station amplifier equipment is sold to OEMs where some level of product customization is typically required.

C and KU Band Very Small Aperture Terminal (VSAT) Transmitter

Introduction

The Transmitter assembly forms the heart of the low power satellite uplink for data communications. The RF Module is incorporated with other electronics in a common housing designed for outdoor environments. It accepts baseband data to direct modulate the carrier or a lower frequency modulated carrier (i.e.: VHF, UHF, or other carrier frequency) which is multiplied and/or up-converted.

Subsystem Description

A phase locked frequency agile source is typically included. This source can be multiplied and/or up-converted to the desired carrier frequency.

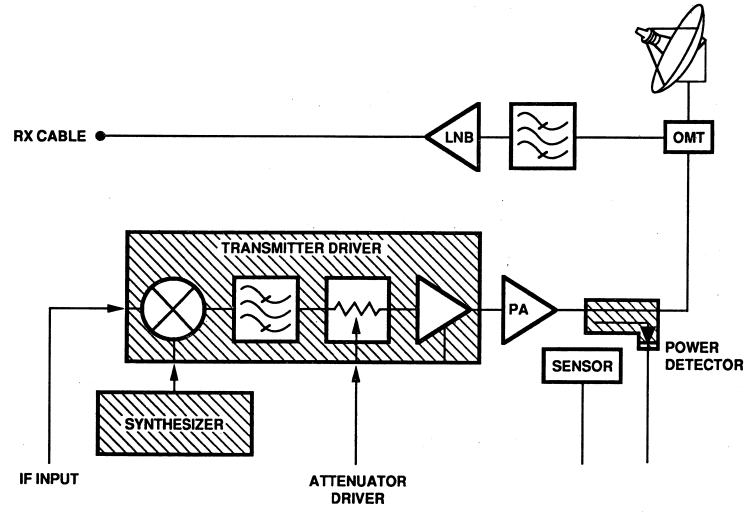
RF Output Power

After modulation the signal is amplified to a level of 0.5 to 2 Watts. Level control is provided after modulation in order to maintain near constant modulation characteristics over wide output power ranges. Filtering is used throughout the chain to provide minimum spurious levels and reduce transmitted noise in the receive bands. The output stages utilize discrete GaAs power FETs and MMIC power FETs.

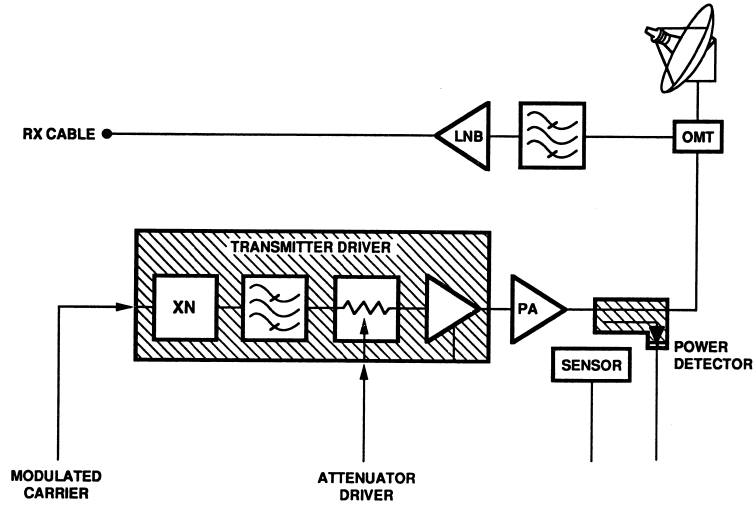
The following block diagrams provide the various modulation schemes utilized in HP's designs.

Communications Amplifier Products

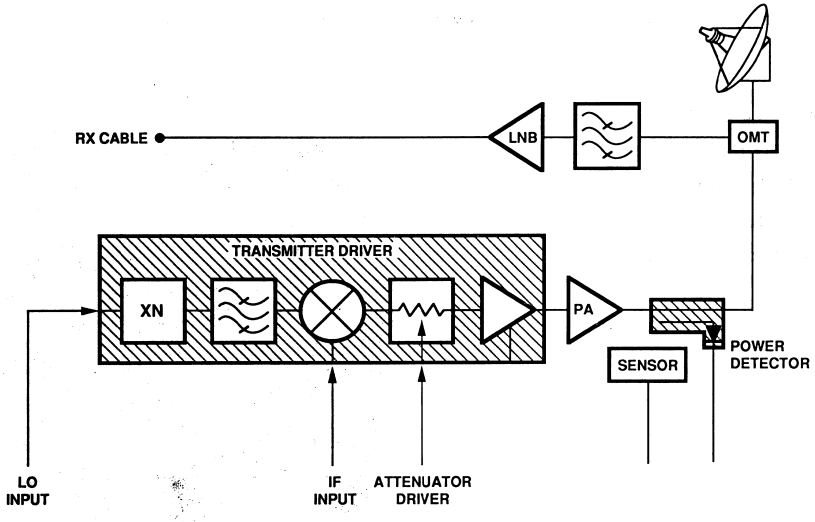
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Case Drawings 12-12–13
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3.7 to 13.25 GHz Frequency Range
Case Drawings 12-28–29



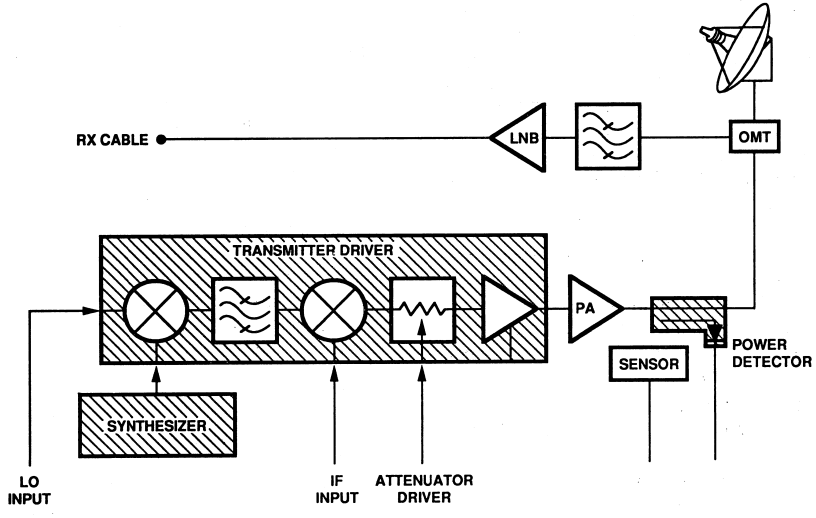
MIXER UPCONVERTER



MULTIPLIER UPCONVERTER



MULTIPLIER UPCONVERTER & DIRECT MODULATOR



MIXER UPCONVERTER & DIRECT MODULATOR

Features

- **150 dB Receiver Isolation**
- **50 to 70 dB Receiver Gain**
- **4 LO Frequency Options**
- **Noise Figures to 1.9 dB**
- **Transmit Powers to +46.0 dBm**
- **1.5:1 VSWR**
- **Reverse Polarity Voltage Protected**

Inmarsat RF Transceiver



Description

The Hewlett-Packard Inmarsat RF Transceiver is an integrated uplink transmitter/upconverter with a power amplifier and downlink receiver front-end for use in shipboard and land-based earth stations for the worldwide Inmarsat telecommunications satellite system. This subsystem operates in the L-band, transmitting signals with +45.0 dBm power output in the 1636.5 to 1645.0 MHz frequency range while simultaneously receiving in the 1535.0 to 1543.5 MHz band. It interfaces with data and voice communications equipment using balanced-voltage digital interface circuitry compliant to EIA Standard RS-422. The assembly connects to the antenna via a single cable which carries both the transmit and receive signals.

While units can be custom designed to operate on many combinations of TX-IF input, RX-IF output and UHF local oscillator frequencies, the standard unit can operate on any one of the four user supplied LO frequencies which predetermines any of three sets of IF input and output frequency bands as detailed in the specifications.

Four functional groups comprise the subassembly (Figure 1): a diplexer, a receiver preamplifier, a frequency translator and a transmitter power amplifier. The translator includes a local oscillator frequency multiplier, a receiver RF-IF downconverter and a transmitter IF-RF upconverter.

The diplexer provides in excess of 20 dB of isolation at each filter port and more than 60 dB of rejection at the band edge of the other filter. The receiver preamplifier consists of a balanced 1.0 dB noise figure, high gain GaAs FET preamplifier followed by a bandpass filter tuned to the receive band.

Frequency translation begins with LO frequency multiplication accomplished by taking the signal from the UHF phase locked local oscillator, multiplying it to the proper system LO frequency (1330, 1460 or 1680 MHz) and dividing it into two equal signals to be used in the upconversion and downconversion sections. The use of narrowband LO frequency bandpass filters assures high rejection of the oscillator input signal and its other multiplication products.

The downconverter is comprised of a double-balanced mixer, two low-pass filters, and two stages of gain. The low-pass filter at the IF port of the mixer rejects any residual external oscillator signals, undesirable multiplication products and any local oscillator signals that may appear there, while the low-pass filter at the output of the downconverter rejects any out of band mixing products.

The upconverter consists of a double balanced mixer, several gain stages, a filter and a limiter. The transmitter power amplifier RF section requires a constant input level which is provided by the limiting circuit. A narrow bandpass filter rejects undesired multiplication products leaking through the mixer and limits the noise power transmitted within the receiver RF band.

The transmitter power amplifier, housed in a separate aluminum case, consists of a class A input stage followed by two single-ended class C stages followed by a balanced class C stage and a high power isolator to provide +42.5 to +46.0 dBm (17.8 to 40.0 watts) of RF output power. The amplifier includes an EIA Standard RS-422 compatible control module which keys the RF power on and off, monitors the RF output power for failure annunciation, and monitors the internal case temperature for thermal shutdown annunciation.

Designed for Reliability

Most microwave transistors used in the Inmarsat transceiver are designed and built in Hewlett-Packard's own facility in Santa Clara, CA in close cooperation with the designers and their particular needs. This assures the best possible performance and reliability by allowing the designers to take full advantage of optimally designed transistors, plus it assures a continuing flow of virtually identical transistors throughout the manufacturing stages of the unit.

All steps in the processing of the transistors are traceable down to the wafer level, and all manufacturing steps are documented for process control and to provide information for a comprehensive in-house failure analysis program. Components purchased from outside vendors are subjected to rigorous incoming inspection and only vendors with a proven record of consistent quality and reliability are selected.

Packaging

The Inmarsat transceiver is environmentally sealed in a cast aluminum housing, designed for maximum flexibility to enable it to be easily adapted to the customer's mounting requirements without expensive customizing costs. It is suitable for either antenna or base mounting, provided that it is adequately cooled by heat sinking and/or cooling fins. If the application requires, the transmitter power amplifier section (fig. 1) may be located remotely from the balance of the system. Slight additional cable losses may be encountered in this configuration.

Specifications

Receiver Section

RF Input

Frequency Range ..... 1535.0-1543.5 MHz
Gain ..... 53 dB
  Optional Gain Available ..... 50-70 dB
Gain Flatness ..... ±1 dB
Gain Variation (under all conditions) ..... ±5 dB
Noise Figure
  +25°C ..... 1.9 dB to 2.7 dB
  +70°C ..... 2.4 dB to 3.2 dB
Bandwidth
  3 dB ..... 20 MHz, Min.
  60 dB ..... 100 MHz, Max.
VSWR (50 ohms) ..... 1.5:1, Max.

IF Output

Frequency Range
  System LO=1330 MHz ..... 205.0–213.5 MHz
  System LO=1460 MHz ..... 75.0–83.5 MHz
  System LO=1680 MHz ..... 136.5–145.0 MHz
Power Output, Min.
  (1 dB Gain Compression) ..... +5 dBm
Third Order
  Intercept Point, Min. ..... +15 dBm
VSWR (50 ohms) ..... 2.0:1, Max.
  (Optional, 75 ohms) ..... 2.0:1, Max.
Spurious and Noise Density Outputs in a 4 kHz BW.
  Referenced to RF input
  (75.0-83.5 MHz, 136.5-145.0 MHz or
  205.0-213.5 MHz) ..... –150 dBm, Max.

Local Oscillator Section

LO Multiplication Factors and Input Power Range (standard)

Input LO, MHz	190	210	292	365
Multiplication Factor	7	8	5	4
System LO, MHz	1330	1680	1460	1460

Input Power Window ..... 10 dB
Extended power ranges are optionally available.
VSWR (50 ohms) ..... 2.0:1, Max.
  (Optional, 75 ohms) ..... 2.0:1, Max.

Transmitter Section

IF Input

Frequency Range
  System LO=1330 MHz ..... 306.5–315.0 MHz
  System LO=1460 MHz ..... 176.5–185.0 MHz
  System LO=1680 MHz ..... 35.0–43.5 MHz
VSWR (50 ohms) ..... 2.0:1, Max.
  (optional, 75 ohms) ..... 2.0:1, Max.
Input Power Window for Any
  IF Input Frequency Range ..... –5 to –15 dBm

RF Output

Frequency Range ..... 1636.5–1645.0 MHz
Power Output (100% duty cycle) ..... +42.5– +46.0 dBm[1]
Power Supply Voltage ..... 27.0–29.0 V[1]
  Tolerance ..... ±0.1 V[1]
Power Supply Current ..... 3.75–6.0 A[1]
VSWR (50 ohms) ..... 1.5:1, Max.
Harmonics ..... –60 dBc, Min.
Note 1: See the following page.

Spurious Signals and Noise Density shall fall below the spectrum envelope defined by the following points.

Frequency, MHz	Power in a 4 kHz Bandwidth, dBm
1535 and below	–55
1622.5	–47
1636.5–1645.0	–17
1660.0	–47
1750 and above	–55

Note 1: The customer may specify a ±0.75 dB power output window between +42.5 and +46.0 dBm which will then occur, under all operating conditions, at an Hewlett-Packard specified supply voltage between 27.0 and 29.0 Volts (±0.1 V) which then determines the maximum current specification.

Transmitter Interface

Transmit Control (Input)
Logic signals control the RF power through the amplifier to suppress or activate (key) power output transmission.

Transmit Monitor (Output)
This signal indicates whether RF signal transmission is occurring.

Thermal Alarm (Output)
Automatically disables the power amplifier when the internal temperature exceeds +80° ±4°C and turns it on again when it cools to +70° ±4°C. The status from the temperature sensing circuit is available as an output signal.

Load Protection
The unit will not be damaged by sustained operation with any passive load.

Power Requirements

+16 VDC Power
Regulation ..... ±1.5%
Current ..... 1.1 amperes, Max.

+27 to +29 VDC Power
Regulation ..... ±0.35%
Current ..... 3.75 to 6.0 amperes, Max.

Protection
The unit will not be damaged by reverse polarity connection of either power supply.

Environmental

Case Temperature
Operating ..... –35° to +70°C
Non-operating ..... –55° to +125°C

Relative Humidity 95%

Interface

All interface to below decks equipment is defined by EIA Standard RS-422.

Weight ..... 16 lb., 6 oz., Typ.

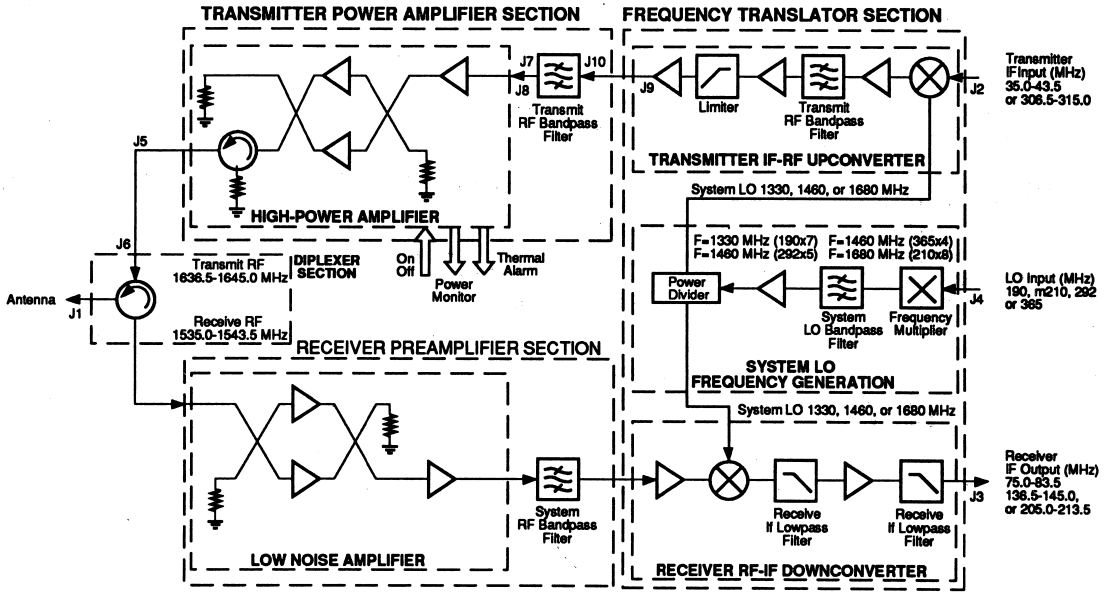
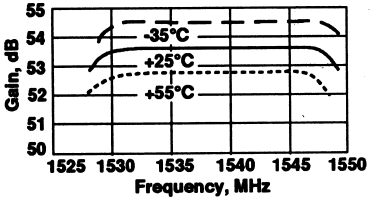


Figure 1

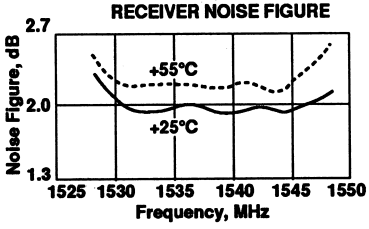
Performance Curves

Typical Performance

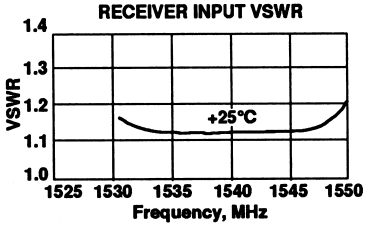
RECEIVER GAIN



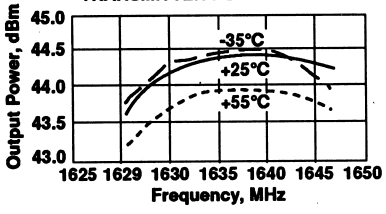
RECEIVER NOISE FIGURE



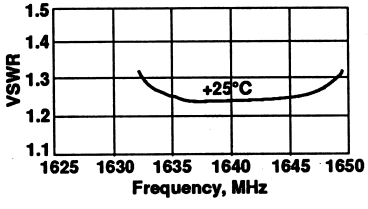
RECEIVER INPUT VSWR



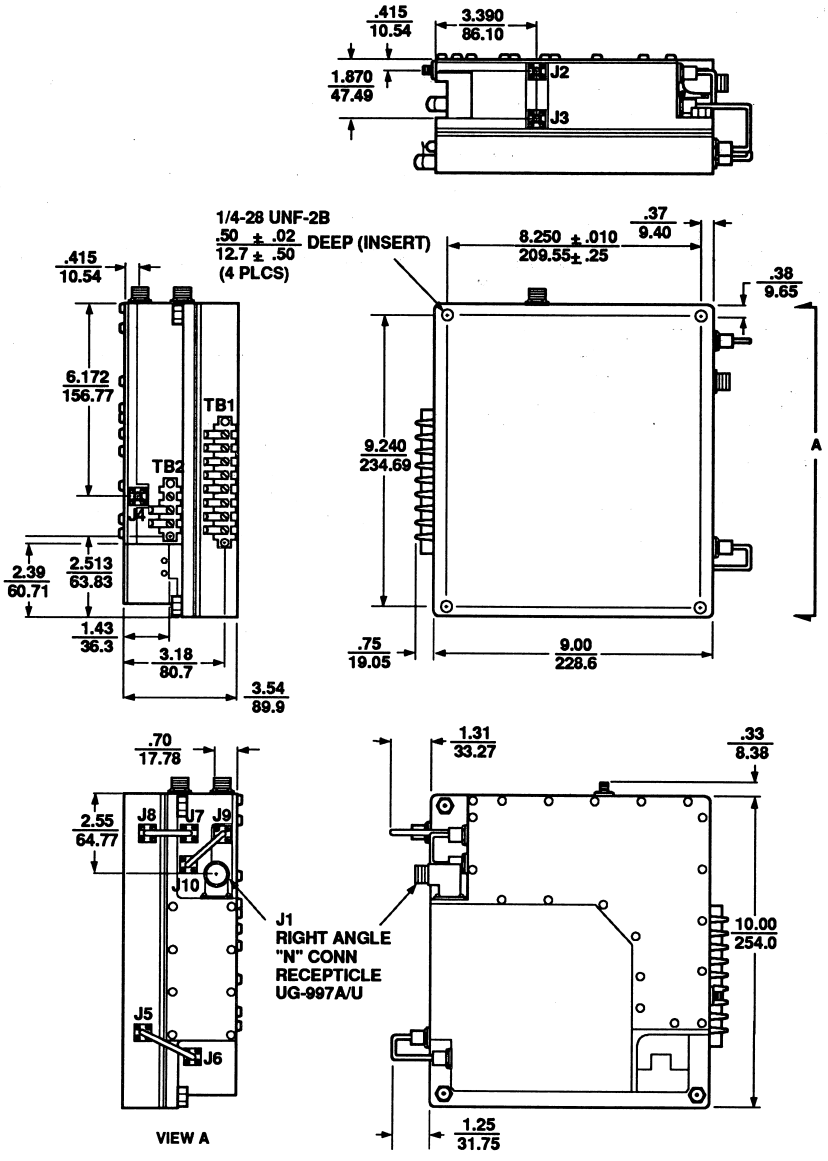
TRANSMITTER POWER OUTPUT



TRANSMITTER OUTPUT VSWR



Case Drawing



J1 ANTENNA	J6 DIPLEXER TRANSMITTER INPUT
J2 TRANSMITTER IF INPUT	J7 TRANSMITTER INPUT-FILTER OUTPUT
J3 RECEIVER IF OUTPUT	J8 POWER AMP INPUT
J4 UHF LOCAL OSCILLATOR INPUT	J9 UPCONVERTER OUTPUT
J5 POWER AMP OUTPUT	J10 TRANSMITTER INPUT-FILTER INPUT

NOTES (UNLESS OTHERWISE SPECIFIED):

1. DIMENSIONS ARE SPECIFIED IN IN / MM
2. TOLERANCES: .XX ± .02
   .XXX ± 0.5
3. COAXIAL CONNECTORS ARE SMA-F

Features

- High Linearity
- High Gain
- Low/No Maintenance
- Long Life
- Fail Soft
- C Band

ACU-64100 RM



Description

Hewlett-Packard's C Band satellite uplink power amplifiers are designed to provide exceptionally high linearity. They may be used to retrofit SCPC, QPSK or other multiple carrier satellite uplinks now using TWTs with stringent third order requirements that normally preclude the use of a solid state amplifier.

The ACU-64100 is a 10 watt, 6 GHz amplifier with integral heatsink that may be conveniently mounted for use in a wide range of systems applications. The ACU-64100 RM (10 watt) and AWP-64200 (20 watt) amplifiers are installed in standard 19 inch rack-mountable cabinets with cooling fans that eliminate the need for an external thermal conduction path. Both versions are designed for retrofitting TWTs in existing applications, however they may also be used by equipment manufacturers whenever a high reliability, low maintenance unit is required.

ACU/AWP—High Power Satellite Communications Uplink

Guaranteed Specifications @ 25°C Case Temperature

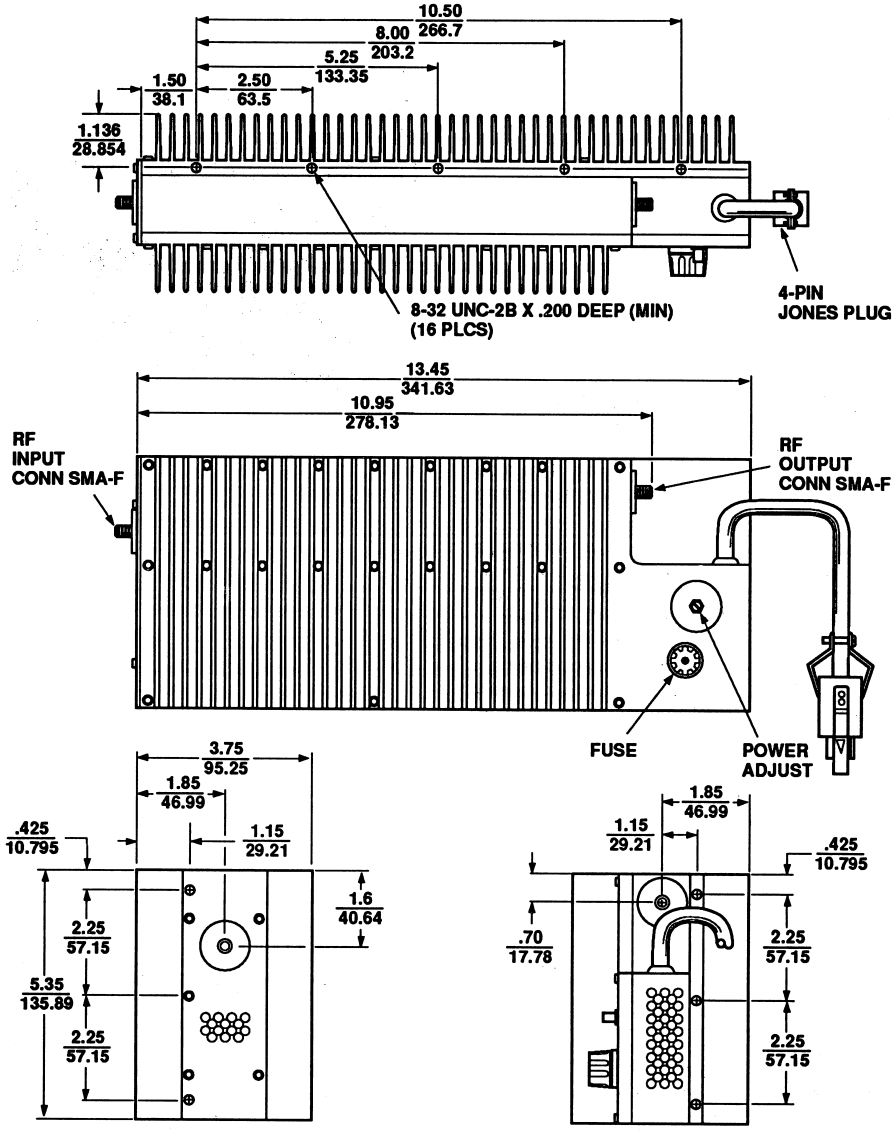
Model	Frequency Range (GHz)	Gain (dB)	Output Power[1] (watts/dBm)	Noise Figure[2] (dB) Max.	AM/PM Conver (°/dB) @ Max. Output Typ./Max.	Output Gain Variation 0° to +50° C (dB) Max.	Output Power Flatness (dB) P-P	Third Order Intercept Point (3 Tone)	Harmonics (dBc) Max.	Spurious (dBc) Max.	Return Loss (dB) Min. Input	Return Loss (dB) Min. Output	DC Input Power[3] (watts) Typ.
ACU-64100	5.925-6.425	45-55[5]	10/+40	10	1.5/2	±3	±.25[6]	48	-53	-60	18	18	110[7]
ACU-64100RM[4]	5.925-6.425	43-53[5]	10/+40	10	1.5/2	±1	±.25[6]	48	-50	-60	18	14	125
AWP-64101RM[4]	5.925-6.425	43-53[5]	10/+40	10	1.5/2	±1	±.25[6]	48	-50	-60	18	14	125
AWP-64200RM[4]	5.925-6.425	45-55[5]	20/+43[8]	10	1.5/2	±1	±.25[6]	50	-53	-60	18	14	240

Notes:

1. @ 1 dB gain compression
2. @ maximum gain
3. -24 or -48 VDC; 115 or 230 VAC
4. Rack-mountable, 19-inch cabinet
5. 10 dB adjustable input attenuator
6. Peak-to-peak across any 40 MHz band at rated output power
7. +15 V option available
8. saturated power output

Case Drawing
ACU-64100

C Band Uplink Power Amplifier

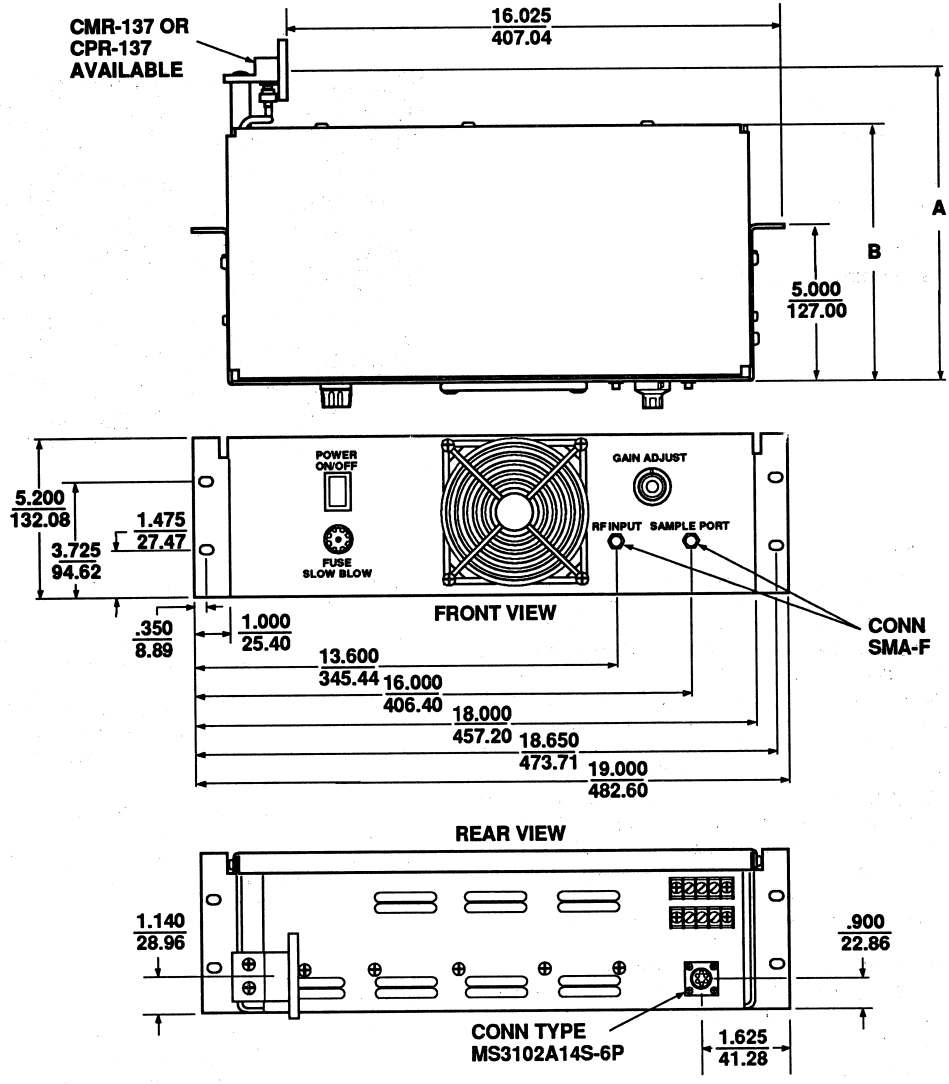


NOTES (UNLESS OTHERWISE SPECIFIED):

1. DIMENSIONS ARE SPECIFIED IN INCHES / MM
2. TOLERANCES: .XX ± 0.02 / ± .5
   .XXX ± 0.010 / ± .25

Case Drawing
ACU-64100RM, AWP-64200RM

C Band Uplink Power Amplifier



CASE	DIMENSION				FUSE
	A		B		
	IN	MM	IN	MM	
ACU-64100RM	9.815	249.30	8.212	208.58	3A @ -48 VDC 7A @ -24 VDC
AWP-64200RM	17.430	442.72	15.475	393.06	7A @ -48 VDC 12A @ -24 VDC

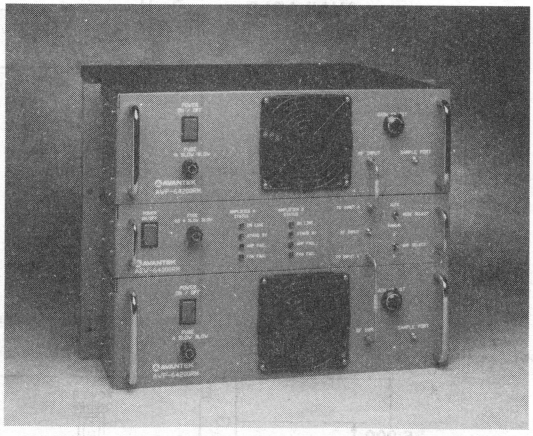
NOTES (UNLESS OTHERWISE SPECIFIED):

1. DIMENSIONS ARE SPECIFIED IN INCHES / MM
2. TOLERANCES: .XX ± 0.02 / ± .5
   .XXX ± 0.010 / ± .25

Features

- 1 x 1 Hot Standby Protection
- +42 dBm Output
- High Linearity
- High Gain
- Low Maintenance
- Long Life
- Fail Soft (Individual Amplifier)

ARS-64200: C Band Uplink Power Amplifier



Description

The Hewlett-Packard Model ARS-64200RM is a redundant C-band uplink power amplifier assembly designed to provide exceptionally high linearity, combined with very low spurious output in the downlink band. The ARS-64200RM may be used to directly replace the 20-watt TWT amplifiers in most satellite uplink transmitters. This includes SCPC, QPSK or other multiple-carrier systems where stringent third-order intermodulation performance requirements would have precluded the use of previous-generation solid-state amplifiers.

The ARS-64200RM consists of two standard Hewlett-Packard AWP-64200RM 20-watt-output C-band power amplifiers and a separate switching unit, each supplied in a standard 19-inch rack panel case. All interconnecting cables provided. The amplifiers incorporate their own cooling fans so no external thermal conduction path is required. The standard rack mounting configuration means that the redundant amplifier assembly will easily fit into most earth terminal installations.

The ARS-64200RM provides up to 50 dB of gain, which can, in some installations, permit the replacement of driver amplifiers with lower-power amplifiers which typically have better AM-to-PM performance.

The ARS-64200RM amplifier assembly will normally exhibit less than 0.2 dB gain compression when a third 1-watt carrier is added to an uplink already transmitting two 1-watt carriers. This makes the ARS-64200RM system ideal for intermittent-carrier applications.

Since the drive level available in various uplink terminals will vary, the AWP-64200RM amplifiers are equipped with a variable attenuator at their RF input ports to permit their gain to be reduced by up to 10 dB. This allows the user to optimize output performance without making system adjustments external to the amplifier assembly. Once the attenuator is set, there are no other scheduled service requirements.

The Hewlett-Packard power amplifier is specifically designed to generate a very low level of spurious outputs in the downlink band—typically less than -117 dBm measured at a 4 kHz bandwidth within the 3.7 to 4.2 GHz band. This means that extremely simple RF isolation networks are all that is required to protect the downlink LNAs.

Both amplifiers in the AWP-64200RM system are powered on at all times. The switching unit determines which of the two amplifiers is on-line. Amplifier or fan failure will automatically initiate a switch to the standby amplifier.

The ARS-64200RM system uses independent high-efficiency DC-to-DC converters, which contain fewer components and operate at voltages no higher than 56 VDC. This directly contributes to higher reliability and greater personnel safety than with TWTA amplifiers.

ARS 64200RM Redundant Rack Mounted C Band Power Amplifier for Satellite Uplink Applications
Guaranteed Specifications at 0° to 50°C Case Temperature

Frequency ..... 5.925 to 6.425 GHz

Gain ..... 50 dB (Min.)
10 dB adjustable with
built in attenuator at input

Saturated Power Out ..... +42 dBm

3rd Order IP ..... +49 dBm
tested with 3 tones and
total P_{OUT} of +36.5 dBm

Gain Variation (0 to 50°C) ..... ±3 dB (Max.)

Power Out Flatness ..... ±1 dB (Max.)

VSWR IN/OUT 1.3:1/1.5:1

Group Delay/40 MHz ..... 2.0 nsec peak to peak

With Total P_{OUT} of +40 dBm:

AM/PM Conversion ..... 2.0°/dB

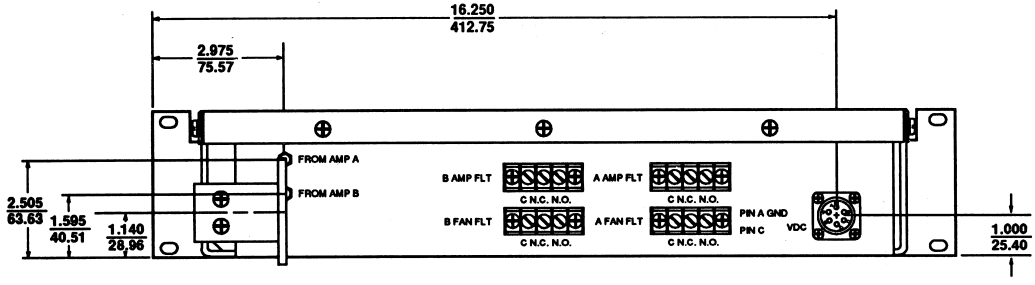
Harmonic Output ..... -53 dBc (Min.)

Spurious Output ..... -60 dBc (Min.)

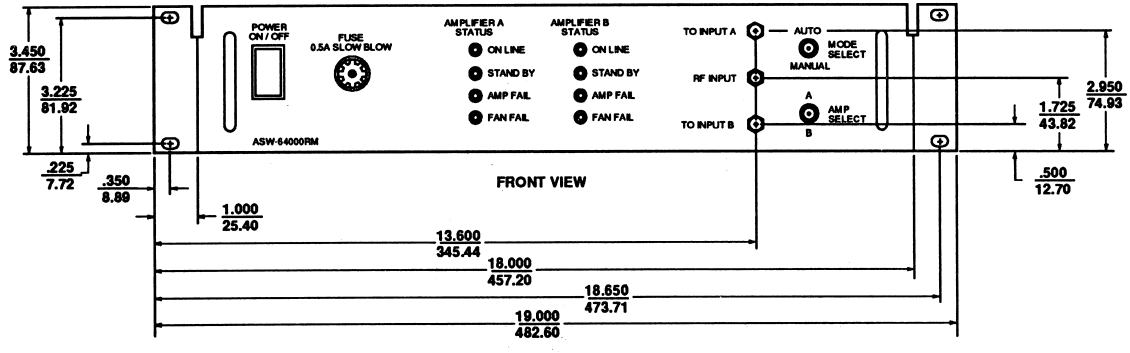
DC Input ..... -24 or -48 VDC

Power Consumption ..... 500 watts

Noise Figure ..... 10 dB (Max.)

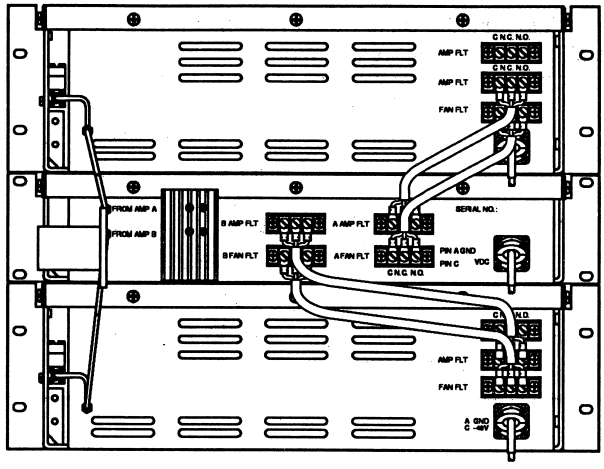


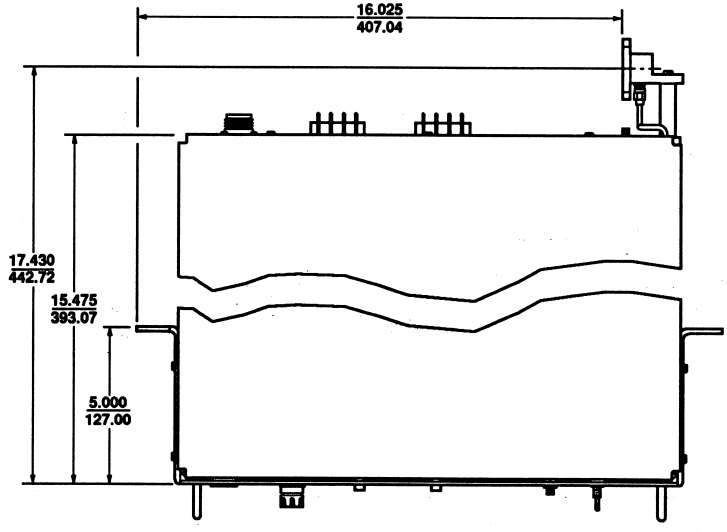
REAR VIEW



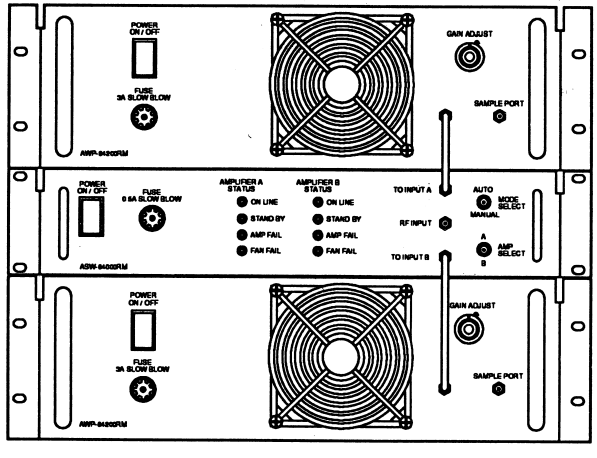
FRONT VIEW

Case Drawing





XXX = INCH
XXX = MM



HEWLETT PACKARD

AWP-64500RM
Rack Mountable
C Band Uplink Power Amplifier

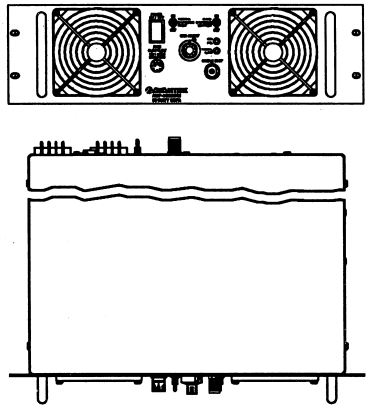
Features

- **High Linearity**
- **High Gain**
- **Low Maintenance**
- **Long Life**
- **Fail Soft**

Applications

- **Satellite Uplink Power Amplifier**
- **TWT Replacement**

AWP-64500RM



Description

The Hewlett-Packard AWP-64500RM is a 50 watt, 6 GHz Amplifier which is designed to provide exceptionally high linearity. It may be used to retrofit SCPC, QPSK or other multiple carrier satellite uplink systems, which now use TWTs, where stringent third order requirements would normally preclude the use of solid state amps.

These systems may utilize any number of carriers as long as the maximum output power of each is calculated using the total frequency plan and resulting intermods.

The Hewlett-Packard amplifier is installed in a standard 19 inch rack mountable cabinet and includes its own fans. No external thermal conduction path is required and it will easily fit into a variety of system applications.

The AWP-64500RM provides up to 60 dB of gain that lets users reduce the amount of pre-amplification in their uplink terminal. Users can then use lower power pre-amps which typically have better AM/PM performance. Additionally, the AWP-64500RM will normally exhibit less than 0.2 dB gain compression when a third 2 watt carrier is added to the two that are already transmitting. This makes it ideal for intermittent carrier applications.

Since the input power that is available in various potential retrofit systems will vary somewhat, the AWP-64500RM is equipped with a variable attenuator at the RF input port to allow gain adjustments of up to 10 dB. Users can optimize output performance without making system adjustments external to the amplifier. Once set, there are no other scheduled service requirements.

The Hewlett-Packard PA is designed to exhibit a very low noise level in the C Band downlink frequency range of 3.7 to 4.2 GHz. Therefore, extremely simple RF isolation networks may be used to protect the system's LNA.

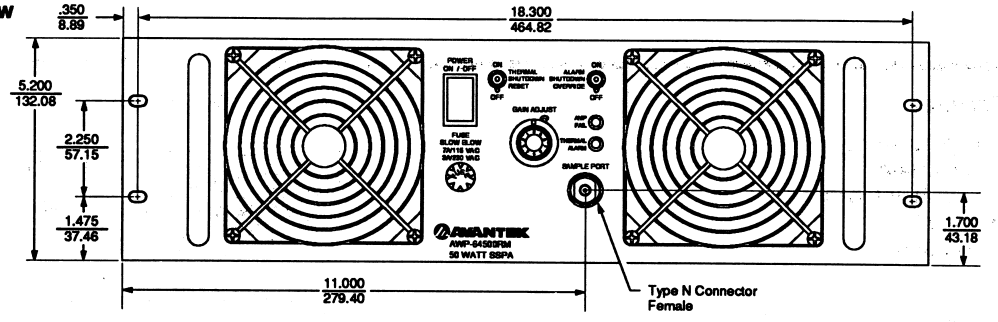
The AWP-64500RM uses a high efficiency AC to DC converter containing fewer components and operating at lower voltage than the typical TWTA power supply. This directly contributes to higher reliability and greater personnel safety than the average tube can offer.

AWP-64500RM – Rack Mounted C Band power amplifier for satellite uplink applications

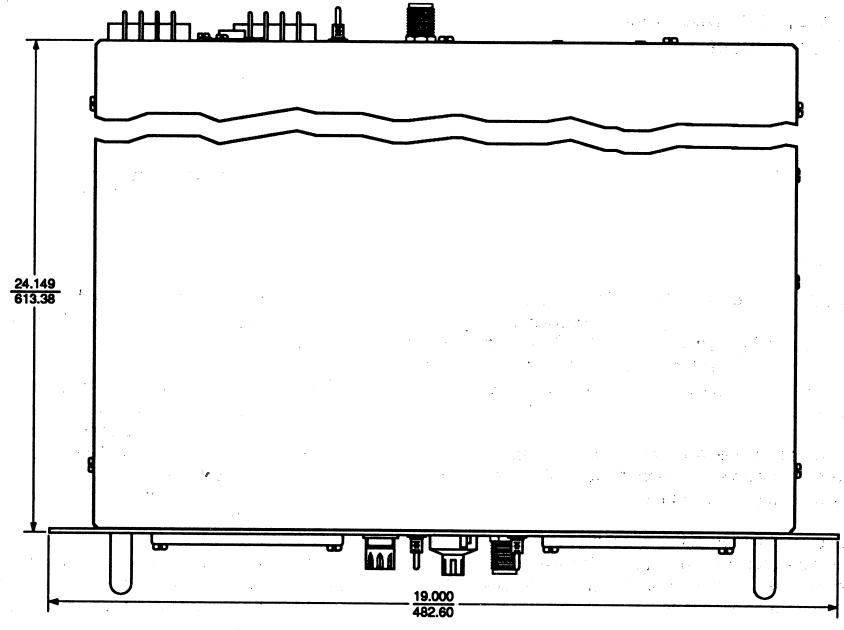
Specifications

Parameter	Characteristics
Frequency Range:	5.925 to 6.425 GHz
Gain:	65 dB min.
10 dB adjustable with built in attenuator at input	
Saturated Power Out:	+ 46.5 dBm
3rd Order IP:	+ 53 dBm
tested with 3 tones and total P_{OUT} of +36.5 dBm	
Gain Variation (0 to 50°C):	± 2 dB max.
Power Out Flatness:	± 1 dB max.
VSWR IN/OUT	1.3:1/1.5:1
Group Delay/40 MHz	2.0 ns peak-to-peak
With total P_{OUT} of +44 dBm:	
AM/PM Conversion	3°/dB
Harmonic Output	–53 dBc min.
Spurious Output	–60 dBc min.
AC Input	115 or 230 VAC
Power Consumption	600 Watts
Noise Figure @ Max Gain	10 dB max.

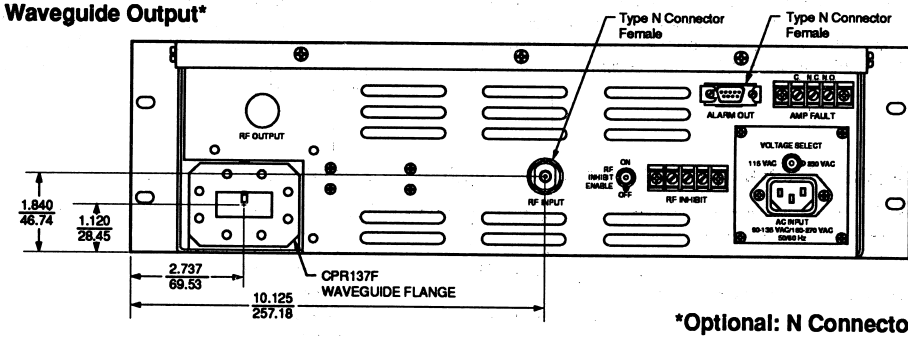
Front View



Top View



Rear View Waveguide Output*



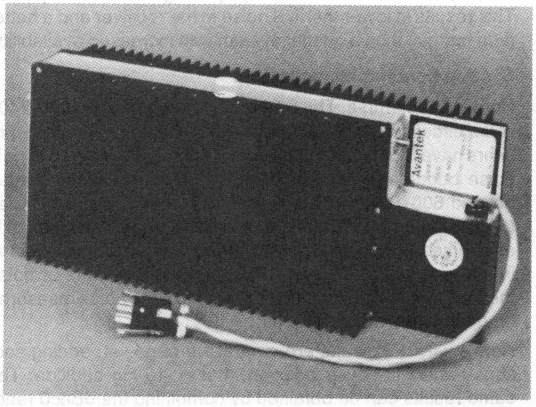
*Optional: N Connector Output

TWT Retrofit: High Power Common Carrier

Features

- High Reliability
- Energy Efficient
- FCC Type Accepted
- High Channel Loading Capacity
- Easy to Install
- No Maintenance Required
- Office Battery Powered
- Cost Competitive
- 4, 6, 7, 8 and 11 GHz Bands

Power Amplifier (Single Unit)



Description

Hewlett-Packard manufactures a complete line of solid state power amplifiers and retrofit accessory kits to replace TWTs and their associated power supplies in terrestrial point-to-point microwave radio transmitters. These full-band amplifiers are available with 10 watts output power at 4, 6, 7, 8 and 11 GHz. The 6 and 11 GHz units are available in two physical styles. Performance characteristics of both styles are identical. The single unit has the RF and DC/DC converter combined into a single package that is ideal for replacing the older style TWTs. The split unit separates the RF and DC/DC converter into two packages with the RF section having the same footprint as the high-efficiency TWT it replaces.

Cost Effective TWT Replacement

HP's solid state power amplifiers are a cost effective solution to TWT replacement. Solid state GaAs FET RF power amplifiers typically require less current than a TWT amplifier. This reduction in DC power consumption can increase the battery plant reserve time or allow additional equipment to be added without increasing battery capacity. Reduced power consumption can eliminate the need for increased rectifier recharging capacity and larger emergency engine alternators. Less power dissipation means less heat is generated, thus the cost of air conditioning can be reduced. If obsolete power plants or air conditioning units are to replaced, the new ones can be smaller and less costly.

The HP amplifier is directly competitive in initial price if any part of the TWT amplifier needs to be changed. Retrofit accessory packages include all hardware, transitions and instructions needed to complete an amplifier retrofit installation in about one hour. Retrofit amplifiers are also equipped with an input attenuator capable of accepting any RF input power level between –1 and +10 dBm, thereby permitting installation of the TWT replacement amplifier without requiring adjustment to any of the previous stages. Additionally, these amplifiers can be used as spares for all of the various radio types that have been retrofitted.

Solid state amplifiers can dramatically reduce maintenance costs. All TWT amplifiers have to be realigned periodically to correct for aging. Older tubes need adjustment three to four times per year. When these tubes are replaced with the HP solid state amplifier, no periodic alignment is required. Once the power amplifier output is set by adjusting the attenuator and the unit is placed into service, only the required FCC checks must be made. Since the HP IMFET™ internally-matched GaAs field effect transistors, at ambient room temperature, operate at a 115°C channel temperature, the calculated device MTBF exceeds 30 years. With this reliability, significant cost savings through long life can be realized. However, in the unlikely event of failure of the IMFET™ device, the output stage is also designed to fail-soft, thus avoiding complete service outage.

Transmission Improvement

Many transmission improvements can result when traveling wave tube amplifiers are replaced with HP solid state power amplifiers. As mentioned above, the output of a TWT amplifier degrades between adjustments. On the day of adjustment,

it will put out its rated power and gradually drop until it needs to be readjusted or a low output alarm comes on at about 3 dB below rated power. Experience has shown that the average output of a tube-type amplifier is 2 dB below design value which corresponds to a 2 dB reduction in fade margin and 59% increase in outages. Since the output power of a solid state amplifier is not affected by the "sag" of cathode erosion as in a TWT, the transmitter is always putting out its rated power. This results in lower thermal noise in the receiver and a better fade margin, thus a quieter system with increased availability.

System Loading Maximization

Here is an example. The 6 GHz band can support 1800-2400 voice circuits in its 30 MHz channels. However, a number of users have found that routes designed and engineered to rigid noise budgets will not meet noise objectives when loaded beyond 600-1200 circuits. Testing short sections of facilities (6-10 hops) may show that each section is performing exactly as engineered. However, when four or five sections are tested in tandem, it may be found that the total picowatts of noise measured is two to three times the sum of the noise measured on each of the short sections.

Here's why. Picowatts are a measure of power; adding sections results in power addition, that is, 10 log addition. The same results can be obtained by combining the dBnc0 readings of the shorter sections on a power ratio (again 10 log) basis. It is very difficult to determine the amount of 20 log (voltage addition) noise in a per hop or short section test, since, in a short section, the 20 log noise may be completely masked by the sources of 10 log noise. On longer sections it can quickly become predominant.

The most common cause of this type of noise is AM/PM conversion in the traveling wave tube amplifier and in the upconverter. TWT amplifiers normally have AM/PM conversion of 4 to 8 degrees per dB. HP solid state retrofit amplifiers typically perform at 1.5°/dB across the 500 MHz band. Replacement of the TWT with an HP solid state low AM/PM amplifier will significantly reduce intermodulation noise due to reduced AM/PM conversion in the transmitting amplifier. With 2 dB reduction in thermal noise by eliminating TWT output sag and with four to five dB improvement in intermodulation noise due to AM/PM reduction, it is possible to fully utilize the 1800 to 2400 channels of system design capability.

Driver Amp Upconverter AM/PM Relief

Depending upon the system that you are retrofitting, you may also be able to remove the AM/PM problem in your upconverter. If your system normally drives the TWT at a level higher than 0 dBm, you could drop the level of IF signal into the driver amplifier section of the upconverter such as to give 0 dBm at the upconverter output. Then, by using the full gain of the HP solid state amplifier, you can maintain a +40 dBm output. Dropping the level into the driver amplifier 4-10 dB should significantly reduce the 20 log noise component.

AWP Series — High Power TWT Replacement Amplifiers

Guaranteed Specifications @ 25°C Case Temperature

Model	Frequency Range (GHz)	RF Input Power (dBm)	Gain (dB)	Output Power[12] (watts/dBm)	Noise Figure (dB) Max.	AM/PM Conver (°/dB) @ Max. Output Typ./Max.	Output Power Variation 0° to +55°C (dB) Max.	Output Power Flatness (dB) P-P	Envelope Delay Distortion (nsec) P-P	Harmonics (dBc) Max.	Spurious (dBc) Max.	Return Loss (dB) Min. Input	Return Loss (dB) Min. Output	Input Power[13] DC watts[9]	Case Type
AWP-42100	3.7-4.2	Note 1	Note 2	10/+40	10[3]	1.5/3	±2.5	±.25[4]	±1[6]	-53	-60	20	20	76	RJA
AWP-64100	5.925-6.425	Note 1	Note 2	10/+40	10[3]	1.5/2	±2.5	±.25[5]	±1[7]	-53	-60	20	20	76	RJA
AWP-64105	5.925-6.425	Note 1	Note 2	10/+40	10[3]	1.5/2	±2.5	±.25[5]	±1[7]	-53	-60	20	20	76	PHL
AWP-64105F	5.925-6.425	Note 1	Note 14	10/+40	10[3]	1.5/2	±2.5	±2.5[5]	±1[7]	-53	-60	20	20	76	CJL
AWP-71100	6.4-7.1	Note 1	Note 2	10/+40	10[3]	1.5/3	±2.5	±.25[10]	±1[11]	-53	-60	20	20	76	RJA
AWP-77100	7.1-7.7	Note 1	Note 2	10/+40	10[3]	1.5/3	±2.5	±.25[10]	±1[11]	-53	-60	20	20	76	RJA
AWP-83100	7.7-8.3	Note 1	Note 2	10/+40	10[3]	1.5/3	±2.5	±.25[10]	±1[11]	-53	-60	20	20	76	RJA
AWP-117500	10.7-11.7	Note 1	Note 8	5/+37	10	1.5/3	±2[15]	±.25[10]	±1[11]	-53	-60	18	18	76	RJA

Notes:

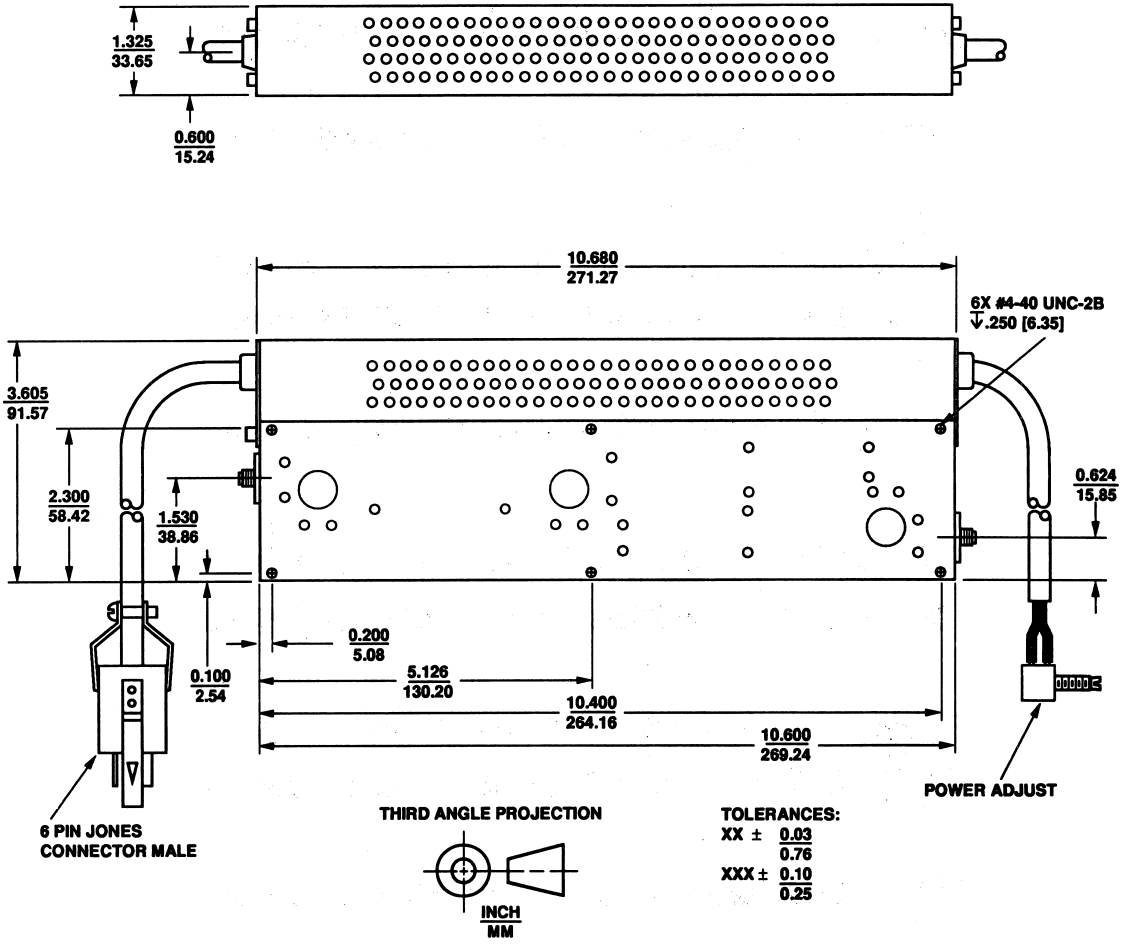
1. Accepts any input level from -1 to +10 dBm for rated output power.
2. Gain adjustable from 30 to 41 dB for an output power level of +40 dBm.
3. At maximum gain.
4. Peak-to-peak across any 20 MHz band at +40 dBm output power.
5. Peak-to-peak across any 30 MHz band at +40 dBm output power.
6. Peak-to-peak across any 20 MHz band.
7. Peak-to-peak across any 30 MHz band.
8. Gain adjustable from 27 to 38 dB for an output power of +37 dBm.
9. At -24 or -48 VDC.
10. Peak-to-peak across any 40 MHz band at rated output power.
11. Peak-to-peak across any 40 MHz band.
12. At nominal input.
13. 1 dB compressed.
14. ±0.75 dB over +10°C to +45°C.
15. Maximum output power variation from 0° to +50°C.

ALL OTHER PARAMETERS THE SAME AS THE AWP 64105 EXCEPT CASE (FOR CASE REFER TO ATTACHED INSTALLATION DWG.)

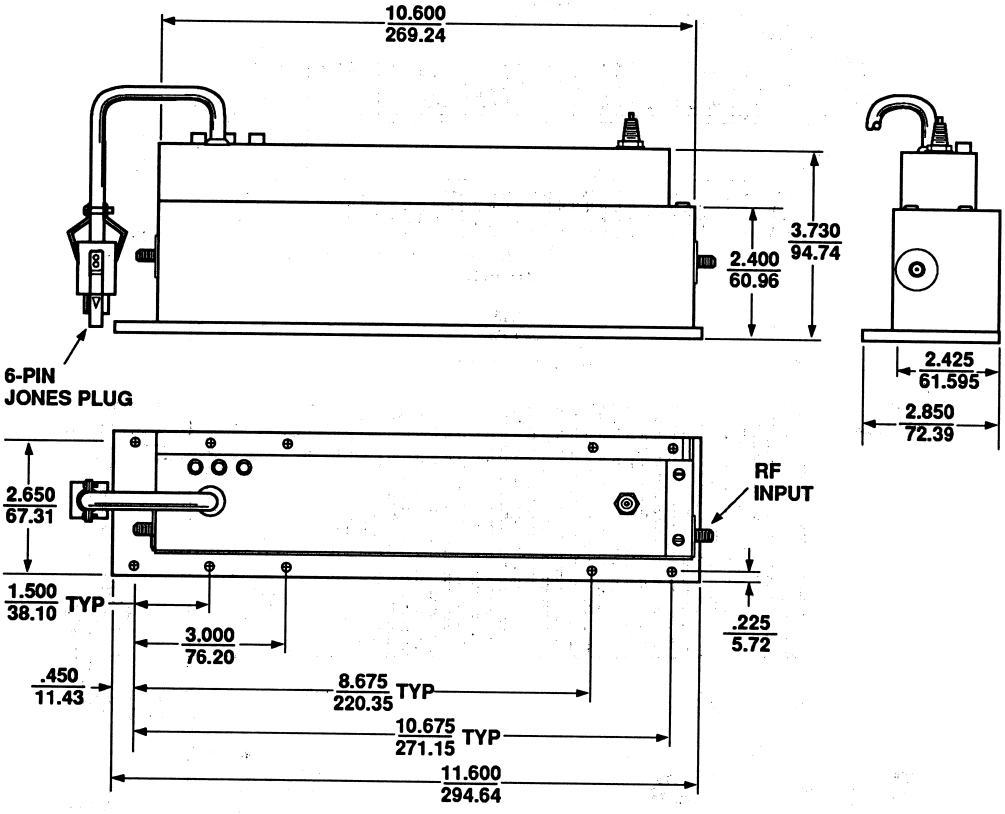
Retrofit Product Selection Guide

	AWP-42100	AWP-64100	AWP-46105	AWP-640500	AWP-640604	AWP-640700	AWP-71100	AWP-77100	AWP-83100	AWP-117500
Collins										
MS109E	X									
MS109E1	X									
MS109ES	X									
MW109E		X								
MW109E1		X								
MDR6			X							
MW109A3		X								
MW109B3		X								
MW609E										X
MW609E1/MW618										X
Lenkurt										
CTR108	X									
775G	X									
775A						X				
TELETTRA										
HT 12/4	X									
HT 12/6L		X								
HT 12/6						X				
HT 12/8									X	
GTE										
CTR 106		X								
SEL										
FM 1800		X								
775C							X			
775D										X
NEC										
6G78MB		X								
Northern Telecom										
RA3T4	X									
RA3T6		X								
RD3									X	
Raytheon										
KTR3A/E		X								
KTR3TS		X								
RDS6200		X								
KTR3A/E11										X
RCA										
MM600		X								
Western Electric										
FR-6						X				
TD-2	X									
TD-3D	X									
660	X									
TH-1		X		X						
TH-3		X								
TMA1		X								
TM2/2A					X					

TWT RETROFIT Installation Drawing



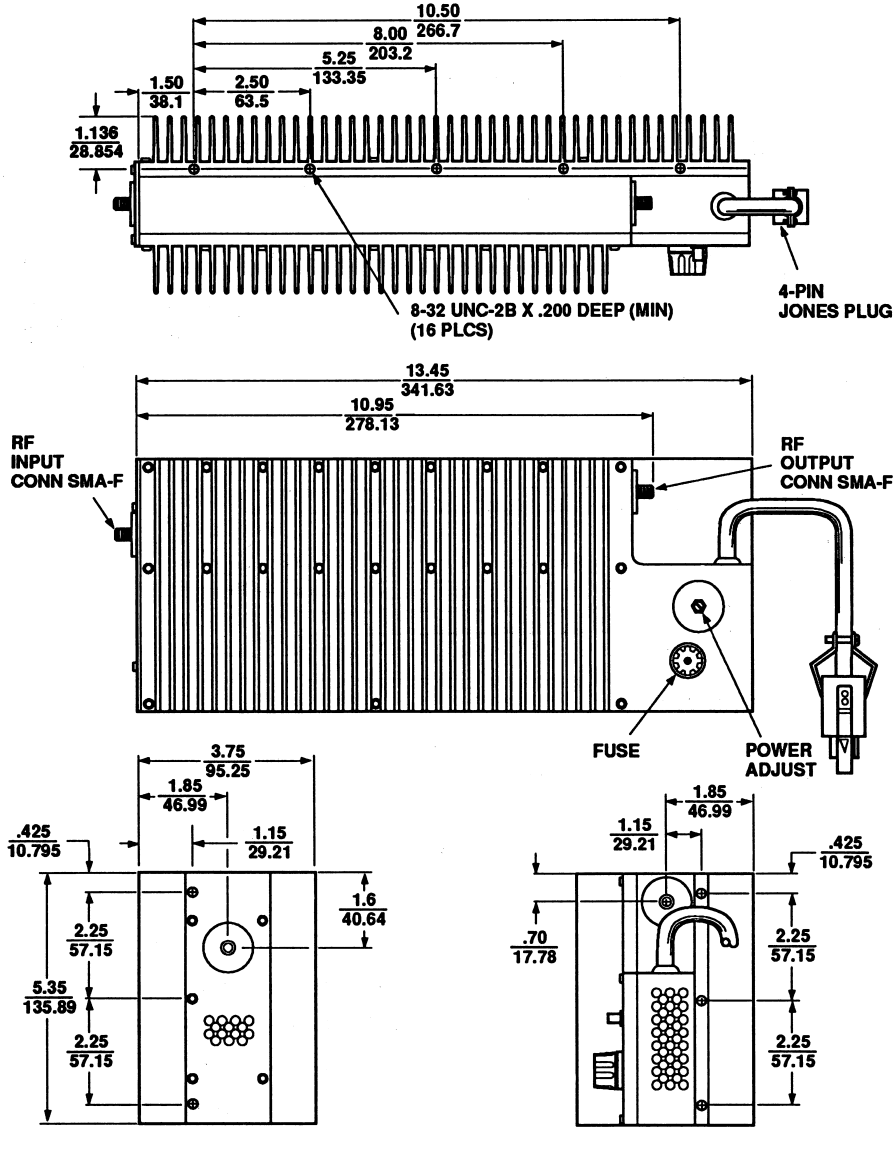
Case Drawing
PHL



NOTES (UNLESS OTHERWISE SPECIFIED):

1. DIMENSIONS ARE SPECIFIED IN INCHES / MM
2. TOLERANCES: .XX ± 0.02 / ± .5
   .XXX ± 0.010 / ± .25

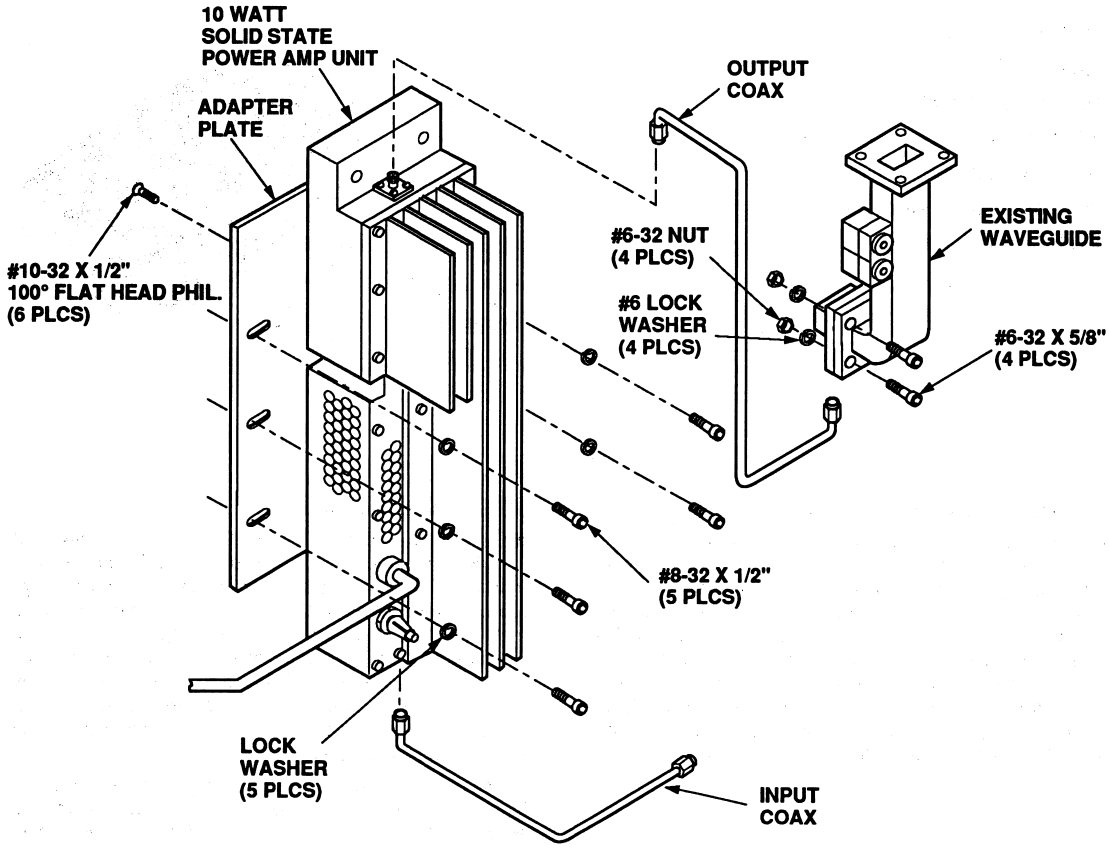
Case Drawing
RJA



NOTES (UNLESS OTHERWISE SPECIFIED):

1. DIMENSIONS ARE SPECIFIED IN $\frac{\text{INCHES}}{\text{MM}}$
2. TOLERANCES: .XX $\frac{\pm 0.02}{\pm .5}$

   .XXX $\frac{\pm 0.010}{\pm .25}$

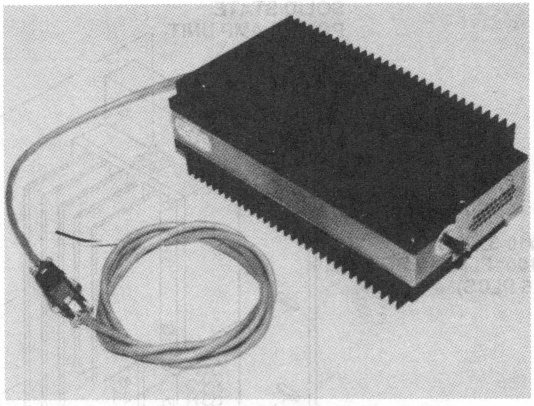

10 WATT
SOLID STATE
POWER AMP UNIT
ADAPTER
PLATE
#10-32 X 1/2"
100° FLAT HEAD PHIL.
(6 PLCS)
OUTPUT
COAX
#6-32 NUT
(4 PLCS)
#6 LOCK
WASHER
(4 PLCS)
EXISTING
WAVEGUIDE
#6-32 X 5/8"
(4 PLCS)
#8-32 X 1/2"
(5 PLCS)
LOCK
WASHER
(5 PLCS)
INPUT
COAX

General Purpose: Narrowband Power Amplifier and CARS Band Preamplifiers

Features

- High Reliability
- Energy Efficiency
- FCC Type Accepted
- High Channel Loading Capacity
- Easy to Install
- No Maintenance Required
- Cost Competitive

AWP Series 3.7 to 11.7 GHz.



Narrowband General Purpose Description

Hewlett-Packard's 4, 6, 7, 8 and 11 GHz amplifiers are cost-effective TWTA replacements. Their performance and reliability has been proven by the more than 10,000 units now in use throughout the world. The AWP series uses substantially less input power than a TWT, has more gain thus reducing AM/PM problems due to the lower output needed from the upconverter, and maintains a constant output power over its calculated lifetime (MTBF) of 30 years. In digital systems, at lowered gain levels, AWP amplifiers offer less than 0.25 dB compression with AM/PM of less than 0.25°/dB over the entire band.

CARS Band Description

This amplifier replaces the klystron tube that is currently used in single-channel AML (SSB) CARS-band (*Community Antenna Relay Service) transmitters for CATV distribution applications. HP's AWP-132200 is a 3 watt linear solid state amplifier that operates in the frequency range of 12.7 to 13.25 GHz with typical gain at approximately 51 dB. The unit runs significantly cooler than the klystron tube and power supply combination, reducing air conditioning costs as well as minimizing maintenance on other electronic equipment, located in the same room as a transmitter.

Amplifier characteristics include exceptional linearity, low higher order IM distortion and low AC power consumption. This design offers months of continuous reliable operation without maintenance adjustments.

AWP—MEDIUM POWER COMMERCIAL COMMUNICATIONS BAND AMPLIFIERS

AWP Series

Guaranteed Specifications @ 25°C Case Temperature

Model	Frequency Response (GHz) Minimum	Power Output for 1 dB Gain Compression (dBm/watts) Minimum	Gain (dB) Min.	Gain Flatness (±dB) Max.	Typical Intercept Point for IM Products (dBm)	Noise Figure (dB) Max.	VSWR (50 ohms) Maximum In	VSWR (50 ohms) Maximum Out	Input Power Voltage (VDC ±3%)	Input Power Current (mA) Typical	Case Type
AWP-42107	3.7-4.2	+25/.3	26	2	+35	10	1.2	1.2	+15	500	SPG
AWP-42108	3.7-4.2	+32/1.5	33	2	+40	10	1.2	1.2	+15	1200	SPG
AWP-42109	3.7-4.2	+40/10	41	2	+47	10	1.2	1.2	+15	6000	SPG
AWP-64107	5.925-6.425	+25/.3	26	2	+34	10	1.2	1.2	+15	500	SPG
AWP-64108	5.925-6.425	+32/1.5	33	2	+40	10	1.2	1.2	+15	1200	SPG
AWP-64109	5.925-6.425	+40/10	41	2	+46	10	1.2	1.2	+15	6000	SPG
AWP-71107	6.425-7.125	+25/.3	26	2	+34	10	1.2	1.2	+15	500	SPG
AWP-71108	6.425-7.125	+32/1.5	33	2	+40	10	1.2	1.2	+15	1200	SPG
AWP-71109	6.425-7.125	+40/10	41	2	+46	10	1.2	1.2	+15	6000	SPG
AWP-77107	7.125-7.725	+25/.3	26	2	+34	10	1.2	1.2	+15	500	SPG
AWP-77108	7.125-7.725	+32/1.5	33	2	+40	10	1.2	1.2	+15	1200	SPG
AWP-77109	7.125-7.725	+40/10	41	2	+46	10	1.2	1.2	+15	6000	SPG
AWP-83107	7.725-8.275	+25/.3	26	2	+34	10	1.2	1.2	+15	500	SPG
AWP-83108	7.725-8.275	+32/1.5	33	2	+40	10	1.2	1.2	+15	1200	SPG
AWP-83109	7.725-8.275	+40/10	41	2	+47	10	1.2	1.2	+15	6000	SPG
AWP-117107	10.7-11.7	+25/.3	26	2	+32	10	1.2	1.2	+15	500	SPG
AWP-117108	10.7-11.7	+32/1.5	33	2	+39	10	1.2	1.2	+15	1200	SPG

Note:
1. Units are available with or without top and/or bottom heatsinks.

AW—CARS BAND POWER AMPLIFIER

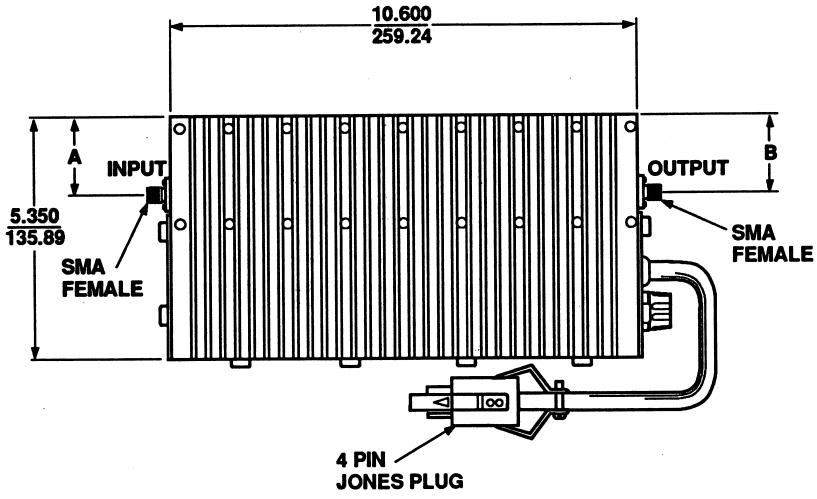
AWP Series

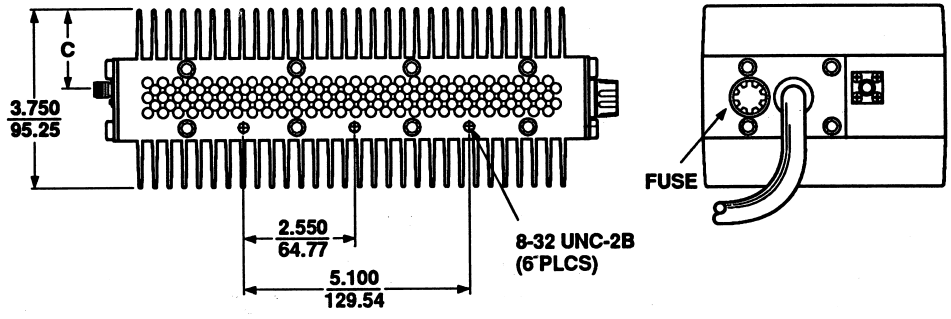
Guaranteed Specifications @ 25°C Case Temperature

Model	Frequency Range (GHz) Minimum	Noise Figure (dB) Maximum	Gain (dB) Min.	Gain Flatness (±dB) Max.	Power Output @ 1 dB Gain Compression (dBm) Minimum	Typ. Intercept Point for Third Order Intermod Products (dBm) Minimum	VSWR (50 ohms) Maximum In	VSWR (50 ohms) Maximum Out	Input Power Voltage	Input Power Current (mA) Typical	Case Type
AWP-132200	12.7-13.15	13	47	1.5	+37	+35	1.25	1.25	105-130 VAC	140 W max	AWP

Case Drawing
SPG

Narrowband Power Amplifier





PART NUMBER	DIMENSION			CASE
	A	B	C	
AWP-42107,8,9	1.400	.665	1.907	SPG-1
AWP-64107,8,9	1.580	.674	1.891	SPG-2
AWP-71107,8,9	1.525	.975	1.891	SPG-3
AWP-77107,8,9	1.525	.975	1.891	SPG-3
AWP-83107,8,9	1.525	.975	1.891	SPG-3
AWP-117107,8	1.750	1.645	1.650	SPG-4
AWP-117109	1.475	1.065	1.650	SPG-5

NOTES (UNLESS OTHERWISE SPECIFIED):

1. DIMENSIONS ARE SPECIFIED IN INCHES / MM
2. TOLERANCES: .XX ± .02 / ± 0.5
   .XXX ± .010 / ± 0.25

Application Design Tools



HEWLETT PACKARD

Applications

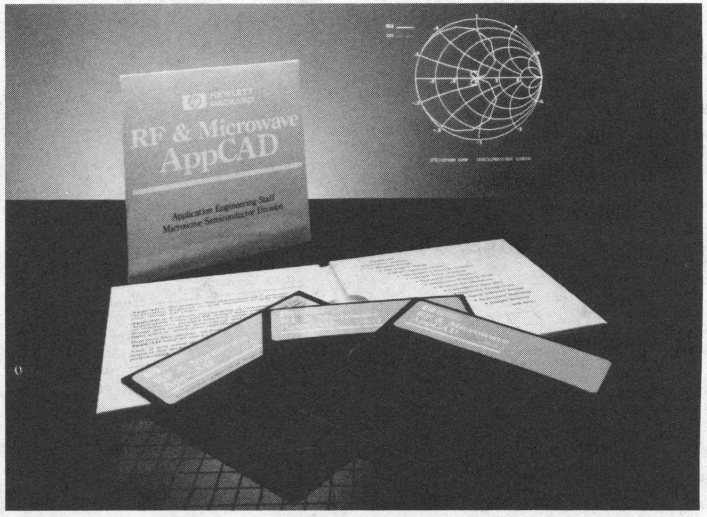
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Hewlett-Packard customers are supported by an Applications Engineering Department. The applications engineering staff investigates circuit applications, design techniques, and device performance. The results of these investigations are published in Application Notes. These technical specialists are also available worldwide to assist customers in the use and selection of products contained in this catalog. For design assistance or to obtain more information about the services of the Applications Engineering Department, please call the HP office nearest you and ask for a Components sales engineer.

Applications Software

The Applications Engineering staff also publishes RF and microwave design software to assist the circuit designer with solutions to everyday engineering problems and to simplify the task of selecting and using the best products for a specific circuit design. Device data are also made available on computer discs to evaluate device performance and facilitate CAD.



Applications software may be obtained without charge by contacting the HP office nearest you and asking for a Components sales engineer.

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Hewlett-Packard's Application Engineering staff has developed the AppCAD software program to assist customers in the selection and application of RF & Microwave products.

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AppCAD is a unique combination of *computerized Application Notes* and *RF design tools* combined with an *interactiue product selection guide* that helps you design and analyze your circuit and then find just the right part to meet your specifications.

*See Sales and Service, Section 15, of this catalog.

Features like *menus, on-line help, and pop-up windows* make AppCAD easy to use to save you time.

And, if you need more help, we've included a built-in request for technical literature, a sample part request for prototyping, and contacts to call for more information.

Contents:
- Two-port Analysis
- Thermal Design
- PIN Switch Design
- Mixer Spurious Search
- Transmission Lines & Couplers
- Cascade Noise Analysis
- Transistor Bias Circuits
- Interactive Selection Guide
- Request for Literature
- S-Parameter Data Files
- Transistor Design Data
- Spiral Inductor Design
- Impedance Matching
- Sample Request .... and more

System requirements: IBM AT/386/486 or compatible with hard disc & 512 K RAM; MS-DOS®2.0 or higher; CGA, EGA, or VGA color or Hercules compatible monochrome monitor.

Not copy protected.

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(Part Number HAPP-0001)

DesignPak™

The *DesignPak is* a comprehensive data library of s-parameter and noise parameter data for the following products:

- Discrete GaAs FET devices
- GaAs MMIC products
- Discrete Bipolar Transistors
- MODAMP™ silicon MMIC gain blocks
- MagIC™ silicon MMIC products

All s-parameters are in a standard *.S2P ASCII file format for use on most linear circuit simulators. (Ordering No. 900550)

Applications Literature

A library of Applications literature is available. These publications include a high frequency transistor primer series which provides a basic introduction to many microwave semiconductor products and a variety of Applications Notes detailing specific design examples. These publications are available without charge and may be obtained by contacting the HP office nearest you and asking for a Components sales engineer.

High Frequency Transistor Primer Series

Primer 1 Silicon Bipolar Electrical Characteristics

Ordering No. 300120

Primer 2 Noise & S-Parameter Characterization

Ordering No. 300122

Primer 3 Thermal Properties

Ordering No. 300124

Primer 3A Thermal Resistance

Ordering No. 300126

Primer 4 GaAs FET Characteristics

Ordering No. 300128

General Application Notes

AN A001 Notes on Choke Network Design
Stability; Bipolar Transistor and GaAs FET choke networks

Ordering No. 300300

AN A002 Design of a 4 GHz LNA for a TVRO Earth Station
Low noise amplifier design; GaAs FET active bias circuits

Ordering No. 300305

AN A004R Electrostatic Discharge Damage and Control
Identifying and preventing ESD damage

Ordering No. 300310

AN A005 Transistor Chip Use
Storage, die attach, and bonding for discrete transistors

Ordering No. 300315

AN A006 Mounting Considerations for Packaged Microwave Semiconductors
Mechanical, thermal, and soldering information

Ordering No. 300320

AN A007 4 GHz Television Receive Only LNB Design
Low noise amplifier, mixer, and 950-1450 MHz IF amplifier design

Ordering No. 300325

AN A008 Microwave Oscillator Design
Using S-parameters to predict frequency of oscillation

Ordering No. 300330

AN A009 Direct Broadcast Satellite Systems

Ordering No. 300335

AN 979 The Handling and Bonding of Beam Lead Devices Made Easy

Beam Lead devices are particularly attractive for hybrid circuits because of their low parasitics and small size. The availability of equipment and techniques specifically designed for their small size has facilitated the handling and bonding of these devices. This application note describes some of this equipment and techniques, and outlines suggestions for the proper handling and bonding of Beam Lead devices.

Ordering No. 5953-4435

AN 992 Beam Lead Attachment Methods

This application bulletin gives a general description of various methods of attaching beam lead components to both hard and soft substrates. A table summarizes the most common attachment methods with advantages, disadvantages, and equipment costs.

Ordering No. 5953-4496

AN 993 Beam Lead Diode Bonding to Soft Substrate

The hard gold surface on standard pc boards with soft substrate material makes it almost impossible to successfully bond beam lead diodes onto the boards with normally recommended thermocompression bonding. Described in this application note is a new method of resistive spot welding or modified gap welding, which uses a single electrode to weld the beam while the conductor is contacted separately. This method allows tight pressure to be used on the weld probe, resulting in an effective bond without damaging the beam lead device.

Ordering No. 5954-2227

AN 1037 Surface Mount Flatpack (HBIC-XXXX) Mounting

This application note describes appropriate techniques for RF grounding, PWB pad layout, and solder attachment of the HBIC-XXXX series of surface mount flatpacks used for RF and High Speed Digital hybrid and MMIC circuits.

Ordering No. 5954-2211

Gallium Arsenide FET and MMIC Application Notes

AN ATP-1054 Measurement and Modeling of GaAs FET Chips

S-parameter measurement at microwave frequencies

Ordering No. 300130

AN G001 ATF-13136 12 GHz Demonstration Amplifier

11.7 - 12.2 GHz single stage low noise amplifier using the ATF-13136

Ordering No. 300470

AN G002 ATF-10136 4 GHz Demonstration Amplifier

3.7 - 4.2 GHz single stage low noise amplifier using the ATF-10136

Ordering No. 5091-4863E

AN G003 MGA-64135 GaAs MMIC

Ordering No. 300475

AN G004 S-Band Low Noise Amplifiers ATF-10136, ATF-13284

Ordering No. 300480

AN G005 Active GaAs FET Mixer Using the Hewlett-Packard ATF-10136, ATF-13736, and ATF-13484

Ordering No. 5091-3744E

AN G006 MGA-64135 GaAs MMIC as a Variable Gain Amplifier and Operation at Reduced V_{dd}

Ordering No. 5091-3745E

AN G007 MGS Series Monolithic GaAs Switches

Ordering No. 5091-3746E

AN 1053 Designing with HMMC-5021, 5022, 5026, and 5027 GaAs MMIC Amplifiers

This note provides a technical overview of the subject GaAs MMIC Traveling Wave Amplifiers (TWA.) These amplifiers normally cover 2 to 22/26.5 GHz, although the low end frequency response can be extended down into the kHz range using external components. A detailed discussion of the variable gain control feature of these amplifiers as well as proper biasing and bonding is also discussed.

Ordering No. 5091-4922E

AN 999 GaAs MMIC Assembly and Handling Guidelines

Suggestions for assembly and handling of GaAs MMIC devices are discussed in this application note. Solder die attach is recom-

mended. Caution is suggested for epoxy die attach.

Typical settings for thermosonic and thermocompression bonding are suggested.

Ordering No. 5954-2141

Schottky Diode Application Notes

AN 923 Hot Carrier Diode Video Detectors

Describes the characteristics of HP Schottky barrier diodes intended for use in video detector or video receiver circuits, and discusses some design features of such circuits.

Though less sensitive than the heterodyne receiver, the many advantages of the video receiver make it extremely useful. The Schottky diode can be used to advantage in applications such as beacon, missile-guidance, fuse-activating, and countermeasure receivers, and as power-leveling and signal-monitoring detectors.

Among the subjects discussed are the performance characteristics of video detector diodes – tangential sensitivity, video resistance, voltage sensitivity and figure of merit; how these characteristics affect the bandwidth of a video detector, video detector design considerations; considerations that affect dynamic range; and considerations that vary the level at which *burnout* can occur.

Ordering No. 5954-2079

AN 956-1 The Criterion for the Tangential Sensitivity Measurement

Discusses the meaning of Tangential Sensitivity and a recommended measurement technique.

Ordering No. 5952-0423

AN 956-3 Flicker Noise in Schottky Diodes

Treats the subject of flicker (1/f) noise in Schottky diodes, comparing four different types.

Ordering No. 5952-0487

AN 956-4 Schottky Diode Voltage Doubler

Explains how Schottky detectors can be combined to achieve higher output voltages than would be produced by a single diode.

Ordering No. 5952-0495

AN 956-5 Dynamic Range Extension of Schottky Detectors

Discusses operation of two types of detectors: the small signal type, also known as square-law detectors; and the large signal type, also known as linear or peak detectors.

Techniques for raising the compression level are presented. An example is given illustrating the effect of bias current level on an HP 5082-2751 detector.

Ordering No. 5952-8335

AN 956-6 Temperature Dependence of Schottky Detector Voltage Sensitivity

A discussion of the effects that temperature changes have on Schottky barrier diodes. Performance improves at lower temperatures in a predictable manner. Data presented was obtained using HP 5082-2750 detector diodes.

Ordering No. 5952-8341

AN 963 Impedance Matching Techniques for Mixers and Detectors

Presents a methodical technique for matching complex loads, such as Schottky diodes, to a transmission line. Direct application to broadband mixers and detectors is illustrated.

Ordering No. 5952-0496

AN 976 Broadband Microstrip Mixer Design, the Butterfly Mixer

A microstrip mixer on RT/duroid substrate is designed for the frequency range 8 GHz to 12 GHz. Hewlett-Packard Schottky barrier diode model 5082-2207 is used. Low impedance shunt transmission lines are difficult to realize and present a problem in this type of circuit. Radial line stubs are used to avoid this problem.

Ordering No. 5954-2126

AN 986 Square Law and Linear Detection

Frequency, diode capacitance, breakdown voltage, and load resistance all have an effect on the slope of a microwave detector. At high input levels the linearity may be controlled by proper tuning.

Ordering No. 5953-4444

AN 987 Is Bias Current Necessary?

Bias current is often necessary to reduce the impedance of

detector diodes to a reasonable level. However, when the signal level is high, rectified current may reduce the impedance without the need for bias current. Measurements with the 5082-2755 diode are used to illustrate this effect.

Ordering No. 5953-4446

AN 988 All Schottky Diodes are Zero Bias Detectors
Diodes which are normally biased make excellent detectors when the bias is eliminated. It is necessary to use a load with an impedance comparable to the diode impedance. This is shown with a 5082-2755 diode used with a 3469B multimeter as the load.

Ordering No. 5953-4449

AN 991 Harmonic Mixing with the HSCH-5530 Series Dual Diode
The dual diode on coplanar waveguide forms an anti-parallel pair. This arrangement is excellent for mixers with subharmonic local oscillators. A mixer for 34 GHz was designed and built. Conversion loss was measured as a function of frequency and local oscillator power level.

Ordering No. 5953-4492

AN 995 The Schottky Diode Mixer
A major application of the Schottky diode is the production of the difference frequency when the two frequencies are combined or mixed in the diode. Mixing efficiency is measured by the conversion loss, the ratio of signal input power to intermediate frequency output power. This application note studies the effect on mixing efficiency of diode parasitics, local oscillator power level, DC bias, barrier voltage, and local resistance. The advantage of multiple diode mixers is considered. Distortion products are also discussed.

Ordering No. 5954-2073

AN 997 A 2 GHz Balanced Mixer Using SOT-23 Surface Mount Schottky Diodes
The HSMS-2822 is a series diode pair in the SOT-23 package – ideal for use in a balanced mixer. The microstrip matching circuit consists of open stubs between the diodes and the I.F. port.

Ordering No. 5954-2090

AN 1052 A Low Cost, Surface Mount X-Band Mixer
This note describes the design and performance of a balanced X-Band mixer. The surface mount design uses low capacitance, SOT-23 packaged Schottky diodes and is useful for high volume applications such as DBS and VSAT.

Ordering No. 5091-4934E

PIN Diode Application Notes
AN 922 Application of PIN Diodes
Discusses how the PIN diode can be applied to a variety of RF control circuits. Such applications as attenuating, leveling, amplitude and pulse modulating, switching, and phase shifting are discussed in detail. Also examines some of the important properties of the PIN diode and how they affect its application.

Ordering No. 5954-2147

AN 929 Fast-Switching PIN Diodes
Discusses the switching speed of the PIN diodes and the considerations which affect switching capability. For HP's 5082-3041/3042 fast-switching PIN diodes, AN 929 outlines basic drive requirements and comments on a few practical switching circuits. Considerations involved in the design of the filters required for use with the diodes are also discussed. For the 5082-3041, AN 929 provides two curves: 1) typical isolation vs. forward bias and 2) switching time vs. forward bias for peak reverse current as a parameter.

Ordering No. 5954-2115

AN 957-1 Broadbanding the Shunt PIN Diode SPDT Switch
Covers an impedance matching technique which improves the bandwidth of shunt PIN diode switches..

Ordering No. 5954-2082

AN 957-2 Reducing the Insertion Loss of a Shunt PIN Diode
Examines a simple filter design which includes the shunt PIN diode capacitance into a low pass filter, thereby extending the upper frequency limit.

Ordering No. 5952-0491

AN 957-3 Rectification Effects in PIN Attenuators
Attenuation levels of PIN diodes are changed by high incident power. Variation in attenuation may be minimized by proper choice of bias resistance. Performance of a PIN diode is limited by both carrier level and frequency because of rectification effects. This note presents the effects of frequency, power level, and bias supply for three types of HP diodes: 5082-3170, 3140, and 3141.

Ordering No. 5952-8429

AN 971 The Beam Lead Mesa PIN in Shunt Applications
The low RC product, fast switching time, and other unique features of the HPND-4050 beam lead PIN diode make it well-suited for switching applications in the shunt configuration. Switching performance, practical circuits, handling, and bonding instructions are included in this application note.

Ordering No. 5954-2112

AN 985 Achieve High Isolation in Series Applications with the Low Capacitance HPND-4005 Beam Lead PIN
Low capacitance is required for a diode to achieve high isolation in the series configuration. On the other hand, low resistance is needed for low insertion loss. This combination of characteristics in the HPND-4005 Beam Lead PIN diode makes it well suited for series switching applications. The performance of this diode in an SPST switch and an SPDT switch is described in this application note. The equivalent circuits derived in this note would be useful in the design of circuits for switching and other signal control applications.

Ordering No. 5953-4443

AN 1048 A High Performance, Low Cost PIN Diode π Attenuator Using Surface Mount Devices
PIN diodes have long been used as current controlled RF resistors in variable attenuators. Of the several types, (π, TEE and bridged TEE), the π offers the best frequency response and distortion performance. However, complicated bias circuits are required to simultaneously maintain good VSWR while providing variable attenuation.

This note describes a new four-diode π attenuator with a simple bias circuit. This simplified network provides flat attenuation and good impedance match over the four decade range of 300 kHz to 3 GHz. The fabrication of the circuit, using inexpensive surface mounted components, is described in detail and measured performance is presented.

Ordering No. 5091-4933E

AN 1049 A Low Distortion PIN Diode Switch Using Surface Mount Devices
One of the practical applications of the surface mounted PIN diode is in the design of low current, low cost RF switches. In the design of such circuits, the diode is generally treated as a current controlled ideal resistor which is switched between low resistance and high resistance states.

However, the PIN diode has some important second order non-linear characteristics which can give rise to the generation of harmonic and intermodulation distortion in switching circuits, particularly those which employ high RF power. A low distortion SPDT switch, using a new type of PIN diode designed specifically for low distortion performance, is described.

Ordering No. 5091-4932E

AN 1050 Low Cost, Surface Mount Power Limiters
Many receivers are often at risk of having their front ends burned out by high power RF and microwave stray signals. This note presents practical design techniques for low cost power limiters operating at frequencies up to 2 GHz. Both circuit techniques and Surface Mount Device (SMD) diode tradeoffs are covered. Measured data on several different prototype limiters are presented.

Ordering No. 5091-4931E

AN 1054 Low Cost Frequency Multipliers Using Surface Mount PIN Diodes
PIN Switching diodes with low values of transition time can multiply frequencies up to 6 GHz similar to step recovery diodes. These diodes are available in the SOT-23 package making them ideal for low cost local oscillators and PLL frequency references. Several examples of surface mount multipliers using these PIN diodes are shown.

Frequency Multiplier, Comb Generator, and SRD Application Notes

AN 918 Pulse and Waveform Generation with Step Recovery Diodes
Step Recovery Diode characteristics are described for application to high speed (ps range) pulse and waveform generating circuits. Design details and example circuits are presented for applications such as pulse sharpness, impulse generators, and square wave generators.

Ordering No. 5954-2080

AN 928 Ku-Band Step Recovery Multipliers
Discusses the use of step recovery diodes in a times-eight single-stage frequency multiplier which, at 16 GHz, has a typical maximum output of 75 mW. The note also provides design modifications, together with references, for meeting other performance requirements.

Ordering No. 5954-2107

AN 983 Comb Generator Simplifies Multiplier Design
Comb generators are often used with bandpass filters to form frequency multipliers. This note discusses this application for the particular case of a bandpass filter passing several frequencies in the comb. The presence of the filter increases the power output by an amount related to the spacing between the filter and the diode.

Ordering No. 5953-4441

AN 984 How to Get More Power from a Comb Generator Module with the Right Bias Resistance
This note shows how to improve the power output at all frequencies in the comb. The modules do not contain a DC return for the bias current produced by rectification in the step recovery diode. AN 984 discusses the proper choice of bias resistor to double the power output compared to a DC short circuit.

Ordering No. 5953-4442

AN 989 Step Recovery Diode Multiplier
A straightforward technique for multiplier design is presented. The input circuit is a low pass filter which allows all of the input power to be absorbed by the diode and reflects harmonic power back to the diode. The output circuit is a bandpass filter which offers a low loss path to the desired frequency while reflecting all other harmonics back to the diode. The technique is illustrated by a doubler to 4 GHz using Hewlett-Packard 5082-0805 step recovery diode.

Ordering No. 5953-4454

AN 1054 Low Cost Frequency Multipliers Using Surface Mount PIN Diodes
PIN Switching diodes with low values of transition time can multiply frequencies up to 6 GHz similar to step recovery diodes. These diodes are available in the SOT-23 package making them ideal for low cost local oscillators and PLL frequency references. Several examples of surface mount multipliers using these PIN diodes are shown.

Ordering No. 5091-4918E

Silicon Transistor and Integrated Circuit Application Notes

AN S001 Basic MODAMP MMIC Circuit Techniques
Circuit layout, board selection, and grounding techniques

Ordering No. 300400

AN S002 MODAMP MMIC Nomenclature
Overview of MODAMP MMIC geometries and packages

Ordering No. 5091-6490E

AN S003 Biasing MODAMP MMICs
Passive and active MMIC amplifier bias circuits

Ordering No. 5091-6489E

AN S004 A Broadband IF Amplifier Using MSA-0235 and MSA-0335
Broadband, high gain cascade amplifier techniques

Ordering No. 300415

AN S005 Using Hewlett-Packard MSF Series Frequency Converters
Self-oscillating mixers using the MSF series

Ordering No. 300420

AN S006 Using External Feedback to Achieve Flat Gain with the MSA-0885
0.1-3 GHz flat gain amplifier design using the MSA-0885

Ordering No. 5091-5075E

AN S007 Using the MSA-0520 and the MSA-1023 Medium Power MODAMP Silicon MMIC Amplifiers
Power amplifier circuits and push-pull MSA-1023 amplifier

Ordering No. 300430

AN S008 Designing with the MSA-9970
75 ohm, ultra flat, negative gain slope amplifiers

Ordering No. 300435

AN S009 MODAMP Silicon MMIC Chip Use
Die attach, bonding, and bond diagrams for MSA series

Ordering No. 300440

AN S010 A 5 GHz Bipolar Active Mixer
IAM series Gilbert cell mixers

Ordering No. 5091-6132E

AN S011 Using Silicon MMIC Gain Blocks as Transimpedance Amplifiers
Key specifications and performance evaluation

Ordering No. 300446

AN S012 MagIC Low Noise Amplifiers
The what, why, and how-to for INA series with a demonstration circuit; SPICE models

Ordering No. 300450

AN S013 MagIC Active Mixers
The what, why, and how-to for IAM series active mixers including a demonstration circuit

Ordering No. 5091-6488E

AN S014 750-1250 MHz VCO
Ordering No. 300453

AN S015 ITA Series Transimpedance Amplifiers
Transimpedance (TZ) amplifiers are a critical element in digital fiber optic receivers. Their role is to take the current output from a photo diode, and convert it to a voltage. This application note gives an overview of Hewlett-Packard's ITA series of transimpedance amplifiers for high speed applications (100 Mb/s to 1.5 Gb/s). Tips on how to get optimum RF performance with the amplifiers is given. Recommended PC board layouts are given for ITAs in chip and package form.

Ordering No. 300455

AN 1055 Clock Recovery Using Si MMICs
One of the functions that must be performed by a fiber optic receiver is the retiming of the output data stream. This clock recovery function can be done using an active mixer (the IAM-81 or IAM-82 series) as a transition detector, a SAW filter, and a limiting amplifier (MSA, INA or IVA series). This application note discusses how these parts can be combined to construct a clock recovery circuit.

Ordering No. 5091-4917E

AN 1051 The IDA-07318 Laser Diode Driver
The IDA-07318 is a high speed silicon Monolithic Microwave Integrated Circuit (MMIC) laser diode driver (LDD) capable of operating at data rates up to 1.5 Gb/s. This application note discusses how to properly drive the IDA-07318 and how to use the modulation and prebias inputs on the laser driver. A brief overview of the theory of operation of the laser driver is covered.

Ordering No. 5091-4927E

Electrostatic Discharge Damage and Control

This is an abstract from Application Note AN-A004R: Electrostatic Discharge Damage and Control.

Parametric or functional failure of silicon or GaAs semiconductors can occur as a result of electrostatic discharge. Failures in bipolar transistors are characterized by low breakdown voltage or high leakage current. FET failures are characterized by resistive shorts. In some cases, leakage current may increase with applied voltage and reduced reverse breakdown voltage.

Static discharge is almost always associated with people, the types of material or clothes that people wear, and the handling equipment that comes into contact with the semiconductor devices.

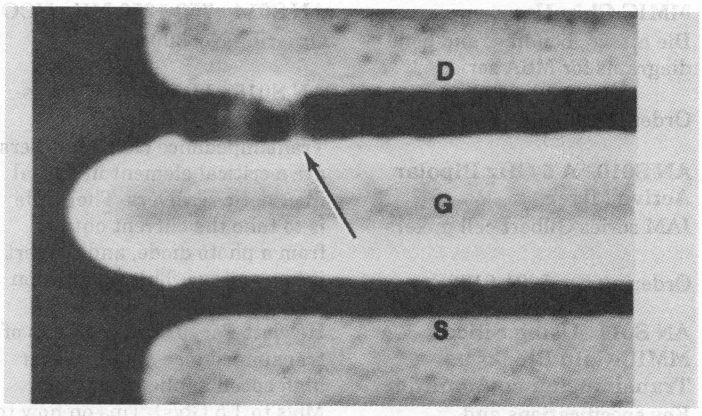
Recommendations for ESD Control

A partial listing of the most common generators of electrostatic charge is as follows:

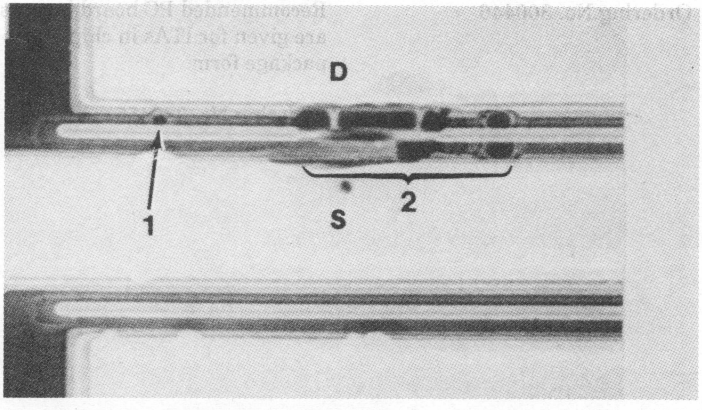
1. Work stations and areas
   a. Work benches and surface coverings (non-conductive)
   b. Floors (vinyl and all waxed surfaces)
   c. Chairs (ungrounded)
2. Operator clothing
   a. Clean-room garments (synthetics)
   b. Personal clothing (synthetics, silk, and wool)
3. Part and assembly packaging materials
   a. Polyethylene bags and films
   b. Polyethylene bubble pack and foam
   c. Plastic boxes, trays, and cabinets
4. Cleaning and test areas
   a. High velocity gas flow temperature chambers for drying

A partial list of corrective measures for use in neutralizing these generators of electrostatic charge is as follows:

1. Work stations and areas
   a. Use grounded conductive mats and plates over non-conducting surfaces
   b. Ground conductive surfaces
   c. Use grounded floor mats
   d. Apply grounded conductive grids or nets to chairs
   e. Use electrostatic precipitators in the immediate work area
2. Operator clothing
   a. Use wrist grounding strap (10 megohm ground)
   b. Use static-free smocks
   c. Use foot-grounded straps on leather soles
   d. Control of personal clothing may be necessary



T-Gate Channel with electrostatic damage (5.8KX).



An example of Hewlett-Packard Interdigitated metallization with electrostatic damage. (1) Initial static damage. (2) Side effect of discharge resulting from damage shown in (a).

3. Part and assembly packaging material
   a. Use conductive bags and wrapping
   b. Eliminate the use of bubble pack
   c. Use shorting collars, rings, or wrappers on individual parts prior to installation
4. Cleaning and test areas
   a. Eliminate high velocity gas flow over assemblies and parts

Last, but definitely not least, are some common mistakes and problems associated with operator grounding. Some of these problems may be difficult to prevent if not carefully looked into.

1. Remember to place ground straps back on after breaks and lunch before handling any susceptible parts.
2. Be sure that the wrist strap is securely attached to the wrist touching the skin snugly for adequate connection. Wrist straps do not work when attached over clothing.
3. Do not wear smocks or clothing made of materials which tend to generate high electrostatic potentials such as synthetics, wool, or silk.
4. Do not use alligator clips or any other kind of quick-disconnect fasteners to ground the operator to the mat, as they tend to fall off easily.
5. Do not use tangled or knotted ground cords.
6. Do not allow wrist straps to become corroded or dirty from excessive use. They must be cleaned or replaced regularly.

Mounting Considerations for Packaged Microwave Semiconductors

This is an abstract from Application Note AN-A006: Mounting Considerations for Packaged Microwave Semiconductors.

This application note discusses how electrical, mechanical, and thermal connections should be made for packaged microwave devices. There are two primary package types: small signal and power.

Small Signal Device Packages

Soldering Small signal microwave semiconductor packages can use the attachment of the leads to the electrical traces of the circuit board as the sole means of device mounting. Thus the lead attachment provides the mechanical, thermal, and electrical connections to the circuit. The most common way of attaching the leads of a package to a circuit board is by soldering.

The soldering process can subject devices to two different kinds of potentially dangerous stresses: electrical and thermal. A transistor or MMIC can suffer permanent electrical damage if any of its breakdown voltages are exceeded. This can happen when soldering equipment is not properly grounded, therefore MAKE SURE ALL SOLDERING EQUIPMENT IS AT GROUND POTENTIAL.

Thermal damage of various kinds can result if any of several critical temperatures are exceeded. Extremely high temperatures (above 425°C) will essentially cause new diffusions of the die, resulting in drastically changed electrical performance. Die attach temperatures establish a second critical temperature. Heating the package during soldering to above the die attach temperature (400°C for Si, 280°C for GaAs) can "float" the die, and seriously degrade the bond to the substrate. The third critical temperature is established by the maximum temperature the package can endure without damaging the integrity of the seal. Since there are a number of different types of seal (glass, epoxy, plastic, various solders) this temperature can vary from above 400°C to as low as 150°C.

In general the temperature at which the seal degrades is the lowest critical temperature in the die - package system, and establishes the maximum temperature ratings of the device. Each critical temperature is time dependent, and has associated with it a certain "dwell time" above which damage will occur.

Because of the relatively small volumes usually encountered in the microwave industry, hand soldering has been by far the most popular way of attaching a device to a circuit. Hewlett-Packard recommends the following guideline for this method: HAND SOLDERING SHOULD BE PERFORMED AT 250°C, IN LESS THAN 2 SECONDS PER LEAD. Hand soldering is the ONLY recommended method of soldering for any GaAs FET devices using low temperature solder seals.

Improved manufacturing technology and the advent of several consumer oriented microwave products has raised interest in more automated soldering techniques. These include wave soldering, vapor phase soldering, IR reflow soldering, and LASER reflow soldering, to name just a few. Rather than try to construct a recommended profile or each package type for each kind of soldering, Hewlett-Packard provides the information shown in Figures 1 through 3 to help the manufacturing engineer design a soldering profile. These curves show maximum recommended time versus temperature for the plastic (04, 05, 11, 84, 85, 86), micro-X ceramic (35, 36), and gold (10, 20, 23, 50, 70, 71) package families.

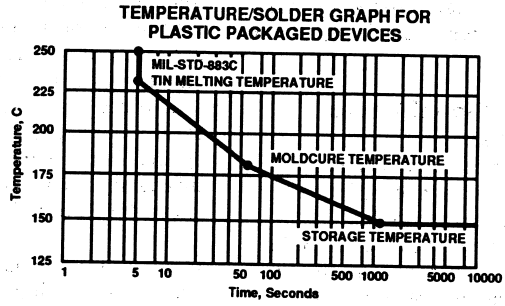


Figure 1.

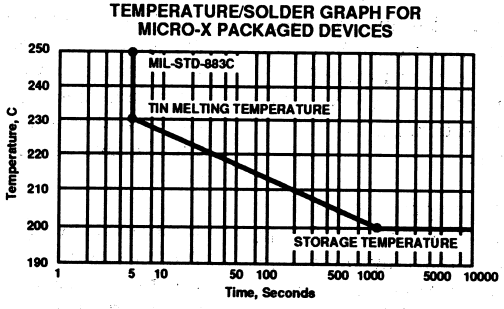


Figure 2.

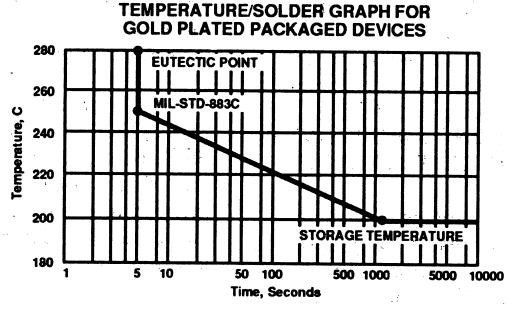


Figure 3.

Electrical and Thermal Considerations One extremely important electrical consideration should be kept in mind while mounting any microwave device. Any extra lead length becomes an additional undesired circuit element at microwave frequencies. This is especially important for ground lead length; seemingly small lengths of lead can result in deciBels of lost gain. In general all leads should mount flush with the pc board, with the smallest gap possible left between package body and circuit traces. For packages where the leads are not co-planar with the bottom of the package, it is better to make a hole in the pc board to allow for flush mounting than to bend the devices' leads.

Thermal considerations involved in the mounting of small signal devices are minimal. The device lead attachment provides sufficient heatsinking to these semiconductors. The output lead is the primary heat path for bipolar transistors and MODAMP™ MMICs for these devices the bottom of the die is the collector (output) meaning these devices tend to be die attached directly to the output trace. The ground leads are the primary heat path in GaAs FETs, since these devices have electrically isolated backsides and are therefore usually die attached directly to ground. Note that this means additional lead length not only degrades electrical performance, it also increases the operating temperature of a small signal device by increasing the case-to-ambient thermal resistance. 100 mils of lead length in free air can raise

the case-to-ambient thermal resistance of a small signal microwave package to between 150°C/W to 300°C/W. In contrast, properly mounted small signal devices should have case-to-ambient thermal resistances of less than 50°C/W.

Power Device Packages

Higher power devices come in specially designed packages that provide sufficient thermal conductivity to allow for reliable device operation at higher power dissipation levels. Packages for devices with bottom side electrical contacts (e.g. bipolar transistors) usually incorporate a Beryllium Oxide (BeO) ceramic substrate for superior thermal conductivity. Devices with electrically isolated backsides (e.g. GaAs FETs) do away with substrates under the die altogether, and mount directly to a rib of the heatsink brought up through the package for this purpose. Typically, power packages are much larger than are the small signal packages, due to the need for heat spreading. Thus such packages often incorporate some additional mechanical means of mounting beyond lead attachment.

Electrical and Thermal Considerations Electrical attachment of power packages is done in the same manner as for small signal packages: through soldering of the leads. The same hand soldering guideline of 2 seconds per lead at 250°C applies. The graph of time vs. temperature for gold packages applies to the power packages as well. Mechanical and thermal attachment vary with the package style. The 20 style package has an electrically isolated area of metallization on the bottom of the package. It is intended that this area be attached to the circuit heatsink, either by soldering, or using a good thermal conductive epoxy. Soldering should follow the time-temperature guidelines of the "gold" packages (see Figure 3). Although the soldering of the leads to the circuit board is sufficient for mechanical attachment of this package, this bottom connection is necessary for proper thermal operation.

Most other power devices come in packages with flanges that can be bolted directly to the circuit heatsink. For best thermal conductivity, the bottom of the flange should be coated with a THIN layer (10 mils or so) of thermal conductive grease. This will result in the lowest possible case-to-ambient thermal resistance (θ_{ca}) – usually giving a value less than 5°C/W. Note that a thick layer of thermal grease is almost as bad a thermal conductor as an air gap and would result in much higher values for θ_{ca}. Additionally, many flange packages use the flange as the ground connection to the device (see individual data sheets for terminal configuration) and excessive grease could degrade this important electrical contact.

Mechanical Considerations Improper mounting techniques, can mechanically damage power device packages. Hewlett-Packard suggests that the following methods be used when a power device is installed in a circuit.

When bolting a flange device into the circuit, it is important to tighten both bolts only until they are finger tight, then ALTERNATELY tighten until the flange is secured to the heat sink. Never tighten one bolt fully before inserting the second bolt; doing so can bow the package, resulting in miserable thermal contact or a cracked substrate.

It is also acceptable to solder the flange of a power device to the heatsink. The time vs. temperature guidelines for "gold" packages should also be used when soldering power devices in "gold" metalized packages (see Figure 3).

Leads of power devices should be soldered to the circuit traces only after the body of the device has been mechanically attached to the circuit. When a semiconductor already soldered to a pc board is bolted to a heatsink, extreme vertical shear forces can result at the package lead braze, fracturing the braze joint where the lead meets the package.

Following the above guidelines will help insure that your circuits built with Hewlett-Packard transistors and MMICs have the best possible longevity and reliability.

Transistor Chip Use

This is an abstract from Application Note AN-A005: Transistor Chip Use.

Packaging, Shipment, and Storage

Hewlett-Packard chips are supplied in two inch trays that use an elastomer as a carrier

medium. The chips are held in place by the surface tension of the elastomer. One corner of the tray is beveled to provide orientation for chip selection. Each chip tray is enclosed in a plastic box to protect the die during shipping. Up to 300 chips can be contained in a tray.

Chip carriers should be opened only at a clean, well-lighted station without fast moving air. A white working surface is recommended for best visibility. The chips are kept in place by the surface tension of the elastomer on which they are placed. Once the clamps have been removed, the pack should be set down on the surface and the lid removed. Then, the paper can slowly (to avoid static electricity generation) be lifted off the lower half. Occasionally a chip may work loose from the surface of the elastomer and turn upside down. If this happens, the chip should be carefully picked up with tweezers, turned over, and placed back on the elastomer. At this point the die can be counted or visually inspected. The reverse of the procedure outlined above should be used to close the die carrier pack prior to storage or die attach operations.

Die can be stored in the trays in which they are shipped. Die that will be stored for long periods of time (greater than 1 to 2 weeks) should be kept in a dry nitrogen atmosphere for optimum reliability. Hewlett-Packard chips use a gold based metal system that is very resistant to deterioration; none the less, the best practice is to always store die in an inert atmosphere.

Die Handling

Normal die handling is with tweezers to prevent contamination of the die attach surface. The brittleness of both silicon and GaAs makes the sharp edges of the chip susceptible to damage if too much pressure is applied. A good precaution is to use only very sharp tweezers with excellent point alignment when handling die (e.g. EREM type 5 SA). Inexperienced operators should practice with bonding samples, which can be obtained from Hewlett-Packard.

The surface of the die is protected with a layer of silicon nitride passivation. This layer provides sufficient scratch protection to allow vacuum picks to also be used for moving die, as long as reasonable care is taken in die handling.

Die Attach

The die attach process serves three functions. First, it mechanically attaches the die to the circuit substrate. Second, it electrically connects the output of the circuit to the trace on which the die is mounted. Third, it establishes the thermal path by which excess heat leaves the die. All three factors must be considered when selecting a die attach process.

Different procedures are used for silicon chips and GaAs devices. To attach a silicon chip, the chip and mounting surface are heated sufficiently for the gold of the mounting surface to mix with the gold backside metal on the chip and melt into the silicon of the chip, forming a gold-silicon eutectic bond. This technique is suitable because devices built on silicon can tolerate the relatively high temperatures needed for eutectic formation without electrical degradation. Eutectic die attach yields the best thermal transfer and lowest contact resistance of available die attach methods. The temperature sensitivity of

GaAs devices precludes the use of eutectic die attach; a low temperature gold alloy "solder-down" technique is used instead. In both cases the process should be carried out under an inert atmosphere blanket of forming gas or nitrogen to prevent die attach contamination.

Recommended Eutectic Die Attach Procedure

1. Set the heater block temperature to 410°C ± 10°C. This temperature should be measured at the point on the die attach stage where the package is to be heated; often there is a significant difference between the dial reading and the actual stage temperature.

2. Place the circuit or package into which the chip will be attached on the heater block. Allow sufficient time for it to heat thoroughly – typically 5 to 15 seconds depending on thermal mass.

3. Using tweezers or a vacuum collet, pick up the chip and orient it properly for placement on the mounting surface.

4. Place the chip directly on the mounting surface (in general preforms are not needed for eutectic die attach). Scrub with a back-and-forth motion, being careful not to scratch the top surface of the chip.

Continue scrubbing until wetting occurs; this should occur within three to four scrubs.

5. If wetting does not occur, check that the heater block is at the correct temperature, that the inert atmosphere is present, and that all gold surfaces are free of contamination. The inert atmosphere should be heated to around 250°C to prevent it from cooling the die to below the gold-silicon eutectic forming temperature of 387°C.

6. When wetting occurs, perform one circular scrub to insure wetting of the chip perimeter. 100 flow should be visible around the die. Carefully remove the tweezers or collet from the die.

7. Remove the circuit or package from the heater block and allow it to cool in air. The total time for die attach should be *less* than 10 seconds. Maintaining the die at the 410°C die attach temperature for longer than this can lead to reduced device reliability.

Recommended "Solder-down" Die Attach Procedure

1. Set the heater block temperature to 300°C ± 10°C. This temperature should be measured at the point on the die attach stage where the package is to be heated; often there is a significant difference between the dial reading and the actual stage temperature.

2. Place the circuit or package into which the die will be attached on the heater block. Allow sufficient time for it to heat thoroughly – typically 5 to 15 seconds depending on thermal mass.

3. Pick up a gold-tin (Au-Sn) preform and place it on the circuit or package in the die attach location. Use a sufficient quantity to insure good wetting and to produce a fillet around the die.

4. Using tweezers or a vacuum collet, pick up the chip that is to be die attached and orient it properly for placement on the mounting surface.

5. Place the chip on the mounting surface and scrub with a back-and-forth motion, being careful not to scratch the top surface of the chip. Continue scrubbing until wetting occurs; this should occur within three to four scrubs. If wetting does not occur, check that the heater block is at the correct temperature, that the inert atmosphere is present, and that all gold surfaces are free of contamination.

6. When wetting occurs, perform one circular scrub to insure wetting of the chip perimeter. 100% flow should be visible around the die. Carefully remove the tweezers or collet from the die.

7. Remove the circuit or package from the heater block and allow it to cool in air. The total time for die attach should be *less* than 10 seconds. Maintaining the die at the 300°C die attach temperature for longer than this can lead to reduced device reliability.

Wire Bonding

Electrical connections to the die are in general made by wire bonds. The output electrical connection to silicon products is most often made through the die attach, but can sometimes also be made through a topside wire bond (e.g. in the case of MODAMP™ chips). The bond pad size and metal adhesion strength of Hewlett-Packard chips are compatible with either gold-ball bonding or wedge bonding. Either technique may be used when building chip assemblies.

Recommended Ball Bonding Procedure

1. If thermocompression ball bonding, set the heater block temperature to 300° ± 10°C for silicon product, or to 260° ± 10°C for GaAs product. If thermosonic (ultrasonic) ball bonding, set the heater block to 150° ± 10°C for either silicon or GaAs product.

2. Use prestressed (annealed) gold wire between 0.0007 to 0.001 inches in diameter.

3. Calibrate the bond force as follows:

Wire Diameter	Bond Force	MWB
0.0007"	15-20 grams	20 ± 2
0.001"	20-30 grams	25 ± 2

4. Proceed with bonding according to machine specifications. For common (emitter, source, or ground) wire bonds, start with the ball on the circuit bonding surface and bond to the common bond pad on the chip, then continue (stitch bond) to a second contact with the circuit bonding surface. Keep both loops of this common bond low and short.

Recommended Wedge Bonding Procedure

1. Set the heater block temperature to 300° ± 10°C for silicon product or to 260° ± 10°C for GaAs product. (Note: If the wedge is heated, the heater block temperature should be lowered slightly from this setting. The exact temperature setting will need to be determined empirically, and will vary from machine to machine.)

2. Use prestressed (annealed) gold wire between 0.0005 to 0.001 inches in diameter.

3. Tip bonding pressure should be between 15 and 20 grams and should not exceed 20 grams. The footprint that the wedge leaves on the gold wire should be between 1.5 and 2.5 wire diameters across for a good bond.

4. Proceed with bonding according to machine specifications. Bonds should be made from the circuit element to the chip bonding pads to minimize pad damage. Also, bonds should be made to the source and drain pads of a FET prior to making the bond to the gate pad, to minimize the potential or electrostatic discharge damage.

Assembly and Handling Procedures for PIN Diode Chips

1. Storage

Devices should be stored in a dry nitrogen purged dessicator or equivalent.

2. Cleaning

If required, surface contamination may be removed with electronic grade solvents such as freon (T.F. or T.M.C.), acetone, deionized water, and methanol used singularly or in combinations. Typical cleaning times per solvent are one to three minutes. DI water and methanol should be used (in that order) in the final cleans. Final drying can be accomplished by placing the cleaned dice on clean filter paper and drying with an infrared lamp for 5-10 minutes. Acids such as hydrofluoric (HF), nitric (HNO_3), and hydrochloric (HCl) should not be used.

The effects of cleaning methods/solutions should be verified on small samples prior to submitting the entire lot.

Following cleaning, dice should be either used in assembly (typically within a few hours) or stored in clean containers in a reducing atmosphere or a vacuum chamber.

3. Die Attach

a. Eutectic

Eutectic die attach can be accomplished by "scrubbing" the die with/without a preform on the header to combine with the silicon in the die. Temperature is approximately 400°C, with heating times of 5-10 seconds. (Note–times and temperature utilized may vary depending on the type, composition, and heat capacity of the header or substrate used.) This method is recommended for the HPND-000X series.

b. Epoxy

For epoxy die-attach, conductive silver-filled epoxies are recommended. This method can be used for all Hewlett-Packard PIN chips.

4. Wire Bonding

Either ultrasonic, thermosonic or thermocompression bonding techniques can be employed. Suggested wire is pure gold, 0.7 to 1.5 mil diameter.

Bonding and Handling Procedures for Beam Lead Diodes

1. Storage

Under normal circumstances, storage of beam lead diodes in HP supplied waffle/gel packs is sufficient. In particularly dusty or chemically hazardous environments, storage in an inert atmosphere desiccator is advised.

2. Handling

In order to avoid damage to beam lead devices, particular care must be exercised during inspection, testing, and assembly. Although the beam lead diode is designed to have exceptional lead strength, its small size and delicate nature requires that special handling techniques be observed so that the devices will not be mechanically or electrically damaged. A vacuum pickup is recommended for picking up beam lead devices, particularly larger ones, e.g., quads. Care must be exercised to assure that the vacuum opening of the needle is sufficiently small to avoid passage of the device through the opening. A #27 tip is recommended for picking up single beam lead devices. A 20X magnification is needed for precise positioning of the tip on the device. Where a vacuum pickup is not used, a sharpened wooden Q-tip dipped in isopropyl alcohol is very commonly used to handle beam lead devices.

3. Cleaning

For organic contamination use a warm (<75°C) rinse of trichloroethane followed by a cold rinse in acetone and methanol. Dry under infrared heat lamp for 5-10 minutes on clean filter paper. Freon degreaser may replace trichloroethane for light organic contamination.

- Ultrasonic cleaning is not recommended.
- Acid solvents should not be used.

4. Bonding

Thermocompression: See Application Note 979 "The Handling and Bonding of Beam Lead Devices Made Easy". This method is good for hard substrates only.

Wobble: This method picks up the device, places it on the substrate and forms a thermocompression bond all in one operation. This is described in MIL-STD-883, Method 2017, and is intended for hard substrates only. Equipment specifically designed for beam lead wobble bonding is available from KULICKE and SOFFA in Horsham, PA.

Resistance Welding or Parallel-GAP Welding: To make welding on soft substrates easier, a low pressure welding head is recommended. Suitable equipment is available from HUGHES, Industrial Products Division in Carlsbad, CA.

Epoxy: With solvent free, low resistivity epoxies (available from ABLESTIK in Gardena, CA, MICON in Lexington, MA, and many others) and improvements in dispensing equipment, the quality of epoxy bonds is sufficient for many applications. Equipment is available from ADVANCED SEMICONDUCTOR MATERIALS AMERICA, INC., Assembly Products Group in Chandler, AZ (Automatic), and WEST BOND in Orange, CA (Manual).

Reflow: By preparing the substrate with tin or solder plating, reflow soldering can be suitably performed using a modified wire bonder. The probe is used as a soldering tip. WEST BOND or UNITEK bonders make suitable bonds.

5. Lead Stress

In the process of bonding a beam lead diode, a certain amount of "bugging" occurs. The term *bugging* refers to the chip lifting away from the substrate during the bonding process due to the deformation of the beam by the bonding tool. This effect is beneficial as it provides stress relief for the diode during thermal cycling of the substrate. The coefficient of expansion of some substrate materials, specifically soft substrates, is such that some bugging is essential if the circuit is to be operated over wide temperature extremes.

Thick metal clad ground planes restrict the thermal expansion of the dielectric substrates in the X-Y axis. The expansion of the dielectric will then be mainly in the Z axis, which does not affect the beam lead device. An alternate solution to the problem of dielectric ground plane expansion is to heat the substrate to the maximum required operating temperature during the beam-lead attachment. Thus, the substrate is at maximum expansion when the device is bonded. Subsequent cooling of the substrate will cause bugging, similar to bugging in thermocompression bonding or epoxy bonding. Other methods of bugging are preforming the leads during assembly or prestressing the substrate.

MODAMP™ Silicon MMIC Chip Use

This is an abstract from Application Note AN-SOO9: MODAMP™ Silicon MMIC Chip Use.

Die Topography

MODAMP MMICs share a common topology, shown in Figure 1. Two bipolar transistors (Q1 and Q2) are connected in Darlington configuration. Shunt (R_F) and series (R_E) resistive feedback are used to set both the gain and the impedance match of the structure. Resistors connecting the bases of Q1 (R_B) and Q2 (R_{bias}) to ground complete the DC bias network. Some geometries have additional resistors (R_{C1}, R_{C2}) connected to the collector of Q2 to allow for optional on-chip biasing. Figure 2 identifies these components on a typical MODAMP chip outline drawing.

The bond pad connected to the base of Q1 is the input to the circuit. The bond pad connected to R_E, R_B, and R_{bias} is the amplifier's common (or ground) terminal. Electrically, the output of the circuit is the collector of Q2. Since the MMIC is built with conventional vertical bipolar technology, the

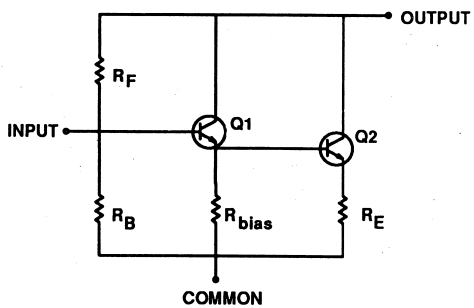
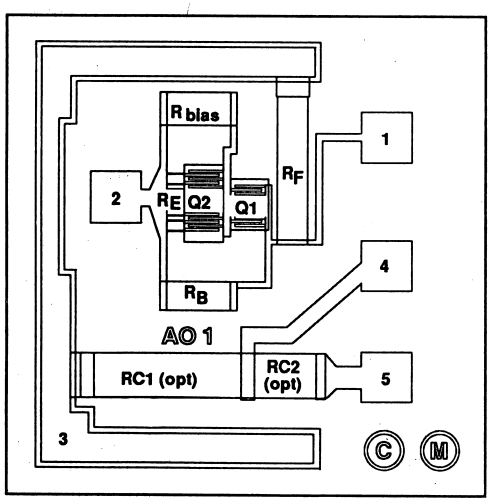


Figure 1. MODAMP Equivalent Circuit Schematic.



1- INPUT
2- COMMON
3- OPTIONAL OUTPUT
4- +12V ON-CHIP RC
5- +15V ON-CHIP RC

Figure 2. Typical MODAMP Chip Outline Labeling Components and Bond Pads. (MSA-0100 shown as an example).

entire bottom surface of the chip is a shared collector contact for the two transistors of the Darlington, and therefore serves as the output terminal of the MMIC. For convenience, a topside collector contact is also provided for designers who would rather wire bond the output connection to the chip. The remaining bond pads are bias options that are not normally connected in typical chip use.

Use of Optional On-ChipBiasResistors

The most common way of biasing MODAMP MMICs is through a dropping resistor from a fixed voltage supply. The biasing resistor acts as a feedback element that stabilizes the DC operating point over temperature. The MSA-0100 MSA-0200, MSA-0300, MSA-0600, and MSA-0700 MODAMP geometries include optional on-chip resistors that can be used to bias the MMIC from a fixed voltage supply. For most designs, these on-chip resistors are left unconnected, and the bias is supplied through an external (off-chip) bias resistor. To make use of the on-chip bias option, wire bond the appropriate bond pad on the MMIC to a circuit trace that will supply the appropriate voltage. The bond pad nearest to the RF input bond pad is for use with a nominal +12 volt supply; the remaining bond pad is for use with a nominal +15 volt supply (see Figure 3).

The MSA-0600 and MSA-0700 geometries have 3 bond pad options: a +5 volt pad which is nearest to the RF input bond pad, a +12 volt pad, and a +15 volt pad which is furthest from the RF input pad. The length of the bond wire is not critical. A long wire is, if anything, preferable as the added series inductance it provides improves the effectiveness of the bias feed as an RF choke. The circuit will no longer require external bias resistors or chokes or biasing the MODAMP MMIC, although an external inductor in series with the bias resistor usually improves P_{1dB} and gain performance. A bypass capacitor at the power supply rail is still recommended.

Several factors should be considered before using the on-chip bias resistors. First, the values of these resistors will vary from one wafer run to another; the nominal tolerance is ±15%. Hewlett-Packard does

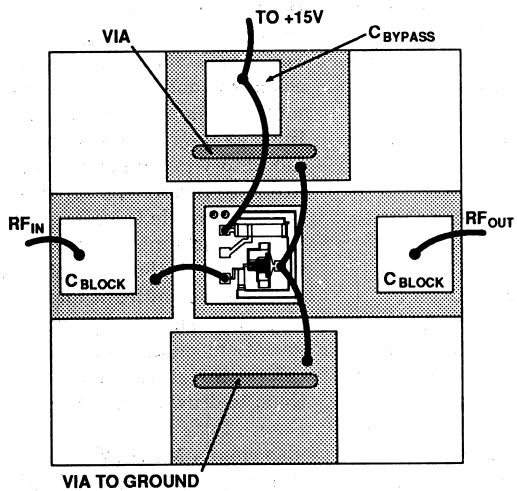


Figure 3. Representative Bond Scheme for Use of On-chip Bias Resistor (+15 V option).

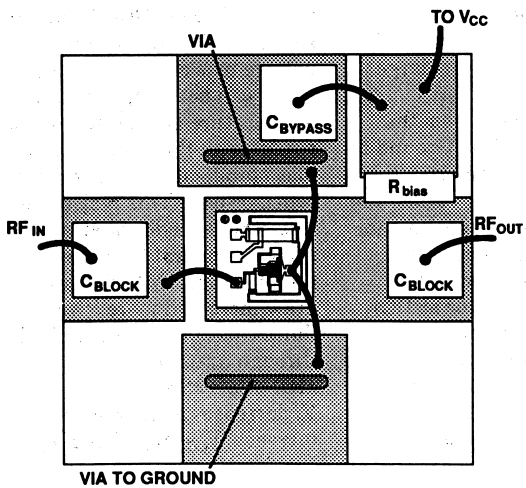


Figure 4. Typical One Stage MODAMP MMIC Circuit.

not guarantee either the values of these resistors or the performance that will be obtained if they are used. Next, these resistors are made of polysilicon, which has a temperature coefficient of -0.08%/°C. Since this coefficient is negative, the on-chip resistors provide less feedback at high temperatures (and hence less bias stability) than would an external carbon resistor possessing a positive temperature coefficient. Finally, using these resistors creates a significant new on-chip heat source that will raise the operating temperature of the transistors in the MODAMP MMIC. This will decrease some aspects of RF performance (especially P_{sat}) and reduce the MTTF of the MMIC.

Sample Circuits

Since MODAMP MMICs are matched 50 Ω gain blocks, no special RF circuit design is required when using these chips. The MODAMP MMIC chip is die attached directly on the output trace, and the input connection is made by a wire bond. The ground connections are also made by wire bonds. Solid metallization should be brought up on either side of the die to allow for stitch bonding on the common bond. The bond attach points should be connected to the backside ground of the circuit through multiple vias.

Both input and output transmission lines need to be DC blocked; blocking capacitors should be of a high enough value to present a low series impedance across the frequency range over which the amplifier will operate. Remember to include the effect of parasitic inductance when calculating capacitor impedance. MOS capacitor die, ceramic chip capacitors, or gap capacitances in the transmission line traces can all be used as blocking capacitors.

MODAMP MMIC chips are DC biased in the same manner as packaged MODAMP products; refer to the next section on Biasing MODAMP MMICs or to Applications Note AN-S003: Biasing MODAMP™ MMICs for more information.

A sample layout for a one stage MODAMP MMIC amplifier is shown in Figure 4. This layout uses MOS chips for blocking capacitors, ceramic chips for bypass capacitors, and thin film resistors for the bias feed. No additional choke inductance is used.

Conclusion

The simplicity and performance offered by MODAMP chips, combined with the reduced size and lower parasitics of chip-and-wire assembly technology, create microwave circuitry with superior performance.

Biasing MODAMP™ MMICs

This is an abstract from Application Note AN-A003: Biasing MODAMP MMICs.

The bias point of the MODAMP MSA-Series MMIC can best be described by specifying the total device current I_d.

Both power and gain can be adjusted by varying I_d. Curves of typical performance as a function of bias are shown on the individual MODAMP MMIC data sheets.

Bias Circuitry Options

Once an appropriate bias point has been chosen, circuitry must be provided to ensure that the MODAMP MMIC operates at that bias point. To be effective, this circuitry must establish an appropriate bias point across the entire operating temperature range the MODAMP MMIC will experience. The internal resistors on the MMIC have a temperature coefficient -0.08%/°C; the on-chip transistors increase in β at a rate of +0.07%/°C. If the bias current I_d is to remain constant over a broad temperature range, the bias circuitry must decrease the device voltage V_d at higher temperatures and increase V_d at lower temperatures.

Three possible biasing schemes are described in detail below.

Voltage Source On Collector The simplest bias scheme available is to provide a fixed voltage to the collector or output terminal of the MODAMP MMIC. This voltage can be supplied either from a voltage regulator or from a power supply. It must be provided through an RFC (Radio Frequency "Choke," or high-value inductor) to keep the high frequency signal isolated from the DC circuitry. A large-value capacitor (e.g. 1 μF) should be connected from the DC side of the RFC to Ground to provide a low impedance path to any signal that does get past the RFC. DC blocking capacitors (or alternatively transformers, if the MSA is to be operated at very low frequencies or at DC) must be used to isolate both the input of the MSA from the drive source and the output of the MSA from the load. The entire circuit is shown in Figure 1.

Because of its very narrow temperature operating range and sensitivity to V_d this bias scheme is not appropriate for most production circuits. It finds its major applications in laboratory testing of devices utilizing variable power supplies to provide the bias. With this bias scheme, temperature variations on the order of 25°C will cause significant alterations in performance; temperature variations on the order of 75°C can destroy devices by causing them to draw too much current. Device-to-device variations may also yield a MODAMP MMIC that draws an excessively high current if V_d is fixed, even at room temperature.

Collector Bias Stabilization Resistor The fixed collector voltage bias circuit described above can be changed into a temperature-compensated bias circuit with the addition of a bias stabilization resistor in the collector feed. This resistor acts as a simple feedback element. As the temperature increases, the MODAMP MMIC tries to draw more and more current. Since this current is supplied through a resistor, the MODAMP MMIC bias voltage V_d decreases as I_d tries to increase: V_{CC} stays fixed; I_d

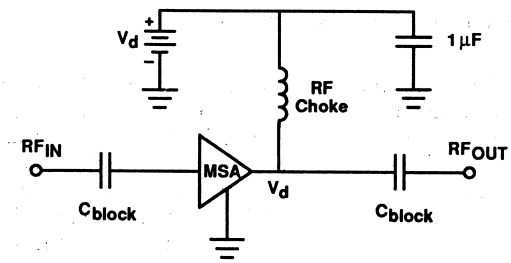


Figure 1. Fixed Collector Voltage Bias Circuit.

increases with temperature causing the voltage drop I_dR_C across R_C to increase, thus lowering V_d and "throttling back" on the bias current I_d, Note that the amount of feedback is proportional to the voltage drop across R_C, and hence to the value of R_C. For effective compensation over normal operating temperature ranges (-25°C to +100°C), a voltage drop of at least 4 volts is recommended.

Remember that R_C itself will change in resistance as the temperature changes. By selecting a bias resistor with an appropriate temperature coefficient the temperature compensation of this circuit can be "fine tuned." Carbon composite resistors typically have a temperature coefficient of +0.0001%/°C, and work particularly well as bias stabilization resistors.

A side benefit of using a bias stabilization resistor is that it is often of high enough impedance that an RFC is no longer needed to keep the high frequency signal out of the DC bias. It is recommended that an RFC still be used if the MODAMP MMIC is being used near saturation; otherwise RC appears in parallel with the load resistance and can cause enough of a shift in load impedance to reduce both gain and saturated power by 1 to 2 dB.

The circuitry needed for a bias stabilization resistor scheme is shown in Figure 2.

Active Bias Active bias circuitry can be used to provide temperature stability without requiring the large voltage drop or relatively high disputed power needed with a bias stabilization resistor. A simple realization using a resistively-biased PNP transistor as a current source is shown in Figure 3.

In this circuit R_1 and R_2 form a resistive divider that establishes the bias point of the PNP bias transistor. R_3 provides a "bleed path" for any excess bias current; it is a safety feature that can be omitted from minimum element realizations of this circuit. D_1 is also an optional element; its purpose is to provide temperature compensation by tracking the voltage

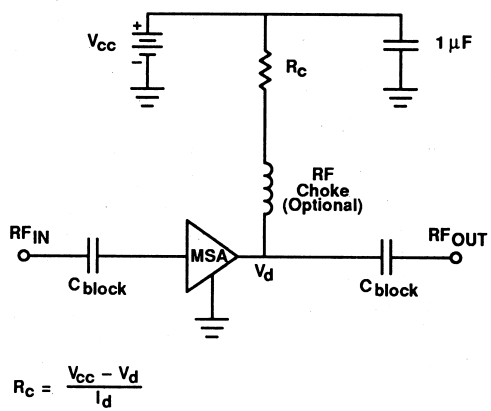


Figure 2. Collector Bias Stabilization Resistor Bias Circuit.

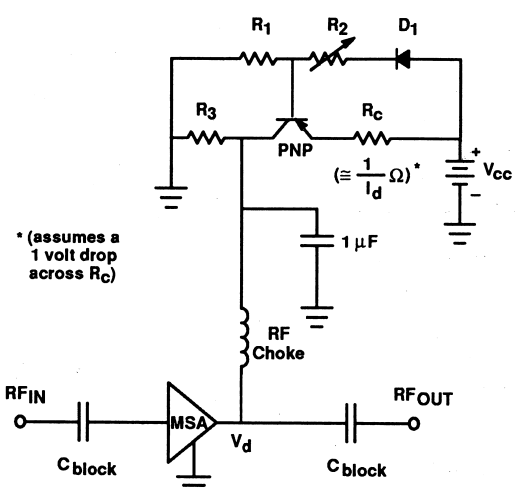


Figure 3. Active Bias

variation with temperature of the emitter-to-base junction of the PNP bias transistor. For this reason, when it is included it is often realized using the E-B junction of a second PNP transistor identical to the bias transistor, connected with its collector-base junction shorted.

R_C is a feedback element that keeps I_d constant. If the device current starts to increase, the voltage drop across R_C also increases, turning off the E-B junction of the PNP transistor, and hence decreasing the bias voltage V_d applied to the MSA. For best circuit operation, there should be at least a 0.5 to 1 volt drop across R_C. The PNP transistor is acting in the saturated mode with both junctions forward biased. The voltage drop needed across the emitter to collector junction of this transistor will therefore be equal to its V_{CEsat} – typically only several tenths of a volt. Thus, the total voltage difference needed between V_{CC} and V_d is only about 1.3 volts for this circuit, as compared to the 4 volts or so needed by the bias stabilization resistor for good bias stability over temperature.

A side effect of the PNP bias transistor operating in the saturated mode is that this bias requires some extra "charge up" time at turn-on and "discharge" time at turn-off. How much extra time is required will depend on the time constants of the PNP transistor.

Systems requiring wide dynamic range operation or AGC (automatic gain control) often require that the MSAs operate at variable operating points. If R_2 is made variable this bias scheme will work well for such applications.

Measurements

The data on the devices presented in this catalog were taken by measurements performed in 50 ohm test fixtures. These measurements may be divided into four basic groups: S-parameters, noise parameters, power parameters and thermal parameters. Except for power parameters, these subjects are covered in detail in the Hewlett-Packard Transistor Primer Series. The following are brief summaries of the topics.

S-Parameters

Scattering parameters are a group of measurements taken at different frequencies which represent the forward and reverse gain, and the input and output reflection coefficients of a microwave component when the input and output ports of the component are terminated in equal impedances – usually 50 ohms. Some pertinent definitions are as follows:

Magnitude–The length of the vector in the polar plane.

Angle–The direction of the vector in the polar plane.

dB–10 $\log_{10}$ (Power Magnitude) or 20 $\log_{10}$ (Voltage Magnitude)

S_{11}–S-parameter input reflection coefficient – Expresses the magnitude and phase of the input reflection coefficient with the input and output ports terminated in a pure resistance of 50 ohms.

S_{21}–S-parameter forward transfer coefficient – Expresses the forward voltage gain magnitude and phase measured with the input and output ports terminated in a pure resistance of 50 ohms.

S_{12}–S-parameter reverse transfer coefficient – Expresses the reverse voltage gain (sometimes called isolation) magnitude and phase, measured with the input and output ports terminated in a pure resistance of 50 ohms.

S_{22}–S-parameter output reflection coefficient – Expresses the magnitude and phase of the output reflection coefficient with the input and output ports terminated in a pure resistance of 50 ohms.

Stability factor, given by

$$k = \frac{1 + |D|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}|\,|S_{12}|}$$

where $D = S_{11}\,S_{22} - S_{21}\,S_{12}$

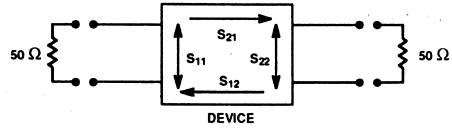


Figure 1. Two Port S-Parameters

If $k > 1$ and $|D| < 1$ then the two-port that k describes is unconditionally stable for all terminations with non-negative resistance. If $k < 1$ some terminations exist which will cause the two-port to oscillate.

The utility of S-parameters as a complete description of a device's small signal (linear) performance has been generally accepted by the microwave industry. S-parameters are preferred over other 2-port parameters (Z, Y, H, etc.) as a means of characterization because they are easier to measure: the terminations required usually result in stable device operation, and commercial equipment designed specifically for S-parameter measurement is readily available. None the less, accurate S-parameter device characterization is difficult to obtain for a number of reasons.

Since a device's performance characteristics are a function of both its bias point and its operating temperature, it follows that the S-parameter description used to describe the device's behavior should also vary with bias point and temperature. For this reason, both the bias and the temperature need to be specified. In general, Hewlett-Packard provides S-parameters measured at the recommended operating bias and at +25°C ambient temperature. In cases where operation at different bias levels might be appropriate, more than one description is generally given.

For a number of reasons, S-parameters will vary from device to device. The major reasons are process variations, material inconsistencies and assembly irregularities. A normal distribution of S-parameters is approximately ±10%. Hewlett-Packard publishes data which is representative of a "typical" unit. This data is based on the measurement of many devices taken from different wafers and several process lots.

The actual measurement of the device is made in a test fixture using an HP8510 Network Analyzer. The style of the fixture will greatly influence the measurement. To achieve the best results, the device should be measured in the medium in which it will be used. Since the majority of Hewlett-Packard's customers design in microstrip, this is the style of fixture that is currently being used to characterize the devices. Such a fixture is shown in Figure 2 where the device is mounted between two 50 ohm microstrip substrates which are sandwiched between two 50 ohm connector assemblies. Note that this fixture features excellent grounding and may have a shorter ground path than does a production circuit. The designer may wish to add some common lead inductance to the published S-parameters to compensate for this effect.

If the S-parameters that are published are to be repeated, the conditions under which they are taken must be duplicated as closely as possible. Measurements should be taken on the Inter-continental Microwave fixture (from the 1000 series or 2000 series) that Hewlett-Packard is currently using and measurements should be made

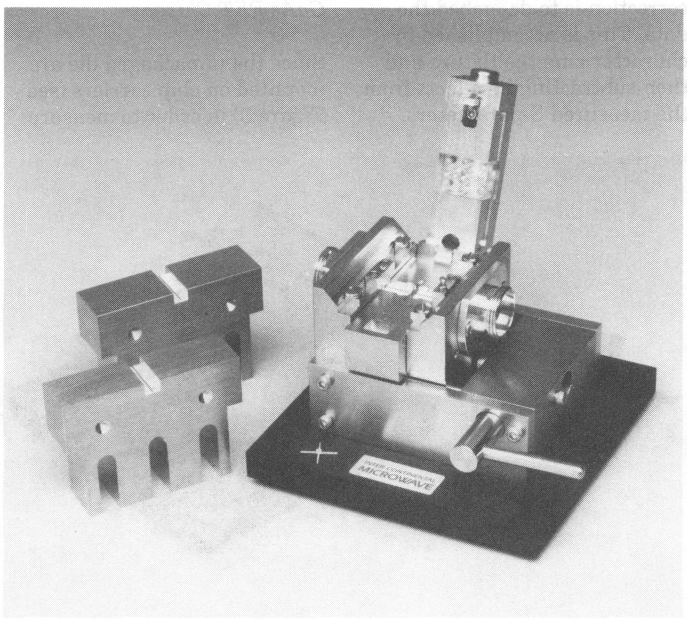


Figure 2. Typical 50 Ohm Test Fixture

on a HP8510 Network Analyzer. The device should be biased at the same bias as specified in the catalog, and the same method of correcting for the effects of the test fixture must be applied.

The simplest method for correcting is the reference plane extension (rpe) technique. Hewlett-Packard uses this method to characterize its silicon products up to 6 GHz. This method assumes a lossless, reflectionless, dispersionless fixture with the input and output having identical properties. The measured S-parameters are simply corrected mathematically by the software to account for the electrical length of the fixture. This electrical length can be determined by either measuring the distance to an open circuit or 1/2 the distance of a "through" line.

A more accurate method of correction is to de-embed the data. This is accomplished by characterizing the fixture and then subtracting its effects from the measured S-parameters. Though generally more time consuming than the reference plane extension methods, this technique must be used to obtain accurate S-parameters above 8 GHz.

Hewlett-Packard uses the "through-delay" method of de-embedding S-parameters for GaAs devices. The "through" is a 50 ohm microstrip transmission line with an electrical length equal to the sum of the input and output substrates used in the fixture. The "delay" is a transmission line similar to the "through" with a 50 mil longer physical length. Since this technique compares electrical lengths it is inaccurate at frequencies where the "through" and the "delay" are essentially the same length (below 1 GHz). For further explanation of this technique refer to the Hewlett-Packard Application Note *Measurement and Modeling of GaAs FET Chips.*

Since the unpackaged die are mounted on chip carriers (see Figure 3) in order to measure their S-parameters, it is impossible to 100% test this kind of device before shipping. Instead, S-parameters are measured on a sample of devices at the wafer qualification step. The chip S-parameters that Hewlett-Packard lists in this catalog are based on chip carrier measurements, and include the inductances associated with the bond wires (about 0.5 nH gate and drain bond and 0.15 nH source bond for a FET and about 0.5 nH base bond and 0.2 nH emitter bond for a bipolar device).

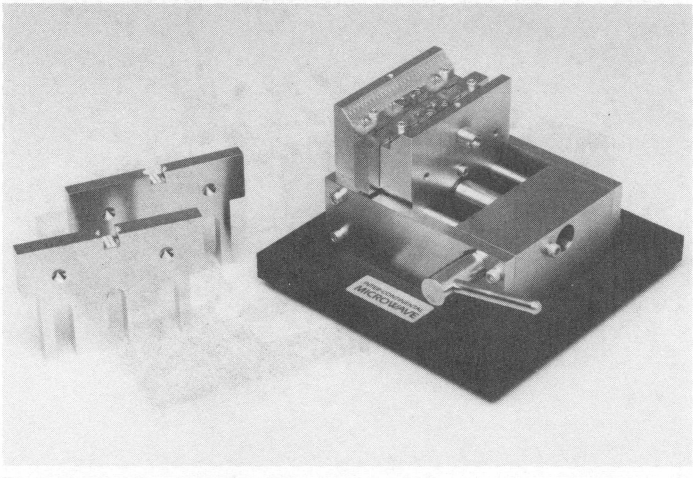


Figure 3. Test Carrier Used to Characterize Unpackaged GaAs FET Chips.

Noise Parameters

The noise performance of a transistor can be described by four noise-parameters in the noise figure equation:

$$F = F_{MIN} + \frac{R_N}{G_G} | V_G - Y_{OPT} |^2$$

where:

F_{MIN} is the minimum transistor noise figure

R_N is the noise resistance in ohms

$Y_{OPT} = G_{OPT} + jB_{OPT}$ is the required generator admittance at the input port for minimum noise figure

$Y_{GP} = G_{GP} + jB_{GP}$ is the generator admittance at the input port

$\Gamma_{OPT} = \frac{Y_O - Y_{OPT}}{Y_O - Y_{OPT}}$ is the generator reflection coefficient corresponding to Y_{OPT}

These parameters are measured in a 50 ohm system with a low

loss tuner at the input and output ports. The transistor is biased for minimum noise, the output tuner set for maximum gain and the input tuner set for minimum noise figure. The measurement of F_{MIN} must include a correction for the tuner loss, as well as for second stage noise correction.[1] The input tuner is later measured for the G_{OPT} noise parameter, which is referred to the transistor input reference plane by translating the reflection coefficient by and equivalent circuit model of the test fixture.

The parameter R_{NI} is determined by measuring the 50 ohm noise figure:

$$F_{50} = F_{MIN} + 50R_N\,|0.02 - Y_{OPT}|^2$$

$$R_N = \frac{F_{50} - F_{MIN}}{50\,|0.02 - Y_{OPT}|^2}$$

This data is further verified by measuring F at several other tuner settings which are later measured for Γ_G or Y_G. As an additional check on the noise data, an internal device modeling program (AMCAP) is used to generate the theoretical noise parameters from the small-signal equivalent circuit. This simulation can also be used to generate noise parameters at other frequencies.

By plotting the noise figure circles in the Γ_G plane, the accuracy of both S-parameter and noise-parameter data can be verified. Figures 4 and 5 show these circles for four Hewlett-Packard low noise devices, AT-41435, AT-60535, ATF-10136 and ATF-13136 at appropriate frequencies when biased for best noise figure in a 50 ohm system.

Power Parameters

The power characteristics of devices in this catalog consist primarily of two parameters: P_{1dB} and G_{1dB}. P_{1dB} is the device output power at one dB gain compression. G_{1dB} is the one dB compressed gain.

Power measurements were made using Class A bias points. This kind of operation gives best linearity, and is typical of device use. In general P_{1dB} can be improved by increasing bias current though tradeoffs with MTTF, noise figure, IP_3, or other parameters may be involved. Improved efficiency can be obtained with the discrete devices by operating them Class C.

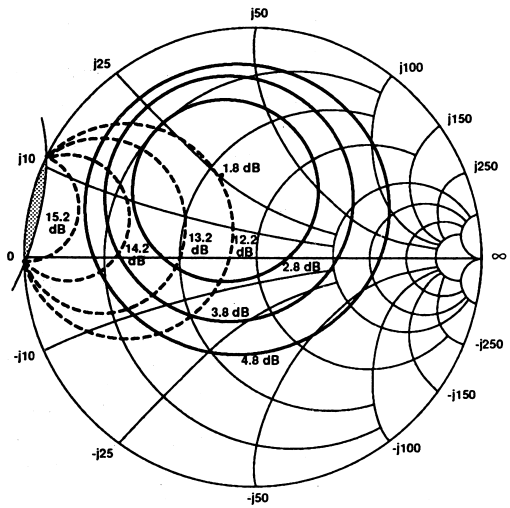
All silicon product power measurements were made in 50 ohm coaxial test fixtures. Bias was provided through HP bias tees. Separate collector and base supplies were used to bias the discrete devices; MODAMP MMICs were biased from a power supply through an appropriate dropping resistor: in all cases the bias point was set to the catalog value of I_C or I_D under DC (no signal) conditions, and not subsequently adjusted during measurements. Note that some amount of current pulling can occur at P_{1dB} using these bias schemes.

Power measurements for small signal and unmatched power GaAs FETs and GaAs MMICs were made in 50 ohm coaxial test fixtures. Bias was provided through HP bias tees. Each device was biased to the catalog value of V_{Ds} and I_D under DC (no signal) conditions. Small signal devices were tested using separate drain and gate supplies with a common ground point and active feedback via an operational amplifier to prevent current pulling. Discrete power devices used separate supplies with no feedback, allowing some amount of current pulling at P_{1dB}.

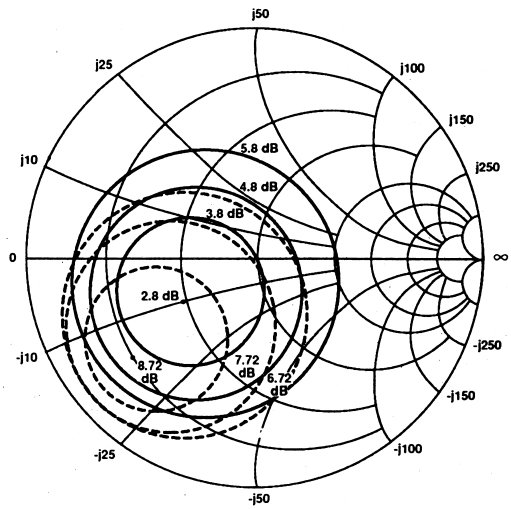
Tuners were used to present the correct large signal impedances to discrete and unmatched GaAs MMIC devices to obtain P_{1dB} and G_{1dB}. Both tuners were adjusted to obtain maximum output power with the device set at the catalog nominal value ($P_{1dB} - G_{1dB}$). The input drive level was then decreased by 10 dB, and the nominal small signal gain was measured. (Measurements for Silicon MODAMP MMICs did not use tuners, as these devices are already matched for operation in a 50 ohm system.) The input drive level was then increased until the measured gain had decreased by one dB from the nominal small-signal value. This gain value was recorded as G_{1dB}. The power level at which this gain was measured was recorded as P_{1dB}.

For best power performance, discrete devices must be matched to the appropriate large signal impedances Γ_{GP} (at the input) and Γ_{LP} (at the load). These impedances are frequency, bias, and power level dependent. They are best obtained by direct measurement of the tuners used in the P_{1dB} setup described above, translating the measured tuner

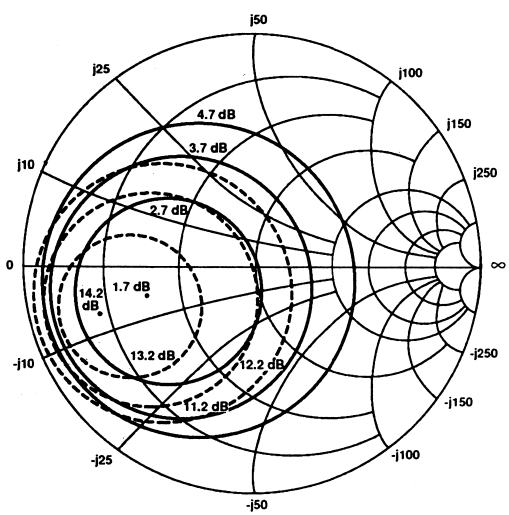
[1]Eric W. Strid, "Measurement of Losses in Noise-Matching Networks" *IEEE Transactions on MTT*, Vol. MTT-29, March 1981, pp 247-252.



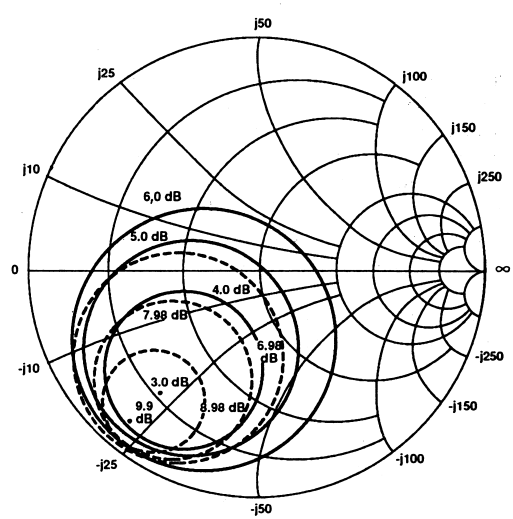
AT-60535: f = 2 GHz, V_{CE} = 8 V, I_C = 2 mA



AT-60535: f = 4 GHz, V_{CE} = 8 V, I_C = 2 mA



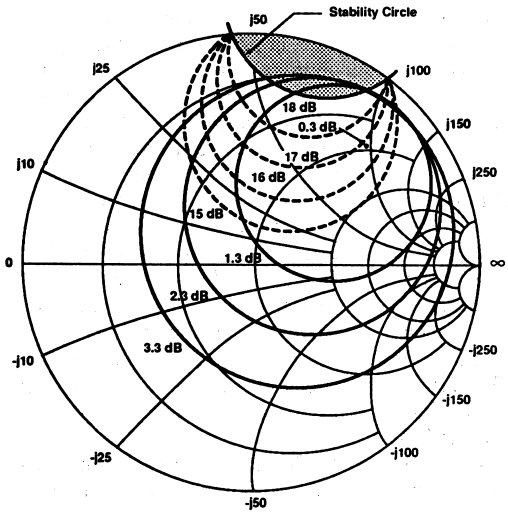
AT-41435: f = 2 GHz, V_{CE} = 8 V, I_C = 10 mA



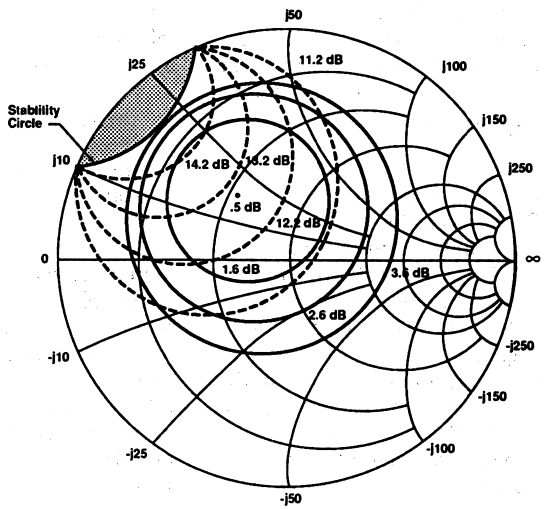
AT-41435: f = 4 GHz, V_{CE} = 8 V, I_C = 10 mA

KEY: ———— Noise Circles; – – – – – – – Gain Circles

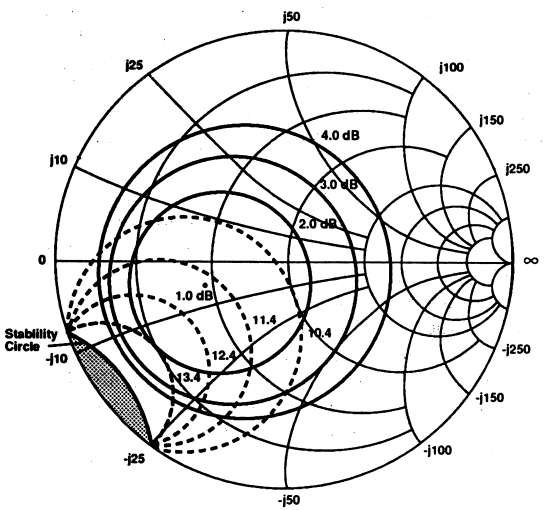
Figure 4. Noise Figure Circles and Available Gain Circles in the Γ_G Plane.



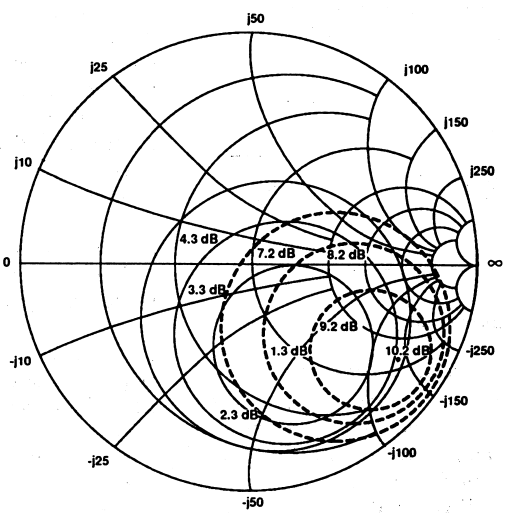
ATF-10136: f = 2 GHz, V_{DS} = 2 V, I_{DS} = 20 mA



ATF-10136: f = 4 GHz, V_{DS} = 2 V, I_{DS} = 20 mA



ATF-13136: f = 8 GHz, V_{DS} = 3 V, I_{DS} = 20 mA



ATF-13136: f = 12 GHz, V_{DS} = 3 V, I_{DS} = 20 mA

KEY: ———— Noise Circles; – – – – – – – – Gain Circles

Figure 5. Noise Figure Circles and Available Gain Circles in the Γ_G Plane.

impedance back to the reference plane of the device. For bipolar devices, if measured large signal impedances are not available Γ_{GP} and Γ_{LP} may be estimated as follows.

Γ_{GP} is approximately equal to S_{11}*. Γ_{LP} can be obtained from the simple output model shown in Figure 6. This figure shows an equivalent circuit for the output of the transistor; this impedance should be matched to the system impedance (usually 50 Ω). For this model R is given by $(0.9\ V_{CE})\ 2/(8P_{OUT})$ for Class A operation where V_{CE} is the device collector to emitter voltage and P_{OUT} is the desired output power. C is approximately 1.5 C_{CB} (C_{CB} measured at $V_C/2$ is a slightly better determination). L depends on package style and is about 1 nH for microstripline packages and about 1.5 nH for larger power packages.[2]

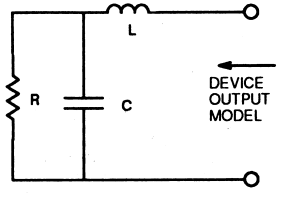


Figure 6. Large-Signal Load Model.

Thermal Resistance

Although a simple concept, the thermal resistance of a device is a complicated parameter that can be defined in several ways. It will vary with the operating temperature of the device being measured, the way in which the junction and case temperatures are specified, the bias point at which the device is operating, the presence or absence of an AC input signal to the device, and the environment.

Hewlett-Packard uses the following simple formula to define thermal resistance θ_{jc}:

$$\theta_{jc} = [T_J - T_C] / P_T$$

In this equation, T_J is the hottest junction or channel temperature on the device being measured. T_C is the case temperature if the device is a packaged component, or the temperature of the surface on which the device is mounted for an unpackaged die. P_T is the total power dissipated in the device, and is equal to the DC and RF power into the device minus the RF power out of the device.

There is also a thermal resistance θ_{ca} that characterizes the heat transfer between the case of the device and the ambient environment. Since this number depends at least as heavily on how the device is mounted, the surface (heatsink) it is mounted on, air flow and near-by heat sources as it does on the device itself, values for θ_{ca} are not included in this catalog.

A variety of measurement techniques exist for determining values for θ_{jc} Hewlett-Packard's preferred method is the liquid crystal technique[3], as it has the required 1 to 2 µm resolution needed for measuring the small device structures found in microwave devices. Although not used for any product in this catalog, infrared (IR) methods can be used in applications that do not require resolution below about 15 µm.

Several electrical methods also exist that rely on the measurement of a thermally sensitive parameter such as delta V_{BE} or delta V_{GS}, but have the drawback of providing an average as opposed to maximum junction temperature. Hewlett-Packard uses an electrical method[4] to determine the thermal resistance of plastic encapsulated transistors, which cannot be measured with methods requiring visual inspection of the die. The thermal resistance of plastic encapsulated MMICs is arrived at by combining separate determinations of die thermal resistance and package heat transfer characteristics.

In the liquid crystal method, the package lid is removed and the die surface is coated with a nematic liquid crystal layer. The active junction area is observed through a microscope having crossed linear polarizers in the incident and reflected light paths. Because of the change in optical properties at its melting point T_{NI} (nematic to isotropic transition), the liquid crystal regions of the die that are above and below the melting point can be visually identified. The device is biased and heated until the specified area exceeds the transition temperature and the thermal resistance is calculated from the measured T_{NI}, T_C, and P_T. Gallium Arsenide products are measured at a channel temperature of 150°C. Silicon products are measured at a junction temperature of +100°C. The θ_{jc} values in this

[2]William Mueller, "Linear Amplifier Design – some General Considerations," *RF Design*, March 1980, pp. 37-41.
[3]K. J. Negus, R. W. Franklin, M. M. Yovanovich, "Thermal Modeling and Experimental Techniques for Microwave Bipolar Devices," IEEE Semiconductor Thermal and Temperature Measurement Symposium, Feb. 7-9, 1989, pp. 63-72.

data book for silicon products are specified at a case temperature of +25°C; a mathematical conversion is performed using a model[5] based on the temperature dependent thermal resistance of the silicon die.

The case temperature T_C is determined by direct measurement with a small thermocouple. For devices in small signal packages with straight leads, the thermocouple is mounted as near as possible to the body of the case on the lead with the highest thermal conductivity path to the die. For plastic surface mount packages with gull wing leads, the thermocouple is mounted to the bottom of the lead. This is the collector lead for silicon bipolar transistors, the output lead for MSA-series silicon MMICs and the ground lead for all other silicon MMICs and GaAs devices.

For hermetic surface mount packages with gull wing leads, the thermocouple is mounted to the bottom of the package. In power packages, the thermocouple is mounted on the flange (230 mil flange package) or on the bottom (200 mil BeO package) of the BeO disc. To determine the thermal resistance of an unpackaged die, the device is either mounted in a package with excellent thermal transfer properties (e.g. the 230 mil flange package), or on a ceramic die carrier.

For additional information on thermal resistance theory and measurements, contact Hewlett-Packard for available applications notes.[6,7]

Device Modeling

Hewlett-Packard makes use of computer models to design high frequency transistors and to predict their performance in various applications. Both linear and non-linear models are used. Linear models apply at one specific set of (non-changing) bias and temperature conditions, and simulate small signal performance in the frequency domain. Non-linear models add the capability of predicting performance changes as a function of temperature or bias, and also allow for analysis of transient behavior. These models work in the time domain, and require much more data and computational time than do linear models.

Bipolar Models

Both linear and non-linear models are available for Hewlett-Packard's bipolar based products. The two kinds of models have the same basic form. Each starts with the intrinsic transistor function. The non-linear model is a SPICE simulation, and uses that program's intrinsic transistor model (Q in the accompanying schematics). The linear model uses a current controlled current source α, the intrinsic emitter resistance R, and the intrinsic emitter capacitance C. The current generator α is described by the equation

$$\alpha = [\alpha_O \exp(-j2\pi f T_C)] / [1 + j\, f/f_b].$$

α_O is given by $(\beta - 1)/\beta$ where β is the DC current gain of the transistor; for Hewlett-Packard's bipolar process a typical value for α is 0.99 (corresponding to a DC β of 100). The frequency roll-off of the current generator can be calculated from the base transit time; for this process this number is 7 psec, corresponding to a corner frequency f_b of 22.7 GHz. The time delay associated with the current generator (T_C) comes from the collector delay, and is a function of bias; values for T_C are included in the tables that follow. The intrinsic emitter resistance can be calculated from the bias as R = 26/(I_C in mA). The intrinsic emitter capacitance is proportional to area, and can be approximated by multiplying the SPICE # for Q in the tables that follow by 0.005 pF.

A transmission line structure of resistors (R_{B1}, R_{B2}, R_{B3}) and capacitors (C_{D1}, C_{D2}, C_{D3}) is added to the basic transistor to simulate the significant electrical length of the base region at microwave frequencies. By using a diode model (similar to a varactor model) rather than a fixed capacitor in this "distributed base" description, the non-linear model obtains the capability of simulating the variation in base capacitance as a function of bias voltage. Both models then ad d collector and emitter contact resistances (R_C and R_E). Both versions of the power device model have an additional emitter ballast resistor (R_{bal}), and a dynamic output capacitance (C_{D4}).

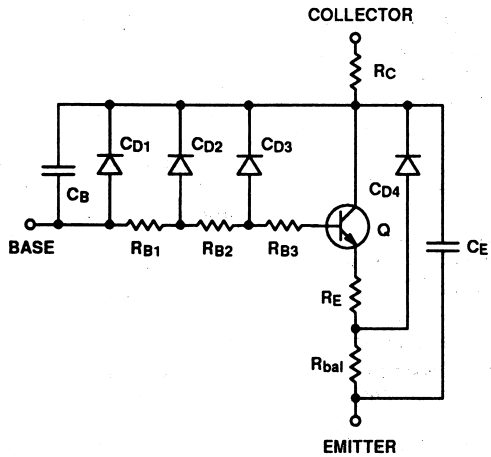
[4]ibid, pg 65.
[5]ibid, pg 67.
[6]Hewlett-Packard Transistor Primer III (Thermal Properties), publication ATP-1040.
[7]Hewlett-Packard Transistor Primer III-A (Thermal Resistance), publication ATP-1072.

All models are completed by adding the bond pad capacitances (C_E and C_B).

A schematic showing the SPICE equivalent circuit used to model the discrete bipolar transistors is given in Figure 1. Figure 2 shows the linear model equivalent circuit. Table 1 lists the values of the circuit elements for the linear model at both low noise and power biases and for the non-linear SPICE model.

MODAMP™ silicon MMICs consist of two bipolar transistors in a Darlington connection, embedded in a network of resistors to provide both feedback and DC bias. Models for these devices consist of two active device models (Q_1 and Q_2), values for the feedback resistors (R_E and R_F), values for the bias resistors (R_B and R_{bias}), and the parasitic capacitors (C_{P1}, C_{P2}, C_{P3}, and C_F) associated with the structure. Note that no C_B or C_E elements exist in the device simulations incorporated in the MODAMP device models as the bond pad capacitances are included at the MMIC level. The interconnection for these elements is shown schematically in Figure 3. Some MODAMPs (the MSA-05XX, MSA-09XX, MSA-10XX, and MSA-11XX) require DC blocking capacitors in series with the shunt feedback resistor to prevent excess power dissipation on the chip. A schematic for this kind of MODAMP is shown in Figure 4. Tables 2 and 3 give the value of the model elements of both kinds of MODAMPs.

The SPICE simulations require a set of SPICE parameters, which are included in Table 4.

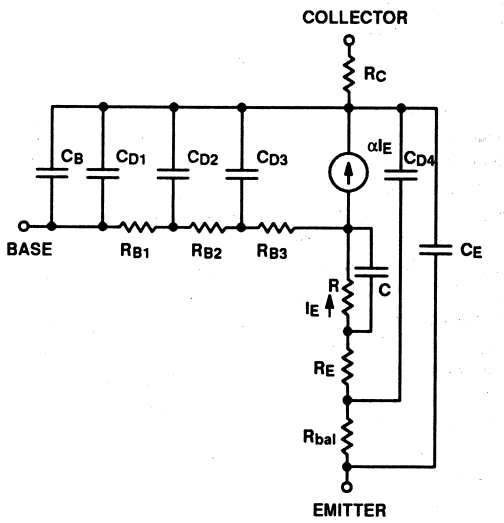


C_{D1}, C_{D2}, C_{D3} use a diode model to represent voltage variable capacitance in the base.

Both diode and transistor models are scaled per unit area; the number of such unit areas needed is given (in parenthesis) in Table 1.

R_{bal} (ballast resistance) and C_{D4} (voltage variable output capacitance) appear only in the model for power devices.

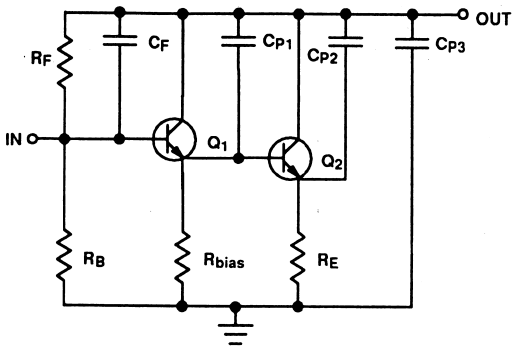
Figure 1. Discrete Transistor SPICE Equivalent Circuit.



C_{D1}, C_{D2}, C_{D3} represent the base capacitance at a specific collector voltage (typ. 8 V).

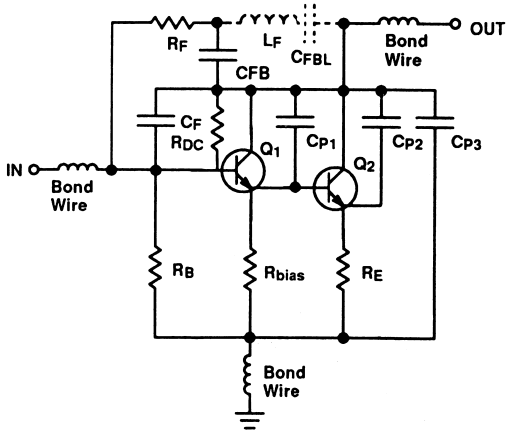
For TOUCHSTONE™ α is a CCCS, where M = .99; A = 0;
R1 = R in Table 1;
R2 = 1E8; F = 22.7; T = T_C in Table 1. Note that R and T are bias dependant.

Figure 2. Discrete Transistor Linear Model Equivalent Circuit.



Note that Q_1 and Q_2 are active devices, and each represents a discrete transistor simulation of the kind described above. Either linear or non-linear simulation may be used.

Figure 3. MODAMP MMIC Equivalent Circuit.



Elements shown in dashed lines are off-chip components.

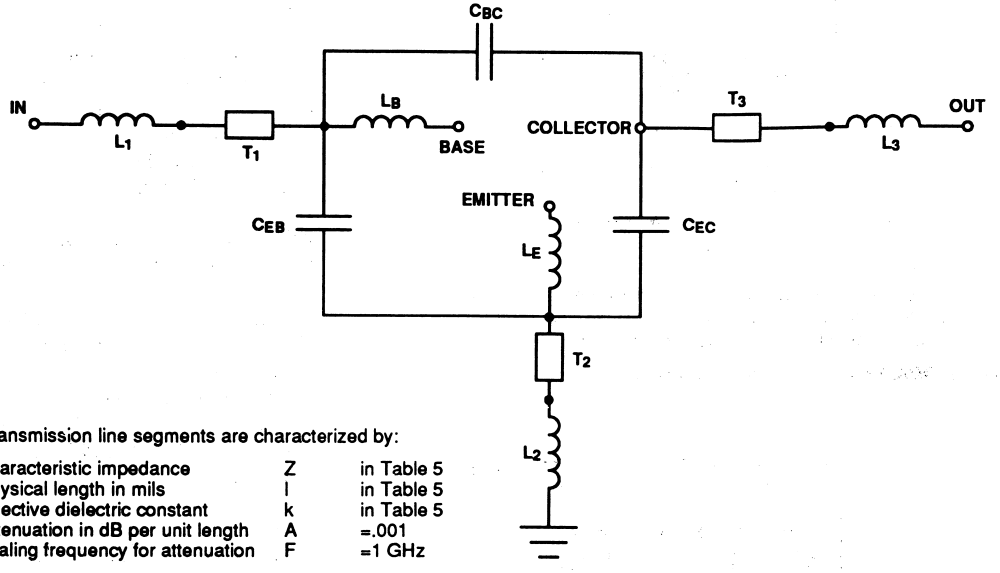
Figure 4. Equivalent Circuit for MODAMP MMICs with DC Blocking Capacitor in Feedback Path.

Since the same fabrication process is used for the bipolar products described here, one basic set of parameters can be used in the models. Changes in epi material between the discrete transistors, the MODAMP MMICs, and the power devices do, however, result in changes in the parameters BF, VA, TF, and PTF for these three groups of devices. To facilitate the use of a "process description" set of parameters, a "unit transistor" is defined for each kind of device (QMSA for MODAMP MMICs, a QDIS for discretes, QPWR for power devices). Individual device models are then constructed using an appropriate number of these unit blocks. The non-linear base capacitances are built up from a "unit diode" model (DMOD) in a similar fashion. The number in parenthesis in the columns labeled Q, C_{D1}, C_{D2}, C_{D3}, and C_{D4} in Tables 2 and 3 are the number of unit transistors or unit diodes needed in the completed SPICE model.

All of the above models are chip level models. To complete device simulations, appropriate package models must be added. The bond wires that connect the device chip to the package (or substrate in the case of chip use) must also be simulated, as they are NOT included in the above chip models.

The standard Hewlett-Packard package model treats the leads and internal metallization as transmission lines (T_1, T_2, and T_3). Coupling capacitances between the device terminals is included (C_{EB}, C_{BC}, C_{EC}), as are the emitter and base bond wires (L_E and L_B). As the bottom (collector) of the transistor chip is typically die attached directly to the output lead metallization, there is usually no collector bond wire in the simulation. The package model is completed by adding small amounts of series inductance (L_1, L_2, L_3) to each device terminal, to simulate the short lengths of lead that occur between circuit and device package. The completed package model is shown schematically in Figure 5. Values for model elements are given in Table 5. The same package models are used for both linear and non-linear simulations.

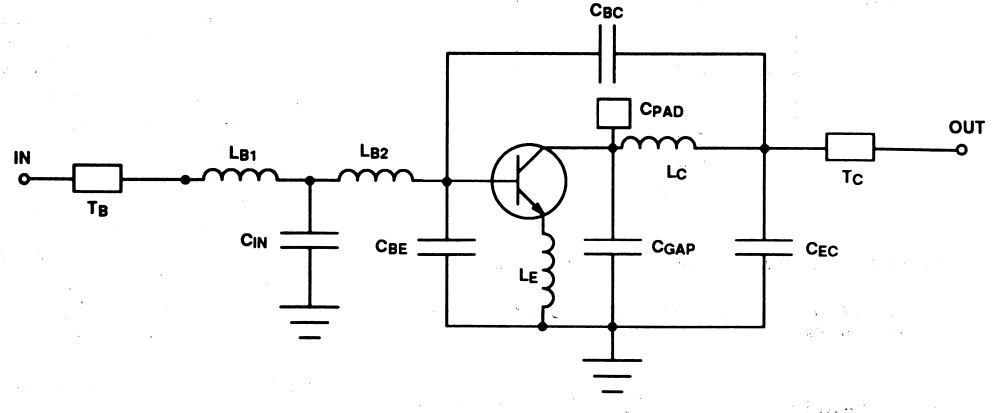
The style 23 package used for power devices has a different topology from the other packages. It can also incorporate an input matching capacitor (C_{IN}). The equivalent circuit for this package is shown in Figure 6. The associated values shown are for the AT-64023 device.



Transmission line segments are characterized by:

characteristic impedance	Z	in Table 5
physical length in mils	l	in Table 5
effective dielectric constant	k	in Table 5
attenuation in dB per unit length	A	=.001
scaling frequency for attenuation	F	=1 GHz

Figure 5. Bipolar Transistor Package Model Equivalent Circuit.



T_B:	ZO=40 Ω	L=80 mils	k=10	A=.001	F=1	L_C:	L=.4 nH				
L_{B1}:	L=.35 nH					T_C:	ZO=40 Ω	L=80 mils	k=10	A=.001	F=1
C_{IN}:	C=3.0 pF					C_{BC}:	C=.03 pF				
L_{B2}:	L=.2 nH					C_{EC}:	C=.03 pF				
L_E:	L=.1 nH					C_{EB}:	C=.03 pF				
C_{PAD}:	ZO=25 Ω	L=100 mils	k=6.8	A=.001	F=1	C_{GAP}:	C=.1 pF				

Figure 6. Package Equivalent Circuit For AT-64023.

```
DIM
  FREQ          GHZ
  RES           OH
  CAP           PF
  IND           NH
  LNG           MIL

CKT
  ! MSA0835 MODEL

  !EQUIVALENT CIRCUIT FOR Q1
  RES_R1Q1      10    11          R=2.6     TC1=0.8E-3
  RES_R2Q1      11    12          R=9.1     TC1=1.2E-3
  RES_R3Q1      12    13          R=7.9     TC1=1.8E-3
  S1PA_D1Q1     10    15          [MODEL=DMOD 377]
  S1PB_D2Q1     11    15          [MODEL=DMOD 218]
  S1PC_D3Q1     12    15          [MODEL=DMOD 138]
  RES_RCQ1      14    15          R=5       TC1=0.6E-3
  RES_REQ1      16    17          R=.63     TC1=0.6E-3
  S2PD_Q1       13    15    17    [MODEL=QMOD 156]
  DEF3P         10    14    16    Q1

  !EQUIVALENT CIRCUIT FOR Q2
  RES_R1Q2      20    21          R=1.0     TC1=0.8E-3
  RES_R2Q2      21    22          R=3.3     TC1=1.2E-3
  RES_R3Q2      22    23          R=2.8     TC1=1.8E-3
  S1PA_D1Q2     20    25          [MODEL=DMOD 782]
  S1PB_D2Q2     21    25          [MODEL=DMOD 609]
  S1PC_D3Q2     22    25          [MODEL=DMOD 386]
  RES_RCQ2      24    25          R=5       TC1=0.6E-3
  RES_REQ2      26    27          R=.22     TC1=0.6E-3
  S2PD_Q2       23    25    27    [MODEL=QMOD 438]
  DEF3P         20    24    26    Q2


  !MODEL FOR MODAMP MMIC CHIP
  RES_RFCH      30    31          R=6000    TC1=-.8E-3
  CAP_CFCH      30    31          C=.0001
  RES_RBCH      30    32          R=1600    TC1=-.8E-3
  Q1_XQ1CH      30    31    33
  RES_RBIASCH   32    33          R=85      TC1=-.8E-3
  Q2_XQ2CH      33    31    34
  RES_RECH      32    34          R=.0001   TC1=-.8E-3
  CAP_CP1CH     31    33          C=.086
  CAP_CP2CH     31    34          C=.021
  CAP_CP3CH     31    32          C=.103
  DEF3P         30    31    32    CHP                   !chip model

  !MODEL FOR PACKAGED CHIP - UX PKG (35)
  IND_LINP      40    41          L=0.05
  TLINP_T1P     41    42          Z=65 L=30 K=7 A=0 F=1
  IND_LBP       42    43          L=0.6
  CAP_CBCP      42    47          C=0.02
  CAP_CBEP      42    44          C=0.01
  IND_LEP       45    44          L=0.3
  TLINP_T3P     44    46          Z=30 L=15 K=7 A=0 F=1
  IND_LGP       46    0           L=0.01
  CAP_CECP      44    47          C=0.03
  TLINP_T2P     47    48          Z=65 L=50 K=7 A=0 F=1
  IND_LDP       48    49          L=.05
  CHP_XCHPP     43    47    45
  DEF2P         40    49          MSA                   ! packaged chip

  !PACKAGED CHIP USED IN CIRCUIT
  MSA_XA0835    50    53
  DEF2P         50    53          A0835

SOURCE
  A0835         IVS_VIN     52 0  AC=1      TRAN=SIN(0 100MV 1GHZ) PWR=(0 10 5 1E9 1.5E9 5E8)
  A0835         RES_RS      51    52        R=50
  A0835         CAP_CS      51    50        C=1000
  A0835         IVS_VCC     56    0         DC=12
  A0835         RES_RC      55    56        R=90          TC1=.1E-3
  A0835         IND_LCK     53    55        L=1E4
  A0835         CAP_COUT    53    54        C=1000
  A0835         RES_RL      54    0         R=50

CONTROL
      A0835     OPTIONS MU=0.3 LVLTIM=1 ACCT LIST NODE
      A0835     OP
      A0835     AC LIN 12 .5GHZ 6GHZ
!     A0835     TRAN .02NS 2NS
!     A0835     PWR VIN RS
!     A0835     TEMP -55 27 100
      Q1        INCLUDE QMSA.MOD
      Q2        INCLUDE QMSA.MOD
      CHP       INCLUDE QMSA.MOD
      MSA       INCLUDE QMSA.MOD
      A0835     INCLUDE QMSA.MOD

SPICEOUT
      A0835     AC      I(ALL) V(ALL)
      A0835     SP      XA0835 MSA0835S.S2P  50
!     A0835     TRAN    ALL
!     A0835     TRAN    I(ALL)
!     A0835     PWR     RL 54 0
```

Figure 7A. Typical MW SPICE MSA-0835 Simulation.

```
!SPICE PARAMETERS FOR MODAMP TRANSISTOR PROCESS
.MODEL DMOD D IS=1E-25 CJO=2.45E-16 VJ=.76 M=.53 BV=45 IBV=1E-9
.MODEL QMOD NPN BF=90 BR=5 IS=1.65E-18 VA=20 TF=12PS CJE=18E-16
+ PE=1.01 ME=.60 PTF=25 XTB=1.818 VTF=6 ITF=.3MA IK=.1333MA XTF=4
+NF=1.03 ISE=5E-15 NE=2.5
```

Figure 7B. QMSA-MOD File Used in Figure 7A.

Table 1. Bipolar SPICE and Linear Model Equivalent Circuit Element Values.

Model		Geometry:		21400	41400	42000	60100	60200	60500	64000	00500	01600
Resistors:	R_{B1}	value	Ω	0.6	1.0	0.7	19.6	10.2	4.2	0.4	4.9	1.6
		temp coeff	ppm/°C	0.8E-3	0.8E-3	0.8E-3	0.8E-3	0.8E-3	0.8E-3	0.8E-3	0.8E-3	0.8E-3
	R_{B2}	value	Ω	2.2	3.1	2.2	51.7	25.9	10.3	1.2	8.9	2.8
		temp coeff	ppm/°C	1.2E-3	1.2E-3	1.2E-3	1.2E-3	1.2E-3	1.2E-3	1.2E-3	1.2E-3	1.2E-3
Nominal Value @ 25°C	R_{B3}	value	Ω	1.9	2.7	1.9	37.5	18.8	7.5	0.98	4.9	1.5
		temp coeff	ppm/°C	1.8E-3	1.8E-3	1.8E-3	1.8E-3	1.8E-3	1.8E-3	1.8E-3	1.8E-3	1.8E-3
	R_C	value	Ω	5	5	5	5	5	5	1.3	5	5
		temp coeff	ppm/°C	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3
	R_E	value	Ω	0.45	0.24	0.17	3.32	1.66	0.66	0.06	0.39	0.14
		temp coeff	ppm/°C	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3
	R_{bal}	value	Ω	–	–	–	–	–	–	1.65	–	–
		temp coeff	ppm/°C	–	–	–	–	–	–	0.8E-3	–	–
Capacitors:	C_B	–	pF	0.010	0.032	0.034	0.025	0.025	0.026	0.082	0.157	0.176
	C_{D1}	SPICE	#		(782)	(1051)	(197)	(242)	(377)	(2287)	(546)	(1262)
		lin. @ 8 V	pF	0.015	0.059	0.080	0.015	0.018	0.029	0.122[1]	0.041	0.096
all SPICE non-linear capacitors use DMOD	C_{D2}	SPICE	#		(629)	(899)	(103)	(206)	(515)	(4692)	(1586)	(5074)
		lin. @ 8 V	pF	0.035	0.048	0.068	0.008	0.016	0.039	0.251[1]	0.120	0.384
	C_{D3}	SPICE	#		(365)	(522)	(26)	(52)	(131)	(1360)	(189)	(605)
		lin. @ 8 V	pF	0.015	0.023	0.040	0.002	0.004	0.010	0.071[1]	0.014	0.046
	C_E	–	pF	0.010	0.032	0.034	0.025	0.025	0.026	0.108	0.157	0.176
	C_{D4}	SPICE	#	–	–	–	–	–	–	(1717)	–	–
		lin. @ 16 V	pF	–	–	–	–	–	–	0.104	–	–
Active Device:	Q	model	–	QDIS	QDIS	QDIS	QDIS	QDIS	QDIS	QPWR	QDIS	QDIS
		SPICE	#		(420)	(600)	(30)	(60)	(150)	(1560)	(228)	(730)
LN: low noise bias	R	value @ N	Ω	–	2.6	2.6	51.5	28.5	12.9	–	5.2	0.8
		value @ G	Ω	–	1.1	0.8	10.4	5.2	2.6	0.3	1.3	0.5
	C	value @ 8 V	pF	0.998	2.1	3.00	0.15	0.30	0.75	7.8[1]	1.14	3.65
G: gain or power bias	T_C	value @ LN	psec	–	6.9	6.9	6.9	6.9	6.9	–	6.9	7.1
		value @ G	psec	–	7.3	7.3	7.9	7.9	7.3	11.35	8.2	8.1

Note:
1. 64000 values given at 16 V.
2. Data for ATF-21400 can be found on page 2-27 of the catalog.

Table 2. MODAMP MMIC Linear and SPICE Models.

Model				Geometry:		A01 Q1	A01 Q2	A02 Q1	A02 Q2	A03 Q1	A03 Q2	A04 Q1	A04 Q2
Active Device Subcircuits	Resistors	Nominal Value @ 25°C	R_{B1}	value	Ω	5.0	3.1	5.0	2.5	3.1	1.7	1.7	1.0
				temp coeff	ppm/°C	0.8E-3	0.8E-3	0.8E-3	0.8E-3	0.8E-3	0.8E-3	0.8E-3	0.8E-3
			R_{B2}	value	Ω	13.2	8.2	13.2	6.6	8.2	4.4	4.4	2.6
				temp coeff	ppm/°C	1.2E-3	1.2E-3	1.2E-3	1.2E-3	1.2E-3	1.2E-3	1.2E-3	1.2E-3
			R_{B3}	value	Ω	9.9	6.2	9.9	5.0	6.2	3.3	3.3	2.0
				temp coeff	ppm/°C	1.8E-3	1.8E-3	1.8E-3	1.8E-3	1.8E-3	1.8E-3	1.8E-3	1.8E-3
			R_C	value	Ω	5	5	5	5	5	5	5	5
				temp coeff	ppm/°C	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3
			R_E	value	Ω	0.78	0.49	0.78	0.39	0.49	0.26	0.26	0.16
				temp coeff	ppm/°C	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3	0.6E-3
	Capacitors		C_{D1}	SPICE	#	(348)	(478)	(348)	(564)	(478)	(780)	(780)	(1204)
				linear	pF	.036	.050	.036	.058	.050	.081	.081	.125
			C_{D2}	SPICE	#	(390)	(624)	(390)	(780)	(624)	(1170)	(1131)	(1885)
				linear	pF	.041	.065	.041	.081	.065	.121	.117	.195
			C_{D3}	SPICE	#	(114)	(182)	(114)	(228)	(182)	(342)	(331)	(551)
				linear	pF	.012	.019	.012	.024	.019	.035	.034	.057
	Intrinsic Device	Non-linear	Q	model	–	QMSA	QMSA	QMSA	QMSA	QMSA	QMSA	QMSA	QMSA
				SPICE	#	(125)	(200)	(125)	(250)	(200)	(375)	(375)	(625)
		Linear	R	linear	Ω	7.39	3.47	5.18	2.61	5.18	1.32	3.06	1.00
			C	linear	pF	.625	1.000	.625	1.250	1.000	1.875	1.875	3.125
			T_C	linear	psec	4.97	5.04	5.00	5.06	4.96	5.14	5.02	5.09
MMIC Subcircuit	Resistors		R_F		Ω	550		330		330		230	
			R_E		Ω	0		5		6.86		11	
			R_B		Ω	245		156		170		122	
			R_{BIAS}		Ω	250		167		190		134	
			temp coeff R_F, R_E, R_B, R_{BIAS}		ppm/°C	–0.8E-3		–0.8E-3		–0.8E-3		–0.8E-3	
	Capacitors		C_F		pF	.12		.12		.12		.12	
			C_{P1}		pF	.033		.033		.033		.033	
			C_{P2}		pF	–		–		–		–	
			C_{P3}		pF	.103		.103		.103		.103	

Table 4. SPICE Parameter Values.

Model Name:	DMOD
Model Type:	D
IS	1E-25
CJO	2.45E-16
VJ	.76
M	.53
BV	45
IBV	1E-9

Model Name:	QDIS	QPWR	QMSA
Model Type:	NPN	NPN	NPN
BF	100	75	90
BR	5	5	5
IS	1.65E-18	1.65E-18	1.65E-18
VA	20	30	20
TF	12PS	14PS	12PS
CJE	1.8E-15	1.8E-15	1.8E-15
PE	1.01	1.01	1.01
ME	.60	.60	.60
PTF	35	50	25
XTB	1.818	1.818	1.818
VTF	6	6	6
ITF	.3 MA	.3 MA	.3 MA
IK	.100 MA	.100 MA	.1333 MA
XTF	4	4	4
NF	1.03	1.03	1.03
ISE	5E-15	5E-15	5E-15
NE	2.5	2.5	2.5

FET Models

At present only linear models are available for the GaAs FET devices in this catalog. The FET model given is a simplified hybrid pi model. The intrinsic FET consists of a voltage controlled current source ($g_m V_c$), the capacitance (C_{gs}) across which the controlling voltage appears, and the input resistance (R_C). Terminal contact resistances (R_g, L_g, R_s) and parasitic inductances (L_s, L_d) then are added to this structure. Included in the values for L_g, L_s, and L_d are both the inductance of the on-chip traces and the bond wire inductances used for carrier measurements. The drain resistance (R_d) is sufficiently low in value that it does not influence the S-parameters or noise performance in the frequency range where the model is applicable (up to ~ 20 GHz), it does not appear in the model. The gate-to-drain coupling capacitance (C_{gd}) – which is the predominant determiner of S_{12} – and the output capacitance (C_{ds}) complete the model. The schematic of the FET model equivalent circuit is shown in Figure 8. Component values for both low noise and gain bias are given in Table 6.

The topology derived for the bipolar package model can also be applied to GaAs FET packages, with one additional element being required. Since the bottom of the bipolar die is also the output terminal, bipolars in general do not require output (collector) bond wires. In contrast, the bottom of a GaAs FET is either electrically isolated or connected to the common terminal, so an output (drain) bond wire (L_d) is required. The consequent differences in metallization patterns means that although the model topology stays the same, the values of the model elements change. Thus, even though a FET package may have the same external appearance and numeric designation as bipolar package, it will have different values for its equivalent circuit elements – a FET style 70 package model will not be the same as a bipolar style 70 package model. For convenience, the package model is repeated in Figure 9 with the appropriate labels for a GaAs FET. Values for this model are listed in Table 7 for the various FET package styles.

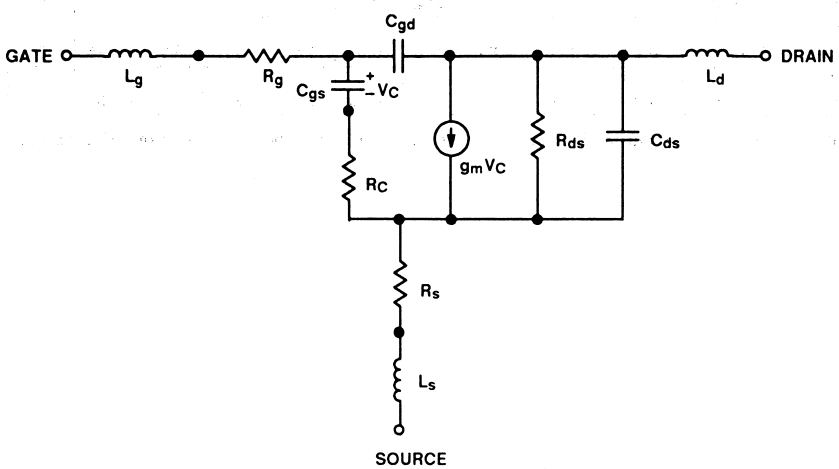


Figure 8. Equivalent Circuit for Linear GaAs FET Models.

Table 6. Circuit Element Values for Linear GaAs FET Models.

Part No., Bias	Components												
	Lg nH	Ld nH	Ls nH	Rd Ω	Rg Ω	Rs Ω	Cgs pF	Cgd pF	Cds pF	gm mS	TF ps	Rds Ω	QF –
ATF-101XX 2 V, 20 mA	0.9	0.6	0.15	2.0	2.5	2.0	0.25	0.1	0.1	70	0.001	200	0.8
ATF-102XX 2 V, 20 mA	0.9	0.6	0.15	2.0	2.5	2.0	0.40	0.1	0.1	60	0.001	200	0.6
ATF-107XX 2 V, 20 mA 4 V, 70 mA	0.9 0.9	0.6 0.6	0.15 0.15	2.0 4.0	3.0 5.0	2.0 2.0	0.40 0.80	0.15 0.1	0.1 0.2	60 130	0.001 0.001	200 200	1.0 1.4
ATF-131/132XX 3 V, 20 mA	0.9	0.6	0.15	2.0	3.0	0.5	0.14	0.05	0.03	50	0.001	250	1.5
ATF-133/134XX 3 V, 20 mA	0.9	0.6	0.15	2.0	3.0	0.5	0.20	0.05	0.03	40	0.001	250	1.0
ATF-137XX 3 V, 20 mA 4 V, 20 mA	0.9 0.9	0.6 0.6	0.15 0.15	2.0 4.0	3.0 3.0	2.0 2.0	0.20 0.24	0.05 0.05	0.03 0.03	40 50	0.001 0.001	250 250	1.5 1.9
ATF-211XX 3 V, 30 mA 5 V, 80 mA	0.4 0.4	0.5 0.5	0.15 0.15	1.5 1.0	1.5 1.0	1.0 0.5	0.70 1.2	0.10 0.08	0.14 0.15	68 115	0.001 0.001	180 180	0.6 1.0
ATF-251XX 3 V, 20 mA 5 V, 50 mA	0.4 0.4	0.7 0.7	0.15 0.15	2.0 1.0	2.5 2.0	1.0 0.5	0.36 0.60	0.07 0.06	0.16 0.08	48 75	0.001 0.001	150 180	0.8 1.2
ATF-261XX 3 V, 10 mA 5 V, 30 mA	0.6 0.6	0.7 0.7	0.15 0.15	2.0 2.0	5.0 5.0	5.0 5.0	0.16 0.26	0.03 0.015	0.06 0.06	27 42	0.001 0.001	275 275	0.6 1.0
ATF-35XXX 1.5 V, 10 mA	29.4 pH	26.6 pH	5 pH	5.0	1.0	0.5	0.088	0.0459	0.0527	53.7	0.47	105.1	
ATF-441XX 9 V, 500 mA	0.20	0.20	0.03	0.15	0.02	0.16	3.0	0.3	1.35	350	5	15	
ATF-451XX 9 V, 250 mA	0.20	0.20	0.06	0.30	0.75	0.32	1.5	0.2	0.70	175	5	30	
ATF-461XX 9 V, 125 mA	0.20	0.20	0.1	0.60	1.50	0.60	0.8	0.1	0.35	80	5	55	

Note: This table represents the product as die mounted on a chip carrier. Use Table 7 to convert to packaged product.

Figure 9. Equivalent Circuit for Package Models.

Table 7. Circuit Element Values for FET Package Models.

Pkg.	Lg nH	Ld nH	Ls nH	T1 Z Ω	T1 1 mil	T1 k –	T2 Z Ω	T2 1 mil	T2 k –	T3 Z Ω	T3 1 mil	T3 k –	Cgs pF	Cds pF	Cgd pF
00	refer to chip model (Table 6)														
01	0.65	0.5	0.15	45	40	7	35	10	7	45	45	7	0.03	0.03	0.03
35	0.9	0.6	0.15	65	35	7	30	15	7	65	35	7	0.05	0.05	0.005
50	0.5	0.8	0.15	65	15	7	30	5	7	65	20	7	0.1	0.1	0.005
70	0.5	0.5	0.15	40	25	7	20	5	7	40	25	7	0.05	0.05	0.005
71	0.5	0.5	0.15	40	25	7	20	5	7	40	25	7	0.05	0.05	0.005
76	0.5	0.5	0.15	40	25	7	20	5	7	40	25	7	0.05	0.05	0.005
84	0.5	0.5	0.15	65	25	9	30	7	9	65	25	9	0.03	0.05	0.010

Note: Both die and package models include inductance values for the gate, drain and source bond wires (Lg, Ld, Ls). When placing the die model in the package model, use the bond wire inductance value given in the package model and omit the values given in the die model.

Schottky Diode Models

Nonlinear analysis is often performed on Schottky diode circuits. A popular model for nonlinear analysis is the SPICE (Simulation Program with Integrated Circuit Emphasis) model. SPICE parameters are listed in the table below for HP Schottky diodes.

Beam lead diodes and chips have the same SPICE parameters when placed in packages. The parameters also apply to the individual diodes within multiple diode configurations. This is the reason for multiple entries on many of the columns in the table.

Table 8. Schottky Diode SPICE Models.

Parameter	Units	Part Number: 5082-0023, 5082-2702, 5082-2723	5082-0097, 5082-2811	5082-0024, 5082-2800, 5082-2837	5082-2900	5082-2350	5082-0087, 5082-2810, 5082-2817, 5082-2824
BV	V	4.0	18	75	10	30	25
CJ0	pF	0.1	1.0	1.6	1.1	1.1	0.8
EG	eV	0.69	0.69	0.69	0.69	0.69	0.69
IBV	A	10E-5	10E-5	10E-5	10E-5	10E-5	10E-5
IS	A	0.3X10E-9	0.3X10E-8	2.2X10E-9	10E-8	10E-8	1.1X10E-9
N		1.08	1.08	1.08	1.08	1.08	1.08
RS	Ω	7	10	25	15	15	10
PB	V	0.65	0.6	0.6	0.64	0.64	0.6
P_T		2	2	2	2	2	2
M		0.5	0.5	0.5	0.5	0.5	0.5

Table 8. Schottky Diode SPICE Models (contd.).

Parameter	Units	Part Number					
		5082-2301 5082-2302 5082-2400	5082-2350	5082-2303	5082-2231 5082-2271 5082-2831	5082-2233	5082-2263
BV	V	35	35	25	10	5	5
CJ0	pF	0.7	0.9	0.7	0.4	0.3	0.3
EG	eV	0.69	0.69	0.69	0.69	0.69	0.69
IBV	A	10E-5	10E-5	10E-5	10E-5	10E-5	10E-5
IS	A	7X10E-9	7X10E-9	7X10E-9	3X10E-7	12X10E-8	3X10E-10
N		1.08	1.08	1.08	1.08	1.08	1.08
RS	Ω	10	10	10	6	10	10
PB	V	0.64	0.64	0.64	0.5	0.5	0.65
P_T		2	2	2	2	2	2
M		0.5	0.5	0.5	0.5	0.5	0.5

Parameter	Units	Part Number					
		5082-2830	5082-2277	5082-2272	5082-2279	5082-2280	5082-2291
BV	V	10	10	10	5	5	10
CJ0	pF	0.4	0.35	0.25	0.12	0.09	0.4
EG	eV	0.69	0.69	0.69	0.69	0.69	0.69
IBV	A	10E-5	10E-5	10E-5	10E-5	10E-5	10E-5
IS	A	2X10E-10	2X10E-10	3X10E-7	12X10E-8	12X10E-8	2X10E-10
N		1.08	1.08	1.08	1.08	1.08	1.08
RS	Ω	6	9	9	10	10	6
PB	V	0.65	0.65	0.5	0.5	0.5	0.65
P_T		2	2	2	2	2	2
M		0.5	0.5	0.5	0.5	0.5	0.5

Parameter	Units	Part Number					
		5082-2292	5082-2294	5082-2765 5082-2774 5082-2785 5082-2794	5082-0013	5082-0009 5082-275X	5082-2787
BV	V	10	5	5	4	5	5
CJ0	pF	0.3	0.09	0.20	0.15	0.10	0.12
EG	eV	0.69	0.69	0.69	0.69	0.69	0.69
IBV	A	10E-5	10E-5	10E-5	10E-5	10E-5	10E-5
IS	A	2X10E-10	3X10E-10	4X10E-8	7.0X10E-8	1.2X10E-9	1.2X10E-9
N		1.08	1.08	1.08	1.08	1.08	1.08
RS	Ω	9	10	6	10	35	35
PB	V	0.65	0.65	0.5	0.5	0.6	0.6
P_T		2	2	2	2	2	2
M		0.5	0.5	0.5	0.5	0.5	0.5

Table 8. Schottky Diode SPICE Models (contd.).

Parameter	Units	Part Number					
		5082-2200 5082-2202 5082-2207 5082-2209	5082-2835	HSCH-9XXX	HSCH-5316 HSCH-5318 HSCH-5514 HSCH-5516 HSCH-6312 HSCH-6512	HSCH-5312 HSCH-5314 HSCH-5512 HSCH-5518 HSCH-6310 HSCH-6510	HSCH-5310 HSCH-5320 HSCH-5510 HSCH-5511 HSCH-5520
BV	V	5	9	5	5	5	5
CJ0	pF	0.2	0.7	0.04	0.2	0.13	0.09
EG	eV	0.69	0.69	1.43	0.69	0.69	0.69
IBV	A	10E-5	10E-5	10E-5	10E-5	10E-5	10E-5
IS	A	3X10E-10	2.2X10E-8	1.6X10E-13	3X10E-10	3X10E-010	3X10E-10
N		1.08	1.08	1.2	1.08	1.08	1.08
RS	Ω	5	5.0	5	5	9	13
PB	V	0.65	0.56	0.65	0.65	0.65	0.65
P_T		2	2	2	2	2	2
M		0.5	0.5	0.5	0.5	0.5	0.5

Parameter	Units	Part Number				
		HSCH-320X	HSCH-3486	HSCH-5330 HSCH-5340 HSCH-5530 HSCH-5531 HSCH-5540	HSCH-5332 HSCH-5334 HSCH-5532 HSCH-5538 HSCH-6330 HSCH-6530	HSCH-5336 HSCH-5338 HSCH-5534 HSCH-5536 HSCH-6332 HSCH-6532
BV	V	4	2.5	5	5	5
CJ0	pF	0.15	0.2	0.09	0.13	0.20
EG	eV	0.69	0.69	0.69	0.69	0.69
IBV	A	10E-5	3X10E-5	10E-5	10E-5	10E-5
IS	A	7.0X10E-8	5X10E-6	4X10E-8	4X10E-8	4X10E-8
N		1.08	1.08	1.08	1.08	1.08
RS	Ω	10	50	13	9	6
PB	V	0.5	0.35	0.5	0.5	0.5
P_T		2	2	2	2	2
M		0.5	0.5	0.5	0.5	0.5

Parameter	Units	Part Number					
		HSCH-5832	HSCH-5830	HSCH-5816	HSCH-5812	HSCH-5810	HSCH-5938
BV	V	4	4	4	4	4	5
CJ0	pF	0.13	0.09	0.2	0.13	0.09	0.4
EG	eV	0.69	0.69	0.69	0.69	0.69	0.69
IBV	A	10E-5	10E-5	10E-5	10E-5	10E-5	10E-5
IS	A	4.6X10E-18	4.6X10E-8	6.2X10E-11	6.2X10E-11	6.2X10E-11	1.6X10E-7
N		1.08	1.08	1.08	1.08	1.08	1.08
RS	Ω	8	12	4	8	12	4
PB	V	0.5	0.5	0.65	0.65	0.65	0.5
P_T		2	2	2	2	2	2
M		0.5	0.5	0.5	0.5	0.5	0.5

Table 8. Schottky Diode SPICE Models (contd.).

Parameter	Units	Part Number					
		HSCH-5918	HSCH-5958	HSCH-5932	HSCH-5912	HSCH-5952	HSCH-5836
BV	V	5	5	5	5	5	4
CJ0	pF	0.4	0.4	0.12	0.12	0.12	0.2
EG	eV	0.69	0.69	0.69	0.69	0.69	0.69
IBV	A	10E-5	10E-5	10E-5	10E-5	10E-5	10E-5
IS	A	1.5X10E-9	1X10E-12	4X10-E-8	4X10E-10	1X10E-13	4.6X10E-8
N		1.08	1.08	1.08	1.08	1.08	1.08
RS	Ω	4	4	10	10	10	4
PB	V	0.65	0.85	0.5	0.65	0.85	0.5
P_T		2	2	2	2	2	2
M		0.5	0.5	0.5	0.5	0.5	0.5

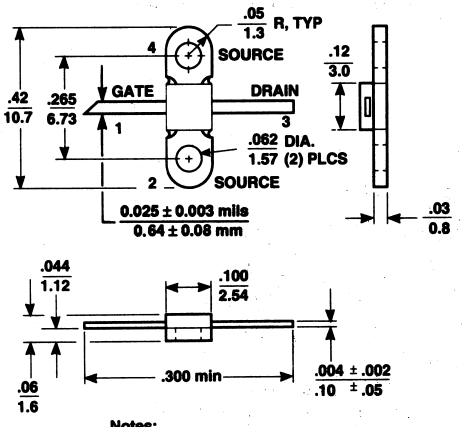
Parameter	Units	Part Number					
		HSMS-0001 HSMS-280X	HSMS-0002 HSMS-281X	HSMS-0003 HSMS-282X	HSMS-284X	HSMS-8001 HSMS-8101	HSMS-8002 HSMS-8202
BV	V	75	25	9	60	5.5	7.3
CJ0	pF	1.6	1.1	0.7	1.8	0.23	0.18
EG	eV	0.69	0.69	0.69	0.69	0.69	0.69
IBV	A	10E-5	10E-5	10E-4	10E-5	10E-5	10E-5
IS	A	3X10E-8	4.8X10E-9	2.2X10E-8	3X10E-8	9X10E-8	4.6X10E-8
N		1.08	1.08	1.08	1.08	1.08	1.08
RS	Ω	30	10	5.0	22	4	6
PB	V	0.65	0.65	0.56	0.65	0.5	0.5
P_T		2	2	2	2	2	2
M		0.5	0.5	0.5	0.5	0.5	0.5

Packaging



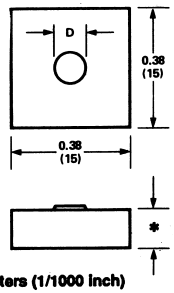
PACKAGE OUTLINES

All dimensions in millimeters (inches), except where noted.
For complete package specifications refer to individual product specification sheets.
Drawings are not to scale.



Notes:
(unless otherwise specified)
1. Dimensions are in mm
2. Tolerances
   in .xxx = ±.005
   mm .xx = ±.13

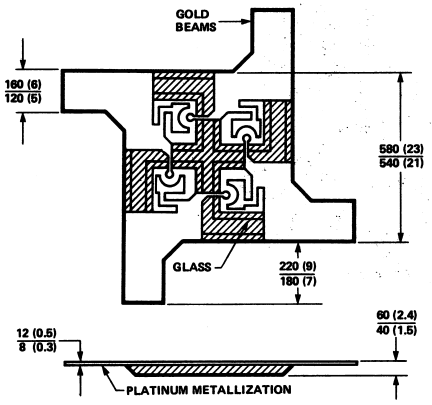
01A: 100 mil Flange



Dimensions in millimeters (1/1000 Inch)

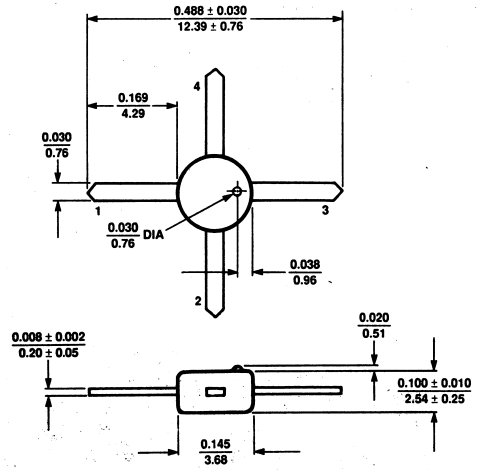
01B

*See data sheet for center junction, off-set junction and nine-point contact.

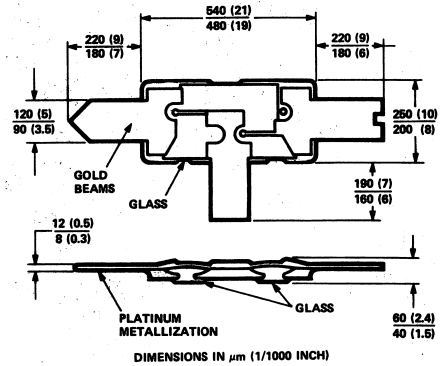


DIMENSIONS IN μm (1/1000 INCH)

03

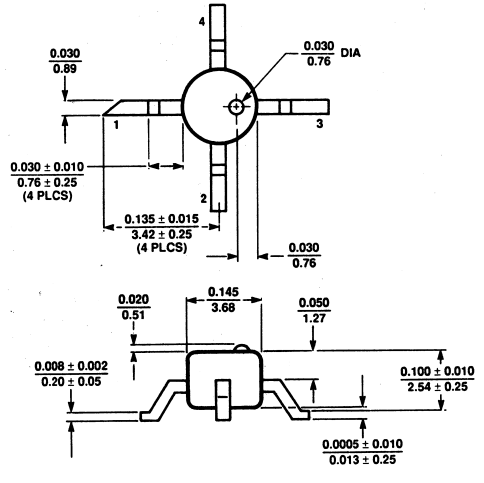


04A: 145 mil Plastic



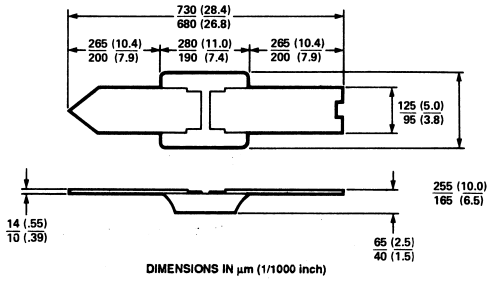
DIMENSIONS IN μm (1/1000 INCH)

04B

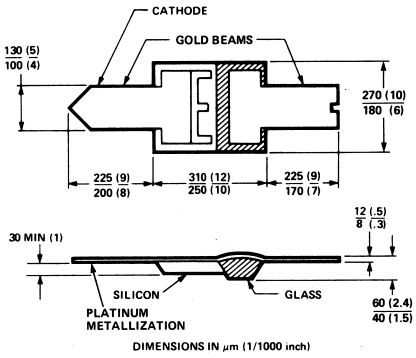


05: 145 mil Surface Mount Plastic

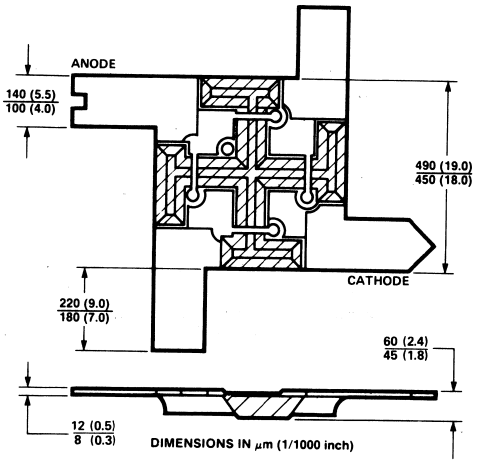
All dimensions in millimeters (inches), except where noted.
For complete package specifications refer to individual product specification sheets.
Drawings are not to scale.



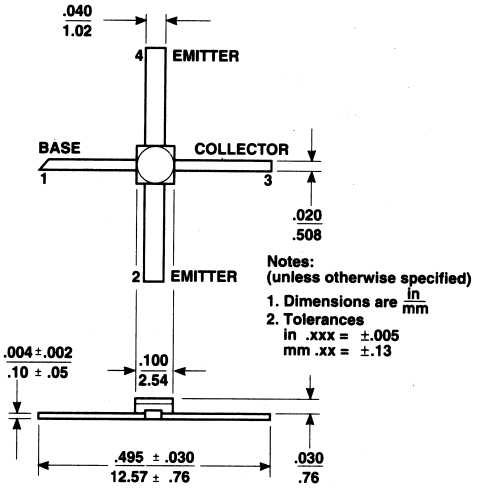
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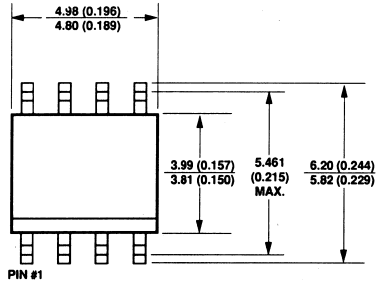
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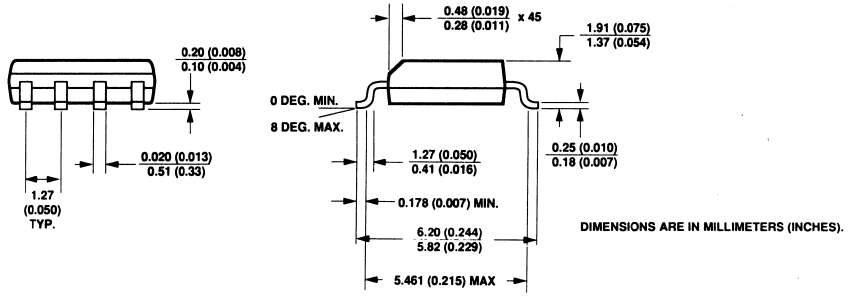


08B



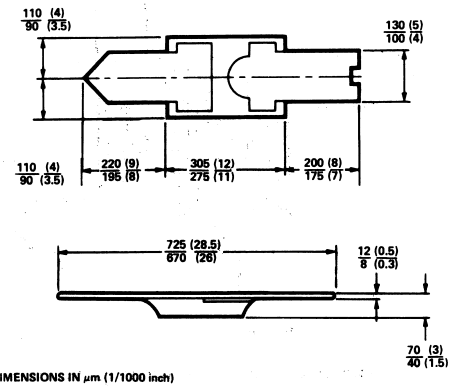
10A: 100 mil Stripline



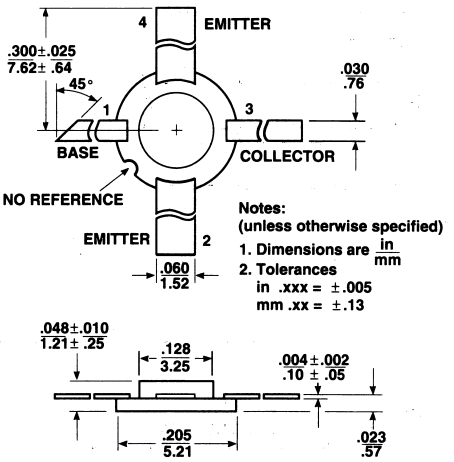


08A: Plastic SO-8

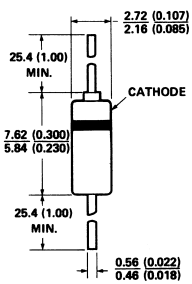
All dimensions in millimeters (inches), except where noted.
For complete package specifications refer to individual product specification sheets.
Drawings are not to scale.



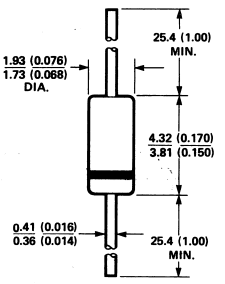
10B



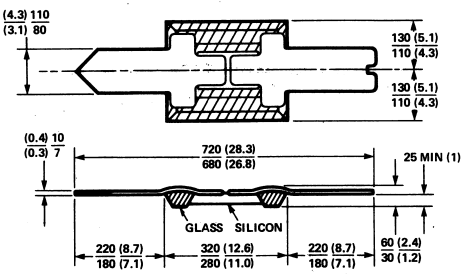
20: 200 mil BeO



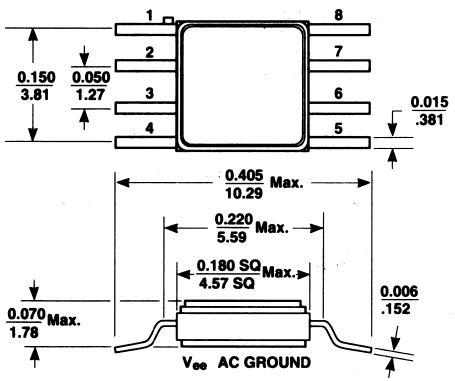
11



15

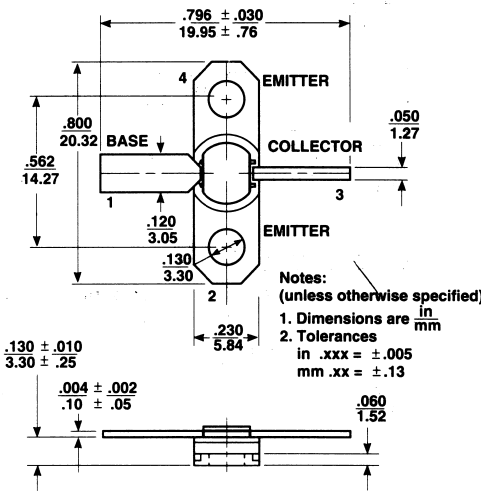


21



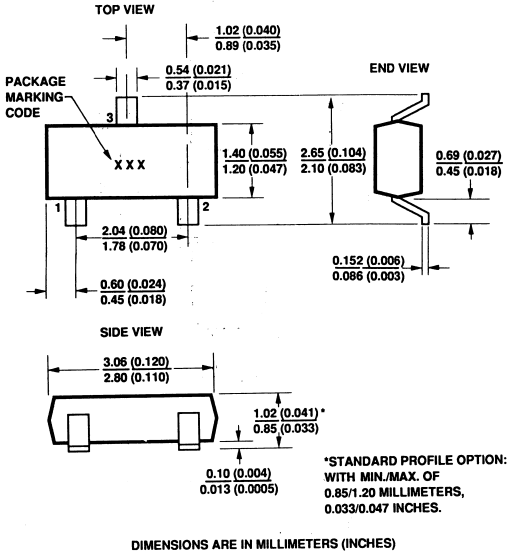
Notes:
(unless otherwise specified)
1. Dimensions are in/mm
2. Tolerances
in .XXX = ±0.005
mm .XX = ±0.13

18: 180 mil Glass/Metal Surface Mount

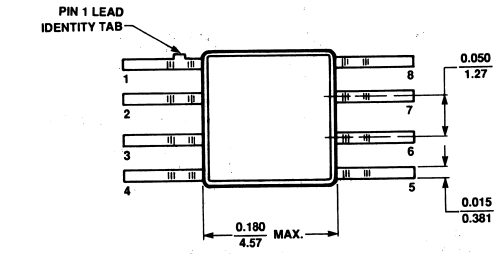


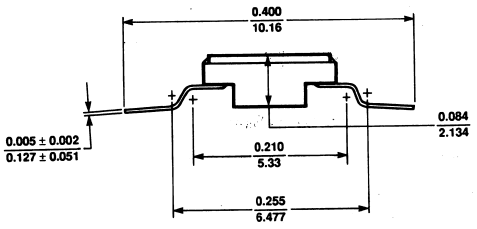
23A: 230 mil BeO Flange

All dimensions in millimeters (inches), except where noted.
For complete package specifications refer to individual product specification sheets.
Drawings are not to scale.



23B

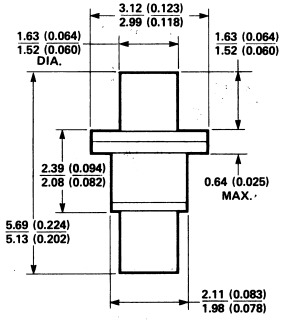




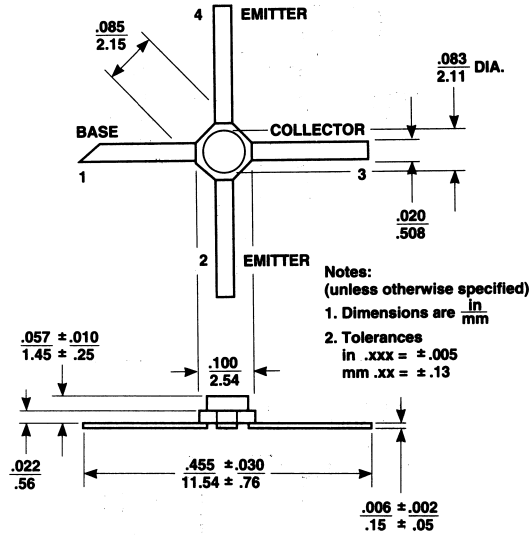
Notes:
(unless otherwise specified)

1. Dimensions are $\frac{\text{in}}{\text{mm}}$
2. Tolerances
   in .XXX = ± 0.005
   mm .XX = ± 0.13

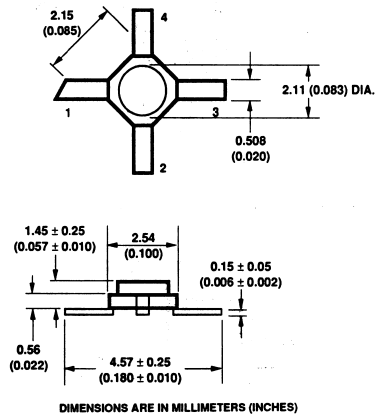
28: 180 mil Ceramic Surface Mount



31

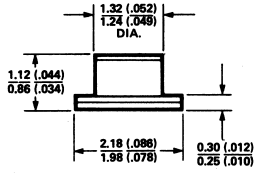


35: micro-X

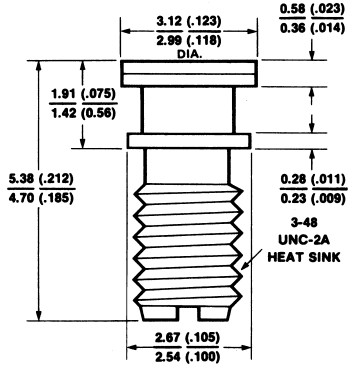


36: Short Lead micro-X

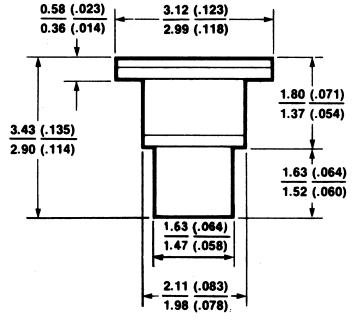
All dimensions in millimeters (inches), except where noted.
For complete package specifications refer to individual product specification sheets.
Drawings are not to scale.



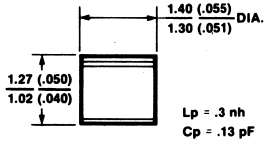
38



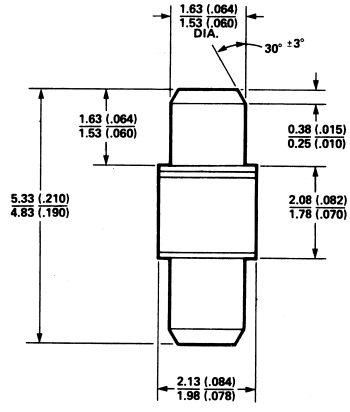
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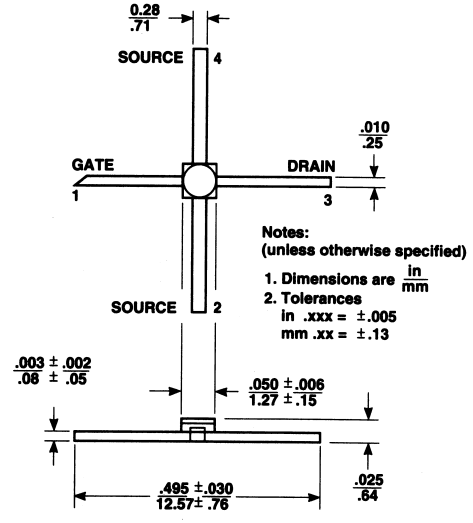
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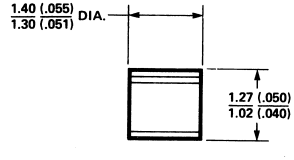
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49

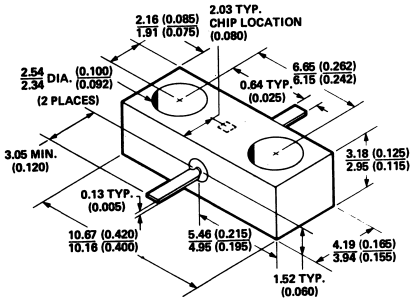


50: 50 mil Stripline

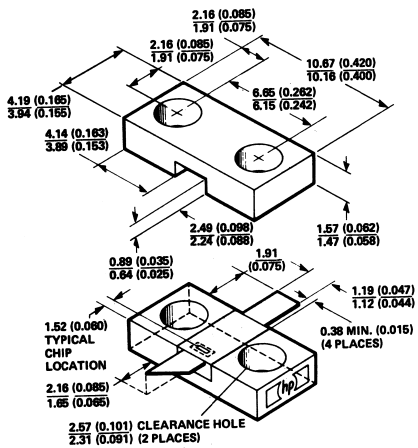


56

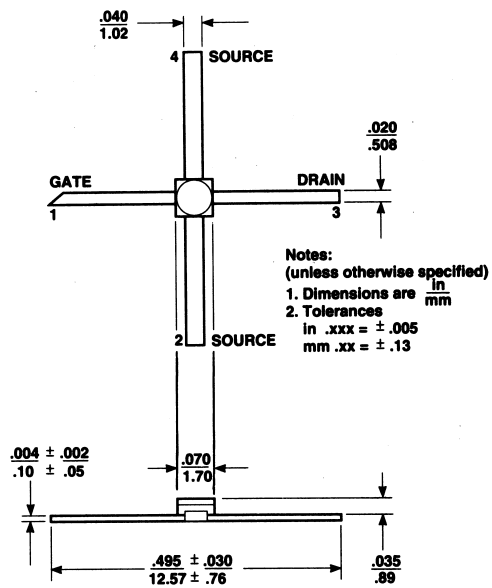
All dimensions in millimeters (inches), except where noted.
For complete package specifications refer to individual product specification sheets.
Drawings are not to scale.



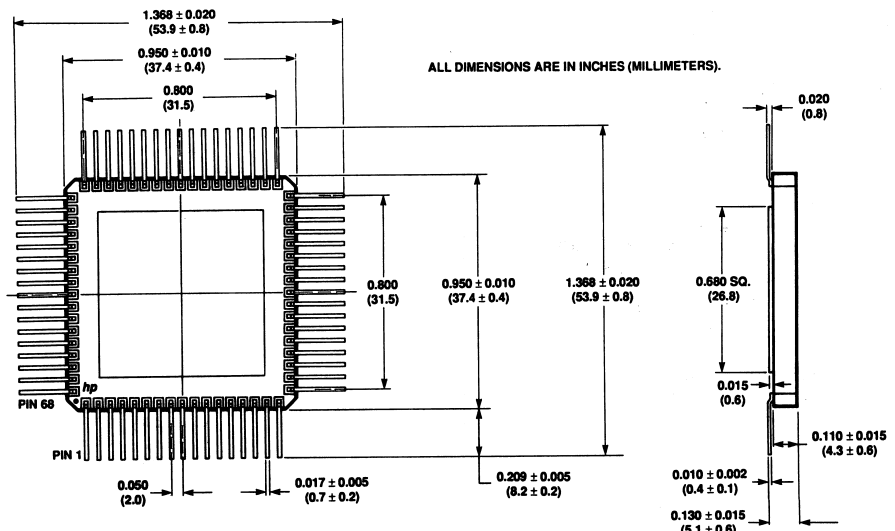
60



61

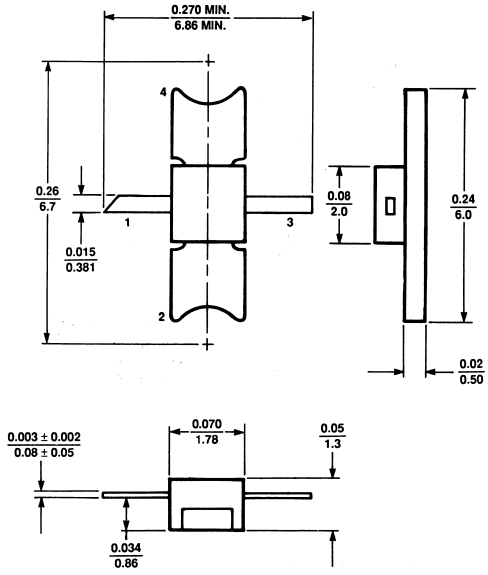


70: 70 mil Stripline

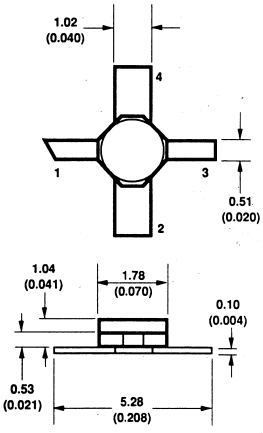


68 Lead Flatpack

All dimensions in millimeters (inches), except where noted.
For complete package specifications refer to individual product specification sheets.
Drawings are not to scale.

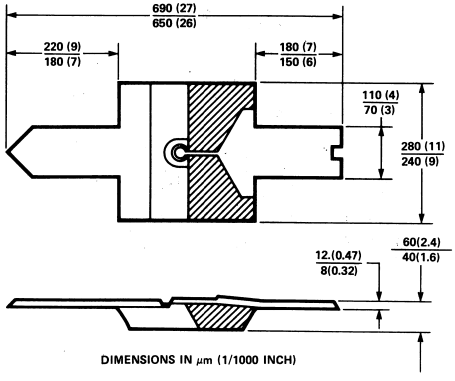


71: 70 mil Flange



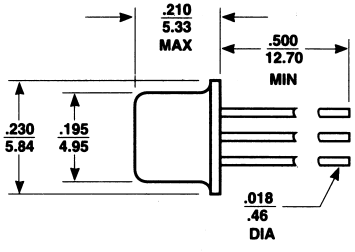
DIMENSIONS ARE IN MILLIMETERS (INCHES)

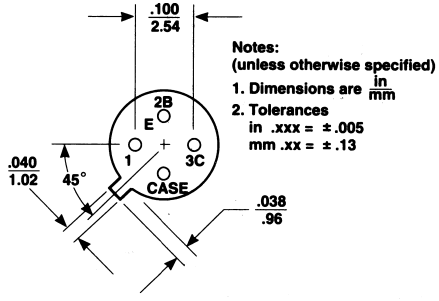
76: 70 mil Ceramic



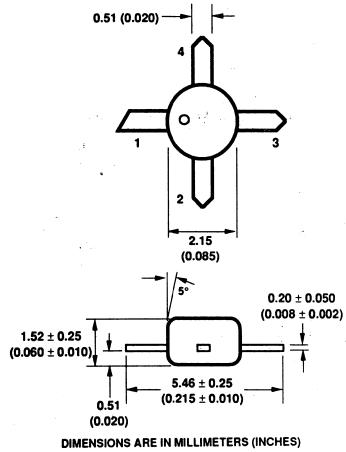
DIMENSIONS IN μm (1/1000 INCH)

83





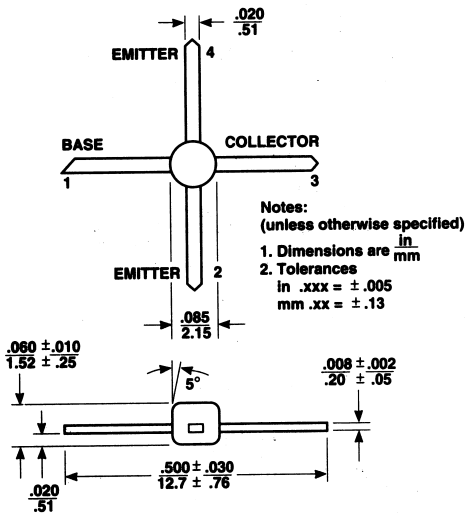
72: TO-72



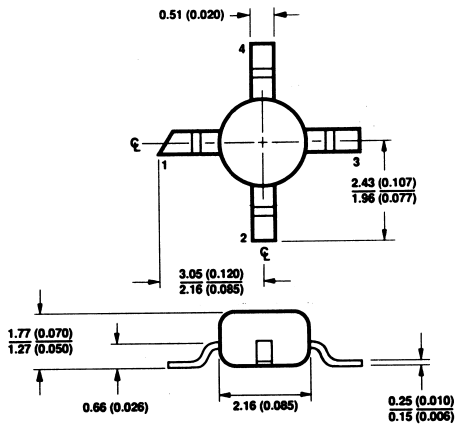
DIMENSIONS ARE IN MILLIMETERS (INCHES)

84: Short Lead 85 mil Plastic

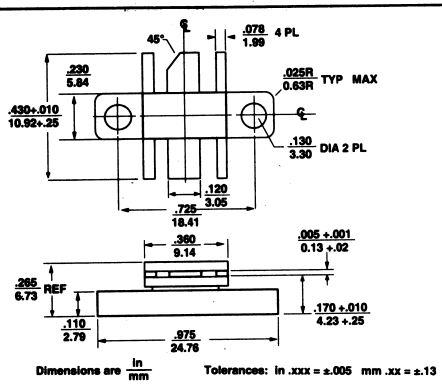
All dimensions in millimeters (inches), except where noted.
For complete package specifications refer to individual product specification sheets.
Drawings are not to scale.



85: 85 mil Plastic

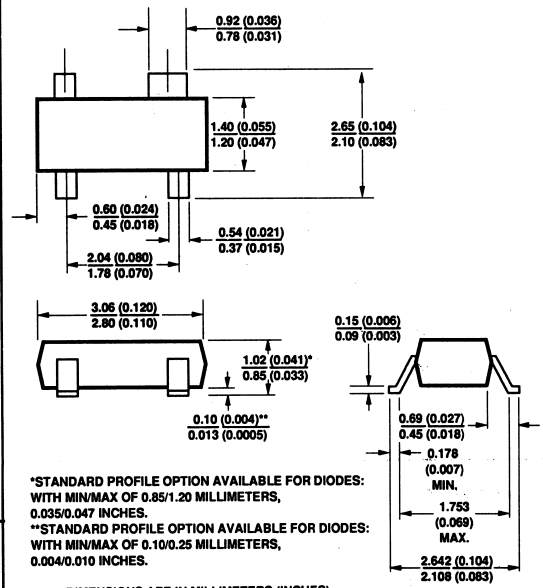


86: 85 mil Surface Mount Plastic



6 Lead BeO Power Flange

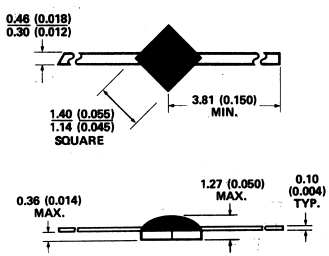
LOW PROFILE



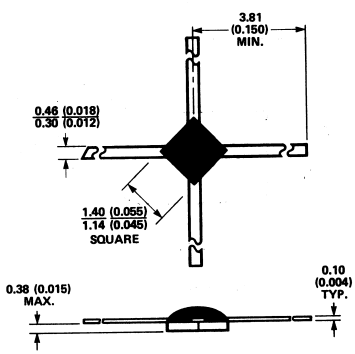
*STANDARD PROFILE OPTION AVAILABLE FOR DIODES: WITH MIN/MAX OF 0.85/1.20 MILLIMETERS, 0.035/0.047 INCHES.
**STANDARD PROFILE OPTION AVAILABLE FOR DIODES: WITH MIN/MAX OF 0.10/0.25 MILLIMETERS, 0.004/0.010 INCHES.

DIMENSIONS ARE IN MILLIMETERS (INCHES)

143

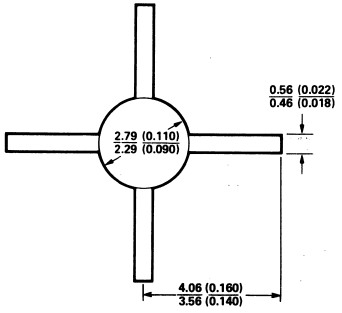


C2

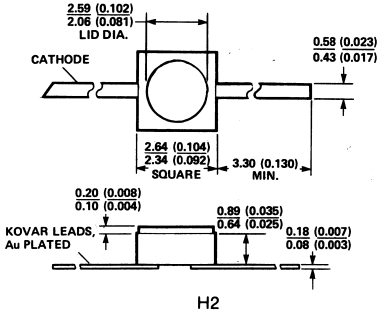


C4

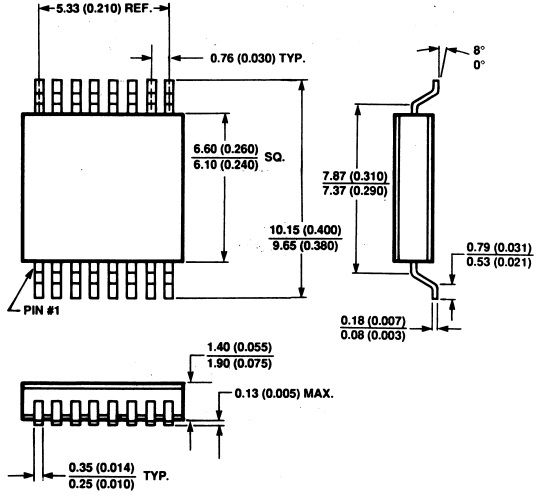
All dimensions in millimeters (inches), except where noted.
For complete package specifications refer to individual product specification sheets.
Drawings are not to scale.



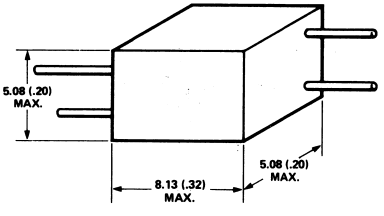
E4



H2

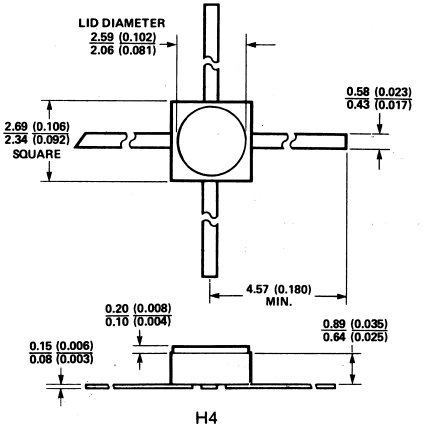


F6

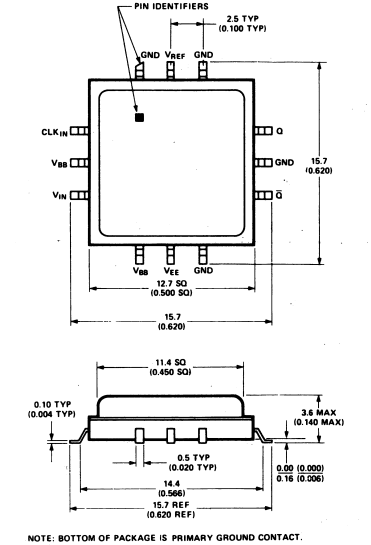


LEAD LENGTH 19.05 (0.75) MIN.

G1/G2



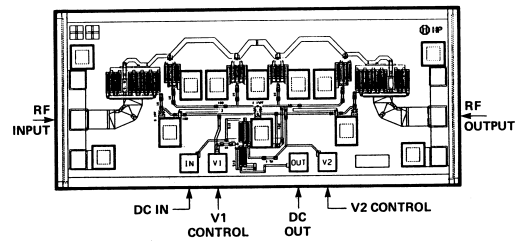
H4

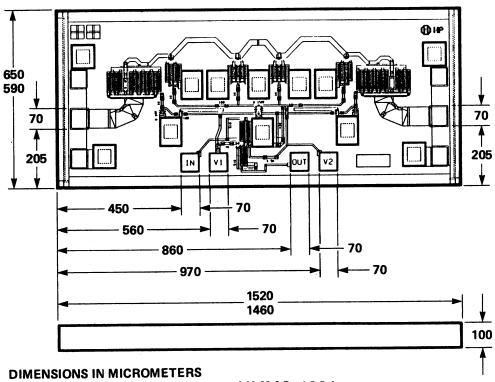


NOTE: BOTTOM OF PACKAGE IS PRIMARY GROUND CONTACT.
ALL DIMENSIONS IN MILLIMETERS (INCHES).

HBIC-0512

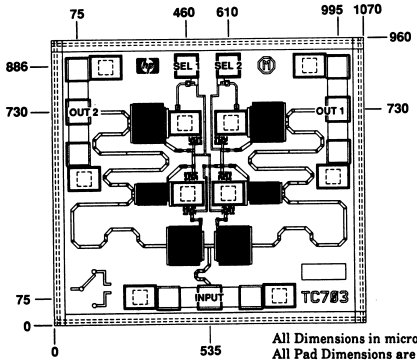
All dimensions in millimeters (inches), except where noted.
For complete package specifications refer to individual product specification sheets.
Drawings are not to scale.





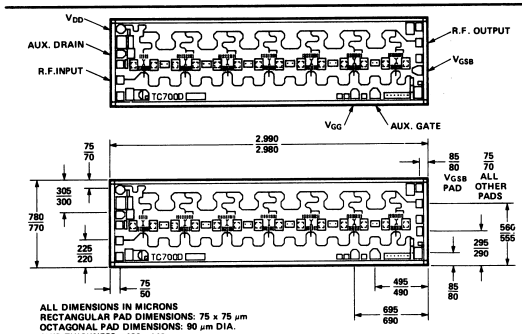
DIMENSIONS IN MICROMETERS

HMMC-1001



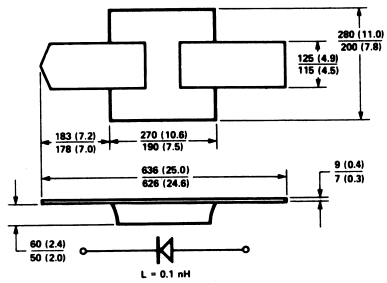
All Dimensions in microns
All Pad Dimensions are 75 x 75 µm
Chip Thickness is 130 +/- 10 µm

HMMC-2006

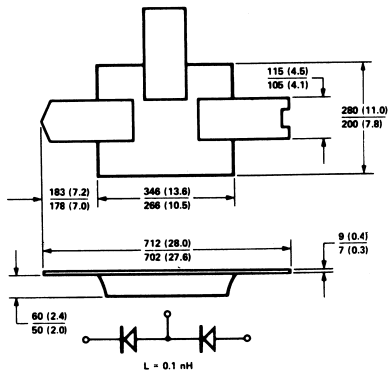


ALL DIMENSIONS IN MICRONS
RECTANGULAR PAD DIMENSIONS: 75 x 75 µm
OCTAGONAL PAD DIMENSIONS: 90 µm DIA.
CHIP THICKNESS: 120 - 140 µm

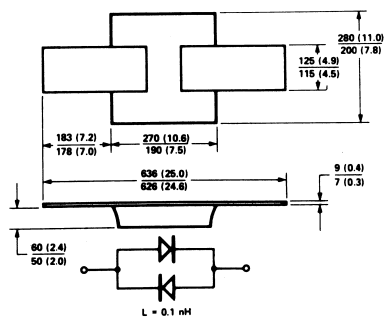
HMMC-5022/5026



HSCH-9101



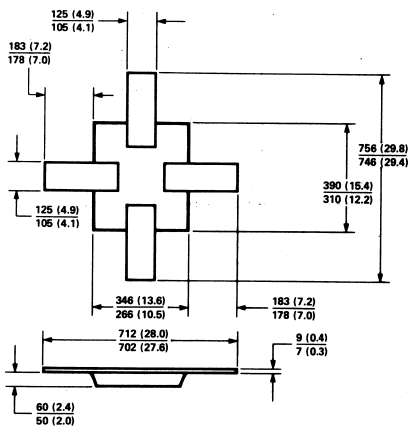
HSCH-9201



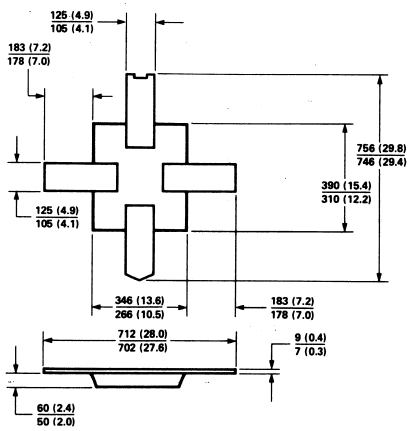
DIMENSIONS IN µm (1/1000 inch)

HSCH-9251

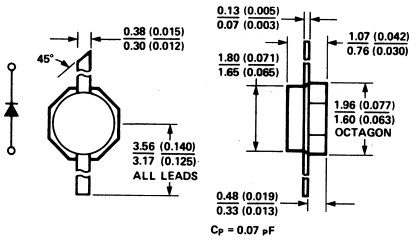
All dimensions in millimeters (inches), except where noted.
For complete package specifications refer to individual product specification sheets.
Drawings are not to scale.



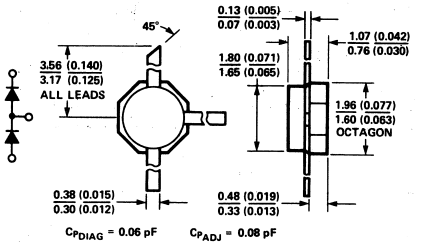
HSCH-9301



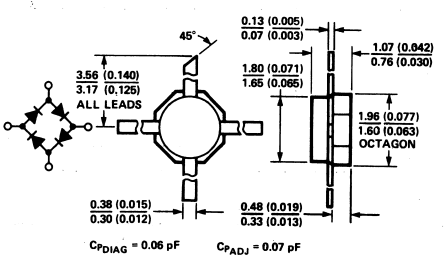
HSCH-9351



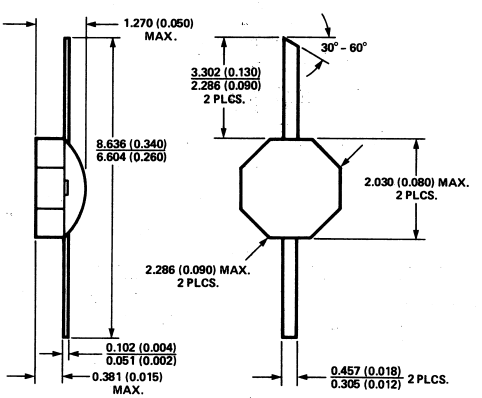
J2



J3

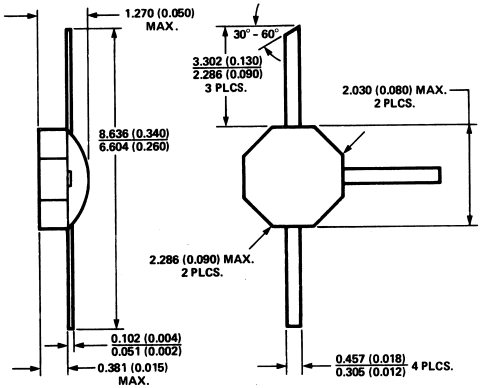


J4

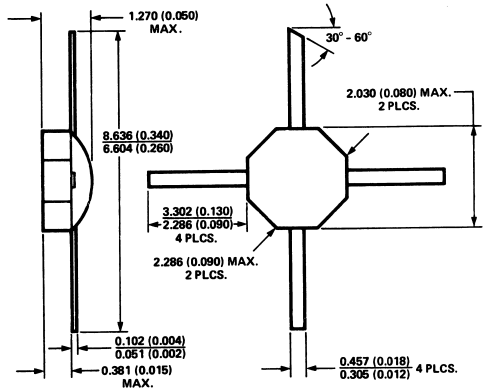


LC 2

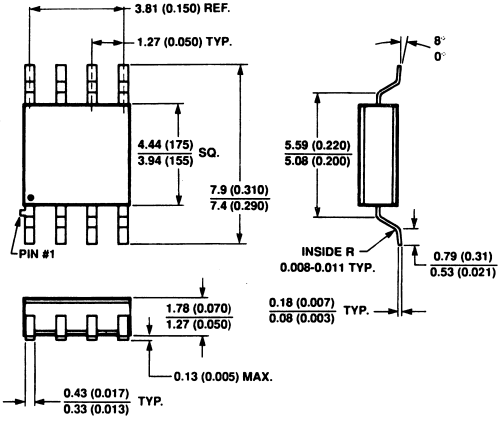
All dimensions in millimeters (inches), except where noted.
For complete package specifications refer to individual product specification sheets.
Drawings are not to scale.



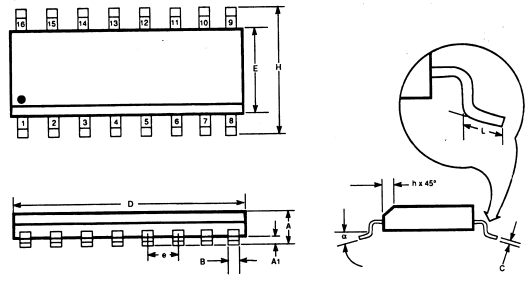
LC 3



LC 4

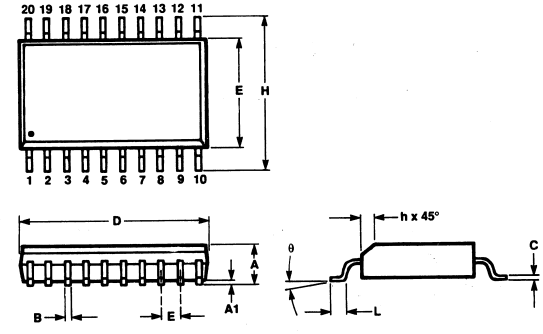


SOIC 8



SYMBOL	DIMENSIONS	
	MIN.	MAX.
A	1.35 (0.053)	1.75 (0.068)
A1	0.10 (0.004)	0.25 (0.0098)
B	0.35 (0.0138)	0.49 (0.0192)
C	0.19 (0.007)	0.25 (0.0098)
D	9.80 (0.386)	10.00 (0.394)
E	3.80 (0.150)	4.00 (0.157)
e	1.27 BSC (0.050)	
H	5.80 (0.228)	6.20 (0.244)
h	0.25 (0.010)	0.50 (0.020)
L	0.40 (0.016)	1.27 (0.050)
α	0°	8°

SO-16



SYMBOL	DIMENSIONS	
	MIN.	MAX.
A	2.35 (0.093)	2.65 (0.104)
A1	0.10 (0.004)	0.30 (0.012)
B	0.35 (0.014)	0.49 (0.019)
C	0.23 (0.009)	0.31 (0.012)
D	12.6 (0.496)	13.0 (0.512)
E	7.40 (0.291)	7.60 (0.299)
e	1.27 BSC (0.050)	
H	10.26 (0.404)	10.65 (0.419)
h	0.50 (0.020)	0.75 (0.030)
L	0.86 (0.034)	1.07 (0.042)
θ	0	8

MEETS JEDEC OUTLINE DIMENSIONS.
DIMENSIONS ARE IN MILLIMETERS (INCHES).

SO-20

HEWLETT PACKARD

Tape and Reel Packaging for Semiconductor Devices

Technical Data

Package Outlines
05, 08A, 23, 36
76, 84, 86, and 143

Description

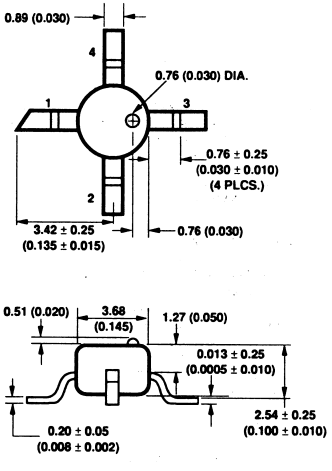
This data sheet is intended to cover standards on tape and reel packaging for Hewlett-Packard Communications Components Division (CMCD) semiconductor devices. This type of tape and reel packaging is designed to be compatible with available automated pick and place machines.

Related Standard

EIA RS481, "Taping of Leadless Components for Automatic Placement." In case of conflict regarding MSD product, this data sheet will govern.

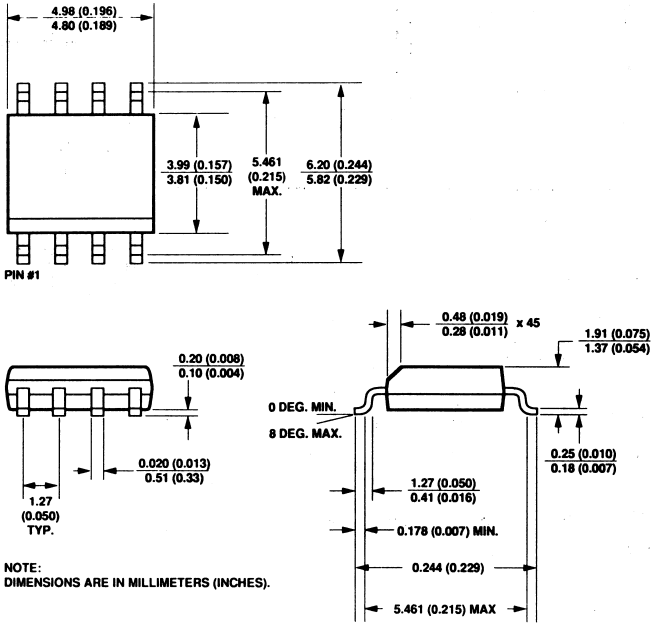
1. Package Outlines

05: 145 mil Surface Mount Plastic (B)



DIMENSIONS ARE IN MILLIMETERS (INCHES)

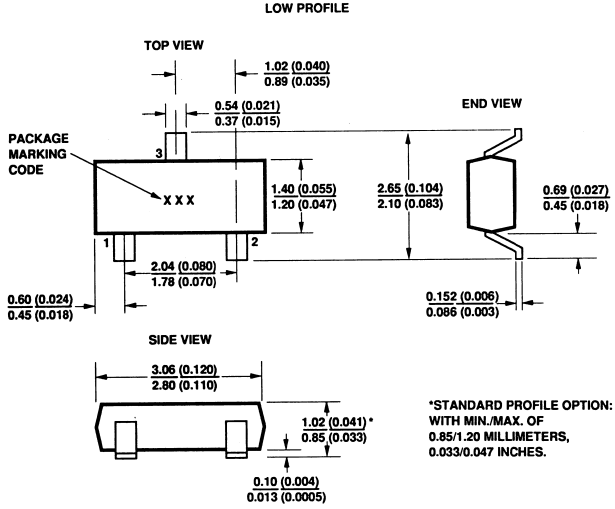
08A: Plastic SO-8



NOTE:
DIMENSIONS ARE IN MILLIMETERS (INCHES).

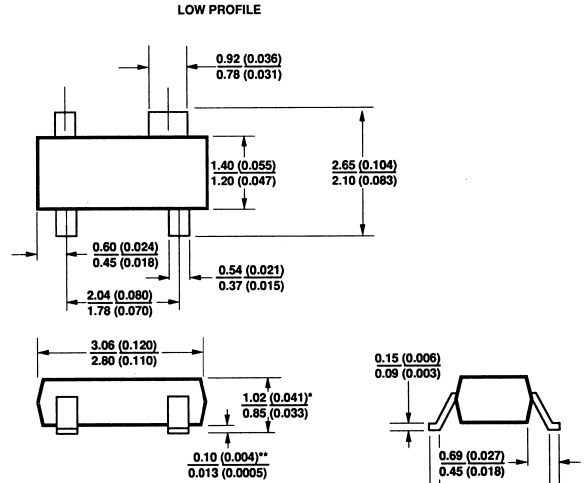
1. Package Outlines (cont.)

Outline 23B (SOT-23)



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Outline 143 (SOT-143)

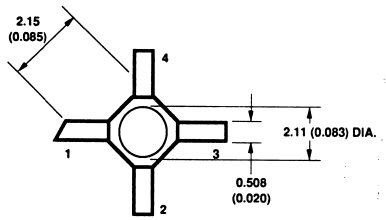


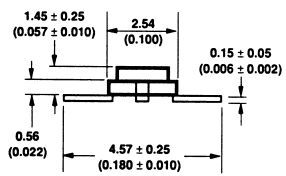
*STANDARD PROFILE OPTION AVAILABLE FOR DIODES:
WITH MIN./MAX. OF 0.85/1.20 MILLIMETERS,
0.035/0.047 INCHES;
**STANDARD PROFILE OPTION AVAILABLE FOR DIODES:
WITH MIN./MAX. OF 0.10/0.25 MILLIMETERS,
0.004/0.010 INCHES.

DIMENSIONS ARE IN MILLIMETERS (INCHES)

1. Package Outlines (cont.)

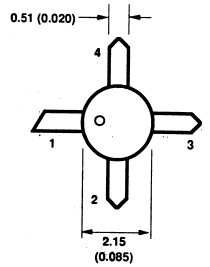
36: Short Lead micro-X (B, D)

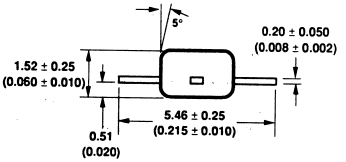




DIMENSIONS ARE IN MILLIMETERS (INCHES)

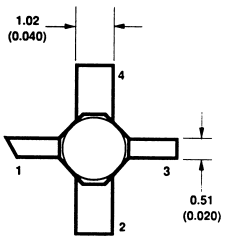
84: Short Lead 85 mil Plastic (D)

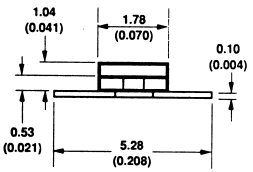




DIMENSIONS ARE IN MILLIMETERS (INCHES)

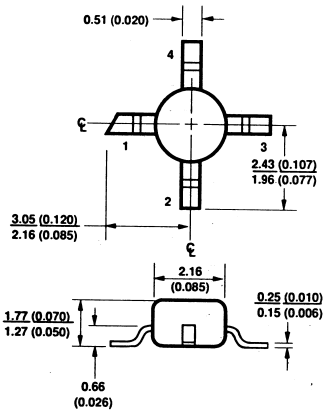
76: 70 mil Ceramic





DIMENSIONS ARE IN MILLIMETERS (INCHES)

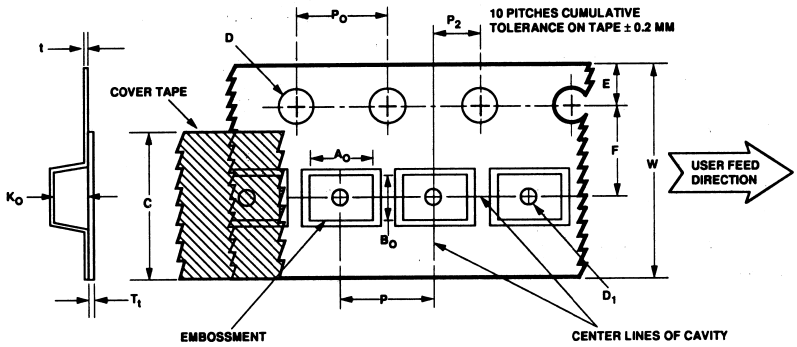
Outline 86



DIMENSIONS ARE IN MILLIMETERS (INCHES)

2. Tape Dimensions

For Outlines 23B and 143



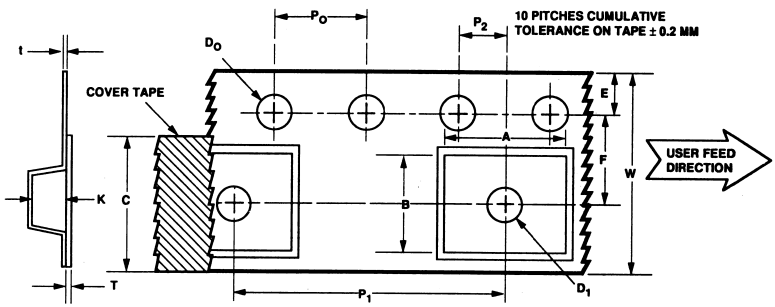
Outline 23B and 143

Description		Symbol	Size (mm)	Size (inches)
Cavity	Length	A_O	3.15 ± 0.15	0.124 ± 0.006
	Width	B_O	2.65 ± 0.25	0.104 ± 0.010
	Depth	K_O	1.30 ± 0.10	0.051 ± 0.004
	Pitch	P	4.00 ± 0.10	0.157 ± 0.004
	Bottom Hole Diameter	D_1	1.00 min.	0.04 min.
Perforation	Diameter	D	1.55 ± 0.10	0.061 ± 0.004
	Pitch	P_O	4.00 ± 0.10	0.157 ± 0.004
	Position	E	1.75 ± 0.10	0.069 ± 0.004
Cover Tape	Width	C	5.40 ± 0.25	0.205 ± 0.010
	Tape Thickness	T_t	0.064 ± 0.01	0.003 ± 0.0004
Carrier Tape	Width	W	8.00 ± 0.2	0.315 ± 0.008
	Thickness	t	0.30 ± 0.05	0.012 ± 0.002
Distance	Cavity to Perforation (Width Direction)	F	3.50 ± 0.10	0.138 ± 0.004
	Cavity to Perforation (Length Direction)	P_2	2.00 ± 0.05	0.079 ± 0.002

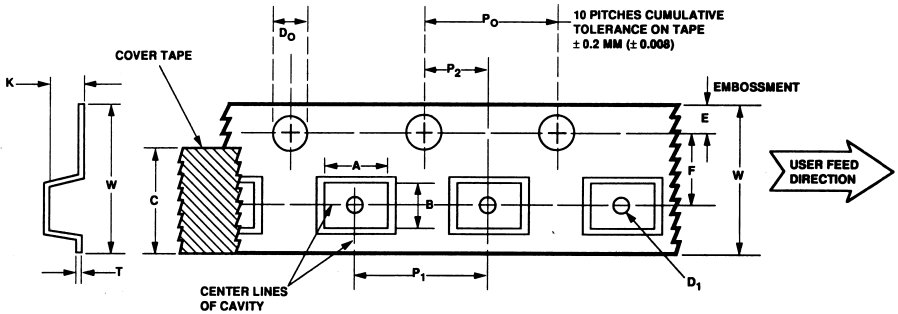
Notes:
1. Metric dimensions will govern.
2. Drawing is not to scale.

2. Tape Dimensions (cont.)

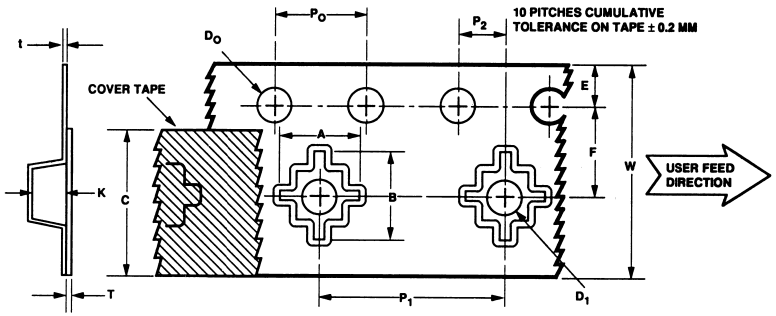
For Outline 05



For Outline 08A



For Outlines 36, 76, 84, and 86



Package 05

Description		Symbol	Size (mm)	Size (inches)
Cavity	Length	A	6.10 ± 0.10	0.240 ± 0.004
	Width	B	6.10 ± 0.10	0.240 ± 0.004
	Depth	K	3.18 ± 0.10	0.125 ± 0.004
	Pitch	P_1	12.00 ± 0.10	0.472 ± 0.004
	Bottom Hole Diameter	D_1	1.50 min.	0.059 min.
Perforation	Diameter	D_O	$1.50^{+0.10}_{-0.05}$	$0.059^{+0.004}_{-0.002}$
	Pitch	P_O	4.00 ± 0.10	0.157 ± 0.004
	Position	E	1.75 ± 0.10	0.069 ± 0.004
Distance Between Centerline	Cavity to Perforation (Length Direction)	P_2	2.00 ± 0.05	0.079 ± 0.002
	Cavity to Perforation (Width Direction)	F	5.50 ± 0.05	0.217 ± 0.002
Cover Tape	Width	C	9.30 ± 0.10	0.366 ± 0.004
	Thickness	T	0.065 ± 0.01	0.003 ± 0.0004
Carrier Tape	Width	W	12.00 ± 0.20	0.472 ± 0.008
	Thickness	t	0.30 ± 0.05	0.012 ± 0.002

Package 08A (SOIC 8)

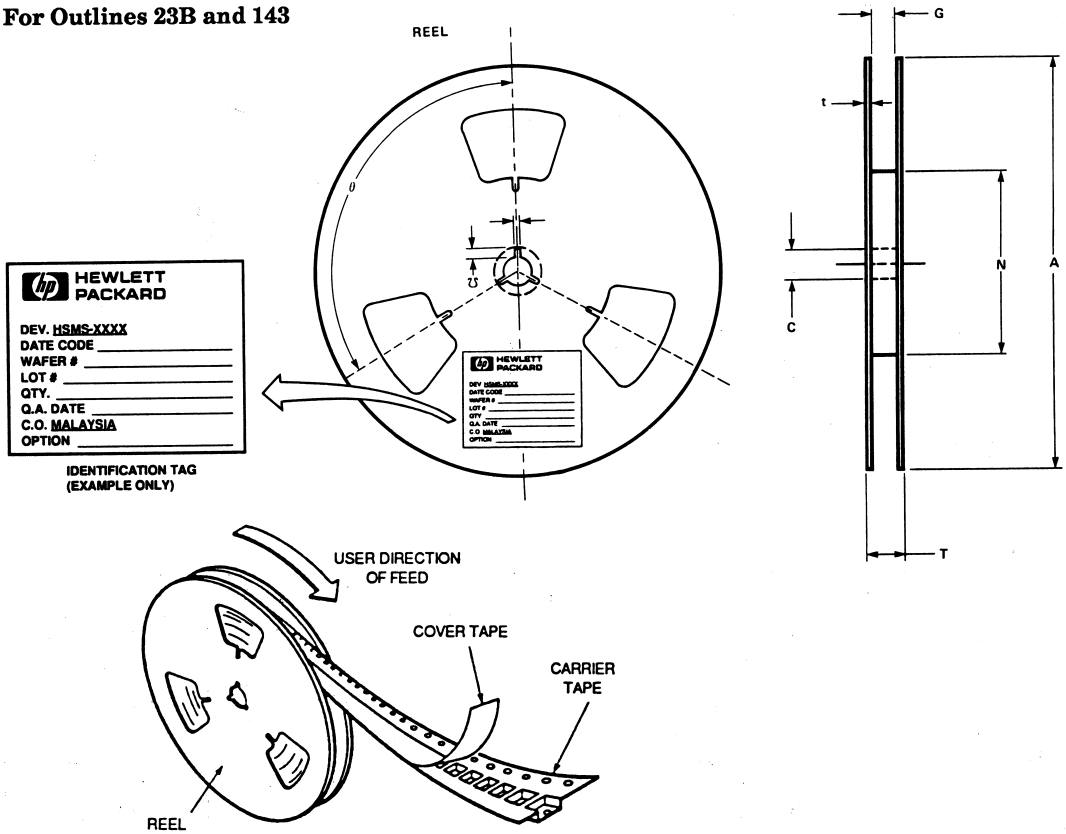
Description		Symbol	Size (mm)	Size (inches)
Cavity	Length	A	6.4 ± 0.10	0.254 ± 0.004
	Width	B	5.1 ± 0.10	0.202 ± 0.004
	Depth	K	2.1 ± 0.10	0.083 ± 0.004
	Pitch	P_1	8.0 ± 0.10	0.315 ± 0.004
	Bottom Hole Diameter	D_1	1.50 min.	0.059 min.
Perforation	Diameter	D_O	$1.5^{+0.10}_{-0.0}$	$0.059^{+0.004}_{-0.0}$
	Pitch	P_O	4.0 ± 0.10	0.157 ± 0.004
	Position	E	1.75 ± 0.10	0.069 ± 0.004
Distance Between Centerline	Cavity to Perforation (Length Direction)	P_2	2.0 ± 0.05	0.079 ± 0.002
	Cavity to Perforation (Width Direction)	F	5.5 ± 0.05	0.217 ± 0.002
Cover Tape	Width	C	9.2 ± 0.1	0.362 ± 0.004
	Thickness	T	0.051 ± 0.01	0.002 ± 0.0004
Carrier Tape	Width	W	12.0 ± 0.3	0.472 ± 0.012
	Thickness	t	0.290 ± 0.025	0.011 ± 0.001

Package 36, 76, 84, 86

Description		Symbol	Size (mm)	Size (inches)
Cavity	Length	A	5.77 ± 0.10	0.227 ± 0.004
	Width	B	6.10 ± 0.10	0.240 ± 0.004
	Depth	K	1.70 ± 0.10	0.067 ± 0.004
	Pitch	P_1	8.00 ± 0.10	0.314 ± 0.004
	Bottom Hole Diameter	D_1	1.50 min.	0.059 min.
Perforation	Diameter	D_O	$1.50^{+0.10}_{-0.05}$	$0.059^{+0.004}_{-0.002}$
	Pitch	P_O	4.00 ± 0.10	0.157 ± 0.004
	Position	E	1.75 ± 0.10	0.069 ± 0.004
Distance Between Centerline	Cavity to Perforation (Length Direction)	P_2	2.00 ± 0.05	0.079 ± 0.002
	Cavity to Perforation (Width Direction)	F	5.50 ± 0.05	0.217 ± 0.002
Cover Tape	Width	C	9.30 ± 0.10	0.366 ± 0.004
	Thickness	T	0.065 ± 0.01	0.003 ± 0.0004
Carrier Tape	Width	W	12.00 ± 0.20	0.472 ± 0.008
	Thickness	t	0.30 ± 0.05	0.012 ± 0.002

3. Reel Dimensions

For Outlines 23B and 143



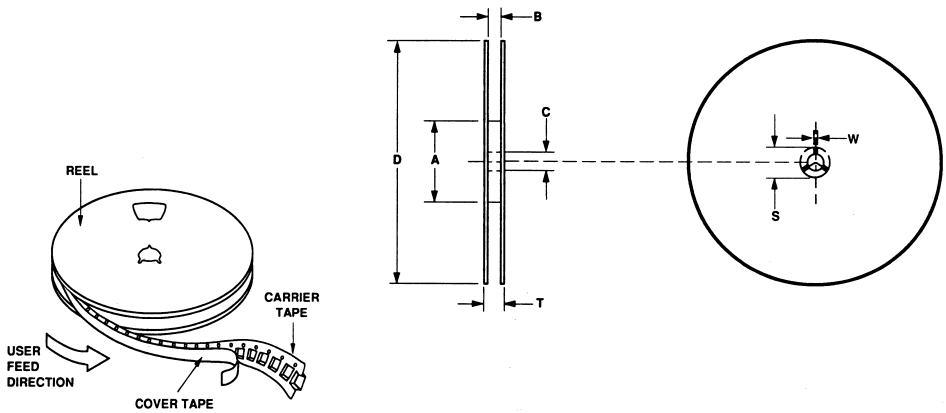
Outline 23B and 143

				7" Reel		13" Reel	
	Items		Symbol	Size (mm)	Size (inches)	Size (mm)	Size (inches)
Flange	Diameter		A	178 ± 2.0	7.00 ± 0.079	330 ± 2.0	13.0 ± 0.079
	Thickness Maximum		T	14.4	0.570	14.4	0.570
	Space Between Flange		G	9.50 ± 1.0	0.374 ± 0.040	9.15 ± 0.75	0.361 ± 0.03
Hub	Outer Diameter		N	66 ± 1.0	2.598 ± 0.040	55 min	12.16 min
	Spindle Hole Diameter		C	13.0 ± 0.5	0.512 ± 0.020	13.0 ± 0.5	0.512 ± 0.02
	Key Slit	Width	B	2.0 ± 0.5	0.079 ± 0.020	1.5 min	0.059 min
		Depth	ʊ	4.0 ± 0.5	0.16 ± 0.020	4.0 ± 0.5	0.16 ± 0.020
		Location	θ	120° ± 5°		120° ± 5°	

Notes:
1. Metric dimensions will govern.
2. Drawing is not to scale.
3. Diodes available on 7" reels only.
4. Monolithic amplifiers and transistors available on 7" (-TR1) and 13" (-TR2) reels.

3. Reel Dimensions (cont.)

For Outlines 05, 08A, 36, 76, 84, and 86



7" Reel

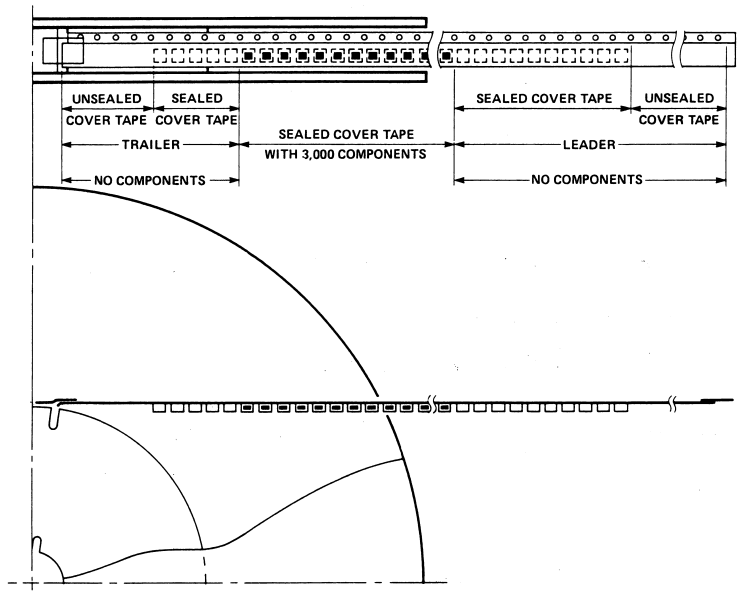
Description		Symbol	Size (mm)	Size (inches)
Flange	Diameter	D	178 ± 2.0	7.0 ± 0.079
	Thickness	T	18.4 max.	0.724 max.
	Space Between Flange	B	12.4 $^{+2.0}_{-0.0}$	0.488 $^{+0.08}_{-0.0}$
Hub	Outer Diameter	A	55 min.	2.16 min.
	Spindle Hole Diameter	C	13.0 ± 0.2	0.512 ± 0.008
	Key Slit Width	W	1.5 min.	0.059 min.
	Diameter	S	20.2 min.	0.795 min.

13" Reel

Description		Symbol	Size (mm)	Size (inches)
Flange	Diameter	D	330 ± 2.0	13.0 ± 0.079
	Thickness	T	18.4 max.	0.724 max.
	Space Between Flange	B	12.4 $^{+2.0}_{-0.0}$	0.488 $^{+0.08}_{-0.0}$
Hub	Outer Diameter	A	63 min.	2.48 min.
	Spindle Hole Diameter	C	13.0 ± 0.2	0.512 ± 0.008
	Key Slit Width	W	1.5 min.	0.059 min.
	Diameter	S	20.2 min.	0.795 min.

4. Packing – Leader and Trailer

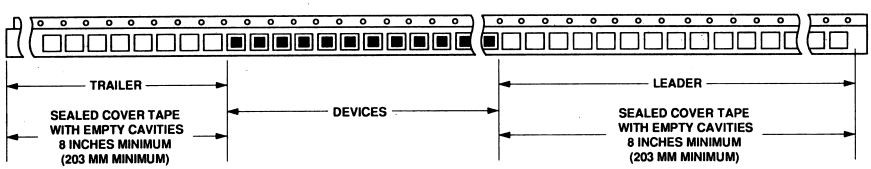
For Outlines 23B and 143



Item		Specification (mm) (minimum)	Specification (inches) (minimum)
Leader	Unsealed Cover Tape	20	0.79
	Sealed Cover Tape with Empty Cavities	160	6.30
Trailer	Unsealed Cover Tape	20	0.79
	Sealed Cover Tape with Empty Cavities	120	4.72

Packing

For Outlines 05, 08A, 36, 76, 84, and 86



5. Materials

For Outlines 23B and 143

A. Carrier Tape:
Static dissipative:
Polystyrene
Surface resistivity:
10^7 Ω/square maximum

B. Cover Tape:
Antistatic semi-transparent polyester

C. Reel:
Cardboard (7")
Plastic (13")

For Outlines 05, 08A, 36, 76, 84, and 86

A. Carrier Tape:
Conductive PVC
Surface resistivity:
1.8×10^3 Ω/square

B. Cover Tape:
Semi-transparent polyester

C. Reel:
Plastic

6. Device Orientation and Ordering Information for Diodes

For Outlines 23B and 143

Standard Profile:
Option T30 = Bulk
Option T31 = Tape and Reel, See Figure 1, 3
Option T32 = Tape and Reel, See Figure 2, 4

Low Profile:
Option L30 = Bulk
Option L31 = Tape and Reel, See Figure 1, 3
Option L32 = Tape and Reel, See Figure 2, 4

Specify Part Number followed by Option Number

Example:

HSMS-XXXX Option X XX

- XX — Bulk or Tape and Reel Option
- X — Profile: Standard = T, Low = L
- XXXX — Part Number
- HSMS- — Prefix*

*AT = Transistor
MSA = Monolithic Silicon Amplifier
HSMS = Surface Mount Schottky SOT 23/143
HSMP = Surface Mount PIN SOT 23/143

Conforms to Electronic Industries Standard RS-481 "Taping of Surface Mounted Components for Automated Placement." Standard Quantity is 3,000 Devices/Reel for SOT-23/143.

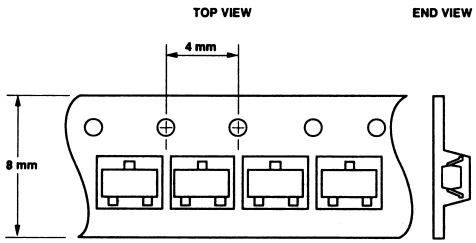


Figure 1. Options T31, L31 for SOT-23 Packages.

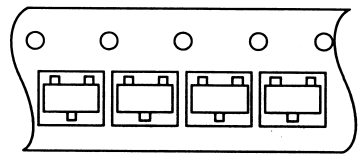


Figure 2. Options T32, L32 for SOT-23 Packages.

6. Device Orientation and Ordering Information (cont.)

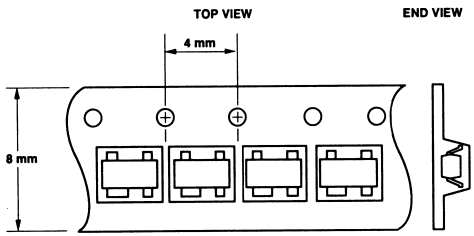


Figure 3. Options T31, L31, -TR1, -TR2 for SOT-143 Packages.

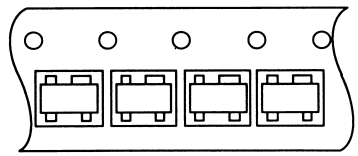
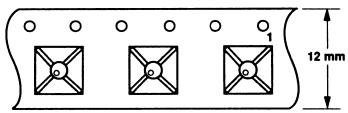


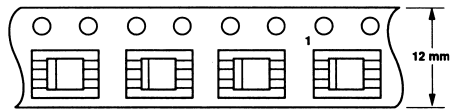
Figure 4. Options T32, L32 for SOT-143 Packages.

For Outlines 05, 08A, 36, 76, 84, and 86 Tape-and-Reel Options

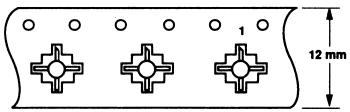
Package 05



Package 08A



Package 36, 76, 84, and 86



NOTE: 1. INDICATES PIN 1 ORIENTATION.

Part Number Ordering Information

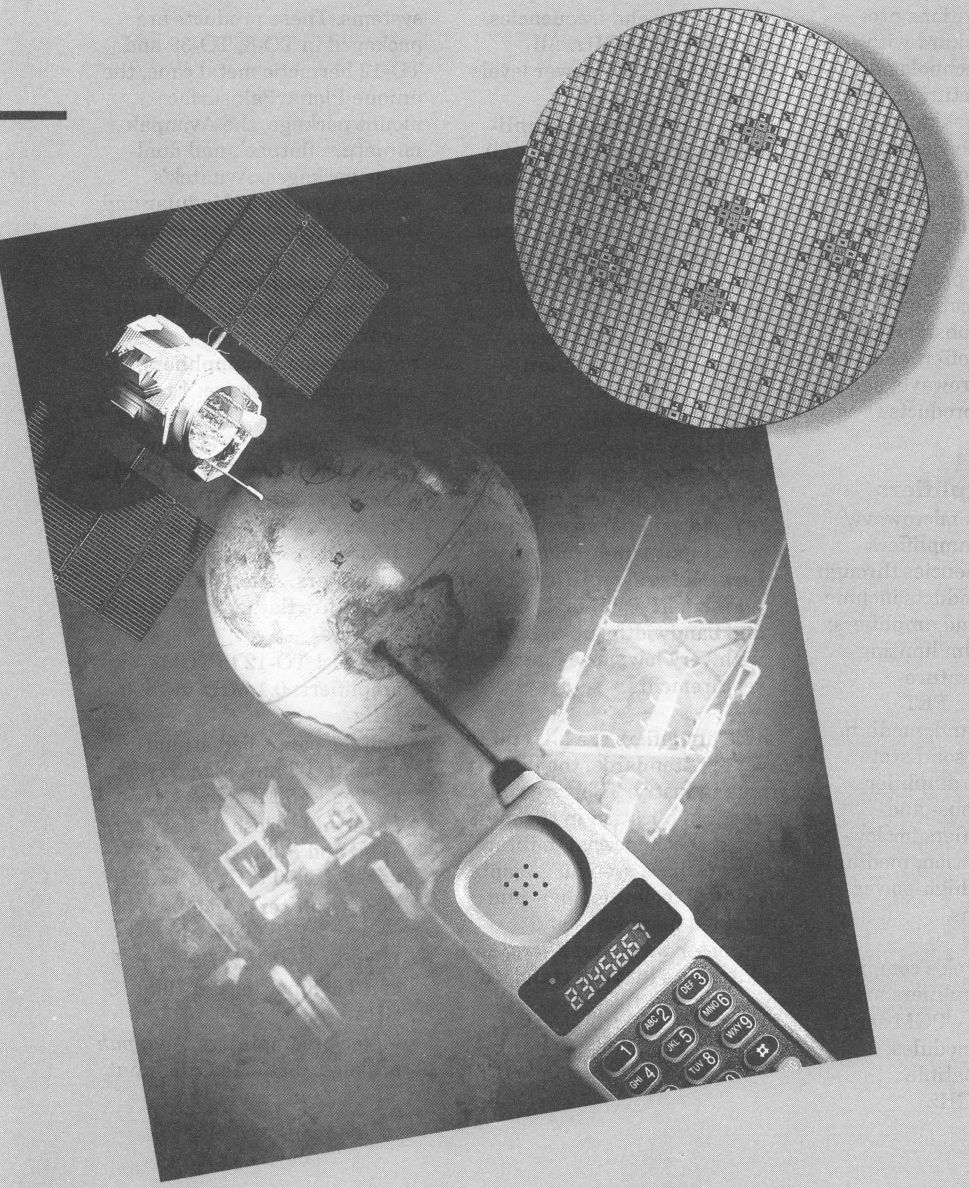
Package Style	Tape Width (mm)	Reel Size	Devices per Reel	Part Number Suffix
Package 05	12 12	7" 13"	5,000 1,500	-TR1 -TR2
Package 08A, 36, 74, 84, 86	12 12	7" 13"	1,000 4,000	-TR1 -TR2
Package 143 (for AT's and MSA's)	12 12	7" 13"	3,000 10,000	-TR1 -TR2

Notes:
1. Minimum order quantity is one (1) reel.
2. Orders are required to be in increments of the single reel quantity.
3. To order, specify the device part number followed by the appropriate suffix.

Examples:

MSA-1105-TR2	ATF-13136-TR1	AT-41486-TR2
Package 05	Package 36	Package 86
13" reel	7" reel	13" reel
1,500 devices/reel	1,000 devices/reel	4,000 devices/reel

Sales and Service



Cross Referral to Avantek, Inc. Products

In 1991, Hewlett-Packard acquired Avantek, a company well known for its microwave products. The combination of these two organizations provides Hewlett-Packard with the complementary technologies, products, manufacturing, and customer support skills to provide broad based component solutions to the worldwide communications, defense, and instrumentation industries.

In addition to the products contained in this catalog, Avantek, Inc., a subsidiary of Hewlett-Packard offers the following RF, microwave, and millimeter wave products.

Microwave and Millimeter Amplifiers

Avantek produces microwave/millimeter-Wave amplifiers operating at frequencies through 60 GHz. These products include low-noise, wideband amplifiers; GaAs FET thin-film limiting amplifiers, temperature-compensated GaAs FET amplifiers; wideband, medium-power amplifiers; solid-state TWT replacement amplifiers and communications- and radar-band amplifiers for low-noise preamplification, medium-power driver and high-power output applications.

Included in Avantek's comprehensive line of amplifiers are:

- **Gain Modules** – PGM series packaged gain modules, microstrip compatible μAVPAK, 2-20 GHz.
- **Small Signal Amplifiers** – frequencies up to 20 GHz, and power levels up to +23 dBm at 1 dB gain compression. Wide band widths, octave and multi-octave.
- **Millimeter Wave Amplifiers** – low end frequencies starting at 18 GHz. All bandwidths and power levels to 45.5 GHz.
- **Wideband Power Amplifiers** – frequencies up to 20 GHz, and power output levels greater than +23 dBm at 1 dB gain compression. Wideband and narrowband.
- **Communications Amplifier Products** – LNAs and Power Amplifiers for satellite, terrestrial, and cellular communications.
- **Output Limiting Amplifiers** – power output minimum-maximum boxes of less than 7 dB (less than 6 dB for octave band) specified over wide input power ranges.
- **Low Noise Amplifier (LNA)** – Frequencies up to 20 GHz and bandwidths up to 33% with very low noise figure requirements.

These amplifiers are all built to Avantek standards, the highest in the industry. They are suitable for application in the most rugged of commercial, military, and aerospace systems. Avantek continues to develop new and upgraded microwave and millimeter wave amplifiers, and to introduce them as standard products.

Modular and Oscillator Components

Avantek modular products are miniature, functional blocks designed to operate in standard 50-ohm environments, for incorporation in microwave systems. These products are packaged in TO-8, TO-39 and TO-12 hermetic metal cans, the unique PlanarPak surface-mount package, the Avanpak miniature flatpack and dual-inline packages. Avantek's extensive range of Modular and Oscillator Components includes:

- IF/RF amplifiers, TO-8 and *PlanarPak* packages: 10 MHz to 2 GHz
- Surface-mount amplifiers, *PlanarPak* package: 1 to 18 GHz
- AGC amplifiers, TO-3 and TO-8 packages: 5 to 1000 MHz
- Limiters, TO-8, DIP and *PlanarPak* packages: 5 to 1000 MHz
- Amplifiers, *Avanpak* miniature flatpack: 10 MHz to 4 GHz
- Low-cost TO-12 to TO-39 amplifiers: 0.1 MHz to 1500 MHz
- Voltage-controlled attenuators, TO-8 and *PlanarPak* packages: 5 MHz to 2 GHz
- Level and threshold detectors, TO-8 and *PlanarPak* packages: 10 MHz to 2 GHz
- Power splitters, *Avanpak* package: 2 to 18 GHz
- Mixers, *Avanpak*, *Planarpak* and TO-8 package: 0.75 to 18 GHz
- Mixer-preamplifiers, *Avanpak* package: 0.5 to 18 GHz input

- PIN diode switches, *Avanpak* package: SPST through SP5T, reflective and non-reflective: 2 to 18 GHz
- Limiters, Avanpak, TO-8, TO-12 packages: 2 to 18 GHz

Signal Sources

- Varactor-tuned oscillators (VCOs): 300 MHz to 18 GHz
- Dielectric Resonator oscillators: fixed; mechanically- and electrically-tunable: 3 to 18 GHz
- YIG-tuned oscillators: 1 to 50 GHz
- YIG-Filters: 0.5 to 26.5 GHz

For information on any of these products, call the Hewlett-Packard office nearest you and ask for a Components sales engineer.

How To Order

To order any component in this catalog or additional applications information, call the HP office nearest you and ask for a Components representative. A complete listing of the U.S. sales offices is on page 15-12; offices located outside of the U.S. are listed on page 15-13.

A worldwide listing of HP authorized distributors is on page 15-5. These distributors can offer off-the-shelf delivery for most Hewlett-Packard components.

Warranty

As an expression of confidence in our products to continue meeting the high standards of reliability and performance that customers have come to expect, Hewlett-Packard silicon and GaAs semiconductor products carry the following warranty.

HP's Components are warranted against defects in material and workmanship for a period of one year from the date of shipment. If HP receives notice of such defects during the warranty period, HP will repair or, at its option, replace components that prove to be defective in material or workmanship under proper use during the warranty period. This warranty extends only to HP customers.

NO OTHER WARRANTIES ARE EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

The foregoing limitation of liability shall not apply in the event that any HP product sold hereunder is determined by a court of competent jurisdiction to be defective and to have directly caused bodily injury, death, or property damage; provided, that in no event shall HP's liability for property damage exceed the greater of $50,000 or the purchase price of the specific product that caused such damage.

Certification

Some customers are especially interested in the test and quality assurance programs that HP applies to its products. These Hewlett-Packard programs are documented in a Certificate of Conformance which is available upon request at the time of purchase. This certification states:

We certify that the Hewlett-Packard Communications Components Division devices were duly tested and inspected prior to shipment and that they met all of the published specifications for these devices.

Hewlett-Packard's calibration measurements are traceable to the National Bureau of Standards to the extent allowed by the Bureau's calibration facilities.

The Hewlett-Packard Quality Program satisfies the requirements of MIL-Q-9858A, MIL-I-45208A, MIL-S-19500, MIL-STD-45662A, and NASA NHB 5300.4 (1.C.).

Service

We firmly believe that our obligation to you as a customer goes beyond just the delivery of your new HP product. This philosophy is implemented by Hewlett-Packard in two basic ways: (1) by designing and building excellent products with good serviceability, and (2) by backing up those products with a customer service program which can respond to your needs with speed and completeness.

The HP customer service program is one of the most important facets of our worldwide operations, providing a local service capability in many of our field offices (listed on pages 15-12, 15-13). Indeed, this customer service program is one of the major factors in Hewlett-Packard's reputation for integrity and responsibility towards its customers.

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9401 James Avenue, South
Ste. 140
Bloomington 55431
(612) 881-2600

Hamilton/Avnet Electronics[1,2]
12400 Whitewater Drive
Minnetonka 55343
(612) 932-0600

Notes:
1. Optoelectronics
2. RF Diodes/Transistors
3. Microwave and Avantek Products

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
1-800-PENSTOC

Missouri

Hall-Mark Electronics[1,2,3]
3783 Rider Trail South
Earth City 63045
(314) 291-5350

Hamilton/Avnet Electronics[1,2]
741 Goddard
Chestfield 63005
(314) 537-1600

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
1-800-PENSTOC

New Jersey

Arrow/Schweber Electronics[1,2]
43 Route 46 East
Pine Brook 07058
(201) 227-7880

Arrow/Schweber Electronics[1,2]
4 Stow Road
Marlton 08053
(609) 596-8000

Hall-Mark Electronics[1,2,3]
200 Lanidex Plaza
2nd Floor
Parisippany 07054
(201) 515-3000

Hall-Mark Electronics[1,2,3]
225 Executive Drive
Ste. 5
Moores Town 08057
(609) 235-1900

Hamilton/Avnet Electronics[1,2]
One Keystone Avenue
Bldg. 36
Cherry Hill 08003
(609) 751-2511

Hamilton/Avnet Electronics[1,2]
10 Lanidex Plaza West
Parisippany 07054-2715
(201) 515-5370

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.
124 B Little Falls Road[2,3]
Fairfield 07004
(201) 808-1414

New Mexico

Hamilton/Avnet Electronics[1,2]
7801 Academy Road, NE
Bldg. 1, Suite 204
Albuquerque 87109
(505) 828-1058

Newark Electronics[1,2]
1-800-367-3573

Sertek, Inc.[2,3]
(602) 894-9405

New York

Arrow/Schweber Electronics[1,2]
20 Oser Avenue
Hauppauge 11788
(201) 231-1000

Arrow/Schweber Electronics[1,2]
3375 Brighton-Henrietta
Townline Road
Rochester 14623
(716) 427-0300

Arrow/Schweber Electronics[1,2]
(Corporate Office)
25 Hub Drive
Melville 11747
(516) 391-1148
(Military)

Hall-Mark Electronics[1,2,3]
6605 Pittsford-Palmyra Road
Ste. E8
Fairport 14450
(716) 425-3300

Hall-Mark Electronics[1,2,3]
3075 Veterans Memorial
Hwy.
Ronkonkoma 11779
(516) 737-0600

Hamilton/Avnet Electroncs[1,2]
933 Motor Park Way
Hauppauge 11788
(516) 434-7421

Hamilton/Avnet Electronics[1,2]
2060 Townline Road
Rochester 14623
(716) 272-2729

Hamilton/Avnet Electronics[1,2]
100 Elwood Davis Road
Syracuse 13212
(315) 453-4000

Hamilton/Avnet Electronics[1,2]
(International)
933A Motor Park Way
Hauppauge 11788
(516) 434-7421

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
251 Townline Road
East Northport 11731
(516) 368-2773

Sickles Distribution Sales[2,3]
(Upstate New York ONLY)
(617) 862-5100

North Carolina

Arrow/Schweber Electronics[1,2]
3301 Terminal Drive
Raleigh 27604
(919) 250-2081

Hall-Mark Electronics[1,2,3]
5234 Greens Dairy Road
Raleigh 27604
(919) 872-0712

Hamilton/Avnet Electronics[1,2]
3510 Spring Forest Road
Raleigh 27604
(919) 878-0819

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
1-800-PENSTOC

Ohio

Arrow/Schweber Electronics[1,2]
6573E Cochran Road
Solon 44139
(216) 248-3990

Arrow/Schweber Electronics[1,2]
8200 Washington Village
Drive
Centerville 45458
(513) 435-5563

Hall-Mark Electronics[1,2,3]
5821 Harper Road
Solon 44139
(216) 349-4632

Hall-Mark Electronics[1,2,3]
777 Dearborne Park Lane
Ste. L
Worthington 43085
(614) 888-3313

Hamilton/Avnet Electronics[1,2]
7760 Washington Village Drive
Dayton 45459
(513) 439-6700

Hamilton/Avnet Electronics[1,2]
30325 Bainbridge Road, Bldg. A
Solon 44139
(216) 349-4910

Hamilton/Avnet Electronics[1,2]
2600 Corporate Exchange Dr.
Columbus 43231
(614) 882-7389

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
1-800-PENSTOC

Oklahoma

Arrow/Schweber Electronics[1,2]
12111 E. 51st Street
Ste. 101
Tulsa 74146
(918) 252-7537

Hall-Mark Electronics[1,2,3]
5411 S. 125th East Ave.
Ste. 305
Tulsa 74146
(918) 254-6110

Hamilton/Avnet Electronics[1,2]
12101 E. 51st Street
Ste. 106
Tulsa 74146
(918) 252-7297

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
1-800-PENSTOC

Oregon

Almac/Arrow Electronics[1,2]
1885 N.W. 169th Place
Beaverton 97006
(503) 629-8090

Hamilton/Avnet Electronics[1,2]
9750 S.W. Nimbus
Beaverton 97005
(503) 526-6202

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
1-800-PENSTOC

Pennsylvania

Arrow/Schweber Electronics[1,2]
1000 R.I.D.C. Plaza
Ste. 203
Pittsburgh 15238
(412) 963-6807

Hamilton/Avnet Electronics[1,2]
213 Executive Drive
Ste. 320
Mars 16046
(412) 772-1881

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
40 Croce Lane
Coatesville 19320
(215) 383-9535

Texas

Arrow/Schweber Electronics[1,2]
2227 West Braker Lane
Austin 78758
(512) 835-4180

Arrow/Schweber Electronics[1,2]
3220 Commander Drive
Carrollton 75006
(214) 380-6464

Arrow/Schweber Electronics[1,2]
10899 Kinghurst
Ste. 100
Houston 77099
(713) 530-4700

Hall-Mark Electronics[1,2,3]
(Corporate Office)
11333 Pagemill Road
Dallas 75243
(214) 343-5000

Hall-Mark Electronics[1,2,3]
11420 Pagemill Road
Dallas 75243
(214) 553-4300

Hall-Mark Electronics[1,2,3]
8000 West Glen
Houston 77063
(713) 781-6100

Hamilton/Avnet Electronics[1,2]
1807A West Braker Lane
Austin 78758
(512) 832-4306

Hamilton/Avnet Electronics[1,2]
4004 Belt Line Road
Ste. 200
Dallas 75244
(214) 308-8111

Hamilton/Avnet Electronics[1,2]
1235 North Loop West
Ste. 521
Houston 77008
(713) 861-8517

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
13740 Midway Road
Dallas 75244
(214) 701-9555

Utah

Applied Specialties[2,3]
1-800-950-8555

Hamilton/Avnet Electronics[1,2]
1100 East 6600 South
Ste. 120
Salt Lake City 84121
(801) 972-2800

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
1-800-PENSTOC

Sertek, Inc.[2,3]
800 334-7127

Washington

Almac/Arrow Electronics[1,2]
14360 S.E. Eastgate Way
Bellevue 98007-6458
(206) 643-9992

Hamilton/Avnet Electronics[1,2]
17761 N.E. 78th Place
Redmond 98052
(206) 881-6697

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
10800 N.E. Street
Ste. 805
Bellevue 98004
(206) 454-2371

Penstock, Inc.[2,3]
1-800-PENSTOC

Wisconsin

Arrow/Schweber Electronics[1,2]
200 North Patrick Blvd.
Brookfield 53045
(414) 792-0150

Hall-Mark Electronics[1,2,3]
2440 South 179th Street
New Berlin 53146
(414) 797-7844

Hamilton/Avnet Electronics[1,2]
20875 Crossroads Circle
Ste. 400
Waukesha 53186
(414) 784-4511

Newark Electronics[1,2]
1-800-367-3573

Penstock, Inc.[2,3]
1-800-PENSTOC

Notes:
1. Optoelectronics
2. RF Diodes/Transistors
3. Microwave and Avantek Products

International

Australia

VSI Promark Electronics Pty. Ltd.[1,2,3]
16 Dickson Avenue
Artarmon, N.S.W. 2064
(61) 2 439 4655

Austria

BFI IBEXSA Elektronik GmbH[2,3]
Microwave Group
Korbinianstr. 6
8057 Eching (München)
Tel (089) 319 51 35

EBV Elektronik[1,2]
Diefenbachgasse 35/6
1150 Wien
(43) 0222 894 17 74

Transistor V.m.b.H. & Co KG [1,2]
Auhofstr. 41A
1130 Wien
(43) 0222 82 94 01

Belgium

BFI Ibexsa B.V.[2,3]
PO Box 3019
2130 KA Hoofddorp
Tel (020) 65 31 350

EBV Electronik[1,2]
Excelsiorlaan 35
Avenue Excelsior 35
1930 Zaventem
(32) 02 720 99 36

Brazil

Intertek Electronica Ltd.[1,2]
Rua Miguel Casagrande, 200
02714-000, Sao Paulo, SP
(011) 266-2922

Canada

Davetek Marketing, Inc.[1,2]
37-4429 Kingsway
Burnaby, BC VSH 2A1
(604) 430-3680

Davetek Marketing, Inc.[1,2]
#206 2723 37th Ave. NE
Calgary, AB T1Y 5R8
(403) 291-4984

Hamilton/Avnet Electronics Ltd.[1,2]
8610 Commerce Court
Burnaby, BC V5A 4N6
(604) 420-4101

Hamilton/Avnet Electronics Ltd.[1,2]
2816 21st Street NE
Calgary, Alberta T2E 6Z2
(403) 250-9380

Hamilton/Avnet Electronics Ltd.[1,2]
6845 Rexwood Drive
Units 3-5
Mississauga,
Ontario L4V 1R2
(416) 677-7432

Hamilton/Avnet Electronics Ltd.[1,2]
190 Colonnade Road
Nepean, Ontario K7E 7J5
(613) 226-1700

Hamilton/Avnet Electronics Ltd.[1,2]
2795 Rue Halpern
St. Laurent, Quebec H4S 1P8
(514) 335-1000

Czechoslovakia

GM Electronic[1,2]
Evropska 73
1600 Praha 6
(42) 422 316 7202

Denmark

BFI Ibexsa Danmark A/S[2,3]
Langebjergvenget 8A, 1. TH
4000 Roskilde
Tel: (046) 75 31 31

Nortec[1,2]
Electronics A/S
Transformarvej 17
2730 Herlev
(45) 42 84 2000

Finland

Field OY[1,2]
Niittylanpolku 10
00620 Helsinki
(358) (0) 757 10 11

France

Almex[1,2]
Zone industrielle d'Antony
48, rue de l'Aubepine
92160 Antony cedex
(33) 1 40 96 54 00

Arrow Electronics[1,2]
73/79 rue des Solets
Silic 585
94668 Rungis Cedex
(33) 1 49 78 49 78

EBV Elektronik[1,2]
16, rue Gallilée
Cité Descartes
77436 Champs sur Marne
(1) 64 68 86 00

Elexience[2,3]
9, rue des Petits Ruisseaux
91370 Verriere le Buisson
Tel: (1) 60 11 94 71

Scie-Dimes Ibexsa SA[2,3]
1 Rue Lavoisier ZI-BP 25
91430 Igny
Tel: (1) 69 41 82 82

S.C.A.I.B. S.A.[1,2]
80, rue d'Arcueil
Silic 137
94523 Rungis Cedex
(33) 1 46 87 23 13

Germany

BFI IBEXSA Elektronik GmbH[2,3]
Microwave Group
Korbinianstr. 6
8057 Eching (München)
Tel: (089) 319 51 35

EBV-Elektronik GmbH[1,2]
Hans-Pinsel-Str. 4
8013 Haar bei Munchen
089 460 09 60

Farnell GmbH[1,2]
Grünwalder Weg 30
8024 Deisenhofen
(49) 089 613 03 01

Ing. Buero K.-H. Dreyer[1,2]
Albert-Schweizer-Ring 36
2000 Hamburg 70
(040) 66 90 27-28

Jermyn GmbH [1,2]
Im Dachsstück 9
6250 Limburg 4
(49) 06431 508-0

Sasco GmbH[1,2]
Hermann-Oberth-Str. 16
8011 Putzbrunn bei München
(49) 089 46 11-0

Great Britain

BFI Ibexsa Electronics Ltd.[2,3]
Burnt Ash Road
Quarry Wood Industrial Estate
Aylesford
Kent
ME20 7NA
Tel: (0622) 88 24 67

Greece

Micronics Ltd.[1,2]
46, Kritis Street
16451 Argyroupolis
Athens
(0301) 9914786Greece

Hong Kong

CET Ltd. (REP)[1,2,3]
22/F Chuang's Finance Centre
81-85, Lockhart Road
(852) 5 200922

Semicon Products and Systems Co. Ltd.[3]
11/F., Evenew House,
485 Lockhart Road
Causeway Bay
(852) 5729183

Hungary

Transistor V.m.b.H. & Co. KG[1,2]
Anhafstr. 41A
1150 Wien
43 1 222 1 82 94 51

India

Blue Star Ltd. (REP)[1,2]
11A, Magarath Road
Bangalore 560025
(91) 812 575668

Blue Star Ltd. (REP)[1,2]
13 Community Centre
New Friends Colony
New Delhi 110065
(91) 11-683-9262

Hinditron Services Pvt. Ltd.[2,3]
Industry House, 23-B
Mahal Industrial Estate
Mahakali Caves Road,
Andheri East,
Bombay 400093
(91) 22 8634035

SKAG INC.[1]
15, Wood Street,
Richmond Road
Bangalore 560025
(91) 812 576502

Israel

CMS[2,3]
Computation & Measurement Systems Ltd.
11, Hashlosha Street
P.O. Box 25089
67060 Tel-Aviv
Tel: (03) 538 03 18

Telsys Ltd.[1,2]
Atidim, Industrial Park, Bldg 3
Dvora Hanevia Street, Neva Sharet
61431 Tel-Aviv
Tel: (03) 49 20 01

Notes:
1. Optoelectronics
2. RF Diodes/Transistors
3. Microwave and Avantek Products

Italy

BFI Ibexsa SPA[2,3]
Via Massena 18
20145 Milano
Tel: (02) 33 10 05 35

Celdis Componenti S.r.1[1,2]
Via Fluvio Testi 280
20126 Milano
Tel: (02)66 10 34 00

Dott. Ing.[1,2]
Giuseppe de Mico S.p.A.
V. Le Vittorio Veneto 8
20060 Cassina de Pecchi
(02) 95 34 36 00

LASI Elettronica S.P.A.[1,2]
Viale Fluvio Test. 280
20126 Milano
(02) 66 10 1370

Japan

Ryoden Trading Co., Limited[1,2]
3-15-15 , Higashi Ikebukuro,
Toshima-ku, Tokyo 170
(81) 3-5396-6206

Ryoden Trading Co., Limited[1,2]
Niski Hanshin Bldg.
2-3-24, Umeda, Kita-ku,
Osaka-shi, Osaka 530
(81) 6-347-1461

Ryoyo Electro Corporation[1,2]
Konwa Bldg.
1-12-22, Tsukiji
Chuo-ku, Tokyo 104
(81) 3-3546-5088

Ryoyo Electro Corporation[1,2]
Nisshin Shokuhin Bldg.
4-1-1, Nishi-Nakajima
Yodogawa-ku, Osaka 532
(81) 6-302-5371

Ryoyo Electro Corporation[1,2]
Nagoya AT Bldg.
1-18-22, Nishiki, Naka-ku,
Nagoya-shi, Aichi 460
(81) 52-203-0277

Tokyo Electron Limited[1,2]
Shinjuku Monolith Bldg.
3-1-2 Nishi Shinjuka
Shinjyuku-Ku, Tokyo 163
(81) 3-3340-8251

Tokyo Electron Limited[1,2]
Sumitomoseimei Shin-Osaka Bldg.
4-1-14, Miyahara,
Yodogawa-ku,
Osaka-shi, Osaka 532
(81) 6-399-0263

Yamada Corporation[3]
Shin-Aoyama Bldg. East
1-1-1 Minami-Aoyama
Minatu-Ku, Tokyo 107
(81) 3-3475-1121

Yamada Corporation[3]
Nagoya Kokusai-Center Bldg.
1-47-1, Nakano,
Naka Ura-Ku
Nagoya-shi, Aichi 450
(81) 52-563-6661

Yamada Corporation[3]
Higobashi Shimizu Bldg.
1-3-7 Tosabori, Nishi-Ku
Osaka-shi, Osaka 550
(81) 6-449-1101

Korea

Panwest Co., Ltd. (REP)[1,2]
2nd Floor, Jeil Life Insurance
New Building
1303-16 Seocho-Dong
Seocho-ku, Seoul
(82) 2-5520344

Malaysia

DCP (M) SDN BHD[1,2]
6th Floor Wisma Denko
41 Aboo Sittee Lane
10400 Penang
(60) 4-363376

Netherlands

EBV Elektronik[1,2]
Planetenbaan 2
3606 AK Maarssenbroek
(31) 03465 623 53

Diode Nederland[1,2]
Coltbaan 17
3439 NG Nieuwegein
Tel: (03402) 912 34

New Zealand

VSI Electronics (NZ) Ltd.[1,2,3]
7 Beasley Ave.
Penrose
Auckland
(64) 9 579 6603

VSI Electronics (NZ) Ltd.[1,2]
295 Cashel Street
Christchurch
(64) 3 660-928

VSI Electronics (NZ) Ltd.[1,2]
Flanders Arcade
71 High Street
Lower Hutt
(64) 4 694-560

Norway

NORTEC[1,2]
Electronics A/S
P.O. Box 123
1364 Hvalstad
(47) 02 846210

ITT Multikomponent AB[1,2]
N. Kalbakkvn. 88
1081 Oslo 10
Tel: (02) 32 12 70

Poland

Meditronik[1,2]
4, Dzika Street
00-194 Warsaw
(02) 63522-63/-64

Portugal

ATD Electronica Lda.[1,2,3]
R. Dr. Faria de Vasconcelos, 3-A
1900 Lisboa
(351) 01 847 2200

Singapore

Dynamar Computer Products[1,2]
PTE Ltd. (REP)
109 Defu Lane 10
Off Hougang Avenue 3
Singapore 1953
(65) 2813388

Hi-Tech Business Associate[3]
230, Upper Bukit Timah Road
Bukit Timah Industrial Complex #04-10
Singapore 2158
(65) 4620668

So. Africa

Advanced Semiconductor Devices (PTY) Ltd.[1,2]
P.O. Box 2944
Johannesburg 2000
(27) 011 444 23 33

Spain

BFI IBEXSA Electronica S.A.[2,3]
C/ Isabel Colbrand, S/N
Edificio Alfa III, Nave 85
Pol. Ind. Fuencarral
28049 Madrid
Tel: (1) 358 85 16

Diode Espana[1,2]
Calle Orense 34
1E Planta
28020 Madrid
(34) 01 555 36 86

BFI IBEXSA[3]
Isabel Colbrand, S/N
Edif. Alfa III, Nave 85
Poligono Ind. Fuencarral
28049 Madrid
(91) 358 47 77

SELCO[1,2]
Sociedad de Electronica y Componentes S.A.
Paseo de la Habana 190
28036 Madrid
(91) 326 42 13

Sweden

BFI - IBEXSA Nordic AB[2,3]
Box 3040
Lövängsvägen 8
19403 Upplands Väsby
Sweden
46/8/626 99 00

ITT Multikomponent AB[1,2]
Ankdammsgatan 32
Box 1330
171 26 Solna
(46) 08 83 00 20

NORTEC Electronics AB[1,2]
Box 1830
17127 Solna
(08) 705 18 00

Switzerland

Basix fur Elektronik AG[1,2]
Hardturmstr. 181
Postfach
8010 Zurich
(41) 01 276 11 11

BFI IBEXSA Elektronik GmbH[2,3]
Microwave Group
Korbinianstr. 6
8057 Eching (München)
Tel: (089) 319 51 35

EBV Elektronik AG[1,2]
Vorstadtstrasse 37
8958 Dietikon
(41) 01 740 1090

Fabrimex Distribution AG[1,2]
Krichenweg 5
8032 Zürich
Tel: (01) 386 86 86

Taiwan (Republic of China)

Morrihan International Inc.[1,2]
No. 57, 8th Floor
Yang Shen Shan Yet Building
337 Fu Hsing North Road
Taipei, Taiwan
(886) 2 7522200

Notes:
1. Optoelectronics
2. RF Diodes/Transistors
3. Microwave and Avantek Products

Turkey

Empa AS[1,2]
Elektronik Mamulleri
Pazarlama A.S.
Forya is Merkezi
Besyol Londra Asfaltl
34630 Florya-Istanbul
(0901) 599 30 50

United Kingdom

Celdis Ltd.[1,2]
37-39 Loverock Road,
Reading
Berkshire RG3 1ED
(44) 0734 585171

ESD Ltd.[1,2]
Edinburgh Way
Harlow,
Essex CM20 2DF
(44) 0279 626777

Farnell Electronic[1,2]
Canal Road
Leeds
West Yorkshire LS12 2TU
(44) 0532-636311

Jermyn Distribution[1,2]
Vestry Estate
Sevenoaks,
Kent TN14 5EU
(44) 0732 74 37 43

Macro Marketing Ltd.[1,2]
Burnham Lane
Slough
Berkshire SL1 6LN
(44) 0628-6044 22

Solvenia/Kroatia/
Yugoslavia

Elektrotehna[1,2]
Do Junel, TOZD ELZAS
Poljanska 25
61000 Ljubljana
(38) 061 318 663

EBV Elektronik[1,2]
Diefenbachgasse 35/6
1150 Vienna
43/222/894 17 74

Notes:
1. Optoelectronics
2. RF Diodes/Transistors
3. Microwave and Avantek Products

HEWLETT PACKARD

US Sales & Support

Alabama
620 Discovery Dr.
Huntsville 35806
Tel: 205-971-2000

Arizona
8080 Pointe Parkway West
Phoenix 85044
Tel: 602-273-8000

3400 E. Britannia Drive
Bldg. C, Suite 124
Tucson 85706
Tel: 602-573-7400

California
26701 West Agoura Road
Calabasas 91302
Tel: 818-880-3400

1421 S. Manhattan Avenue
Fullerton 92631
Tel: 714-999-6700

5245 Pacific Concourse Drive
Suite 100
Los Angeles 90045
Tel: 310-643-5112

351 E. Evelyn Ave.
Mountain View 94041
Tel: 415-694-2000

4244 So. Market Court,
Suite A
Sacramento 95834
Tel: 916-929-7222

9606 Aero Drive
San Diego 92123
Tel: 619-279-3200

9800 Muirlands Ave.
Irvine 92718
Tel: 714-472-3000

Colorado
24 Inverness Place East
Englewood 80112
Tel: 303-649-5000

Connecticut
#4 The Forum
9th Floor
Stamford, CT 06901
Tel: 203-324-1003

115 Glastonbury Boulevard
Glastonbury 06033
Tel: 203-633-8100

Florida
5900 N. Andrews Ave.
Suite 100
Ft. Lauderdale 33309
Tel: 305-938-9800

6177 Lake Ellenor Drive
Orlando 32809
Tel: 407-859-2900

5550 W. Idlewild Ave.,
Suite 150
Tampa 33634
Tel: 813-884-3282

Georgia
1995 North Park Place
Atlanta 30339
Tel: 404-955-1500

Illinois
5201 Tollview Dr.
Rolling Meadows 60008
Tel: 708-255-9800

Indiana
201 W. 103rd St.
Suite 100
Indianapolis, IN 46290
Tel: 317-844-4100

Maryland
3701 Koppers St.
Baltimore 21227
Tel: 301-644-5800

Massachusetts
29 Burlington Mall Rd.
Burlington 01803
Tel: 619-270-7000

Michigan
39550 Orchard Hill Place
Novi 48376
Tel: 313-349-9200

Minnesota
2025 W. Larpenteur Avenue
St. Paul 55113
Tel: 612-644-1100

Missouri
6601 Winchester Avenue
Kansas City 64133
Tel: 816-737-0071

New Jersey
W. 120 Century Rd.
Paramus 07652
Tel: 201-599-5000

New York
290 Woodcliff Dr.
Fairport 14450
Tel: 716-264-4000

7 Old Sod Farm Road
Melville 11747
Tel: 516-753-0555

North Carolina
2000 Regency Pk
Suite 600
Cary, NC 27511
Tel: 919-467-6600

Ohio
7887 Washington Village
Dayton 45459
Tel: 513-433-2223

15885 Sprague Rd.
Strongsville 44136
Tel: 216-243-7300

Oregon
15115 SW Sequoia Parkway, Suite 100
Portland 97224
Tel: 503-598-8000

Pennsylvania
2750 Monroe Blvd.
Valley Forge 19482
Tel: 215-666-9000

Texas
930 E. Campbell Rd.
Richardson 75081
Tel: 214-231-6101

Washington
15815 SE 37th St.
Bellevue 98006
Tel: 206-643-4000

HEWLETT PACKARD

International Sales & Marketing Support

Austria and Eastern Region
Hewlett-Packard
Lieblgasse 1
P.O. Box 72
A-1222 Vienna
Tel: 43/2 22/25 00 461

Belgium/Luxemburg
Hewlett-Packard
Boulevard de la Woluwe 100
Woluwedal
B-1200 Brussels
Tel: 32/2/7 78 31 11

Brazil
Edisa Informática S.A.
Alameda Rio Negro 750
06454 - Alphaville - Barueri - SP
Brazil
Tel: (+55 11) 709-1444

Canada
Hewlett-Packard Ltd.
6877 Goreway Drive
Mississauga, Ontario
L4V1M8
Tel: 416-678-9430

China
Hewlett-Packard Co., Ltd.
5-6/F West Wing Office
China World Trade Center
No. 1 Jian Guo Men Wai Ave.
Beijing, 100004, PRC
Tel: 86-1-505-3888

Finland
Hewlett-Packard Oy
Piispankalliontie 17
SF-02200 Espoo
Tel: 358/0/8 87 21

France
Hewlett-Packard
Z.A. de Courtaboeuf
1, Avenue du Canada
F-91947 Les Ulis Cedex
Tel: 33/1/69 82 60 60

Greece/Turkey
Hewlett-Packard S.A.
P.O.Box
150 Route du Nant-d'Avril
CH-1217 Meyrin 2
Tel: 41/22/780 81 11

Israel
Computation & Measurement
Systems Ltd.
11 Hashlosha Street
P.O.Box 25089
IL-Tel Aviv 67060
Tel: 972/3/538 03 18

Italy
Hewlett-Packard Italiana S.p.A.
Via G. Di Vittorio 9
I-20063 Cernusco S/N (MI)
Tel: 39/2/92 121

Japan
Yokogawa Hewlett-Packard
29-21 Takaido-Higashi 3 Chome
Sugimani-Ku, Tokyo 168
Japan
Tel: 81-3-3331-8153

Netherlands
Hewlett-Packard B.V.
Boschdijk 137
NL-5612 HB Eindhoven
Tel: 31/40/32 42 18

Korea
Samsung Hewlett-Packard
Samsung Life Bldg.
36-1 Yeoeui Do-Dong
Youngdeungpo-Ku
Seoul, 150-010, Korea
Tel: 82-2-769-0114

Mexico
Hewlett-Packard de México
S.A. de C.V.
Monte Pelvoux No. 111
Fracc. Lomas de Virreyes
11000 Mexico D.F.
Mexico
(+52 5) 326-4000

Singapore
Hewlett-Packard Singapore
150 Beach Rd. #29-00
Gateway West Singapore 0718
Tel: 65-291-9088

Spain/Portugal
Hewlett-Packard Espanola S.A.
Corta de la Coruna km 16 500
Madrid
E-28230 Las Rozas
Tel: 34/1/626 16 00

Sweden, Denmark, Norway
Hewlett-Packard AB
Skalholtsgatan 9, Kista
Box 19
S-164 93 Kista
Tel: 46/8/7 50 20 00

Switzerland/South Africa
Hewlett-Packard
Allmend 2
CH-8967 Widen
Tel: 41/57/31 21 11

Taiwan

Hewlett-Packard Taiwan Ltd.
20, Kao Shuang Rd, Ping Chen
Tao-Yuan, Taiwan, R.O.C.
Tel: 886-3-492-9666

United/Kingdom/Ireland

Hewlett-Packard Ltd.
Amen Corner
Cain Road
Bracknell
UK-Berkshire RG12 1HN
Tel: 44/344/ 36 00 00

Frimley Microwave Centre
Hewlett-Packard
Unit 6
Frimley Business Park
Frimley, Camberley
Surrey GU16 5SG
United Kingdom 44 276-685753

West Germany

Hewlett-Packard GmbH
Components Marketing
Operation
P.O. Box 1430
Herrenberger Str, 124
D-7030 Böblingen
Tel: 49/7031/14-0

Hewlett-Packard GmbH
Hewlett-Packard-Strasse
D-6380 bad Homburg
Tel: 49/6172/16-0



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